PLESSEY
Solid State

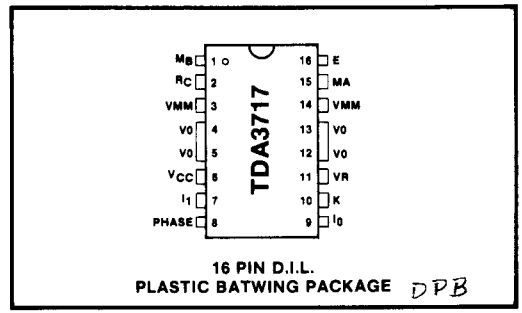
ADVANCED INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

TDA3717

STEPPER MOTOR DRIVE CIRCUIT

The TDA3717 is a bipolar integrated circuit intended to control and drive the current in one winding of a stepper motor using a switch mode technique. The output drive bridge is capable of producing a bidirectional current and incorporates all required clamping diodes. The logic control inputs may by driven by TTL, CMOS, or a microprocessor control system.



16 PIN D.I.L.
PLASTIC BATWING PACKAGE DPB

Fig. 1 Pin connections

SPECIAL FEATURES

- Bipolar output current drive enabling maximum performance to be obtained from the stepper motor.
- Full-step, half-step and quarter-step operating modes may be utilized by digital control.
- Built in clamping diodes on output drives.
- Separate supplies for internal logic and motor drive may be powered up and down in any sequence.
- Wide range of unstabilized motor supply voltage may be used (10-50 Volts).
- Wide range of output current control (20-500 mA).
- Output current levels may be selected in steps digitally or varied continuously by analog control.

CIRCUIT DESCRIPTION

A differential output drive is provided by means of a transistor bridge circuit which is capable of regulating a bidirectional current into a motor winding. The motor supply voltage is applied to the load by turning on two diametrically opposed output drive transistors causing the current to build up at a rate dependant on the applied voltage and the inductance of the motor winding. When the programmed current trip level is reached the monostable circuit is triggered which turns off only the negative pulling output drive transistor. Due to the inductive nature of the motor winding current continues to flow through the positive pulling transistor and the positive clamping diode on the opposite side of the bridge. The current will 'freewheel' since no forcing voltage is applied and only the diode and transistor voltage drops resist the flow causing a gradual reduction. After a period of time defined by the monostable circuit the supply is reestablished by turning on the negative pulling transistor causing the current to build back up to the trip level. By the above switch mode technique the load current is quickly established and maintained at the programmed level.

Power dissipation in the device is reduced by cross coupling the output drives such that advantage is taken of the extra positive potential generated across the clamping diode to drive the opposite positive pulling output transistor. This will only occur during the 'freewheel' periods which are normally the greater part of the cycle.

The load current is sensed by monitoring the voltage across a low impedance resistor placed in series with the negative supply to the transistor output bridge. Current only flows through this resistor during the forcing period of the switch mode cycle and is unidirectional. At the start of the forcing period a current spike occurs due to the charge storage effect of the clamping diodes. To stop this prematurely triggering the monostable circuit a low pass RC filter is attached to the current sensing input.

Three load current trip levels can be digitally selected by the I0 & I1 inputs (pins 7 & 9). These are derived from the analog reference level (V_R) on pin 11, which is normally connected direct to the 5 volt logic supply. The fourth combination of I_0 & I_1 inhibits the output drive.

The 'phase' control (pin 8) is a third logic input which determines the direction of the current flow in the motor winding. This input incorporates a latch with hysteresis to eliminate switching jitter.

APPLICATION NOTES

Some stepper motors are not suited to switch mode current regulation due to high core losses, a motor that has a predominant inductive load characteristic at the switching frequency is most desirable.

Power dissipation is predominatly due to the regulated load current flowing through the output drive transistors and diodes, although the power dissipated by the logic supply current should not be neglected. The upper transistor voltage drops are reduced by cross-coupling during the 'freewheel' periods and hence the power dissipation will be dependent on the duty cycle required to maintain the load current.

The maximum working ambient temperature will be dependent on the overall chip to ambient power dissipation temperature coefficient and a limitation of 145°C for the maximum working chip temperature. This chip temperature limitation is due to degradation of the plastic packaging which can occur above this limit. The overall temperature coefficient will be the sum of the chip to pin and pin to ambient coefficients.

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Typically an overall temperature coefficient of 45°C/Watt can be obtained on a P.C.B. without additional heatsinking giving a maximum working ambient temperature of 75°C when regulating 420mA giving a power dissipation of 1.5 Watts.

ABSOLUTE MAXIMUM RATINGS

Electrical			Value		Units
			Min.	Max.	
Motor Supply Voltage	Pins 3 & 14	V_{MM}	0	50	V
Motor Drive Current	Pins 1 & 15	I_M	−500	500	mA
Logic Supply Voltage	Pin 6	V_{CC}	0	7.5	V
Input Voltage on Logic Inputs	Pins 7,8 & 9		0	V_{CC}	V
Analog Control Input	Pin 11	V_R	0	15	V
Input Voltage	Pins 2 & 10		0	V_{CC}	V
Thermal					
Storage Temperature		T_G	−55	145	°C
Operating Chip Junction Temperature		T_J		145	°C

0 to +70 °C for B

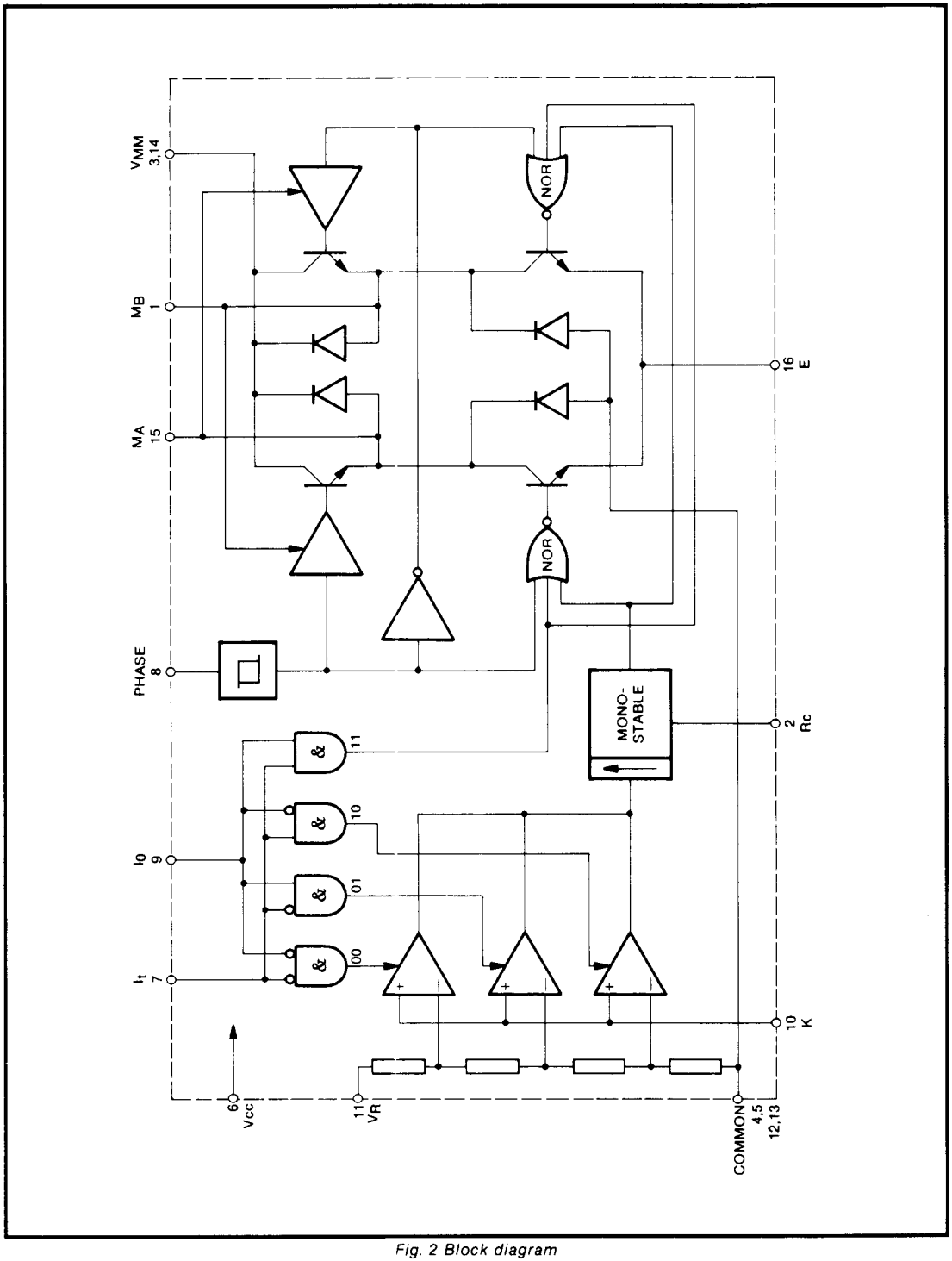


Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS (contd)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Logic Inputs						
Pins 7,8 & 9 I_1, I_0 & Phase						
Logic 1 Voltage	V_{IH}	2.0		V_{CC}	V	
Logic 0 Voltage	V_{IL}	0.0		0.8	V	
Input Current Low Level	I_{IL}			−0.2	mA	V_I = 0.4V
Input Current High Level	I_{IH}			5.0	μA	V_1 = 2.4V
Pin 8 Phase Input Hysteresis			0.6		V	
Control Comparator						
Pin 10 Input Threshold Voltage	V_{ER}					V_R = 5V. Pin 11 Pin 10 Driving Impedance = 1Kn Inhibit—Lower Output Transistors Turned Off
I_1 = 0, I_0 = 0.		396	416	436	mV	
I_1 = 0, I_0 = 1.		236	251	266	mV	
I_1 = 1, I_0 = 0.		66	78	90	mV	
I_1 = 1, I_0 = 1.		--	—	—	—	
Input Current	I_K			−10	μA	
Monostable Circuit & Timing						
Pin 2 Reset Voltage	V_{T1}		1.2		V	
Trip Voltage	V_{T2}		0.6		V	
Reset Charging Current		2.5		5.0	mA	
Input Bias Current				−10.0	μA	Pin 2 Voltage = V_{T2}
Timing Period $T_{OFF} = 0.69 R_T C_T$	T_{OFF}	28	31	35	μS	Measured At Motor o/p I_M = 240mA, Ton ≥5μS U_M = 10V, dUk/dt, = 50mV/μS R_T = 56Kn, C_t = 820pF
Cut Off Delay	T_D		1	2	μS	
Thermal Power Dissipation						
Package Thermal Resistance Chip Junction to Center Pins			11		°C/W	Measured to copper side of P.C.B. on center four pins. Note: This is not the chip to ambient temp coefficient

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Vcc = 5V
Umm = 45V
Chip Temperature (θj) = 25°C

Input and supply voltages measured with respect to common (Pins 4,5,12 & 13).

Characteristics	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Current Consumption						
Pin 6 Logic Supply Current	ICC		12.5	16.0	mA	$I_1 = I_0 = 0$
'Output Off' Logic Supply Current	ICL					$I_1 = I_0 = 1$
Pin 11 Input Bias Current	IR		0.55	0.8	mA	$V_R = 5V$
Motor Output Drive						
Pins 1 and 15 Lower Transistor Saturation Voltage	VML			1.35	V	$V_E = 0V$, $I_M = 500mA$
Lower Transistor Leakage Current	IMLL			300	μA	$V_M = 50V$, $V_E = 0V$ $I_0 = I_1 = 1$ Current Measured at Pin 16
Lower Diode Clamp Voltage	VMLC			-1.5	V	$I_M = -500mA$, $I_0 = I_1 = 1$.
Upper Transistor Forcing Saturation Voltage	VMH			-2.1	V	$I_M = 500mA$, Measured W.R.T. U_{MM}
Upper Transistor Cross-Coupled Saturation Voltage	VMHX			-1.3	V	
Upper Transistor Leakage Current	IMHL			300	μA	$V_M = 1V$, $I_0 = I_1 = 1$
Upper Diode Clamp Voltage	VMHC			1.25	V	$I_M = 500mA$, Measured W.R.T. U_{MM}
Diode Substrate Leakage Current When Clamped	ILS			2.0	mA	$I_M = 500mA$, V_{CC}, V_R and other inputs not connected
Upper Diode Charge Storage			—	— 100	nQ	$I_M = 500mA$ $I_M = 240mA$

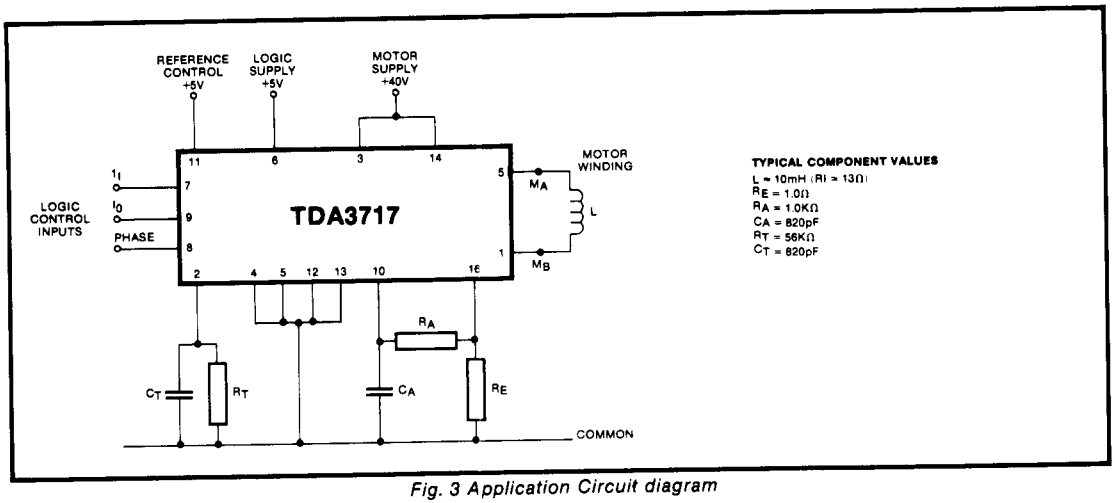


Fig. 3 Application Circuit diagram