TDA10025HN

Dual cable demodulator

Rev. 1 — 22 August 2011 Product short data sheet

1. General description

The TDA10025HN is a Dual Cable Downstream Processor.

The Cable Downstream Processor (CDP) implements the physical interfaces and protocols required to provide the highest quality services of an in-band DOCSIS, EuroDOCSIS, DVB and OpenCable Set-Top Box (STB). The downstream signals are digitized by 12-bit ADC and passed to the Demod and Forward Error Correction (FEC) blocks, which do all the cable physical layer processing. This processing includes demodulating and Annex A (Europe), Annex B (US) or Annex C (Japan) FEC for the in-band data.

2. Features and benefits

- QPSK, 16 QAM, 32 QAM, 64 QAM, 128 QAM and 256 QAM Demodulator
- ITU-T J83 Annex A, B and C FEC
- Transport Stream Multiplex Frame (TSMF) module for Annex C compliance
- Time interleaved parallel mode or serial mode for Transport Stream (TS) interface
- On chip PLL for crystal frequency multiplication (16 MHz external)
- Reuse of the tuner clock, saving one crystal
- Embedded 12-bit ADC
- 3.3 V and 1.2 V power supplies
- Low power < 235 mW for dual stream operation
- Small size package
- Low cost Bill Of Material (BOM)

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P	power dissipation	Standby mode: all 3 ADC in Power-down mode and all clocks disabled	-	10[1]	30[2]	mW
		operation mode:				
		1.2 V supply voltage; 2 simultaneous DVB-C demodulations (256 QAM 6.9 Msps)	-	205[1]	280[2]	mW
		3.3 V supply voltage; 2 simultaneous DVB-C demodulations (256 QAM 6.9 Msps)	-	30[1]	50[2]	mW
P_{tot}	total power dissipation	2 simultaneous DVB-C demodulations (256 QAM 6.9 Msps)	-	235[1]	330[2]	mW
$V_{DD(1V2)}$	supply voltage (1.2 V)		1.15	1.2	1.3	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		3.0	3.3	3.6	V
V_{IH}	HIGH-level input voltage	$V_{DD(3V3)}$ related input levels	2.0	-	$V_{DD(3V3)}$ + 0.5	V
V_{IL}	LOW-level input voltage		−0.5	-	+0.8	V

[1] T_{amb} = 25 °C, $V_{DD(1V2)}$ and $V_{DD(3V3)}$ typical.

[2] T_j = 120 °C, $V_{DD(1V2)}$ and $V_{DD(3V3)}$ maximum.

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA10025HN/C1	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-1

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5. Block diagram

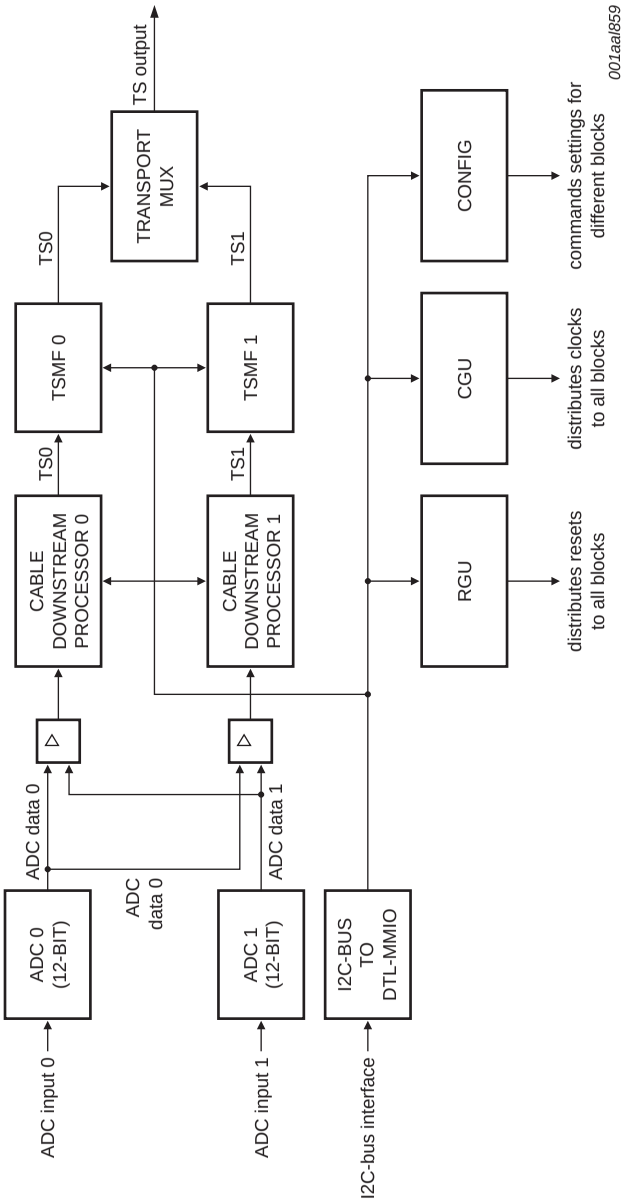


Fig 1. Block diagram

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6. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
T_{stg}	storage temperature			–40	+150	°C
T_j	junction temperature			-	120	°C
V_{ESD}	electrostatic discharge voltage	EIA/JESD22-A114 (human body model)		2	-	kV
		EIA/JESD22-C101-C (FCDM)	[1]	0.5	-	kV

[1] It withstands class IV of JEDEC standard.

7. Abbreviations

Table 4. Abbreviations

Acronym	Description
ADC	Analog to Digital Converter
CDP	Cable Downstream Processor
CGU	Clock Generation Unit
DOCSIS	Data Over Cable Service Interface Specifications
DVB-C	Digital Video Broadcasting - Cable
DVD	Digital Versatile Disc
FCDM	Field-Induced Charged-Device Model
FEC	Forward Error Correction
MUX	MUltipleXer
PLL	Phase-Locked Loop
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RGU	Reset Generation Unit
STB	Set-Top Box
TS	Transport Stream
TSMF	Transport Stream Multiplex Frame
US	United States

8. Revision history

Table 5. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA10025HN_SDS v.1	20110822	Product short data sheet	-	-

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9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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11. Tables

Table 1. Quick reference data 2
Table 2. Ordering information 2
Table 3. Limiting values 4
Table 4. Abbreviations 4
Table 5. Revision history 4

12. Figures

Fig 1. Block diagram 3

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13. Contents

1	**General description**	**1**
2	**Features and benefits**	**1**
3	**Quick reference data**	**2**
4	**Ordering information**	**2**
5	**Block diagram**	**3**
6	**Limiting values**	**4**
7	**Abbreviations**	**4**
8	**Revision history**	**4**
9	**Legal information**	**5**
9.1	Data sheet status	5
9.2	Definitions	5
9.3	Disclaimers	5
9.4	Trademarks	6
10	**Contact information**	**6**
11	**Tables**	**7**
12	**Figures**	**7**
13	**Contents**	**8**

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