

TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TD62304P, TD62304AP, TD62304F, TD62304AF
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7CH LOW ACTIVE DARLINGTON SINK DRIVER

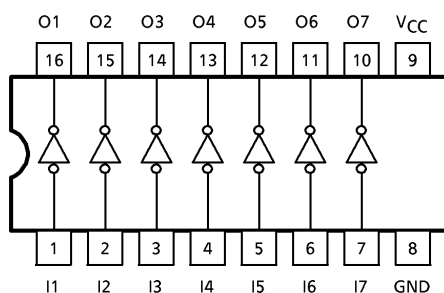
The TD62304P/AP/F/AF and TD62305P/AP/F/AF are non-inverting transistor arrays, which are comprised of eight NPN darlington output stages and PNP input stages.

These devices are Low Level input active drivers and are suitable for operations with TTL, 5V CMOS and 5V Microprocessor which have sink current output drivers. Applications include relay, hammer, lamp and LED driver.

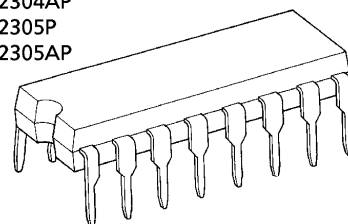
FEATURES

- Output current (single output) 500mA (Max.)
- High sustaining voltage 35V (TD62304P/F, 62305P/F) 50V (TD62304AP/AF, 62305AP/AF) (Min.)
- Low level active input
- Standard supply voltage
- Input compatible with TTL and 5V CMOS

PIN CONNECTION (TOP VIEW)

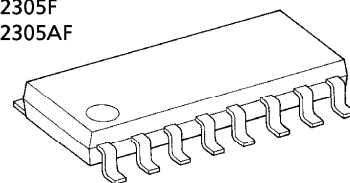


TD62304P
 TD62304AP
 TD62305P
 TD62305AP



DIP16-P-300-2.54A

TD62304F
 TD62304AF
 TD62305F
 TD62305AF



SOP16-P-225-1.27

Weight

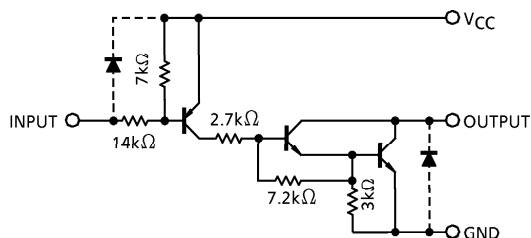
DIP16-P-300-2.54A : 1.11g (Typ.)
 SOP16-P-225-1.27 : 0.16g (Typ.)

961001EBA2

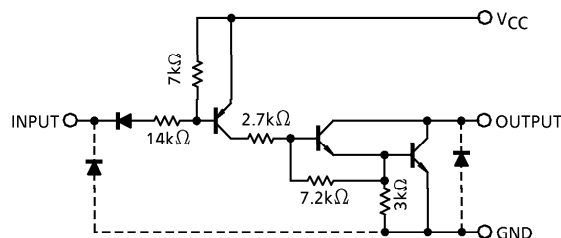
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SCHEMATICS (EACH DRIVER)

TD62304P / AP / F / AF



TD62305P / AP / F / AF



(Note) The input and output parasitic diodes cannot be used as clamp diodes.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V _{CC}	− 0.5~7.0	V
Output Sustaining Voltage	P, F	V _{CE (SUS)}	− 0.5~35	V
	AF		− 0.5~50	
	AP		− 0.5~50	
Output Current		I _{OUT}	500	mA / ch
Input Voltage		V _{IN}	− 22~V _{CC} + 0.5	V
			− 0.5~7 (Note 1)	
Input Current		I _{IN}	− 10	mA
Power Dissipation	P	P _D	1.0	W
	AP		1.47	
	F, AF		0.625 (Note 2)	
Operating Temperature	P	T _{opr}	− 30~75	°C
			− 40~85	
Storage Temperature		T _{stg}	− 50~150	°C

(Note 1) TD62305P / AP / F / AF

(Note 2) On glass epoxy PCB (30 × 30 × 1.6mm Cu 50%)

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim 85^\circ\text{C}$ and $T_a = -30 \sim 75^\circ\text{C}$ for Type-P)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage		V _{CC}	—	4.5	5.0	5.5	V
Output Sustaining Voltage	P, F	V _{CE} (SUS)	—	0	—	35	V
	AF			0	—	50	
	AP			0	—	50	
Output Current		I _{OUT}	DC 1 circuit	0	—	350	mA / ch
			T _{pw} = 25ms, duty = 10% 7 circuits	0	—	300	
			T _{pw} = 25ms, duty = 10% 7 circuits	0	—	350	
			T _{pw} = 25ms, duty = 20% 7 circuits	0	—	200	
Input Voltage	TD62304P / AP / F / AF	V _{IN}	—	− 20	—	V _{CC}	V
	TD62305P / AP / F / AF			0	—	5.5	
Power Dissipation		P	—	—	—	0.44	W
		AP	—	—	—	0.52	
		F, AF	(Note 1)	—	—	0.325	

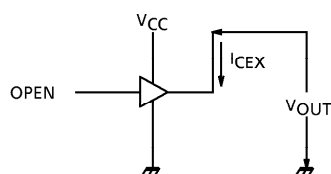
(Note 1) On glass epoxy PCB (30×30×1.6mm Cu 50%)

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

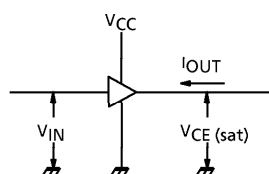
CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Leakage Current	P / F	I _{CEX}	1	V _{CC} = 5.5V V _{IN} = 0V	V _{OUT} = 35V, Ta = 75°C	—	—	- 100	μA
					V _{OUT} = 50V, Ta = 85°C				
Output Saturation Voltage		V _{CE} (sat)	2	V _{CC} = 4.5V I _{OUT} = 350mA	V _{IN} = V _{IN} (ON) MAX.	—	1.4	2.0	V
Input Current	(Output On)	I _{IN} (ON)	3	V _{CC} = 5.5V, V _{IN} = 0.4V		—	- 0.32	- 0.45	mA
				V _{CC} = 5.5V, V _{IN} = - 20V		—	—	- 2.6	
	(Output Off)	I _{IN} (OFF)	4	—		—	—	- 40	μA
Input Voltage (Output On)	TD62304	V _{IN} (ON)	5	—		—	—	V _{CC} - 2.8	V
	TD62305					—	—	V _{CC} - 3.7	
Supply Current	(Output On)	I _{CC} (ON)	6	V _{CC} = 5.5V, V _{IN} = 0V		—	17	22	mA
	(Output Off)	I _{CC} (OFF)	6	V _{CC} = V _{IN} = 5.5V		—	—	100	
Turn-On Delay	P, F	t _{ON}	7	V _{CC} = 5V C _L = 15pF	V _{OUT} = 35V, R _L = 87.5Ω	—	0.1	—	μs
	AP, AF				V _{OUT} = 50V, R _L = 125Ω				
Turn-Off Delay	P, F	t _{OFF}			V _{OUT} = 35V, R _L = 87.5Ω	—	3	—	
	AP, AF				V _{OUT} = 50V, R _L = 125Ω				

TEST CIRCUIT

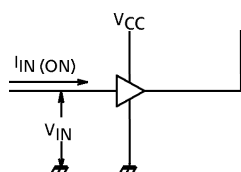
1. I_{CEX}



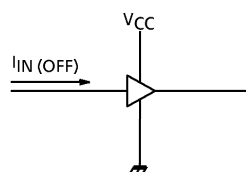
2. $V_{CE(sat)}$



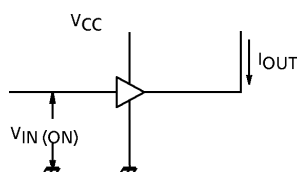
3. $I_{IN(ON)}$



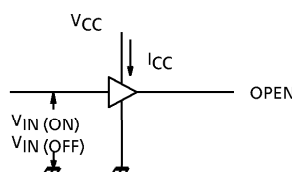
4. $I_{IN(OFF)}$



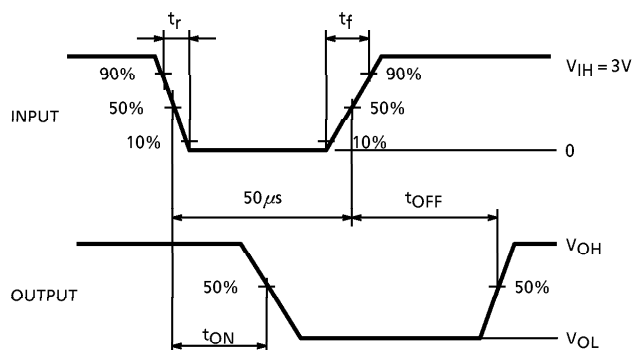
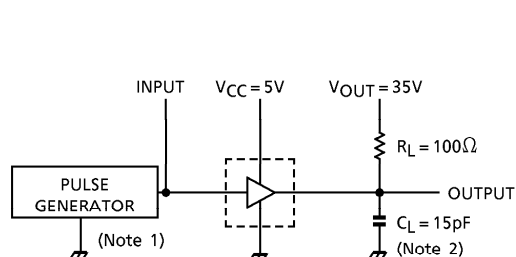
5. $V_{IN(ON)}$



6. I_{CC}



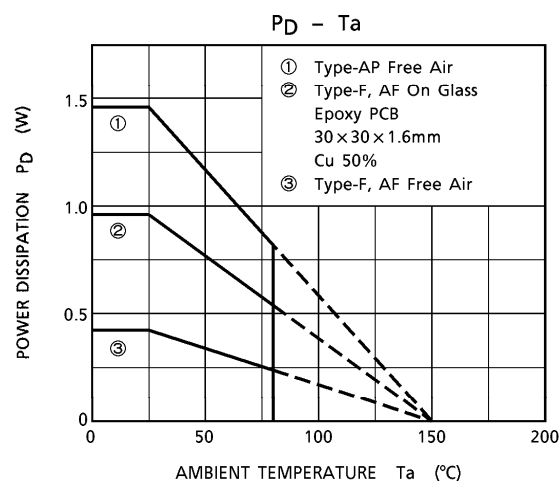
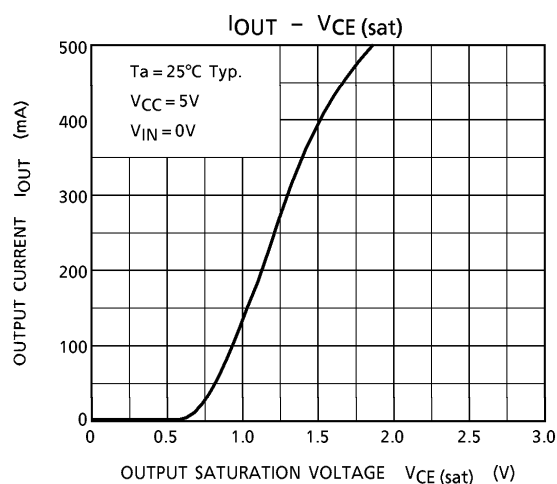
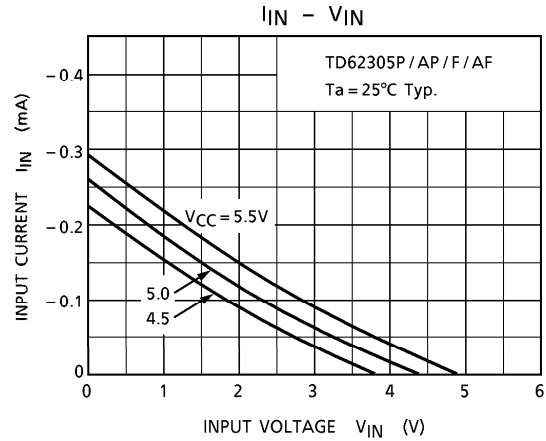
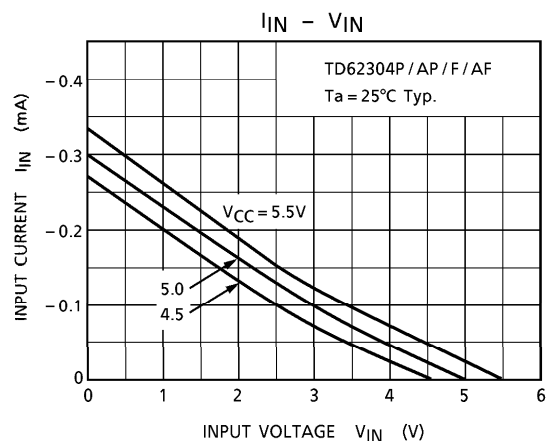
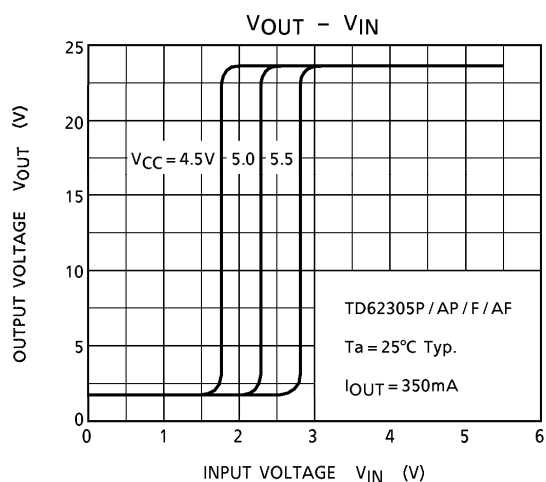
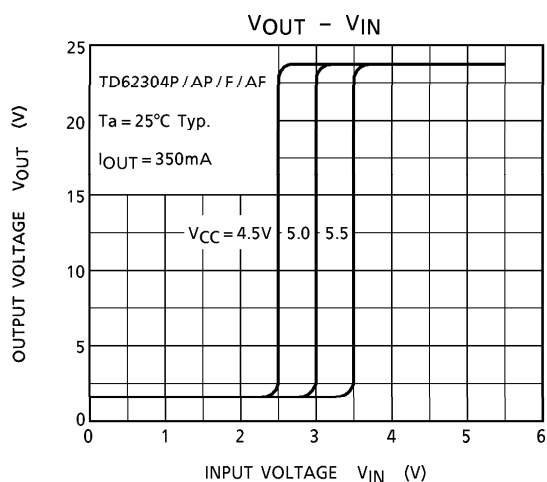
7. t_{ON} , t_{OFF}

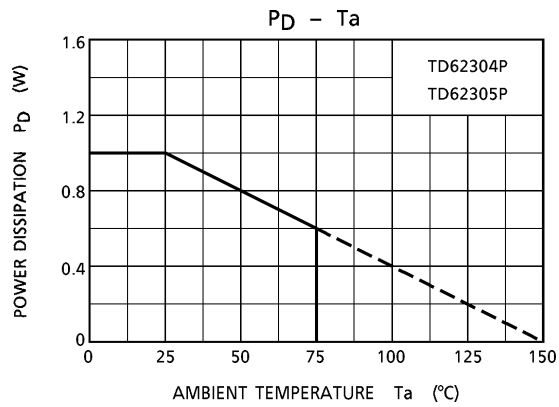


- (Note 1) Pulse width $50\mu s$, duty cycle 10%
Output impedance 50Ω , $t_r \leq 10ns$, $t_f \leq 5ns$
(Note 2) C_L includes probe and jig capacitance.

PRECAUTIONS FOR USING

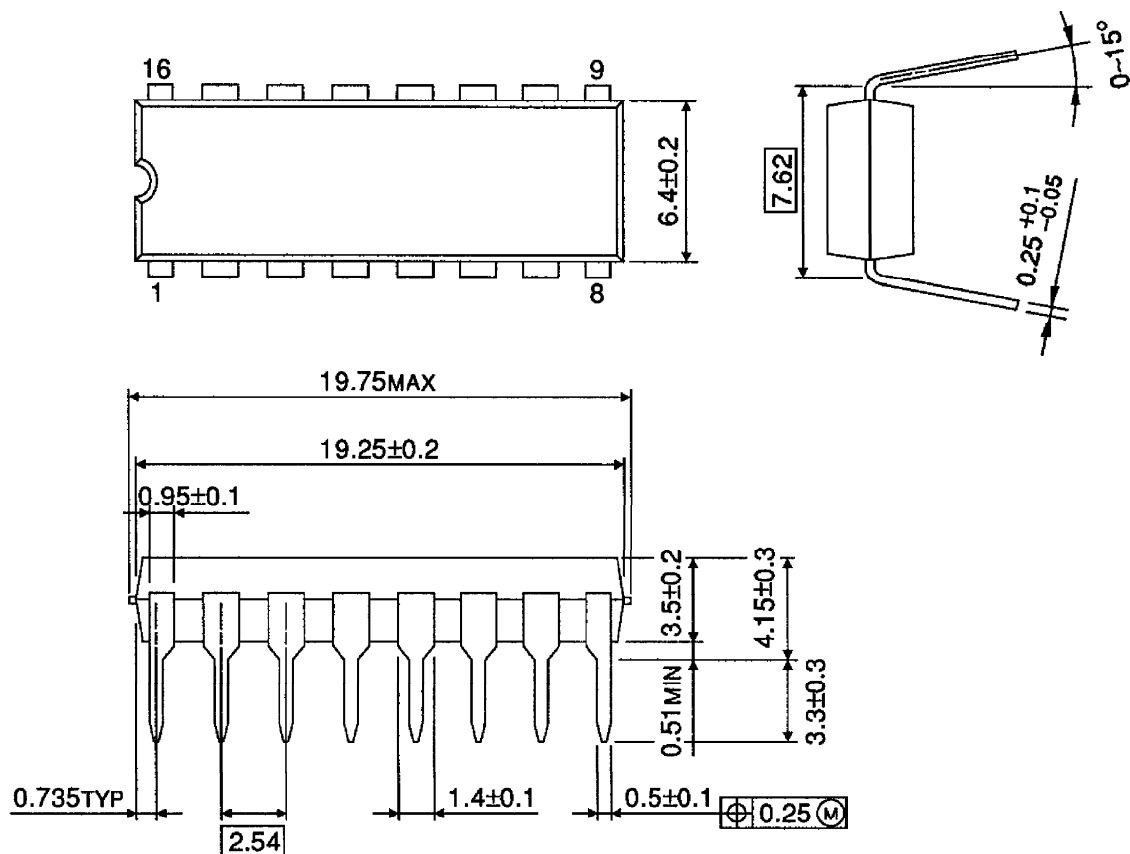
Utmost care is necessary in the design of the output line, V_{CC} and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.





OUTLINE DRAWING
DIP16-P-300-2.54A

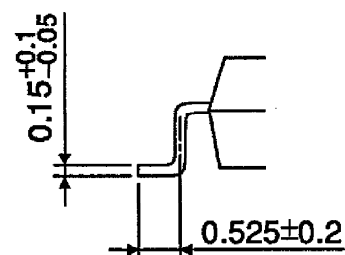
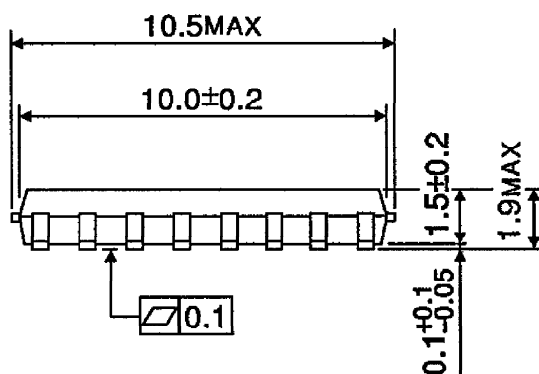
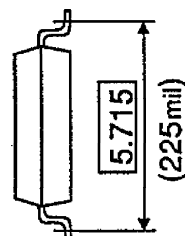
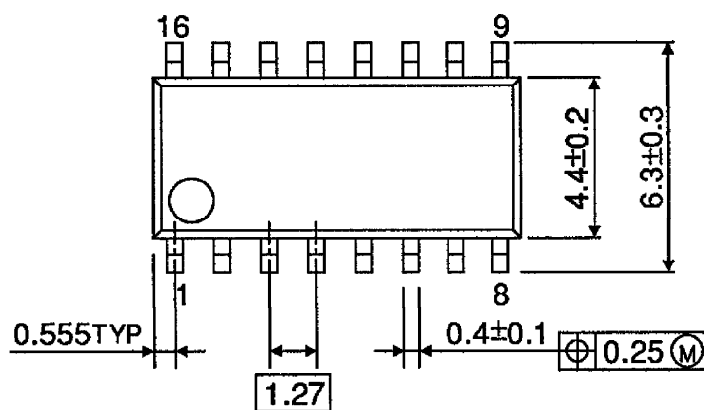
Unit : mm



Weight : 1.11g (Typ.)

OUTLINE DRAWING
SOP16-P-225-1.27

Unit : mm



Weight : 0.16g (Typ.)