TCP-4182UB

8.2 pF Passive Tunable Integrated Circuits (PTIC)

Introduction

ON Semiconductor's PTICs have excellent RF performance and power consumption, making them suitable for any mobile handset or radio application. The fundamental building block of our PTIC product line is a tunable material called ParaScan™, based on Barium Strontium Titanate (BST). PTICs have the ability to change their capacitance from a supplied bias voltage generated by the Control IC. The 8.2 pF ultra−high tuning PTICs are available as wafer-level chip scale packages (WLCSP).

Key Features

- Ultra−High Tuning Range and Operation up to 24 V
- Usable Frequency Range: from 700 MHz to 2.7 GHz
- High Quality Factor (Q) for Low Loss
- High Power Handling Capability
- Compatible with PTIC Control IC TCC-10x, 20x
- WLCSP Package: 0.609 x 1.009 x 0.310 mm (4 bump)
- These devices are Pb−Free and RoHS Compliant

Typical Applications

- Multi-band, Multi-standard, Advanced and Simple Mobile Phones
- Tunable Antenna Matching Networks
- Tunable RF Filters
- Active Antennas

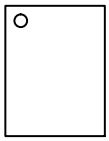
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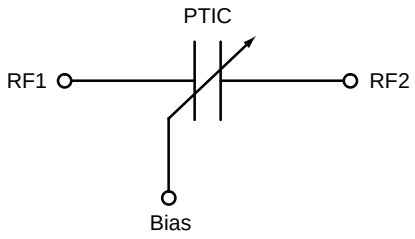


WLCSP4
1.009x0.609
CASE 567LZ

MARKING DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



PTIC Functional Block Diagram

ORDERING INFORMATION

Device	Package	Shipping†
TCP−4182UB−DT	WLCSP4 (Pb−Free)	4000 Units / 7" Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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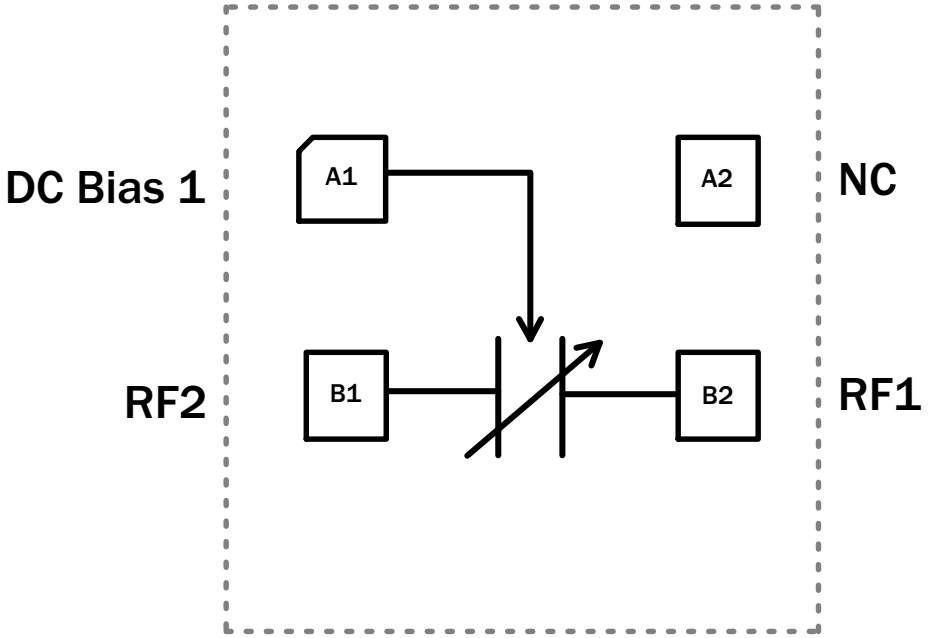


Figure 1. PTIC Functional Block Diagram

Table 1. SIGNAL DESCRIPTIONS

Ball / Pad Number	Pin Name	Description
A1	DC Bias 1	DC Bias Voltage
B1	RF2	RF Input / Output
A2	NC	Not Connected
B2	RF1	RF Input / Output

TYPICAL SPECIFICATIONS

Representative Performance Data at 25°C

Table 2. PERFORMANCE DATA

Parameter	Min	Typ	Max	Units
Operating Bias Voltage	1.0		24	V
Capacitance (V_{bias} = 2 V)	7.38	8.20	9.02	pF
Capacitance (V_{bias} = 24 V)	1.570	1.745	1.919	pF
Tuning Range (1 V - 24 V)	4.80	5.30	6.00	
Tuning Range (2 V - 24 V)	4.20	4.70	5.30	
Leakage Current (WLCSP)			0.5	μA
Operating Frequency	700		2700	MHz
Quality Factor @ 700 MHz, 10 V		100		
Quality Factor @ 2.4 GHz, 10 V		70		
IP3 (V_{bias} = 2 V) [1,3]		70		dBm
IP3 (V_{bias} = 24 V) [1,3]		85		dBm
2nd Harmonic (V_{bias} = 2 V) [2,3]		-75		dBm
2nd Harmonic (V_{bias} = 24 V) [2,3]		-85		dBm
3rd Harmonic (V_{bias} = 2 V) [2,3]		-40		dBm
3rd Harmonic (V_{bias} = 24 V) [2,3]		-70		dBm
Transition Time (Cmin → Cmax) [4]		80		μs
Transition Time (Cmax → Cmin) [4]		70		μs

1. f_1 = 850 MHz, f_2 = 860 MHz, Pin 25 dBm/Tone
2. 850 MHz, Pin +34 dBm
3. IP3 and Harmonics are measured in the shunt configuration in a 50 Ω environment
4. RF_{IN} and RF_{OUT} are both connected to DC ground

Representative performance data at 25°C for 8.2 pF WLCSP Package

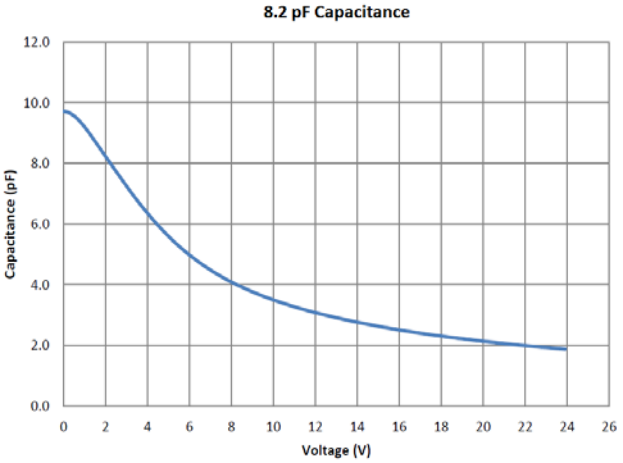


Figure 2. Capacitance

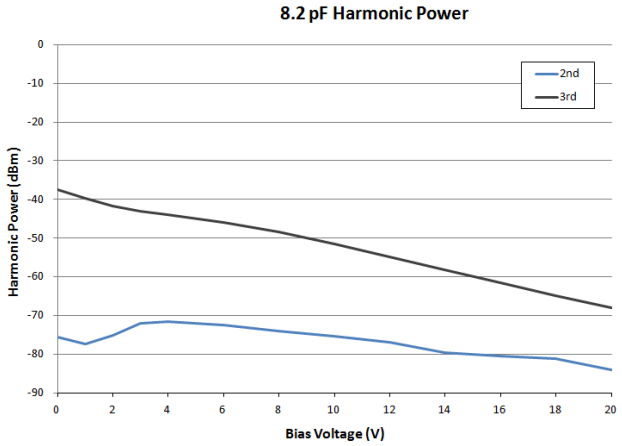


Figure 3. Harmonic Power*

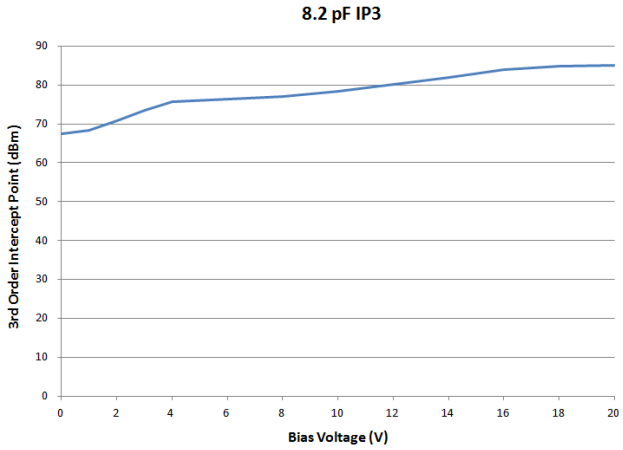


Figure 4. IP3*

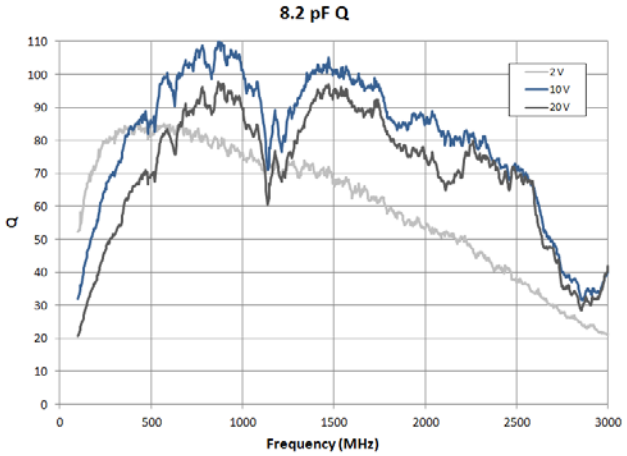


Figure 5. Q*

*Data shown is representative only.

Table 3. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Input Power	+40	dBm
Bias Voltage	+25 (Note 5)	V
Operating Temperature Range	−30 to +85	°C
Storage Temperature Range	−55 to +125	°C
ESD − Human Body Model	Class 1B JEDEC HBM Standard (Note 6)	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

5. WLCSP: Recommended Bias Voltage not to exceed 24 V.
6. Class 1B defined as passing 500 V, but may fail after exposure to 1000 V ESD pulse.

ASSEMBLY CONSIDERATIONS AND REFLOW PROFILE

The following assembly considerations should be observed:

Cleanliness

These chips should be handled in a clean environment.

Electro-static Sensitivity

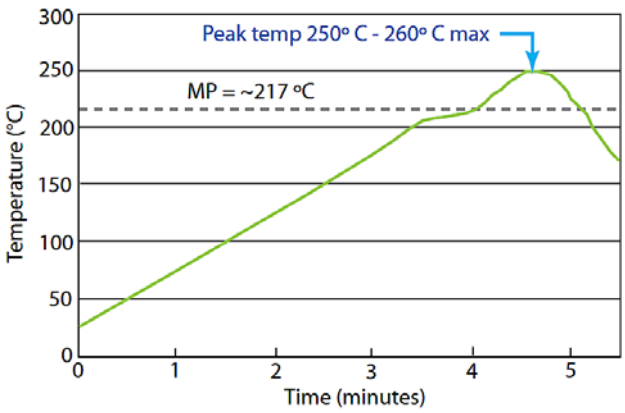
ON Semiconductor's PTICs are ESD Class 1B sensitive. The proper ESD handling procedures should be used.

Mounting

The WLCSP PTIC is fabricated for Flip Chip solder mounting. Connectivity to the RF and Bias terminations on the PTIC die is established through SAC305 solder balls with 65 µm nominal height (45 µm to 85 µm height variation). The PTIC die is RoHS-compliant and compatible with lead-free soldering profile.

Molding

The PTIC die is compatible for over-molding or under-fill.



This reflow profile is a guideline for Pb-free solder materials. Adjustments to this profile are necessary based on specific process requirements and board size, thickness and density.
Not to exceed 260° C for 5 seconds.

Figure 6. Reflow Profile

ORIENTATION OF THE PTIC FOR OPTIMUM LOSSES

When configuring the PTIC in your specific circuit design, at least one of the RF terminals must be connected to DC ground. If minimum transition times are required, DC ground on both RF terminals is recommended. To minimize losses, the PTIC should be oriented such that RF2 is at the lower RF impedance of the two RF nodes. A shunt PTIC, for example, should have RF2 connected to RF ground.

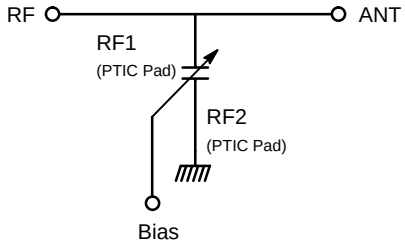


Figure 7. PTIC Orientation Functional Block Diagram

PART NUMBER DEFINITION

Table 4. PART NUMBERS

Part Number	Capacitance		Package*
	2 V	24 V	
TCP−4182UB-DT	8.20	1.822	4-bump WLCSP

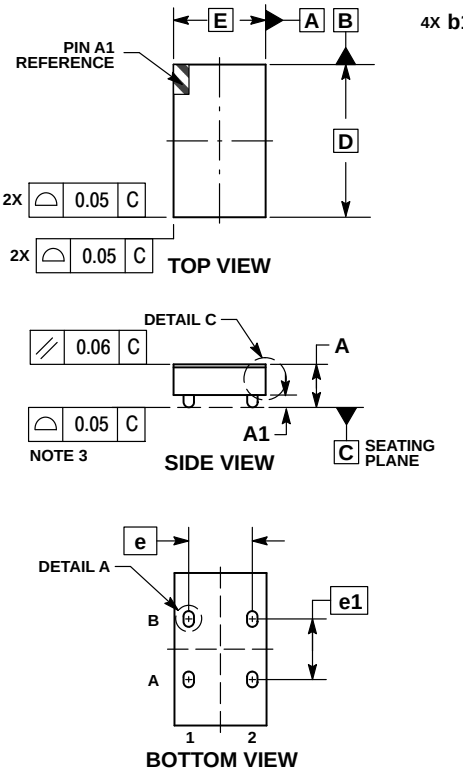
*See PTIC package dimensions on following page.

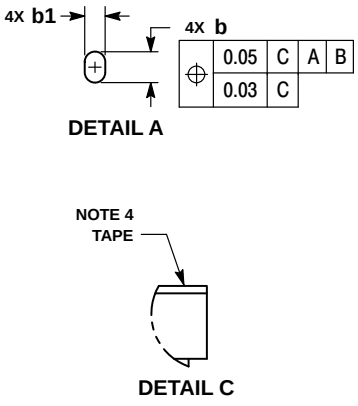
For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

TCP−4182UB

PACKAGE DIMENSIONS

WLCSP4, 1.009x0.609
CASE 567LZ
ISSUE O

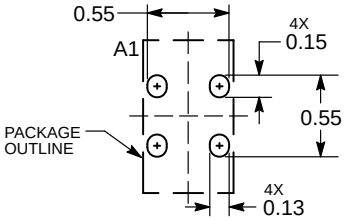




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.
4. BACKSIDE TAPE APPLIED TO IMPROVE PIN 1 MARKING.

DIM	MILLIMETERS	
	MIN	MAX
A	0.275	0.345
A1	0.045	0.085
b	0.079	0.129
b1	0.044	0.094
D	1.009 BSC	
E	0.609 BSC	
e	0.420 BSC	
e1	0.400 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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