SLWS008C – SEPTEMBER 1994 – REVISED JUNE 1996

- **Single Chip for AMPS/TACS Data and SAT Processing**
- **3.3-V or 5-V Operation**
- **Simple Serial Interface**
- **User-Configurable Interrupt Structure**
- **TX and RX Data Buffers**
- **Programmable Timer**
- **Independent Watchdog Timer**
- **RX/TX Automatic Mute Functions**
- **Arbitration Processing**
- **20 Programmable Expansion I/O Ports**
- **44-Pin Mini-QFP FR Package**

description

The TCM8002 provides the data transceiving, data processing, and SAT (supervisory audio tone) functions for the AMPS (advanced mobile phone service) and TACS (total access communications system) cellular telephone standards. A highly integrated device, the TCM8002 includes a number of additional functions that are helpful in the implementation of the typical cellular telephone. These extra functions include a watchdog timer, which is normally external to the telephone microcontroller, and two 8-bit- and one 4-bit-wide user-programmable general-purpose input/output ports. These can be used to provide port expansion for the microcontroller. An 8-bit counter/timer for user-defined purposes is also included.

To facilitate the application of the TCM8002 and to minimize the number of connections, a single serial interface to the microcontroller is used for controlling, receiving, and transmitting data. There is also a dedicated interface, including a compatible clock signal, to the companion TCM8010 audio processor that performs most of the audio processing required in a cellular telephone. Additional outputs are also provided for interfacing to other audio processors.

The TCM8002 is built using a low-power CMOS process and operates with a 5-V or 3.3-V power supply. When used in conjunction with the TCM8010, a unique and very compact low-power solution for AMPS/TACS baseband processing in 5-V and 3-V systems is realized.



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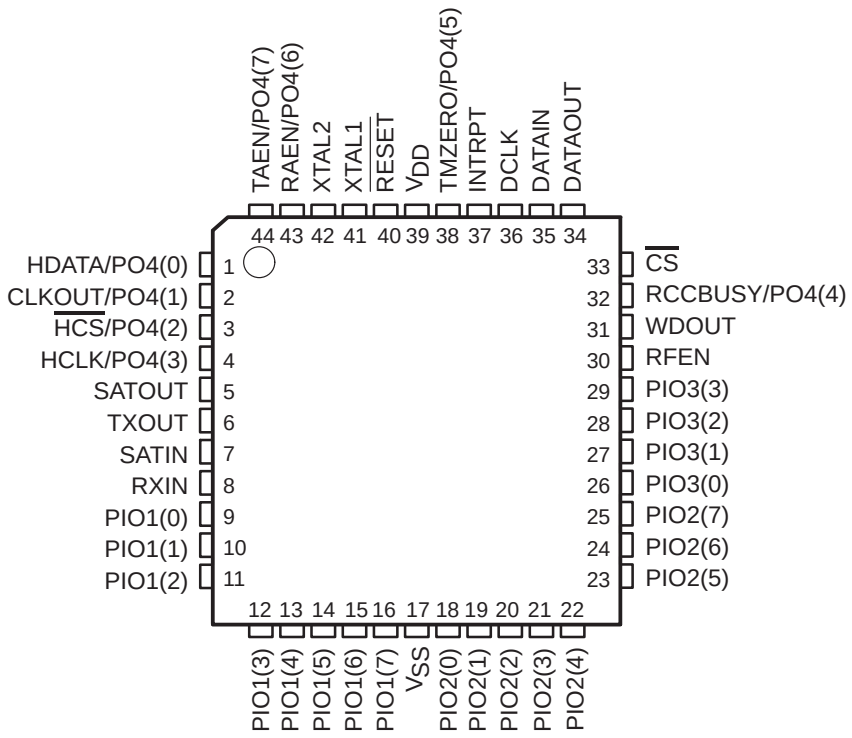
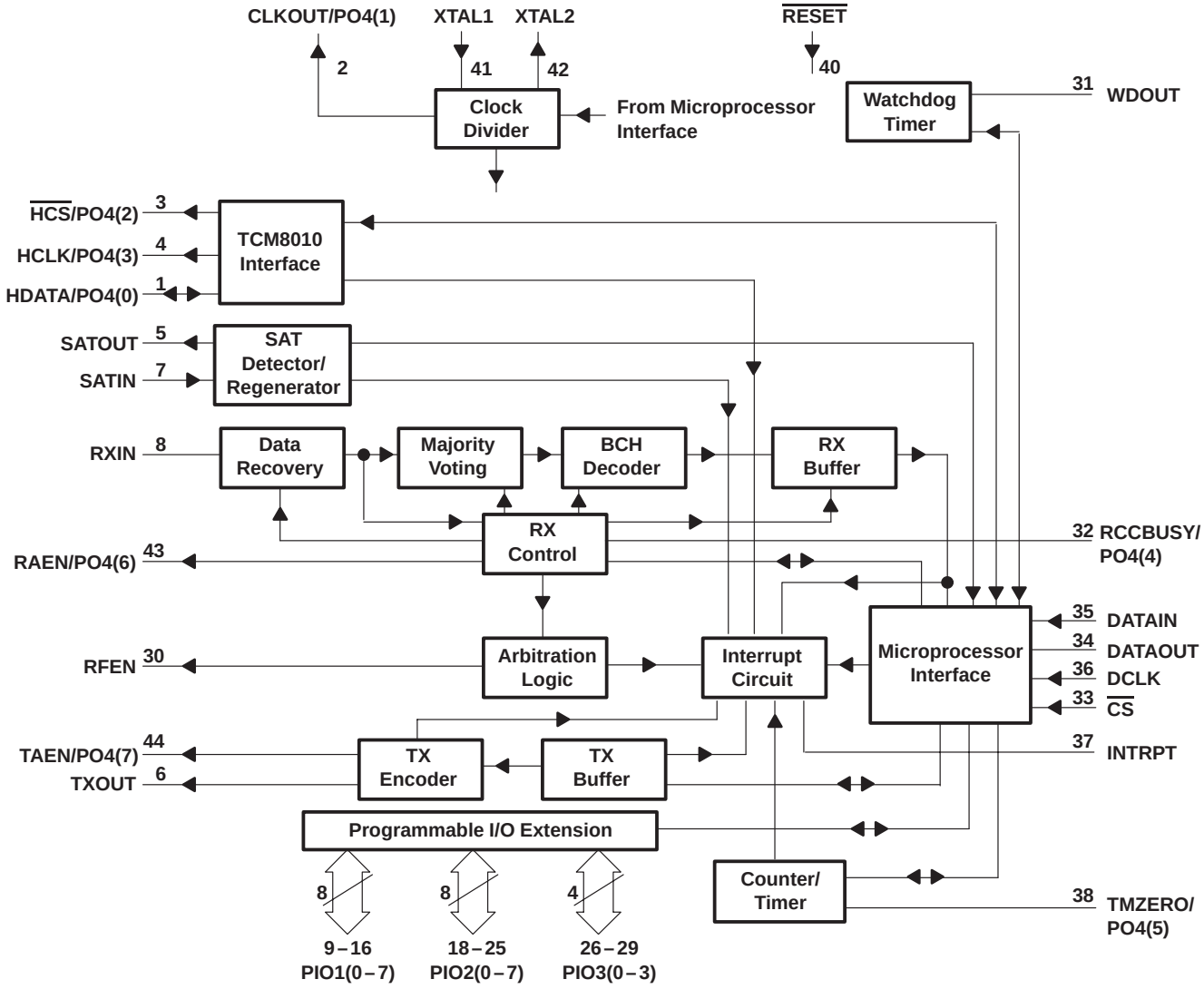
FR PACKAGE
(TOP VIEW)



functional block diagram



( ) = bit count

Terminal Functions†

TERMINAL‡ NAME	TERMINAL‡ NO.	I/O	DESCRIPTION
CLKOUT/PO4(1)	2	O	Clock output / programmable output #4, bit 1. A 2.56-MHz clock signal is output on this terminal or the device can be set so that it is bit 1 of PO4.
$\overline{CS}$	33	I	Chip select (active low). This is the chip select input from the microcontroller.
DATAIN	35	I	Data input. Serial data from the microcontroller is input on this terminal.
DATAOUT	34	O	Data output. This is the serial data output to the microcontroller (3-state).
DCLK	36	I	Data clock. This is the serial microcontroller interface clock input.
HCLK/PO4(3)	4	O	TCM8010 interface clock / programmable output #4, bit 3. A clock signal to the TCM8010 or bit 3 of programmable output 4 is output on this terminal.
HDATA/PO4(0)	1	I/O	TCM8010 interface data line/programmable output #4, bit 0. This terminal is used for data to and from the TCM8010, or is bit 3 of programmable output 4.
$\overline{HCS}$/PO4(2)	3	O	TCM8010 interface chip select output (active-low) / programmable output #4, bit 2. This terminal selects the TCM8010, or is bit 2 of programmable output 4.
INTRPT	37	O	Interrupt output. This is the interrupt line to the microprocessor.
PIO1(0–7)	9–16	I/O	Programmable I/O port #1, bits 0 – 7. This 8-bit port can be configured as either inputs or outputs (microcontroller port expansion).
PIO2(0–7)	18–25	I/O	Programmable I/O port #2, bits 0 – 7. This 8-bit port can be configured as either inputs or outputs (microcontroller port expansion).
PIO3(0–3)	26–29	I/O	Programmable I/O port #3, bits 0 – 3. This 4-bit port can be configured as either inputs or outputs (microcontroller port expansion).
RAEN/PO4(6)	43	O	Receive audio enable output/programmable output #4, bit 6. This terminal is used to enable the receive audio section of the phone, or is bit 6 of programmable output 4 (open drain).
RCCBUSY/PO4(4)	32	O	RECC busy status/programmable output #4, bit 4. This terminal outputs the status result of the majority vote of the three most recent busy/idle bits, or is bit 4 of programmable output 4.
$\overline{RESET}$	40	I	Reset input, active low. A low applied to this terminal resets the TCM8002 and loads the default values listed in the write map.
RFEN	30	O	RF enable. This terminal is used to enable the transmitter section of the phone (open drain).
RXIN	8	I	Baseband Manchester data input. Manchester-encoded data from control or voice channel is input on this terminal.
SATIN	7	I	SAT input. Square-wave SAT data from the TCM8010 audio processor is input on this terminal.
SATOUT	5	O	Regenerated SAT output. Regenerated SAT data is output to the TCM8010 audio processor on this terminal.
TAEN/PO4(7)	44	O	Transmit audio enable/programmable output #4, bit 7. The logic level on this terminal changes state during RVC message or ST transmission, or is bit 7 of programmable output 4 (open drain).
TMZERO/PO4(5)	38	O	Timer zero/programmable output #4, bit 5. The logic level on this terminal changes state when the counter/timer passes or reaches zero, or is bit 5 of programmable output 4.
TXOUT	6	O	Transmit data output. Encoded transmit data is output to the TMC8010 audio processor on this terminal.
V_{DD}	39		Positive supply voltage. Input is 3.3-V or 5-V.
V_{SS}	17		Ground supply voltage.
WDOUT	31	O	Watchdog timer output. A logic-low pulse is output on this terminal when the watchdog timer times out.
XTAL1	41	I	Crystal terminal 1/external clock source input. An external crystal is connected to this terminal for the internal clock oscillator. An external clock signal can also be input on this terminal.
XTAL2	42	O	Crystal terminal 2. An external crystal is connected to this terminal for the internal clock oscillator.

† All inputs feature Schmitt triggers. All of the PIO terminals also feature optional 10-μA pullups.
‡ ( ) = bit count when in the terminal column

detailed description

Data communication between the mobile station and the land station in AMPS and TACS systems is achieved over forward and reverse control channels when a call is not in progress, or in short bursts over the forward and reverse voice channels when a call is in progress. The TCM8002 device has a receive path that recovers data from the FOCC (forward control-channel) and FVC (forward voice-channel) formats. The transmit path encodes and formats data for the RECC (reverse control channel) and RVC (reverse voice channel).

For voice-channel communications, the received SAT is detected and regenerated for transmission. Communication with the microcontroller/microprocessor in the telephone is through a serial interface. The TCM8002 also provides interrupts to alert the processor to the occurrence of specific events. The receiver is made up of the Data Recovery, Majority Voting, BCH (Bose-Chaudhuri-Hocquenghem) Decoder, RX Buffer, Arbitration Logic, and RX Control blocks. The SAT Detector/Regenerator is used during FVC reception and RVC transmission.

The transmit path consists of the TX Buffer and TX Encoder blocks. A serial microprocessor interface and the interrupt logic are also provided. Four ancillary functions are included:

- TCM8010 interface
- Watchdog Timer
- Counter/Timer
- twenty programmable digital bidirectional I/O lines (eight of the output terminals can be reconfigured as processor output ports)

clock divider

The clock signal for the TCM8002 is supplied in two ways:

- A crystal can be connected to XTAL1 and XTAL2.
- A clock signal from another source can be connected to XTAL1.

When a crystal is used, a resistor (typical value 1 MΩ) should be connected between XTAL1 and XTAL2 to provide a bias for the oscillator. The crystal frequency must be 2.56 MHz, 5.12 MHz, 7.68 MHz, or 10.24 MHz. If an external clock signal is connected, it must be at one of these crystal frequencies or one of two additional frequencies: 15.36 MHz or 20.48 MHz.

The clock frequency defaults to 2.56 MHz when the TCM8002 is reset. The clock-divider circuit provides a 2.56-MHz clock for internal use and must be configured according to the selected crystal or external clock frequency. Control word 2, bits 5 and 6, and control word 4, bit 1, are used to configure the clock divider. The output from the clock-divider circuit is provided at CLKOUT and is always 2.56 MHz. This can be used to clock the TCM8010 advanced audio processor.

The bit rate of the transmitted Manchester-encoded data, the signaling-tone frequency, and the accuracy of the SAT measurement are all determined by the crystal or external clock. The AMPS and TACS system requirements both specify a maximum transmitted bit frequency error of ±100 ppm; therefore, over the operating temperature range of the phone, the crystal or clock frequency error must be no more than ±100 ppm.

absolute maximum ratings over operating temperature range†

Supply voltage range, V_{DD}, V_{SS} (see Note 1) . . . . . –0.5 V to 6 V
Input voltage range, V_I . . . . . –0.5 V to V_{DD} + 0.5 V
Output voltage range (includes open-drain outputs), V_O . . . . . –0.5 V to V_{DD} + 0.5 V
Operating ambient temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage Values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	V_{DD} = 3 V	2.7	3.3	3.6	V
	V_{DD} = 5 V	4.5	5	5.5	
Input voltage, V_I		0		V_{DD}	V
Output voltage, V_O		0		V_{DD}	V
High-level input voltage, V_{IH}		0.7 V_{DD}			
Low-level input voltage, V_{IL}	V_{DD} = 3 V			0.3 V_{DD}	V
	V_{DD} = 5 V			0.2 V_{DD}	
Operating ambient temperature range, T_A		–40	25	85	°C

electrical characteristics over recommended operating conditions, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –0.9 mA	V_{DD}–0.55			V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.5	V
V_{IT+}	Positive-going input threshold voltage				0.7 V_{DD}	V
V_{IT-}	Negative-going input threshold voltage		0.3 V_{DD}			V
V_{hys}	Hysteresis ($V_{IT+} - V_{IT-}$)		0.1 V_{DD}		0.3 V_{DD}	V
I_{OZ}	High-impedance output current	V_I = V_{DD} or V_{SS}			±10	µA
I_{IL}	Low-level input current	V_I = V_{SS}			–1	µA
I_{IH}	High-level input current	V_I = V_{DD}			1	µA
I_O	Pullup output current	V_I = V_{SS}	–2.12	–5.32	–10.18	µA
I_{DD}	Supply current with 2.56-MHz crystal	Default mode		1.4		mA
		Low-power mode		1.1		
		Low-power mode, SAT off		0.9		

electrical characteristics over recommended operating conditions, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	V_{DD} – 0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.5	V
V_{IT+}	Positive-going input threshold voltage				0.7 V_{DD}	V
V_{IT-}	Negative-going input threshold voltage		0.2 V_{DD}			V
V_{hys}	Hysteresis ($V_{IT+} – V_{IT-}$)		0.1 V_{DD}		0.3 V_{DD}	V
I_{OZ}	High-impedance output current	V_I = V_{DD} or V_{SS}			±10	µA
I_{IL}	Low-level input current	V_I = V_{SS}			–1	µA
I_{IH}	High-level input current	V_I = V_{DD}			1	µA
I_O	Pullup output current	V_I = V_{SS}	–7.2	–14.84	–24.47	µA
I_{DD}	Supply current with 2.56-MHz crystal	Default mode		3.6		mA
		Low-power mode		2.8		
		Low-power mode, SAT off		2.5		

timing requirements over recommended ranges of operating conditions (see Figure 1)

		MIN	MAX	UNIT
t_{su1}	Setup time, $\overline{CS}$ low before DCLK↑	300		ns
t_{h1}	Hold time, $\overline{CS}$ low after DCLK↓	300		ns
t_{su2}	Setup time, DATAIN before DCLK↑	300		ns
t_{h2}	Hold time, DATAIN after DCLK↑	300		ns
t_c	DCLK clock period (nominal)	1		µs
$t_{c(er)}$	DCLK clock period, Read start bit – Event Register	2		µs
$t_{c(or)}$	DCLK clock period, Read start bit – Other Register	1		µs
	Period that $\overline{CS}$ must be high between read or write operations	100		ns

PARAMETER MEASUREMENT INFORMATION

Figure 1 shows the timing for processor read and write operations. DATAOUT has a 3-state driver and normally presents the high-impedance state as shown in Figure 1. This allows DATAIN and DATAOUT be be tied together to a bidirectional microprocessor pin.

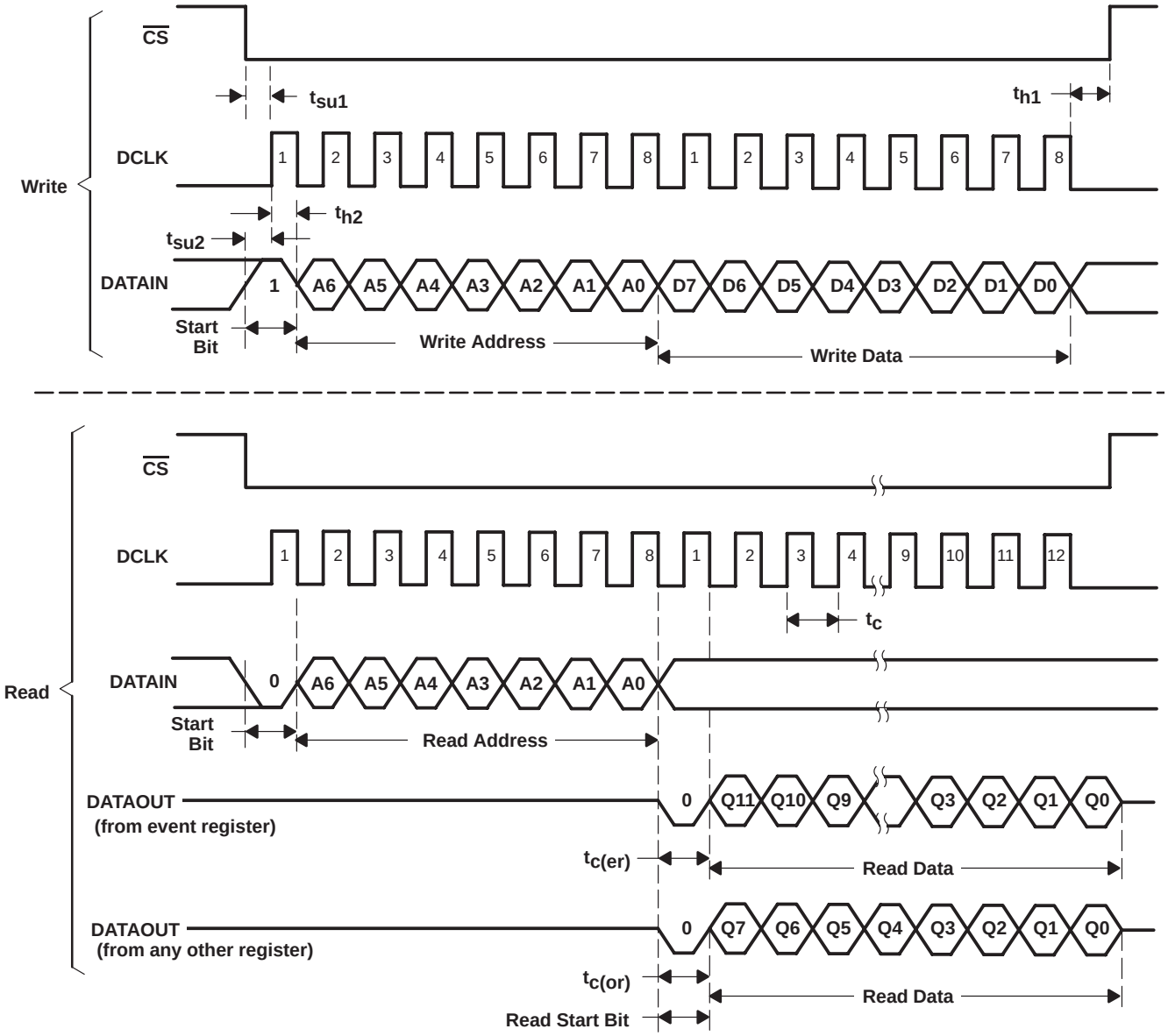


Figure 1. Microprocessor-Interface Timing

PRINCIPLES OF OPERATION

receive path

The following paragraphs detail the TCM8002 receive path, which includes the function blocks as given in the functional block diagram.

Data Recovery

The input to the Data Recovery block is RXIN and the signal applied to this terminal should be a digital version of the output from the FM demodulator/discriminator in the phone. Data recovery is performed by a digital phase-lock circuit with its center frequency at the designated bit rate (i.e., 10 kbps for AMPS and 8 kbps for TACS).

The dotting preamble produces a square wave with a frequency one-half of the bit rate and transitions at the center of each bit period. This is used by the data recovery circuit to acquire bit synchronization with the acquisition coefficient (DATAREC coef 1). After synchronization is achieved, the lock coefficient is used (DATAREC coef 2) to allow phase adjustment during subsequent occurrences of dotting.

RX Control

The receiver control circuit detects the dotting sequence and the frame synchronization code (11100010010). Once frame synchonization has been achieved, the received data stream is separated. The FOCC stream is separated into busy/idle bits, bits of word A, and bits of word B. Recovered FVC bits are separated into bits of the received word, dotting bits, and word sync bits. For both FOCC and FVC, a word repeat count is also maintained. For the FOCC, a count is maintained of the number of consecutive sync words matched and the number not matched. Two matches are required to acquire and confirm frame synchronization. Five consecutive mismatches indicate loss-of-frame synchronization.

During FOCC reception, the busy/idle bits are fed directly to the Arbitration Logic block. A majority vote of the most recent three busy/idle bits is made available at RCCBUSY and at status word 1, bit 4.

During FVC message reception, the receive audio enable output (RAEN) changes state. The output changes on frame synchronization and returns to the initial state 928 bit periods later. Status word 2, bit 1 is set for this period.

The receive audio circuit in a connected TCM8010 can be automatically controlled through the TCM8010 interface (see control word 2). During FVC wideband data reception, a copy of the previous TCM8010 control word 1 is resent with bits 0 and 1 set to 0, muting the received audio path. After the end of data reception, the original TCM8010 control word 1 is resent.

Majority Voting

The Majority Voting function performs a bit-wise majority vote on the repeated FOCC or FVC words. All five repeats of the (A or B) FOCC word are used and up to 11 repeats of the FVC word are used. The result is to recognize each of the 40 bits as a logic 0 or logic 1.

BCH Decoder

The error-correction circuit corrects the received BCH code. This is a 40-bit code word consisting of 28 data bits and 12 parity bits. The circuit is able to correct errors in the received majority-voted 40-bit word from the 12 parity bits. Up to two errors in either the data or parity can be detected. The corrected 28 data bits together with 4 correction status bits may be read from the RX data word 0 to RX data word 3 locations. In low-power mode, this block is turned on only when there is data to be corrected and is selected by control word 4, bit 0.

PRINCIPLES OF OPERATION

RX Buffer

The 28-bit output from the BCH Decoder is fed into the RX Buffer, which can then be read by the microprocessor. Every time new data is available, an interrupt is generated and a status bit is set. The interrupt may be masked. The data is read in four 8-bit bytes, and when the last byte (least significant bit) is read, the status bit is reset.

Arbitration Logic

During FOCC reception, the arbitration logic uses the busy/idle bits to determine the status of the RECC. The arbitration logic monitors the busy/idle status of the FOCC at the start of each RECC transmission. A collision is detected when the status becomes busy within the first 56 bit periods or when it remains idle after 104 bit periods. When a collision is detected, the arbitration-failure flag in the event register is set and an interrupt can be generated (depending on interrupt control word 1). RFEN changes state and the transmission of data to TXOUT is also aborted if bit 5 of control word 1 is set. To reset the state of RFEN and allow the transmission of data to TXOUT after an arbitration failure, it is necessary to reset the arbitration-fail latch by writing to address 26 (reset arbitration).

SAT Detector/Regenerator

The SAT detection and regeneration circuit takes the square wave at SATIN as its input. The detection and regeneration functions are performed by a digital phase-locked loop. The regenerated SAT is output at SATOUT. SAT determination is performed using this circuit and the result is updated every 0.2 seconds and then output to the microcontroller interface. The SAT color code (SCC) is determined from the frequency measurement and the result is available from status word 1, bit 6 and bit 7. If the SAT output frequency is outside of the SAT frequency range, the SAT is considered invalid and zeros are loaded into word 1, bit 6 and bit 7. In low-power mode (selected by control word 4, bit 0), this functional block can be turned off by control word 1, bit 7.

transmit path

The TCM8002 transmit path includes the following function blocks as given in the functional block diagram:

TX Buffer

The TX Buffer is a 36-bit buffer that is written to by the processor in five write operations. After the fifth write (the least significant bit), the TX buffer-available status bit is reset. The status bit is set when the transmit data is read by the TX Encoder.

TX Encoder

The TX Encoder reads the contents of the TX Buffer and then performs BCH encoding, Manchester encoding, and RECC or RVC frame formatting. The result is output at TXOUT. The encoding and transmit cycle is initiated by one of the following conditions:

- With the TX Encoder function not active, transmission is initiated by a processor write to the Commence-TX address.
- With data to be read from the TX Buffer and the TX Encoder active, transmission of the next frame follows directly after completion of an active frame and the seizure precursor is omitted.

Under processor control, the TX Encoder generates a signaling tone (ST), which is 10 kHz for AMPS and 8 kHz for TACS.

During RVC message transmission or ST transmission, the transmit audio enable output (TAEN) changes state.

The transmit audio circuit in a connected TCM8010 can be automatically controlled via the TCM8010 interface (see control word 2). During RVC wide-band data transmission, a copy of the previous TCM8010 control word 1 is resent with bit 5 cleared to 0 and bit 6 set to 1. This mutes the transmit audio path and enables the transmit data path. At the end of data reception, the original TCM8010 control word 1 is resent.

PRINCIPLES OF OPERATION

miscellaneous functions

The following paragraphs detail TCM8010 miscellaneous functions shown in the functional block diagram.

TCM8010 Interface

The TCM8010 Interface provides a serial communication channel to the TCM8010 advanced audio processor using terminals $\overline{\text{HCS}}$, HCLK, and HDATA.

Write operation: The TCM8010 address bits and data bits are written in two write operations to the TCM8010 interface with word 1 first and then word 0. On completion of the write to the TCM8010 interface word 0, the data is clocked out to the TCM8010 chip over the 3-wire serial interface. The TCM8010 interface status bit (status word 2, bit 0) indicates when the interface is active.

Read operation: The TCM8010 address bits and HCLK speed are written to the TCM8010 interface word 0. This initiates an A/D conversion and results in retrieval using the 3-bit serial interface. The status bit (status word 2, bit 0) is set for the duration of the interaction. On completion, the 8-bit result can be read from the TCM8010 result location. The HCLK speed is detailed in Table 1.

Table 1. TCM8010 HCLK Speed Control Bits (Interface Word 0)

7	6	5	4	HCLK SPEED CONTROL BITS		1	0	HCLK SPEED IN kHz
				3	2			
0	TCM8010 Read Address			0	0	X	X	20
				0	1			40
				1	0			80
				1	1			160

Counter/Timer

The Counter/Timer is an 8-bit down counter that counts at the bit rate (i.e., 10 kHz for AMPS, 8 kHz for TACS). This circuit can be configured to repeatedly count down from the programmed coefficient or to count down once only and stop at zero. A countdown is initiated by a write to the coefficient location. TMZERO can be used to detect when the counter passes/reaches zero. When the counter/timer is configured to cycle continuously, TMZERO changes state for one bit period. An interrupt can also be generated.

Watchdog Timer

The watchdog timer provides a timeout of a minimum of 1 second to a maximum of 1.2 seconds. The timer is initially started by the first write to address 21 (start/restart watchdog). After this first write, timeout is prevented by writing to the watchdog timer address at intervals not exceeding 1 second.

When timeout occurs, WDOUT pulses low for 100 μs (AMPS operation) or 125 μs (TACS operation) and RFEN changes state, but the data in the control registers remain unchanged. It is then necessary to reset the TCM8002 to return the RFEN output to its original state.

WDOUT is also held low for the duration of a low input at $\overline{\text{RESET}}$. WDOUT remains high in its normal (high) state during a software reset (write to location reset).

PRINCIPLES OF OPERATION

Programmable I/O Extension

The Programmable I/O Extension provides processor port expansion. PIO1(0–7), PIO2(0–7), and PIO3(0–3) can be configured as either inputs or outputs. For those pins configured as outputs, the output values are set through the microprocessor interface. The values at all of the ports can be read through the microprocessor interface.

Eight output terminals can also be configured as programmable outputs instead of the named functions. The programmable outputs are the terminals with the /PO4(. . .) in their names. All inputs feature Schmitt triggers and all the PIO terminals feature optional 10-μA pullups.

$\overline{\text{RESET}}$

A low logic level at $\overline{\text{RESET}}$ performs a chip reset. The default values listed in the write address map are loaded.

microcontroller interface

The TCM8002 microcontroller interface is described in subsequent paragraphs.

write

For a write operation, $\overline{\text{CS}}$ is taken low and data on DATAIN is clocked into the TCM8002 on each rising edge of DCLK. It is important that $\overline{\text{CS}}$ is taken low when DCLK is low for the correct operation of the read/write selection logic in the microprocessor interface. The input sequence is start bit (logic 1), 7-bit address, then 8 bits of data. The operation is completed by $\overline{\text{CS}}$ returning to a high logic level with DCLK low. If DCLK is not low, an extra clock pulse is required. The address and data to be written to control the TCM8002 and to transmit Manchester-encoded signals are detailed in the write address map (Table 2). Eight bits of data are always written to the interface and data is right-justified. When writing to addresses 20 – 26, it is necessary to supply clock cycles to write dummy data to the microprocessor interface to start the actions. The state of DATAIN during these write-data clock cycles is not important.

read

For a read operation, the start bit is cleared to 0. Following the seven address bits, DATAOUT is enabled and the output data is updated on each falling edge of DCLK. DCLK must be low when $\overline{\text{CS}}$ is taken low for correct operation of the read/write selection logic in the microprocessor interface. The operation is completed by $\overline{\text{CS}}$ returning to a high logic level with DCLK low. When DCLK is not low, an extra clock pulse is required.

When reading from the event register only, DCLK must be changed from its nominal period of 1 μs to a period of 2 μs so that the start bit is 2 μs long. This can be accomplished by skipping a clock pulse while the start bit is low. Reading from all other registers requires no adjustment to the DCLK nominal period of 1 μs.

DATAOUT returns to the high-impedance state when $\overline{\text{CS}}$ returns high. During the read operation, eight bits of data are output on DATAOUT in the order of bit 7 to bit 0. During a read from the event register, however, 12 bits of data appear in the order of bit 11 to bit 0; i.e., 12 DCLK cycles should be made before $\overline{\text{CS}}$ returns high. The data is right-justified.

Interrupt Circuit

Interrupt-control words 1 and 2 are used to program which events cause an interrupt. When any of the events occur, the associated bit of the event register is set. INTRPT is set whenever an enabled interrupt occurs.

When the event register is read, its contents are first transferred to a buffer and the register is cleared. The bits are then read out in series. At the end of the read sequence, INTRPT is reset. When an interrupt event occurs during the read operation, INTRPT remains low for approximately 1 μs and then returns high.

PRINCIPLES OF OPERATION

write address map

Table 2 shows the write address map. Table 3 through Table 12 explain control words listed in Table 2; the other addresses are described in subsequent paragraphs.

Table 2. Write Address Map

ADDRESS (7 BITS) HEX	NAME	FUNCTION	NO. OF SIGNIFICANT BITS	DEFAULT VALUE
00	Control Word 1	Operational control word	8	00
01	Control Word 2	Operational control word	8	00
02	Control Word 3	Signal polarity selection	8	00
03	Interrupt Control Word 1	Interrupt enables	7	00
04	Interrupt Control Word 2	Interrupt enables	5	00
05	PIO1 Control Word	PIO1 direction selection	8	00
06	PIO1 Output Word	PIO1 values for outputs	8	00
07	PIO2 Control Word	PIO2 direction selection	8	00
08	PIO2 Output Word	PIO2 values for outputs	8	00
09	PIO3 Control Word	PIO3 direction selection	4	00
0A	PIO3 Output Word	PIO3 values for outputs	4	00
0B	PO4 Control Word	PO4 configuration selection	8	00
0C	PO4 Output Word	PO4 values for selected terminals	8	00
20	Commence TX	Commence TX command	0	—
21	Start Watchdog	Start/restart watchdog	0	—
22	Abort TX	Abort TX command	0	—
23	Clear TX Buffer	Clear TX buffer command	0	—
24	Restart Frame Sync	Restarted frame-sync command	0	—
25	Reset	Reset chip command	0	—
26	Reset Arbitration	Reset arbitration circuit	0	—
40	TX Data Word 0	TX data bits 35–32	4	00
41	TX Data Word 1	TX data bits 31–24	8	00
42	TX Data Word 2	TX data bits 23–16	8	00
43	TX Data Word 3	TX data bits 15–8	8	00
44	TX Data Word 4	TX data bits 7–0 (LSBs)	8	00
48	TCM8010 Interface Word 0	Read/write bit, address and D9 – D6	8	00
49	TCM8010 Interface Word 1	TCM8010 data bits D5 – D0	6	00
4D	Counter/Timer Coef	Coef and start command	8	00
50	SAT Coef	SAT circuit-time constant coefficient	5	20
51	DATAREC Coef 1	Acquisition coefficient	6	16
52	DATAREC Coef 2	Lock coefficient	6	63
53	Control Word 4	Operational control word	2	00
57	Mismatch	Frame mismatch coefficient	4	04
59	FOCC Dotting	Detect coefficient	4	07
5A	FVC Dotting	Detect coefficient	7	29

PRINCIPLES OF OPERATION

Table 3. Address 00 – Control Word 1

BIT	FUNCTION (WHEN BIT IS SET)
0	Enable SATOUT output
1	Signalling tone (ST) select (to TXOUT)
2	Voice-channel operation (RVC) (not control channel RECC)
3	Digital color code first bit (DCC) (see Table 4)
4	Digital color code second bit (DCC) (see Table 4)
5	Enable RFEN and TOUT; disable on detection of an arbitration fail
6	Timer/counter continuously cycles
7	Disable SAT detector and regenerator (only in low-power mode)

The translation between the 2-bit DCC code and the transmitted data is shown in Table 4.

Table 4. Two-Bit DCC Code Translation

CONTROL WORD 1		TRANSMITTED CODE
BIT4	BIT3	
0	0	0000000
0	1	0011111
1	0	1100011
1	1	1111100

Table 5. Address 01 – Control Word 2

BIT	FUNCTION (WHEN BIT IS SET)
0	AMPS (not TACS)
1	FOCC B word (not A word)
2	Enable automatic control of TCM8010 receive audio circuit through the TCM8010 interface
3	Enable automatic control of TCM8010 transmit audio circuit through the TCM8010 interface
4	Disable all 10-μA pullups of PIO1, PIO2, and PIO3
5	Clock selection (along with bit 1 of control word 4)
6	Clock selection (along with bit 1 of control word 4)
7	TCM8010 interface write-speed selection

PRINCIPLES OF OPERATION

Table 6. Clock-Selection Bits

CONTROL WORD 4	CONTROL WORD 2			SELECTED CLOCK FREQUENCY	TCM8010 INTERFACE CLOCK
BIT 1	BIT 7	BIT 6	BIT 5		
0	0	0	0	2.56 MHz	320 kHz
0	0	0	1	5.12 MHz	320 kHz
0	0	1	0	7.68 MHz	320 kHz
0	0	1	1	10.24 MHz	320 kHz
0	1	0	0	2.56 MHz	1.28 MHz
0	1	0	1	5.12 MHz	1.28 MHz
0	1	1	0	7.68 MHz	1.28 MHz
0	1	1	1	10.24 MHz	1.28 MHz
1	0	0	0	Not used	Not used
1	0	0	1	Not used	Not used
1	0	1	0	15.36 MHz	320 kHz
1	0	1	1	20.48 MHz	320 kHz
1	1	0	0	Not used	Not used
1	1	0	1	Not used	Not used
1	1	1	0	15.36 MHz	1.28 MHz
1	1	1	1	20.48 MHz	1.28 MHz

Table 7. Address 02 – Control Word 3 Functions

BIT	FUNCTION (WHEN BIT IS SET)
0	Invert polarity of RXIN
1	Invert polarity of TXOUT
2	Invert polarity of RFEN†
3	Invert polarity of INTRPT, active low
4	RAEN active low†
5	TAEN active low†
6	TMZERO active low
7	RCCBUSY active low

† RFEN, RAEN, and TAEN have open-drain output drivers. These drivers have active pulldowns and require provision of external pullups.

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Table 8. Address 03 – Interrupt-Control Word 1

BIT	INTERRUPT ENABLED (WHEN BIT IS SET)
0	RX data available
1	TX buffer available
2	Arbitration failure
3	TX sequence completed
4	Change of RECC bus/idle status
5	Counter/timer reaches zero state
6	SAT measurement decision changes

Table 9. Address 04 – Interrupt-Control Word 2

BIT	INTERRUPT ENABLED (WHEN BIT IS SET)
0	TCM8010 interface activity completed
1	FVC dotting detected
2	FVC frame sync achieved
3	Change of FOCC frame-sync status
4	SAT measurement update (every 0.2 seconds)

Table 10. Address 05 – PIO1 Control Word

BIT (0 – 7)	CORRESPONDING TERMINAL FUNCTION (0 – 7)
0	Input
1	Output

The eight terminals of the port are configured as inputs by default. The terminals have programmable 10-μA pullups that can be disabled using bit 4 of control word 2.

address 06 – PIO1 output word

This sets the state of the PIO1 terminals when configured as outputs.

address 07 – PIO2 control word

This selects whether the individual port 2 terminals are configured as inputs or outputs.

address 08 – PIO2 output word

This sets the state of the PIO2 terminals when configured as outputs.

address 09 – PIO3 control word

This selects whether the individual port 3 terminals are configured as inputs or outputs.

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address 0A – PIO3 output word

This sets the state of the PIO3 terminals when configured as outputs.

address 0B – PO4 control word

The eight output terminals HDATA, CLKOUT, $\overline{\text{HCS}}$, HCLK, RCCBUSY, TMZERO, RAEN, and TAEN can be independently reconfigured as outputs. Control bits set the terminals as programmable outputs.

address 0C – PO4 output word

This sets the value of the PO4 terminals configured as outputs. RAEN and TAEN remain open-drain outputs when configured as programmable outputs.

address 20 – commence TX

Writing to address 20 transfers data from the TX Buffer to the TX Encoder and starts the encoding and transmission of the data.

address 21 – start watchdog

Writing to address 21 starts one cycle of the Watchdog Timer.

address 22 – abort TX

Writing to address 22 immediately stops a transmission sequence that is in progress.

address 23 – clear TX buffer

Writing to address 23 clears the contents of the TX Buffer. This command can be used to stop the automatic transmission of a second word written to the TX Buffer when the TX Encoder is active. This command does not stop the complete transmission of the first word.

address 24 – restart frame sync

Writing to address 24 resets the data-recovery circuit, which then uses the acquisition coefficient initially to achieve bit synchronization to the received data. It can be used when the phone switches to a new FOCC (forward control channel) to reduce the time taken to acquire bit synchronization. The data-recovery circuit does not have to wait until it has detected loss of bit synchronization to change from using the lock coefficient to using the acquisition coefficient.

address 25 – reset

Writing to address 25 performs a device reset. Its function is identical to that of $\overline{\text{RESET}}$ except that it does not affect WDOUT. The default values listed in the write address map are then loaded.

address 26 – reset arbitration

Writing to address 26 resets the arbitration-failure circuit.

addresses 40 to 44 – TX data words 0 to 4

The data to be transmitted is written to these five addresses, thereby loading the TX Buffer.

PRINCIPLES OF OPERATION

address 48 – TCM8010 interface word 0

Table 11. Interface Word 0

BIT	FUNCTION
7	Value = 0 for TCM8010 read operation, 1 for write operation
6–4	TCM8010 address
3–0	TCM8010 write data bits D9–D6

Writing to the TCM8010 interface word 0 initiates a TCM8010 interaction. The result of any read operation (i.e., an ADC conversion result) can be accessed by a subsequent read from the TCM8010 result location.

address 49 – TCM8010 interface word 1

These are the TCM8010 data bits D5 to D0.

address 4D – counter/timer coefficient

Writing to address 4D sets the count length and starts a down count from the value written.

address 50 – SAT coef

This coefficient controls the SAT detector digital phase-locked loop time constant.

address 51 – DATAREC coef 1

This controls the data-recovery circuit acquisition performance before bit synchronization is achieved.

address 52 – DATAREC coef 2

This controls the data-recovery circuit lock performance after bit synchronization is achieved.

address 53 – control word 4

Table 12. Control Word 4

BIT	FUNCTION (WHEN BIT IS SET)
0	Low-power mode select
1	Clock selection (with control word 2)

With low-power mode selected, the BCH decoder circuit is turned on only when there is data to be error-corrected. The SAT detector and regenerator can be turned off when not required (control word 1).

address 57 – mismatch

This relates to the number of successive frames that are not recognized during data recovery before bit synchronization is searched again.

address 59 – FOCC dotting

This is a coefficient for the data-recovery circuit and is related to how much of the dotting preamble of the forward control channel data is required before it is accepted that bit synchronization has been achieved.

address 5A – FVC dotting

This is a coefficient for the data-recovery circuit and is related to how much of the dotting preamble of the forward voice channel data is required before it is accepted that bit synchronization has been achieved.

PRINCIPLES OF OPERATION

read address map

Table 13 shows the read address map. This is followed by an explanation of all the bits contained in this address map including detailed information in Table 14 through Table 19.

Table 13. Read Address Map

ADDRESS (7 BITS) HEX	NAME	FUNCTION	NO. OF SIGNIFICANT BITS
00	Status Word 1	Status word 1	8
01	Status Word 2	Status word 2	3
02	Event Register	Event register	12
04	PIO1 Status Word	State of PIO1 terminals	8
05	PIO2 Status Word	State of PIO2 terminals	8
06	PIO3 Status Word	State of PIO3 terminals	4
10	RX Data Word 0	RX bits 27–20	8
11	RX Data Word 1	RX bits 19–12	8
12	RX Data Word 2	RX bits 11–4	8
13	RX Data Word 3 (bits 7–4)	RX bits 3–0 and error-correction status	8
18	Uncorrected RX Data Word 0	Uncorrected received data bits 39–32	8
19	Uncorrected RX Data Word 1	Uncorrected received data bits 31–24	8
1A	Uncorrected RX Data Word 2	Uncorrected received data bits 23–16	8
1B	Uncorrected RX Data Word 3	Uncorrected received data bits 15–8	8
1C	Uncorrected RX Data Word 4	Uncorrected received data bits 7–0	8
1D	RX Repeat Count	Number of word repeats used for the majority voting	4
20	TCM8010 Result	8-bit result of TCM8010 A/D conversion	8
30	SAT (supervisory audio tone)	SAT frequency measurement	8

Table 14. Address 00 – Status Word 1

BIT	STATUS (WHEN BIT IS SET)
0	RX data available
1	TX buffer available
2	Most recent TX aborted or arbitration failure
3	TX encoder active
4	RECC busy (not idle)
5	Counter/timer at zero state
6	SAT frequency band as detailed in Table 13
7	SAT frequency band as detailed in Table 13

PRINCIPLES OF OPERATION

Table 15. SAT Frequency Band

STATUS WORD 1		MEASURED FREQUENCY
BIT 7	BIT 6	
0	0	6047 Hz < f < 5957 Hz†
0	1	5957 Hz < f < 5987 Hz
1	0	5987 Hz < f < 6017 Hz
1	1	6017 Hz < f < 6047 Hz

† This indicates an invalid SAT.

Table 16. Address 01 – Status Word 2

BIT	STATUS (WHEN BIT IS SET)
0	TCM8010 interface active
1	FVC message being received
2	In FOCC frame sync

Table 17. Address 02 – Event Register

BIT	OCCURRENCES SINCE PREVIOUS READ OF THIS WORD (WHEN BIT IS SET)
0	RX data available
1	TX buffer available
2	Arbitration failure
3	TX sequence completed
4	Change of FOCC busy/idle status
5	Counter/timer reaches zero state
6	SAT result changed value
7	TCM8010 interface activity completed
8	FVC dotting detected
9	FVC frame sync achieved
10	Change of FOCC frame-sync status
11	SAT measurement update (every 0.2 seconds)

These flags indicate which event(s) have occurred since the previous read, regardless of their associated interrupt control bits.

addresses 04, 05, and 06 – PIO1, PIO2, and PIO3 status words

These registers contain the states of the PIO1, PIO2, and PIO3 terminals.

address 10 – RX data word 0

This register contains the corrected received data bits 27–20.

address 11 – RX data word 1

This register contains the corrected received data bits 19–12.

address 12 – RX data word 2

This register contains the corrected received data bits 11–4.

PRINCIPLES OF OPERATION

address 13 – RX data word 3

This register contains the corrected received data bits 3–0 and the error-correction status detailed in Table 17.

Table 18. Received Data Word 3

BIT	FUNCTION
7	RX data bit 3
6	RX data bit 2
5	RX data bit 1
4	RX data bit 0
3–0	Received-data decode status

Table 19. Error-Correction Status

RECEIVED DATA WORD 3				DECODE STATUS
BIT 3	BIT 2	BIT 1	BIT 0	
0	0	0	0	No errors detected
0	0	0	1	One error detected in parity bits
0	0	1	0	Two errors detected in parity bits
0	0	1	1	Not used
0	1	0	0	One error corrected in data
0	1	0	1	One error corrected in data, one error detected in parity bits
0	1	1	0	Not used
0	1	1	1	Not used
1	0	0	0	Two errors corrected in data
1	0	0	1	Not used
1	0	1	0	Not used
1	0	1	1	Not used
1	1	0	0	More than two erasures occurred (see Note 2). Up to two data bits are corrected.
1	1	0	1	More than two erasures occurred (see Note 2). One error detected in parity bits. Up to one data bit are corrected.
1	1	1	0	More than two erasures occurred (see Note 2). Two errors in parity bits are detected.
1	1	1	1	More than two errors detected. Data is not corrected.

NOTE 2: A bit erasure occurs when the bit is detected an equal number of times as a 1 and as a 0 over the valid repeats.

PRINCIPLES OF OPERATION

addresses 18 to 1C – uncorrected received data

The uncorrected received data can be read from the five uncorrected received data words. The 12 LSBs are the received parity bits, and the remaining 28 bits are the received data.

address 1D – received repeat count

The received repeat count gives the number of repeats of the received word that were used by the bit-wise majority voting circuit to generate the uncorrected received data.

address 20 – TCM8010 read result

Address 20 contains the ADC result retrieved from the TCM8010 audio processor. This data is valid once the TCM8010 interface has completed the read operation.

address 30 – SAT (supervisory audio tone)

The SAT tone provides the SAT frequency measurement in 2's-complement format with a resolution of 1 Hz and with respect to the frequency of 6 kHz, as shown in Table 20.

Table 20. SAT Frequency Measurements

FREQUENCY IN kHz	MEASUREMENT CODE
6.004	00000011
6.000	11111111
5.996	11111011

APPLICATION INFORMATION

Figure 2 shows a typical complete baseband solution using a TCM8002 data processor and a TCM8010 audio processor.

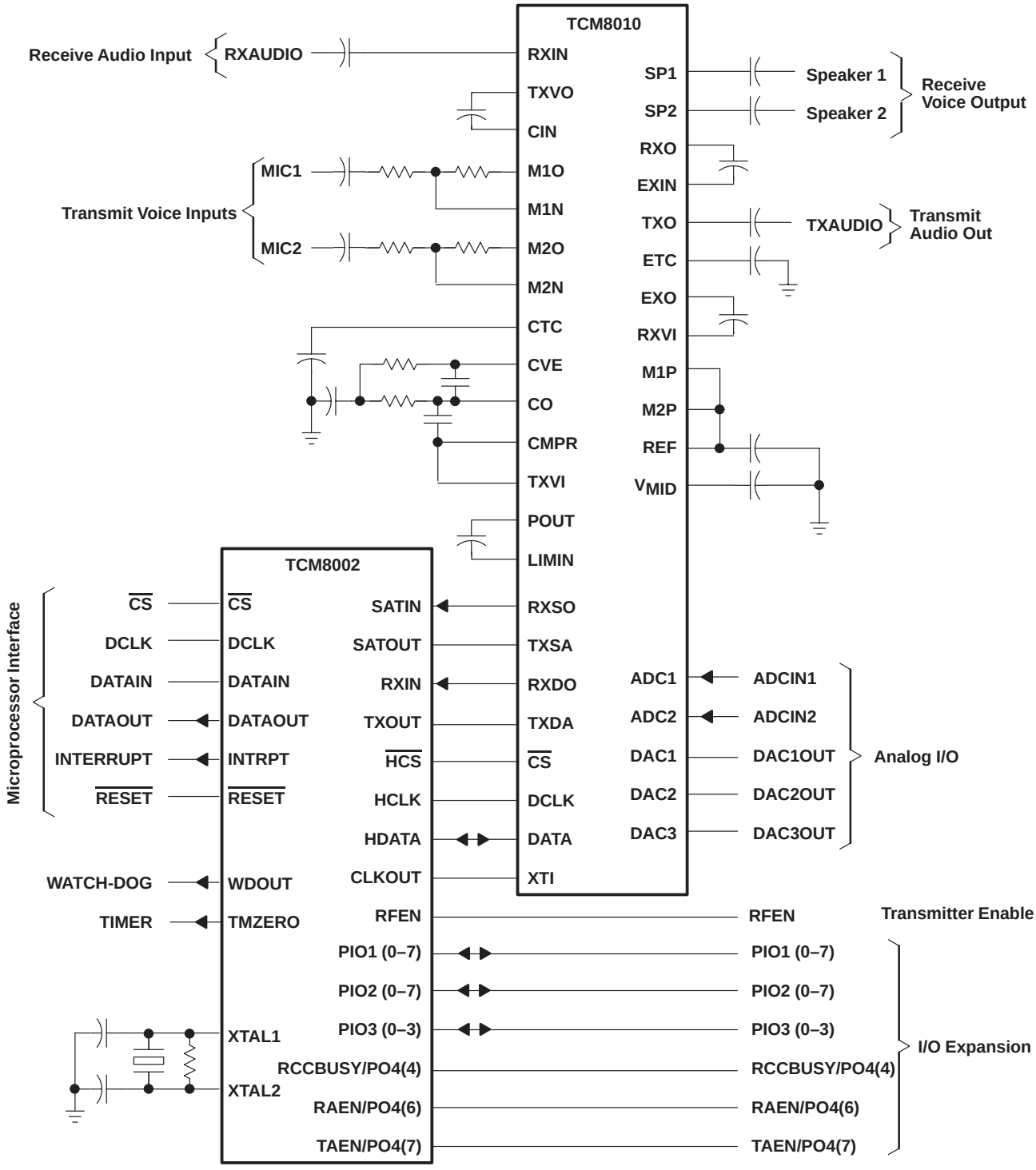
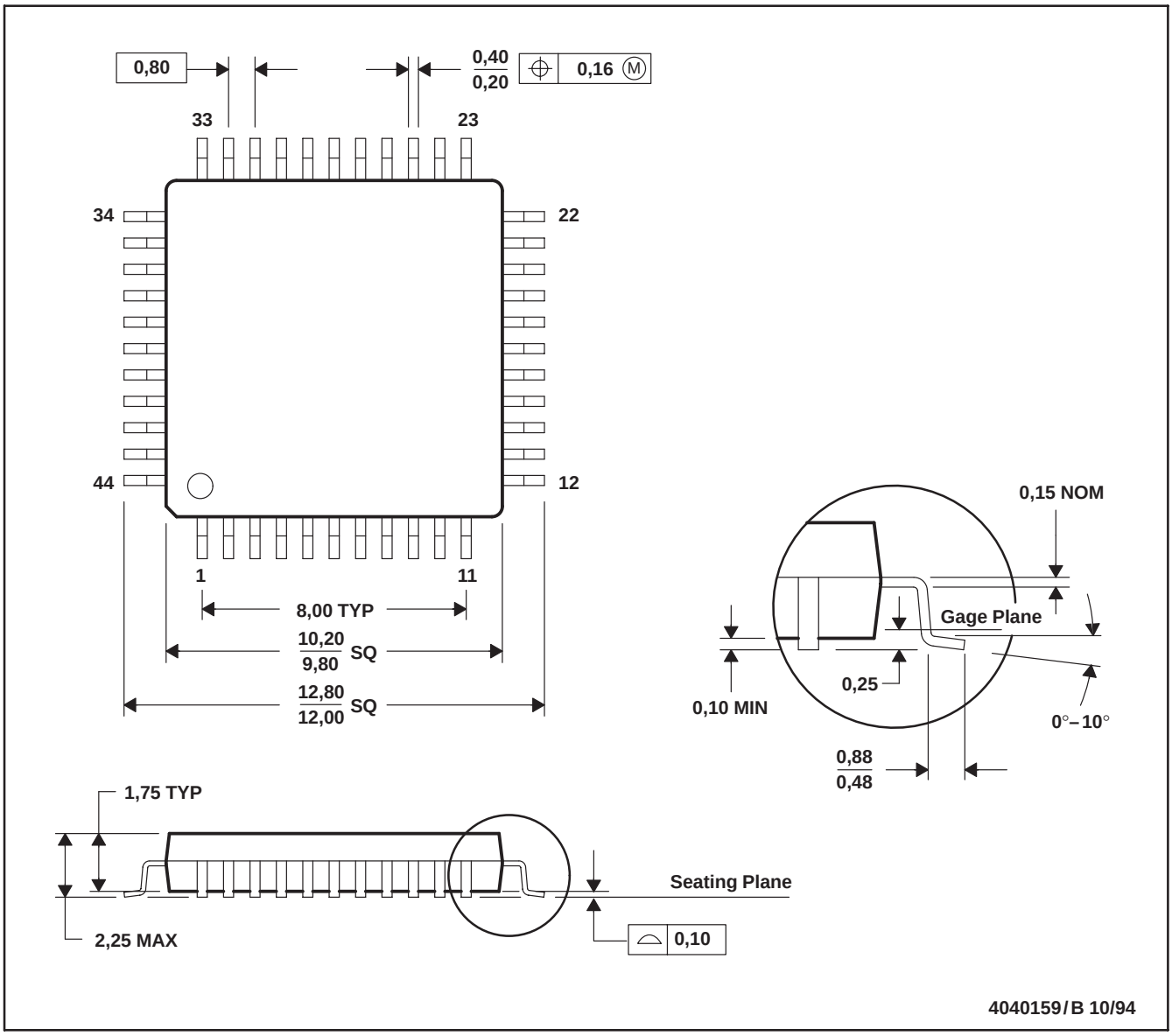


Figure 2. Complete Baseband Solution

FR (S-PDFP-G44) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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