TCM4400
Data Manual

GSM/DCS Baseband and Voice A/D D/A Interface Circuit

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1 Introduction

The TCM4400 global system for mobile communication (GSM) baseband RF interface circuit is designed for GSM 900 and DCS 1800 European digital cellular systems (DCS), and PCS 1900 North America personal communications systems (PCS). It includes a complete set of functions to perform the interface and processing of voice signals, generate baseband in-phase (I) and quadrature (Q) signals, and control the signals between a digital signal processor (DSP) and associated RF circuits.

The TCM4400 includes a second serial interface for use with a microcontroller. Through this interface, a microcontroller can access all the internal registers that can be accessed through the DSP digital serial interface. This option is for applications in which part of the L1 software is implemented in the microcontroller.

A 4-pin parallel port is dedicated to the full control of the digital audio interface (DAI) to the GSM system simulator; the DAI consists of system simulator reset (SSRST) control, clock generation, and rate adaptation with the DSP.

The voice processing portion of the device includes microphone and earphone amplifiers, analog-to-digital converter (ADC) and digital-to-analog converter (DAC), speech digital filtering, and a serial port.

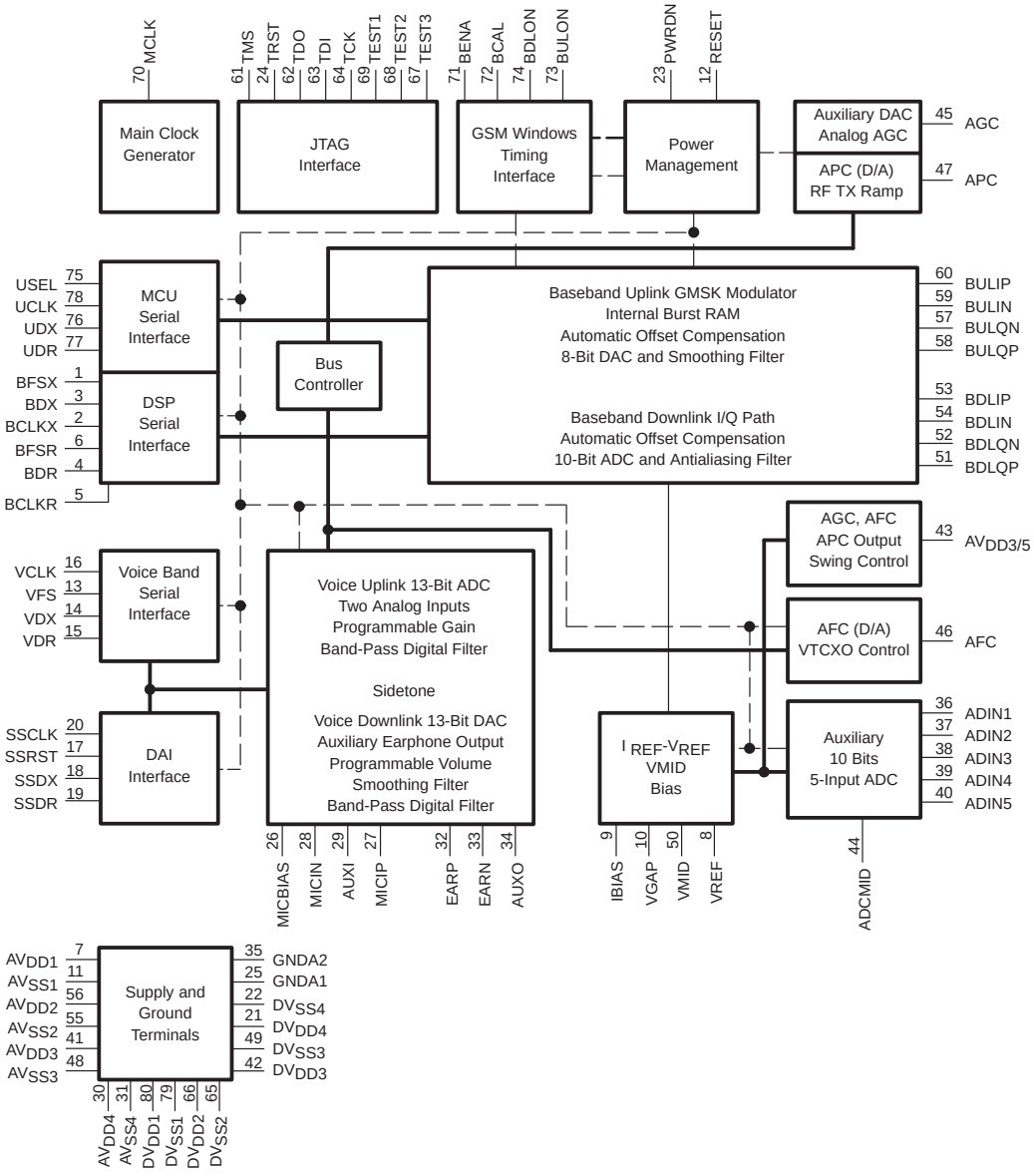
The baseband processing portion of the device includes a two-channel uplink path, a two-channel downlink path, a serial port, and a parallel port. The uplink path performs Gaussian minimum shift keying (GMSK) modulation, D/A conversion, and has smoothing filters to provide the external RF circuit with I and Q baseband signals. The downlink path performs antialiasing, analog/digital (A/D) conversion, and channel separation filtering of the baseband I and Q signals. The serial port allows baseband data exchange with the DSP, and the parallel port controls precise timing signals.

Auxiliary RF functions such as automatic frequency control (AFC), automatic gain control (AGC), power control, and analog monitoring are also implemented in the TCM4400. Internal functional blocks of the device can be separately and automatically powered down with GSM RF windows.

1.1 Features

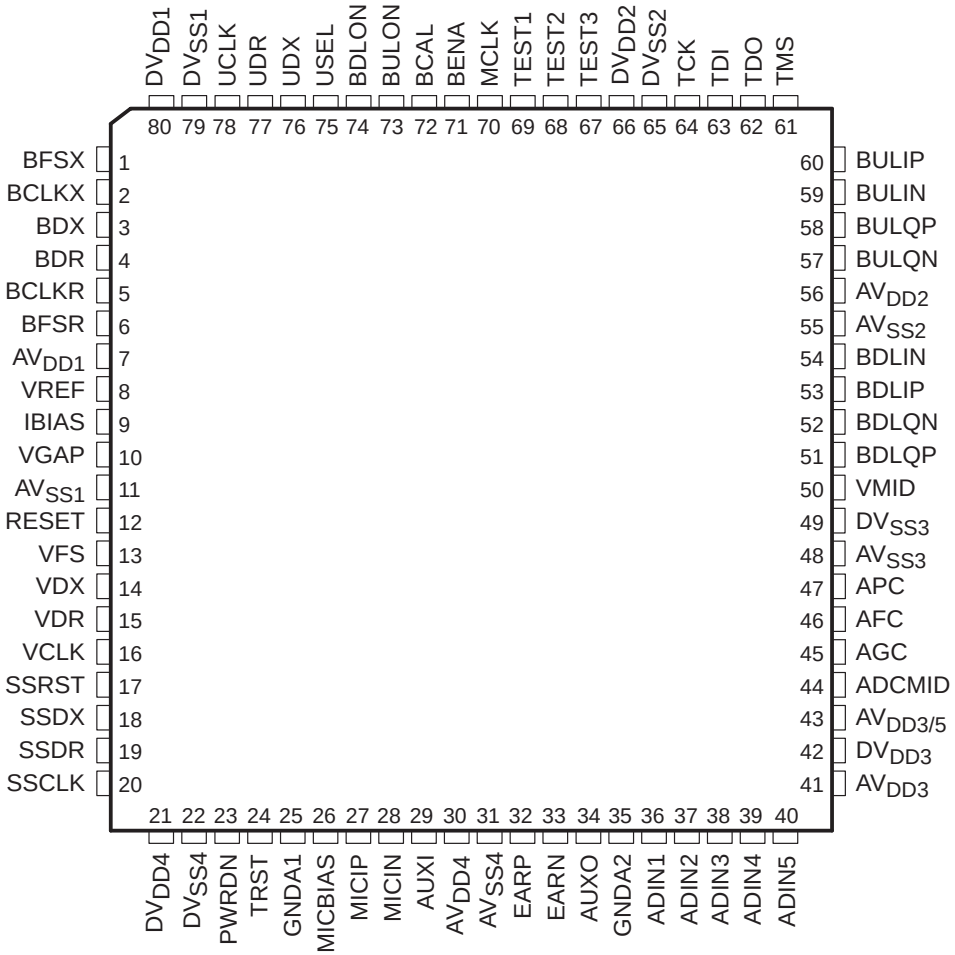
- Applications Include GSM 900, DCS 1800, and PCS 1900 Cellular Telephones
- 80-Pin TQFP Package
- Single 3-V Supply Voltage
- Internal Voltage Reference
- Extended RF Control Voltages
- Advanced Power Management
- GSM-Digital Audio Interface (DAI)
- MCU and DSP Serial Interface
- Five-Port Auxiliary A/D
- Meets JTAG Testability Standard (IEEE Std 1131.1-1990)
- Baseband Codec-GMSK Modulator with On-Chip Burst Buffer
- Voice Codec Features: Microphone Amplifier and Bias Source, Programmable Gain Amplifiers, Volume Control, and Sidetone Control

1.2 Functional Block Diagram



1.3 Terminal Assignments

80-PIN TQFP PACKAGE
(TOP VIEW)



1.4 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADCMID	44	I/O	Reference voltage of auxiliary A/D converters; decoupling only (analog)
ADIN1	36	I	Auxiliary 10-bit ADC input 1 (analog)
ADIN2	37	I	Auxiliary 10-bit ADC input 2 (analog)
ADIN3	38	I	Auxiliary 10-bit ADC input 3 (analog)
ADIN4	39	I	Auxiliary 10-bit ADC input 4 (analog)
ADIN5	40	I	Auxiliary 10-bit ADC input 5 (analog)
AFC	46	O	Automatic frequency control DAC output (analog)
AGC	45	O	Automatic gain control DAC output (analog)
APC	47	O	Automatic power control DAC output (analog)
AUXI	29	I	Auxiliary (high-level) speech signal input (analog)
AUXO	34	O	Auxiliary downlink (voice codec) amplifier output – single-ended (analog)
AV_{DD1}	7		Analog positive power supply (band gap, internal common-mode generator, bias current generator)
AV_{DD2}	56		Analog positive power supply (baseband codec)
AV_{DD3}	41		Analog positive power supply (auxiliary RF functions)
$AV_{DD3/5}$	43		Analog positive power supply (auxiliary RF functions) – can be in the 3-V to 5-V range
AV_{DD4}	30		Analog positive power supply (voice codec)
AV_{SS1}	11		Analog negative power supply (band gap, internal common-mode generator, bias current generator)
AV_{SS2}	55		Analog negative power supply (baseband codec)
AV_{SS3}	48		Analog negative power supply (auxiliary RF functions)
AV_{SS4}	31		Analog negative power supply (voice codec)
BCAL	72	I	Baseband uplink or downlink offset calibration enable (timing interface)
BCLKR	5	I/O	DSP serial interface clock input. This clock signal is provided by the DSP or the TCM4400 (digital).
BCLKX	2	O	DSP serial interface clock output. The frequency is the same as MCLK (digital/3-state).
BDR	4	I	DSP serial interface serial data input (digital)
BDX	3	O	DSP serial interface serial data output (digital/3-state)
BENA	71	I	Burst transmit or receive enable (depends on status of BULON and BDLON) (digital)
BDLON	74	I	Power on of baseband downlink (timing interface)
BFSR	6	I	DSP serial interface receive frame synchronization input (digital)
BFSX	1	O	DSP serial interface transmit frame synchronization output (digital/3-state)
BDLIN	54	I	In-phase baseband input (–) – downlink path (analog)
BDLIP	53	I	In-phase baseband input (+) – downlink path (analog)
BDLQN	52	I	Quadrature baseband input (–) – downlink path (analog)
BDLQP	51	I	Quadrature baseband input (+) – downlink path (analog)
BULIN	59	O	In-phase baseband output (–) – uplink path (analog)
BULIP	60	O	In-phase baseband output (+) – uplink path (analog)
BULON	73	I	Serial clock input (serial interface) (digital)
BULQN	57	O	Quadrature baseband output (–) – uplink path (analog)
BULQP	58	O	Quadrature baseband output (+) – uplink path (analog)
DV_{DD1}	80		Digital positive power supply (baseband and timing serial interfaces)
DV_{DD2}	66		Digital positive power supply (baseband codec)
DV_{DD3}	42		Digital positive power supply (auxiliary RF functions)
DV_{DD4}	21		Digital positive power supply (voice band codec and serial interface)

1.4 Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DV_{SS1}	79		Digital negative power supply (baseband and timing serial interfaces)
DV_{SS2}	65		Digital negative power supply (baseband codec)
DV_{SS3}	49		Digital negative power supply (auxiliary RF functions)
DV_{SS4}	22		Digital negative power supply (voice band codec and serial interface)
EARN	33	O	Earphone amplifier output (–) (analog)
EARP	32	O	Earphone amplifier output (+) (analog)
GNDA1	25		Analog signal ground for the microphone amplifier and auxiliary input
GNDA2	35		Signal return (ground) for AUXO output
IBIAS	9	I/O	Internal bias reference current adjust – adjust with external resistor (analog)
MCLK	70	I	Master system clock input (13 MHz)
MICBIAS	26	I	Microphone bias supply output – also used to decouple bias supply with external capacitor (analog)
MICIP	27	I	Microphone amplifier input (+) (analog)
MICIN	28	I	Microphone amplifier input (–) (analog)
PWRDN	23	I	Power-down mode control input (digital) – active high
RESET	12	I	Device global hardware reset (digital) – active low
SSCLK	20	O	DAI external 104-kHz clock output (digital)
SSDR	19	I	DAI data transfer input – connect to GSM-SS TDAI (digital/pullup)
SSDX	18	O	DAI data transfer output – connect to GSM-SS RDAI (digital)
SSRST	17	I	DAI reset input (digital/pullup)
TCK	64	I	Scan test clock (digital/pulldown)
TDI	63	I	Scan path input (for testing purposes) (digital/pullup)
TDO	62	I	Scan path output (for testing purposes) (digital/3-state)
TEST1	69	I/O	Test I/O (digital/3-state and pullup)
TEST2	68	I/O	Test I/O (digital/3-state and pullup)
TEST3	67	O	Test output (digital)
TMS	61	I	JTAG test mode select (digital/pullup)
TRST	24	I	JTAG serial interface and boundary-scan register reset (digital/pullup) – active low
UCLK	78	I	Microcontroller unit (MCU) interface clock input (digital)
UDR	77	I	MCU interface data transfer input (digital)
UDX	76	O	MCU interface data transfer output (digital/3-state)
USEL	75	I	MCU serial interface select (digital)
VCLK	16	O	Voice band serial interface clock output (digital/3-state)
VDR	15	I	Voice band serial interface receive data input (digital)
VDX	14	O	Voice band serial interface transmit data output (digital/3-state)
VFS	13	O	Voice band serial interface transmit frame synchronization output (digital/3-state)
VGAP	10	I/O	Band gap reference voltage – decouple with external capacitor (analog)
VMID	50	O	Baseband uplink midrail voltage output – serves as reference common-mode voltage for RF device when directly dc coupled (analog)
V_{REF}	8	I/O	Reference voltage – decouple with external capacitor (analog)

2 Electrical Specifications

2.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, AV_{DD}, DV_{DD} (see Note 1) . . . . . −0.3 to 6 V
Maximum voltage on any input, V_I max . . . . . V_{DD} +0.3 V / V_{SS} −0.3 V
Storage temperature, T_{stg} . . . . . −65°C to 150°C
Maximum junction temperature, T_J . . . . . 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage measurements in respect to GND

2.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage range (AV_{DD}, DV_{DD})	2.7	3.0	3.3	Vdc
Supply extended voltage range for RF blocks (AV_{DD}3/5) – 3-V supply	2.7	3.0	3.3	Vdc
Supply extended voltage range for RF blocks (AV_{DD}3/5) – 5-V supply	4.75	5.0	5.25	Vdc
Operating temperature range	−25		85	°C
Digital I/O voltage with respect to DV_{SS}	−0.3		DV_{DD} + 0.3	Vdc
Analog I/O voltage with respect to AV_{SS}	−0.3		AV_{DD} + 0.3	V
Difference between any AV_{DD} or DV_{DD}			0.3	V

2.3 Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

2.3.1 Digital Inputs And Outputs

PARAMETER	MIN	TYP	MAX	UNIT
Low-level output current with digital pad lower than 0.1 V (CMOS)	0		40	µA
Low-level output current with digital pad lower than 0.4 V (TTL)	0		1	mA
High-level output current with digital pad higher than V_{DD} −0.1 V (CMOS)	−40		0	µA
High-level output current with digital pad higher than V_{DD} −0.4 V (TTL)	−1		0	mA
Minimum high-level input voltage, V_{IH}	V_{DD}−0.3			V
Maximum low-level input voltage, V_{IL}			V_{SS}+0.3	V
Output current on high-impedance state outputs	−15		+15	µA
Input current (any input) when input high	−1			µA
Input current (standard inputs) when input low			1	µA
Input current (inputs with pullup TMS, TDI, TEST1, TEST2) when input low			15	µA

2.3.2 Voltage References

REFERENCE		MIN	TYP	MAX	UNIT
VGAP	Voltage on band gap (used for all other references)	1.16	1.22	1.28	Vdc
	Band gap output resistance		200		kΩ
	Band gap external decoupling capacitance		0.1		μF
	Band gap start time (bit CHGUP = 0)		100		ms
	Band gap start time (bit CHGUP = 1)		2.5		ms
VREF	Voltage reference of GMSK internal ADC and DAC: V_{VREF}	1.66	1.75	1.84	Vdc
	Voltage reference output resistance		200		kΩ
	Voltage reference external decoupling capacitance		0.1		μF
	Voltage reference start time (bit CHGUP = 0)		300		ms
	Voltage reference start time (bit CHGUP = 1)		10		ms
VMID	Common-mode reference for baseband uplink: V_{VMID} (bit SELVMID = 0)	–10%	$V_{DD}/2$	10%	Vdc
	Common-mode reference for baseband uplink: V_{VMID} (bit SELVMID = 1)	1.25	1.35	1.45	Vdc
	Load resistance on VMID output	10			kΩ
MICBIAS	Microphone-driving voltage (bit MICBIAS = 0)	1.80	2	2.20	Vdc
	Microphone-driving voltage (bit MICBIAS = 1)	2.25	2.5	2.75	Vdc
	Microphone-bias current drive capability (bit MICBIAS = 1)	450	500		μA
	Microphone-bias current drive capability (bit MICBIAS = 0)	350	400		μA
ADCMID	DC bias reference of the auxiliary ADCs	–10%	$V_{DD}/2$	10%	Vdc
	ADCMID external decoupling capacitance		0.1		μF
IBIAS	Bias current adjust external resistance		100		kΩ

2.3.3 Master Clock Input (MCLK)

	MIN	NOM	MAX	UNIT
Master clock signal frequency		13		MHz
Master clock duty cycle (sine wave)	40		60	%
Maximum peak-to-peak amplitude			1.3	Vpp
Minimum peak-to-peak amplitude	0.5			Vpp
Common-mode input voltage	$V_{SS}+0.5$		$V_{DD}-0.5$	Vdc
Input resistance at 13 MHz (MCLK to ground)	4.1	5	6.5	kΩ
Input capacitance at 13 MHz (MCLK to ground)	12.5	15	18	pF

2.3.4 Baseband Uplink Path

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I and Q DAC resolution			8		bit
Dynamic range on each output	Centered on V_{VMID}		V_{VREF}		Vpp
Differential output dynamic range†	BULQP-BULQN or BULIP-BULIN		$2\times V_{VREF}$		Vpp
Output load resistance, differential		10			kΩ
Output load capacitance, differential			50		pF
Output common-mode voltage	Programmable by bit SELVMID		V_{VMID}		V
I and Q output state in power down			HiZ		

† Initial values after reset and at beginning of each burst are BULIP–BULIN=V_{REF} and BULQP–BULQN=0 corresponding to a phase angle of 0°.

2.3.5 dc Accuracy – Baseband Uplink Path

PARAMETER	MIN	TYP	MAX	UNIT
Offset error before calibration	–90	0	90	mV
Offset error after calibration	–5	0	5	mV
Offset correction range	–100	0	100	mV

2.3.6 Dynamic Parameters – Baseband Uplink Path

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Absolute gain error relative to V_{VREF}	Measured with 67.7-kHz sine wave	–1	0	1	dB
Maximum output random modulation spectrum relative to in-band average level. Measured by average fast Fourier transforms (FFTs) of random bursts using a flat top window‡ with 30-kHz bandwidth.	100 kHz			–3	dB
	200 kHz			– 34	dB
	250 kHz			– 37	dB
	400 kHz			– 65	dB
	600 kHz			–72	dB
	800 kHz			–72	dB

‡ Flat top window is defined as: $Dw(i)=D(i) \times wf0 \times (wf1 + wf2 \times \cos(2 \times i \times \Pi/n) + wf3 \times \cos(4 \times i \times \Pi/n))$. With wf0=2.0660373, wf1 = 0.2810639, wf2 = –0.5208972, wf3 = 0.1980399.

2.3.7 Smoothing Filters Characteristics – Baseband Uplink Path

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Group delay	0 Hz to 100 kHz		1.5		µs

2.3.8 I and Q Channels Gain and Phase Matching – Baseband Uplink Path

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain matching between channels	0 Hz to 96 kHz	Measured on 67.7 kHz sine wave before calibration	–1	0	1	dB
		Measured on 67.7 kHz sine wave after calibration	–0.3	0	0.3	
Phase matching between channels	0 Hz to 96 kHz		–0.5°	0	0.5°	
I and Q gain imbalance		Programmable with bits IQSEL, G1, and G0	–0.15	0.0	0.15	dB
			–0.42	–0.27	–0.12	
			–0.68	–0.53	–0.38	
			–0.93	–0.78	–0.63	

2.3.9 Baseband Uplink Path Global Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
GMSK phase trajectory error			6°	peak
			1.5°	rms
Power supply rejection	46			dB

2.4 Timing Requirements of Baseband Uplink Path

2.4.1 Programmable Delays – Baseband Uplink Path (See Figure 3–1)

			MIN	NOM	MAX	UNIT†
t_{su1}	Setup time, BENA↑ before APC↑	Bits DELU of register BULRUDEL	0		15	1/4-bit
t_{h1}	Hold time, ramp-down from BENA low	Bits DELD of register BULRUDEL	0		15	1/4-bit
t_r, t_f	Transition time, APC	Bit APCSPD = 0	0		64	1/16-bit
		Bit APCSPD = 1				1/8-bit

2.4.2 Fixed Delays – Baseband Uplink Path (See Figure 3–1)

			MIN	NOM	MAX	UNIT†
t_{su2}	Setup time, BULON↑ to BCAL↑		15			µs
t_{w1}	Pulse duration, BCAL high		132			µs
t_{su3}	Setup time, BCAL low before BENA↑		0			µs
t_{w2}	Pulse duration, BENA high	N effective duration of burst controlled by BENA		N–32		1/4-bit
t_{h2}	Hold time, modulation low after BENA low			32		bit
t_{h3}	Hold time, BULON↓ after APC low		1			bit
$t_{dd(mod)}$	Input-to-output modulator delay	Digital delay of modulator		1.5		bit

† Bit is relative to GSM bit = 1/270 kHz. Units can be a fractional part of the GSM bit as noted. Values in the above table are given for system information only.

2.4.3 Baseband Downlink Path

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic range on each input	Centered on external common mode (V_{BDLCOM})		V_{VREF}		Vpp
Differential input dynamic range	DLQP–DLQN or DLIP–DLIN		$2\times V_{VREF}$		Vpp
Differential input resistance at BDLQP–BDLQN or BDLIP–BDLIN		130	200	270	kΩ
Differential input capacitance at BDLQP–BDLQN or BDLIP–BDLIN		1.5	4	6.5	pF
Single-ended input resistance at BDLQP or BDLQN or BDLIP or BDLIN to ground		90	130	180	kΩ
Single-ended input capacitance at BDLQP or BDLQN or BDLIP or BDLIN to ground		6	8	12	pF
External common-mode input voltage: V_{BDLCOM}		0.8	$V_{DD}/2$	$V_{DD}-0.8$	V
Range of digital output data	Maximum digital code value on 16-bit I and Q samples		± 21060		

2.4.4 dc Accuracy – Baseband Downlink Path

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Offset error before calibration†		–60	0	60	LSB
Offset error after calibration	±21 on 16-bit I and Q words†	–2	0	2	LSB
Offset correction range			full scale		

† The LSB corresponds to the one of the ADC which is specified with 66-dB dynamic range (±1024), which means 11-bit, but the output data bits are transmitted through the serial interface with 16-bit words. The decimation ratio of 24 (6.5 MHz/270 kHz) makes the maximum code on a 16-bit word 21060 instead of 32767. Therefore, one LSB of the ADC corresponds to a value of 21060/1024 = 20.57 on the 16-bit output serial words on I and Q.

2.5 Channel Characteristics

2.5.1 Frequency Response – Baseband Downlink Path

PARAMETER		MIN	TYP	MAX	UNIT
Frequency response of the total path with values referenced to 18 kHz	< 0 Hz	–0.2		0.2	dB
	67.5 kHz	–0.3		0.25	
	96 kHz	–4		0.3	
	135 kHz			–40	
	200 kHz			–40	
	400 kHz			–40	

2.5.2 SNR vs Signal Level-baseband Downlink Path

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal level	–45 dBm0	200-kHz bandwidth	21			dB
	–40 dBm0		26			
	–30 dBm0		36			
	–20 dBm0		46			
	–10 dBm0		50			
	–3 dBm0		57			
	0 dBm0		30			
Idle channel noise, 0 Hz–200 kHz					–66	dBm0

2.5.3 Gain Characteristics of the Baseband Downlink Path

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Absolute gain error relative to V_{VREF}		at –10 dBm0 and 18 kHz	–11	–10	–9	dB
Gain tracking error over the range 3 dBm0 to – 50 dBm0 at 18 kHz with reference –10 dBm0	3 dBm0		–0.25		0.25	dB
	0 dBm0		–0.25		0.25	
	– 5 dBm0		–0.25		0.25	
	–10 dBm0	Reference level	–0.25		0.25	
	–20 dBm0		–0.25		0.25	
	–30 dBm0		–0.25		0.25	
	–40 dBm0		–0.25		0.25	
	–50 dBm0		–0.50		0.50	

2.5.4 Group Delay – Baseband Downlink Path

PARAMETER		MIN	TYP	MAX	UNIT
Group delay	0 Hz to 100 kHz		28		µs

2.5.5 I and Q Channels Matching – Baseband Downlink Path

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain matching between channels	0 Hz to 96 kHz	18-kHz sine wave	–0.5		0.5	dB
Delay matching between channels	0 Hz to 96 kHz	18-kHz sine wave	–5		5	ns

2.5.6 Baseband Downlink Path Global Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Power supply rejection, 0 Hz –100 kHz band	60			dB

2.6 Timing Requirements of Baseband Downlink Path (See Figure 3–2)

			MIN	NOM	MAX	UNIT†
t_{su4}	Setup time, BDLON↑ to BCAL↑		5			µs
t_{w3}	Pulse duration, BCAL		60			µs
t_{su5}	Setup time BCAL low before BENA↑		0			µs
t_{w4}	Pulse duration, BENA high	N effective duration of burst controlled by BENA		N		1/4-bit
t_{su6}	Setup time, BENA↑ before DATAOUT valid		24.3		28	µs
t_{h4}	Hold time, DATAOUT valid after BENA↓				3.7	µs
t_{h5}	Hold time, BDLON low after BENA low		0			µs

† Value given is for system information only.

2.7 Automatic Power Control (APC)

2.7.1 APC Level (8-bit DAC)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Integral nonlinearity (best fitting)	Shaper at maximum full-scale load 10 kΩ, 50 pF	–1		1	LSB
Differential nonlinearity		–1		1	LSB
Settling time				10	µs

2.7.2 APC Shaper (5-bit DAC)

PARAMETER	MIN	TYP	MAX	UNIT
Integral nonlinearity (best fitting)	–1		1	LSB
Differential nonlinearity	–1		1	LSB
Settling time†			1	µs

† Value given is for system information only.

2.7.3 APC Output Stage

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage at shape = 3 and level = 255 ($AV_{DD3/5}$ = 3 V)	Bit APCSWG = 0	2	2.2	2.4	V
Output voltage at shape = 31 and level = 255 ($AV_{DD3/5}$ = 5 V)	Bit APCSWG = 1	4	4.4	4.8	V
Output voltage at shape = 0 and level = xx ($AV_{DD3/5}$ = 3 V)	Bit APCSWG = 0, Bit APCMODE = 0	0		15	mV
Output voltage at shape = 0 and level = xx ($AV_{DD3/5}$ = 5 V)	Bit APCSWG = 1, Bit APCMODE = 0	0		30	mV
Ouptut voltage at shape = 0 and level = xx ($AV_{DD3/5}$ = 3 V)†	Bit APCSWG = 0, Bit APCMODE = 1	80	120	160	mV
Output voltage at shape = 0 and level = xx ($AV_{DD3/5}$ = 5 V)†	Bit APCSWG = 1, Bit APCMODE = 1	160	240	320	mV
Output voltage at shape = xx and level = 0			0	5	mV
Output voltage in power down			0		V
DC power supply sensitivity				1	%
Output impedance in power down			20		Ω
Load resistance		10			kΩ
Load capacitance				50	pF

† Temperature variations of these voltages are ±1% from –50°C to +100°C and ±0.6% from 0°C to 70°C.

2.8 Monitoring ADC

2.8.1 10-bit ADC

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Integral nonlinearity (best fitting)	Input signal range < 0.95 V_{VREF}	–4		4	LSB
Differential nonlinearity	Input signal range < 0.95 V_{VREF}	–2		2	LSB
Conversion time‡				10	µs
Input range		0		V_{VREF}	V
Input leakage current		–10		10	µA
Input capacitance				25	pF

‡ Value given is for system information only.

2.9 Automatic Gain Control (AGC)

2.9.1 AGC 10-bit DAC

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Integral nonlinearity	Best fitting line	–1		1	LSB
Differential nonlinearity		–1		1	LSB
Settling time	From AUXAGC load			100	µs

2.9.2 AGC Output Stage

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage with code max ($AV_{DD3}/5$ = 3 V ± 10%)	Bit AGCSWG = 0	2	2.2	2.4	V
Offset voltage with code 000 ($AV_{DD3/5}$ = 3 V ± 10%)	Bit AGCSWG = 0	0.18	0.24	0.30	V
Output swing with code max ($AV_{DD3/5}$ = 5 V ± 5%)	Bit AGCSWG = 1	4	4.4	4.8	V
Offset voltage with code 000 ($AV_{DD3/5}$ = 5 V ± 5%)	Bit AGCSWG = 1	0.36	0.48	0.60	V
Output voltage in power down			0		V
DC power supply sensitivity				1	%
Output impedance in power down			200		kΩ
Load resistance		10			kΩ
Load capacitance				50	pF

2.10 Automatic Frequency Control (AFC)

2.10.1 AFC 13-bit DAC

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sampling frequency, f_S	AFCCK1 = 1, AFCCK0 = 1		2		MHz
	AFCCK1 = 1, AFCCK0 = 0		1		MHz
	AFCCK1 = 0, AFCCK0 = 1		0.5		MHz
	AFCCK1 = 0, AFCCK0 = 0		0.25		MHz
Integral nonlinearity from 0 to 75% output range	Best fitting line		±1		LSB
Differential nonlinearity from 0 to 75% output range			±1		LSB
Settling time				1	µs
DC power-supply sensitivity	Over power supply range: at 2.0 V for AFCZ = 0 or at 4.0V for AFCZ = 1			1	%

2.10.2 AFC Output Stage

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal output resistance (±30% tolerance)	Bit AFCZ = 0		25		kΩ
Internal output resistance (±30% tolerance)	Bit AFCZ = 1		50		kΩ
External filtering capacitance	Bit AFCZ = 1		33		nF
Output voltage with code max ($AV_{DD3/5}$ = 3 V)	Bit AFCZ = 0	2	2.5	2.8	V
Output voltage with code max ($AV_{DD3/5}$ = 5 V)	Bit AFCZ = 1	4	4.7	5.1	V
Output voltage with code min ($AV_{DD3/5}$ = 3 V)	Bit AFCZ = 0	0	3	6	mV
Output voltage with code min ($AV_{DD3/5}$ = 5 V)	Bit AFCZ = 1	0	5	10	mV
Output voltage in power down			0		V
Output impedance in power down	Bit AFCZ= 0, Bit AFCZ=1		25		kΩ
			50		

2.11 Voice Uplink Path

2.11.1 Global Characteristics of Voice Uplink Path

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Maximum input range (MICP – MICN)	Inputs 3 dBm0 (maximum digital sample amplitude) with PGA gain. Set to 0dB (default value).			32.5		mVrms
Nominal reference level (MICP – MICN)				–10		dBm0
Differential input resistance (MICP – MICN)			90	140	200	kΩ
Micro amplifier gain				27		dB
Maximum input range at AUXI	Inputs 3 dBm0 (maximum digital sample amplitude) with PGA gain. Set to 0dB (default value).			365		mVrms
Nominal reference level at AUXI				–10		dBm0
Input resistance at AUXI			140	220	300	kΩ
Auxiliary amplifier gain				6		dB
PGA absolute gain				4.6		dB
PGA gain step	VULPGA code =10000	–12 dB	–12.7	–12.2	–11.7	dB
	VULPGA code = 10111	–11 dB	–11.3	–10.8	–10.3	
	VULPGA code = 11000	–10 dB	–10.6	–10.1	–9.6	
	VULPGA code = 11001	–9 dB	–9.5	–9.0	– 8.5	
	VULPGA code = 11010	– 8 dB	– 8.5	– 8.0	–7.5	
	VULPGA code = 11011	–7 dB	–7.5	–7.0	– 6.5	
	VULPGA code = 00000 (default)	– 6 dB	– 6.7	– 6.2	– 5.7	
	VULPGA code = 00001	–5 dB	– 5.6	– 5.1	– 4.6	
	VULPGA code = 00010	–4 dB	– 4.6	– 4.1	– 3.6	
	VULPGA code = 00011	–3 dB	– 3.5	– 3.0	–2.5	
	VULPGA code = 00100	–2 dB	–2.4	–1.9	–1.4	
	VULPGA code = 00101	–1 dB	–1.5	–1.0	– 0.5	
	VULPGA code = 00110 (ref)	0 dB		0		
	VULPGA code = 00111	1 dB	0.7	1.2	1.7	
	VULPGA code = 01000	2 dB	1.4	1.9	2.4	
	VULPGA code = 01001	3 dB	2.6	3.1	3.6	
	VULPGA code = 01010	4 dB	3.6	4.1	4.6	
	VULPGA code = 01011	5 dB	4.5	5.0	5.5	
	VULPGA code = 01100	6 dB	5.3	5.8	6.3	
	VULPGA code = 10001	7 dB	6.4	6.9	7.4	
	VULPGA code = 10010	8 dB	7.4	7.9	8.4	
	VULPGA code = 10011	9 dB	8.6	9.1	9.6	
	VULPGA code = 10100	10 dB	9.6	10.1	10.6	
	VULPGA code = 10101	11 dB	10.5	11.0	11.5	
	VULPGA code = 10110	12 dB	11.5	12.0	12.5	
Power supply rejection, 0-Hz – 100-kHz band			52			dB

2.11.2 Frequency Response of the Voice Band Uplink Path

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response (gain relative to reference gain at 1 kHz)	100 Hz			–37.4	–20	dB
	150 Hz			–25.9	–15	
	200 Hz			–16.5	–10	
	300 Hz		–2.0	–1.46	1.0	
	1000 Hz	Reference point is 1000 Hz	–1.0	0	1.0	
	2000 Hz		–1.0	–0.58	1.0	
	3000 Hz		–1.0	–0.77	1.0	
	3400 Hz		–2.0	–1	1.0	
	3600 Hz			–12.4	–6	
	3800 Hz			–23.3	–18	
	4000 Hz			–35	–30	
	> 4600 Hz			>–52	–40	

2.11.3 Psophometric SNR vs Signal Level of the Voice Band Uplink Path

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal to noise + distortion	3 dBm0		35			dB
	0 dBm0		40			
	–5 dBm0		42			
	–10 dBm0		45			
	–20 dBm0		42			
	–30 dBm0		40			
	–40 dBm0		30			
	–45 dBm0		25			
Maximum idle channel noise	300 Hz–3 kHz				–72	dBm0
Crosstalk with the downlink path		Downlink path loaded with 33 Ω			–66	dB

2.11.4 Gain Characteristics of the Voice Band Uplink Path

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Absolute gain error		at 0 dBm 0 and 1 kHz	–1.8		0.2	dB
		at –10 dBm 0 and 1 kHz	–11.8	–10	–9.8	
Gain tracking error over the range 3 dBm0 to – 45 dBm0 at 1 kHz with reference –10 dBm0	3 dBm0		–0.25		0.25	dB
	0 dBm0		–0.25		0.25	
	–5 dBm0		–0.25		0.25	
	–10 dBm0	Reference level		0		
	–20 dBm0		–0.25		0.25	
	–30 dBm0		–0.25		0.25	
	–40 dBm0		–0.35		0.35	
	–45 dBm0		–0.50		0.50	

2.12 Voice Downlink Path

2.12.1 Global Characteristics of Voice Downlink Path

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum output swing (EARP_ EARN)	5% distortion and 150 Ω		3.1	3.92		Vpp
	5% distortion and 33 Ω		1.2	1.5		Vpp
Minimum output resistive load at EARP_EARN		Output swing 3.9 Vpp	120	150		Ω
		Output swing 1.5 Vpp	30	33		Ω
Maximum output capacitive load at EARP_EARN					100	pF
Earphone amplifier gain				0		dB
Earphone amplifier state in power down				HiZ		
Maximum output swing (AUXO), 5% distortion, maximum		Load = 1 kΩ	1.6	1.96		Vpeak
Minimum output resistive load at AUXO		AC coupled	1.0	1.2		kΩ
Maximum output capacitive load at AUXO					100	pF
Auxo amplifier gain				−6dB		dB
Auxo amplifier state in power down				HiZ		
Volume control gains		VOLCTL code = 010	−1	0	1	dB
		VOLCTL code = 110	−7	−6	−5	
		VOLCTL code = 000 (default and reference)		−12		
		VOLCTL code = 100	−19	−18	−17	
		VOLCTL code = 011	−25	−24	−23	
		VOLCTL code = 101 or 001 or 111 (mute)			−40	
PGA gain steps		VDLPGA code = 0000 (default) −6dB	−6.5	−6.0	−5.5	dB
		VDLPGA code = 0001 −5dB	−5.5	−5.0	−4.5	
		VDLPGA code = 0010 −4dB	−4.5	−4.0	−3.5	
		VDLPGA code = 0011 −3dB	−3.7	−3.2	−2.7	
		VDLPGA code = 0100 −2dB	−2.3	−1.8	−1.3	
		VDLPGA code = 0101 −1dB	−1.7	−1.2	−0.7	
		VDLPGA code = 0110 (ref) 0dB		0		
		VDLPGA code = 0111 1dB	0.5	1.0	1.5	
		VDLPGA code = 1000 2dB	1.4	1.9	2.4	
		VDLPGA code = 1001 3dB	2.6	3.1	3.6	
		VDLPGA code = 1010 4dB	3.4	3.9	4.4	
		VDLPGA code = 1011 5dB	4.3	4.8	5.3	
		VDLPGA code = 1100 6dB	5.5	6.0	6.5	

2.12.1 Global Characteristics of Voice Downlink Path (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sidetone gain steps	VDLST code = 1101 –23dB	–24.6	–24.1	–23.6	dB
	VDLST code = 1100 –20dB	–21.1	–20.6	–20.1	
	VDLST code = 0110 –17dB	–18.3	–17.8	–17.3	
	VDLST code = 0010 –14dB	–14.8	–14.3	–13.8	
	VDLST code = 0111 –11dB	–12.3	–11.8	–11.3	
	VDLST code = 0011 –8dB	–8.8	–8.3	–7.8	
	VDLST code = 0000 (ref) –5dB	–5.3	–4.8	–4.3	
	VDLST code = 0100 –2dB	–2.1	–1.6	–1.1	
	VDLST code = 0001 1dB	0.7	1.2	1.7	
	VDLST code = 1000 Mute		–60	–55	
Power supply rejection, 0 Hz – 100 kHz	In the band	48			dB

2.12.2 Frequency Response of the Voice Band Downlink Path

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response (gain relative to reference gain at 1 kHz)	100 Hz			–5.8	–5	dB
	150 Hz			–3.6	–2	
	200 Hz			–2.5	1	
	300 Hz		–3	–1.4	1	
	1000 Hz	Reference point		0		
	2000 Hz		–1	–0.6	1	
	3000 Hz		–1	–0.15	1	
	3400 Hz		–3	–0.35	1	
	3600 Hz			–9.0	–6	
	3800 Hz			–21.0	–15	
	4000 Hz			–32.0	–28	
	>4600 Hz			–60.0		

2.12.3 Psophometric SNR vs Signal Level Downlink Path

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal level	–45 dBm0		25			dB
	–40 dBm0		30			
	–30 dBm0		40			
	–20 dBm0		42			
	–10 dBm0		45			
	–3 dBm0		42			
	0 dBm0		35			
Idle channel noise, 0 Hz – 30 kHz					–71	dBm
Crosstalk with the uplink path					–66	dB

2.12.4 Gain Characteristics of the Voice Band Downlink Path

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Absolute gain error		at 0 dbm0 and 1 kHz	–1	0	1	dB
		at –10 dbm0 and 1 kHz	–11	–10	–9	
Gain tracking error over the range 3 dBm0 to – 45 dBm0 at 1 kHz with reference –10 dBm0 PGA gain = 0dB. Volume control = –12 dB.	3 dBm0		–0.25		0.25	dB
	0 dBm0		–0.25		0.25	
	–5 dBm0		–0.25		0.25	
	–10 dBm0	Reference level		0		
	–20 dBm0		–0.25		0.25	
	–30 dBm0		–0.25		0.25	
	–40 dBm0		–0.35		0.35	
	–45 dBm0		–0.50		0.50	

2.13 Power Consumption

2.13.1 Consumption by Circuit Block

CIRCUIT BLOCK		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AFC	DV_{DD3}			0.013		mA
	AV_{DD3}			0.021		
	$AV_{DD3/5}$			0.027		
AGC	AV_{DD3}			0.054		mA
	$AV_{DD3/5}$			0.683		
APC	DV_{DD3}			0.133		mA
	AV_{DD3}			0.108		
	$AV_{DD3/5}$			0.442		
Auxiliary input stage	AV_{DD4}			2.240		mA
Auxiliary output stage	AV_{DD4}			1.550		
Band gap	AV_{DD1}			0.163		mA
Baseband downlink	DV_{DD2}			2.810		mA
	AV_{DD2}			9.310		
Baseband uplink	DV_{DD2}			0.460		mA
	AV_{DD2}			4.910		
BBIF	DV_{DD1}	BDL active		1.490		mA
Clock generator BBIF	DV_{DD1}			0.122		mA
Clock generator idle	DV_{DD1}			0.204		mA
Clock generator TIIF	DV_{DD1}			0.181		mA
Clock generator VBIF	DV_{DD1}			0.144		mA
Digital modulator	DV_{DD4}			0.183		mA
Earphone output stage	AV_{DD4}			4.170		mA
Microphone input stage	AV_{DD4}			3.000		mA
Voice band downlink	DV_{DD4}			1.380		mA
	AV_{DD4}			2.990		
Voice band uplink	DV_{DD4}			1.200		mA
	AV_{DD4}			0.115		

2.13.2 Current Consumption for Typical Configurations

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Deep power down	13-MHz clock applied; PWRDN active; band-gap voltage reference off.			250	μA
Power down with AFC active	AFC programmed with internal 50-kΩ and 1-MHz clock		0.7	1.1	mA
AFC + GMSK – Rx	Paging		14	16	mA
Audio + GMSK – Tx + APC + AFC	Transmit burst		19	21	mA
Audio + GMSK – Rx +AGC+ AFC	Receive burst		27	30	mA

2.13.3 MCU Serial Interface Timing Requirements (See Figure 3–3)

		MIN	NOM	MAX	UNIT
t_{su10}	Setup time, UCLK stable before USEL↓	20			ns
t_{v1}	Hold time, UDX valid after USEL↓			20	ns
t_{v2}	Hold time, UDX valid after UCLK↑			20	ns
t_{h9}	Sequential transfer delay between 16-bit word acquisition t_W pulse duration, USEL high	3000			ns
t_{h10}	Hold time, UCLK↑ after USEL↓	20			ns
t_{h11}	Hold time, UCLK unknown after USEL↑	20			ns
t_{su11}	Setup time, data valid before UCLK↓	20			ns
t_{h12}	Hold time, data valid after UCLK↓	20			ns
t_c	Cycle time, ULCK	154			ns

2.13.4 DSP Serial Interface Timing Requirements (See Figure 3–4)

			MIN	NOM	MAX	UNIT
BCLKX	BCLKX signal frequency (burst mode or continuous mode depending on bit BCLKMODE)			13		MHz
BCLKX	BCLKX duty cycle		45	50	55	%
t_{su12}	Setup time, BFSX high before BCLKX ↓		20			ns
t_{h12}	Hold time, BFSX high after BCLKX ↓		20			ns
t_{su13}	Setup time, BDX valid before BCLKX ↓		20			ns
t_{h13}	Hold time, BDX valid after BCLKX ↓		20			ns
BCLKR	BCLKR signal frequency	(Output BCLKDIR = 0)		4.33		MHz
		(Input BCLKDIR = 1)			13	
BCLKR	BCLKR duty cycle		45	50	55	%
t_{su14}	Setup time, BFSR high before BCLKR ↓		20			ns
t_{h14}	Hold time, BFSR high after BCLKR ↓		20			ns
t_{su16}	Setup time, BDR valid before BCLKR ↓		20			ns
t_{h15}	Setup time, BDR valid after BCLKR ↓		20			ns

2.13.5 Voice Timing Requirements (See Figure 3–5)

		MIN	NOM	MAX	UNIT
VCLK	VCLK signal frequency (burst mode or continuous mode depending on bit VCLKMODE)		520		kHz
VCLK	VCLK duty cycle	45	50	55	%
t_{su7}	Setup time, VFS high before VCLK ↓	100			ns
t_{h6}	Hold time, VFS high after VCLK ↓	100			ns
t_{su8}	Setup time, VDX valid before VCLK ↓	100			ns
t_{h8}	Hold time, VDX valid after VCLK ↓	100			ns
t_{su9}	Setup time, VDR valid before VCLK ↓	100			ns
t_{h7}	Hold time, VDR valid after VCLK ↓	100			ns

3 Parameter Measurement Information

3.1 Uplink Timing Considerations

Figure 3–1 shows the timing diagram for the uplink operation.

Timing for power up, offset calibration, data transmission, and power ramp up are driven by control bits applied to BULON (base uplink on), BCAL (calibration), and BENA (enable). The burst content including guard bits, tail bits, and data bits, is sent by the DSP by way of the DSP interface and then stored by the TCM4400 in a burst buffer. Transmission start is indicated by the control bit BENA when the BULON is active. The transmission, sequencing, and power ramp up are then controlled by an on-chip burst sequencer with a one-quarter-bit timing accuracy. For a detailed description of the baseband in-length path, see the functional description of the baseband uplink path in the principles of operation section.

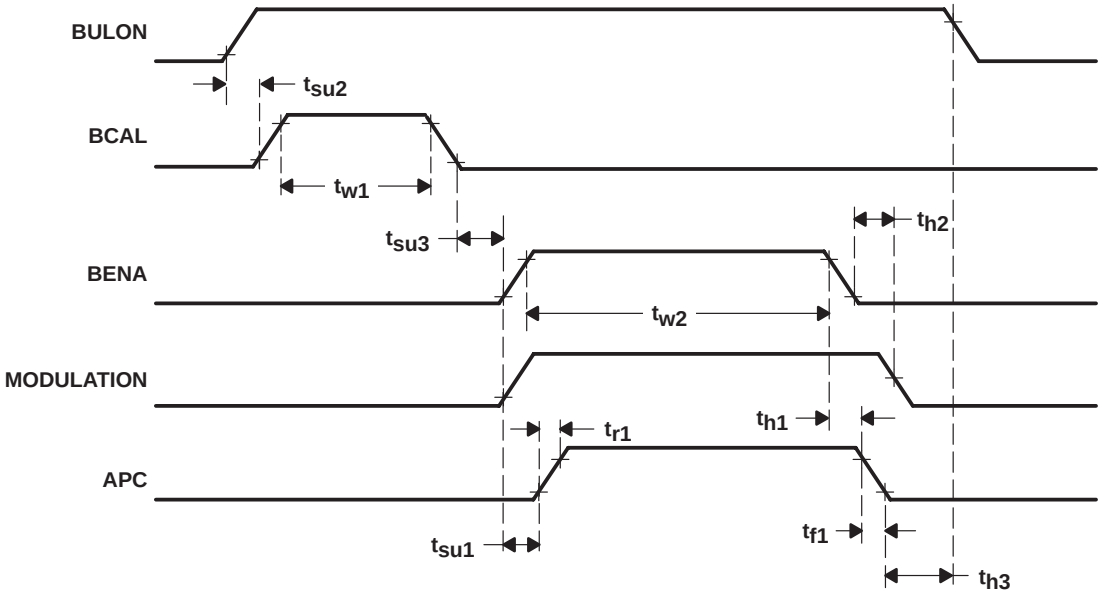


Figure 3–1. Uplink Timing Diagram

3.2 Downlink Timing Considerations

Figure 3–2 shows the timing diagram for downlink operation.

Timing of the baseband downlink path is controlled by bits DLON (downlink on), BCAL (calibration), and BENA (enable) when BDLON is active (see the topic, timing and interface). BDLON controls the power up of the baseband downlink path; BCAL controls the start and duration of the autocalibration sequence; and BENA controls the beginning and the duration of data transmission to the DSP using the DSP serial interface.

The power-down sequence is controlled with two bits. The first bit (BBDLW of PWDNRG1 register) determines whether the baseband downlink path can be powered down with external GSM receive window activation (BDLON); the second bit (BBDLPD of PWDNRG1 register) controls the activation of the baseband downlink path. For more information about power down control, see Section 4.8 in this document.

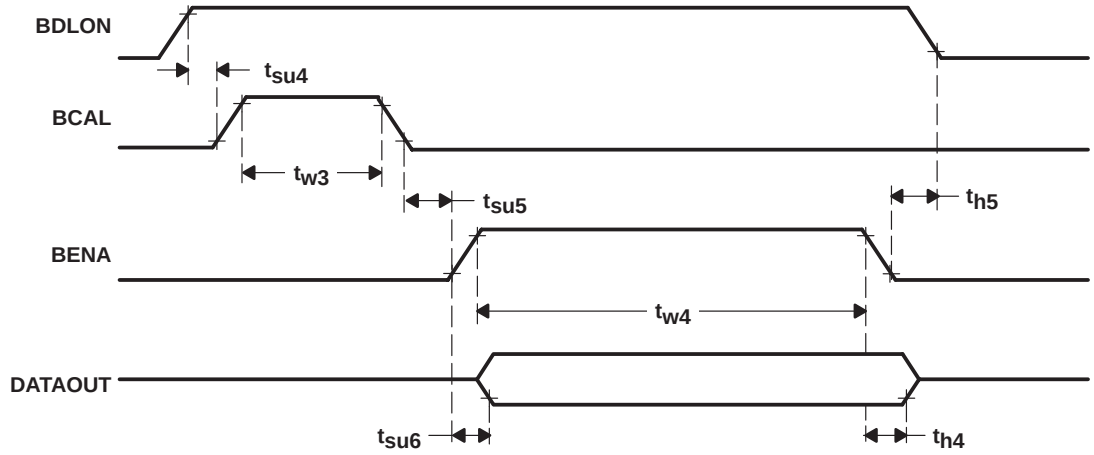


Figure 3–2. Downlink Timing Sequence

3.3 Microcontroller Unit Serial Interface Timing Considerations

Figure 3–3 shows the timing diagram for the microcontroller unit (MCU) serial interface.

The MCU is compliant with 8-bit standard synchronous serial ports. The microcontroller operates on 16-bit words; this interface consists of four pins.

UCLK: A clock provided by the microcontroller to control access to baseband, voice band, and auxiliary functions registers

UDR: An input terminal to control read and write access to baseband, voice band, and auxiliary functions registers

UDX: An output terminal to transmit data from read access of baseband, voice band, and auxiliary functions registers

USEL: An input terminal to enable read and write access to baseband, voice band, and auxiliary functions registers through the microcontroller interface

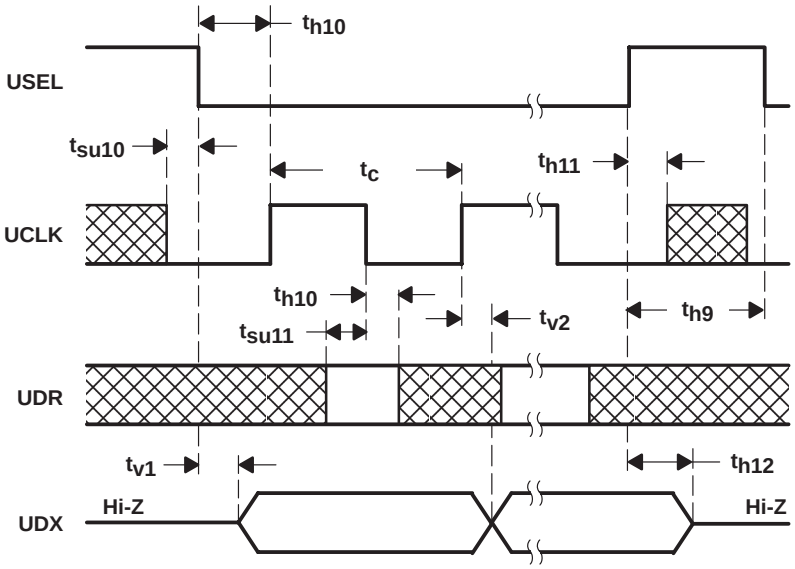


Figure 3–3. Microcontroller Unit Serial Interface Timing Waveforms (Mode Rising Edge Without Delay)

3.4 DSP Serial Port Timing Considerations

Figure 3–4 shows the timing diagram for DSP serial port operation.

Six terminals are used for the serial port interface. The terminal BCLKR is an I/O port for the serial clock used to control the reception of the data BDR. At reset BCLKR is configured as an output and the clock frequency is set to MCLK/3 (4.333 MHz with MCLK = 13 MHz); the clock signal is running permanently. The port BCLKR can be reconfigured as an input by programming an internal register. In this case BCLKR is provided by the DSP and can run in burst mode to reduce power consumption. The receive frame synchronization (BFSR) identifies the beginning of a data packet transfer on port BDR.

The transmitted serial data (BDX) is the serial data input; the transmit frame synchronization (BFSX) initiates the transmission of data. The transmit clock (BCLKX) is provided by the GSM baseband and voice A/D and D/A converters with a frequency of MCLK. The downlink data bus (BFSX, BCLKX, BDX) can be driven to V_{SS} or placed in high-impedance state when no data is to be transferred to the DSP. The bit BCLKDIR of the register BCTLREG controls the direction of the BCLKR clock.

As with the voice serial interface, an extra clock cycle must be generated because the last 16-bit word received on the DSP serial interface is latched on the next two falling BCLKR edges, following the least significant bit (LSB). As for the voice serial interface, one extra clock period is generated on the BCLKX before the first synchronization BFSX of downlink data sequence.

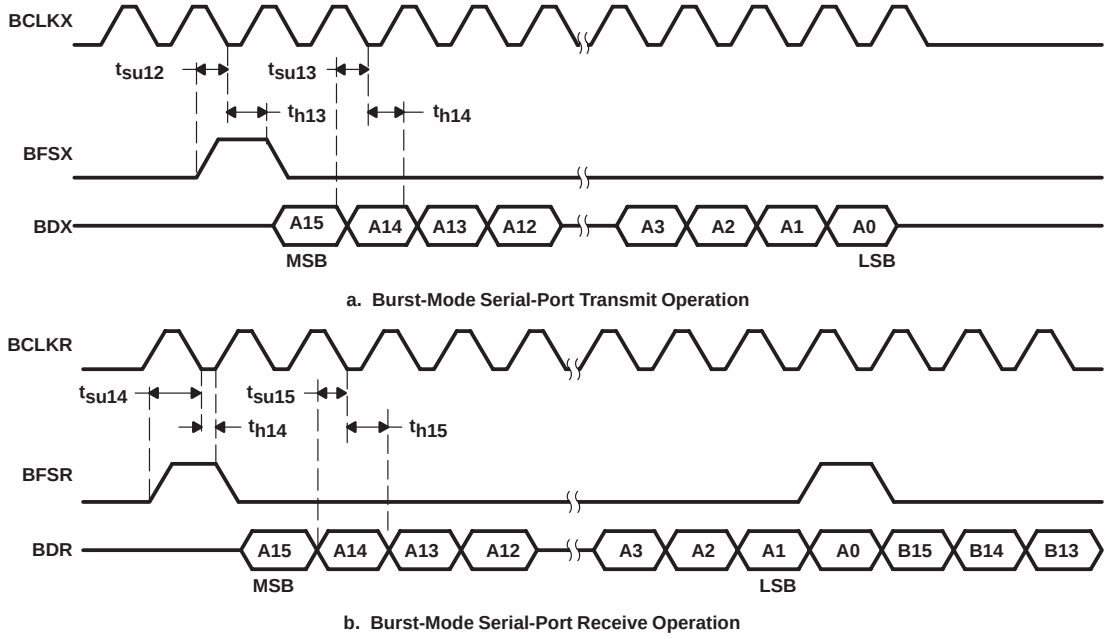


Figure 3–4. DSP Serial Port Timings

3.5 Voice Band Serial Interface Timing Considerations

Figure 3–5 shows the timing diagram for both transmit and receive voice band serial interface operation.

The signal VCLK is the output serial clock used to control the transmission or reception of the data. The transmitted serial data (VDX) is the serial data output; the frame synchronization (VFS) initiates the transfer of transmit and receive data. The received data (VDR) is the serial data input.

Each serial port includes four registers: the data transmit register (DXR), the data receive register (DRR), the transmit shift register (XSR), and the receive shift register (RSR).

The voice serial interface has the same structure and timing diagram as the serial interface; one extra cycle is generated before VFS and two extra cycles are generated after the LSB.

XLOAD and RLOAD are internal signals.

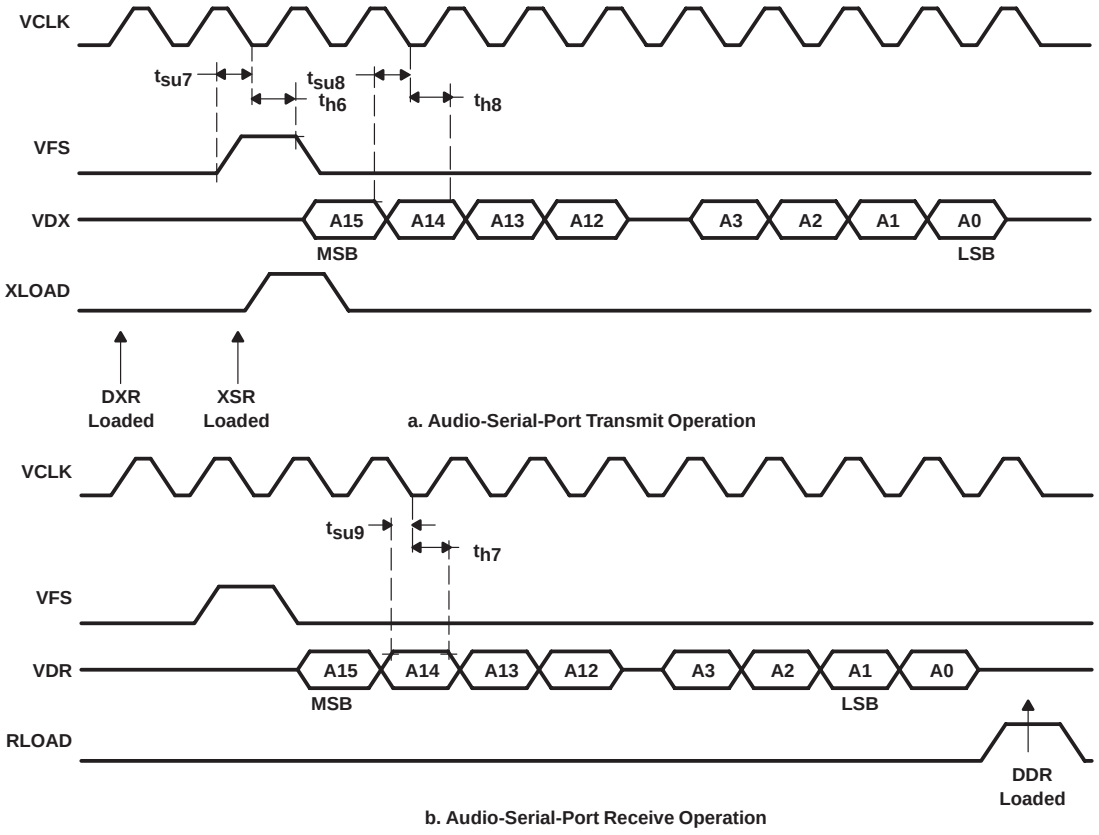


Figure 3–5. Voice Band Serial Interface Timing Waveforms

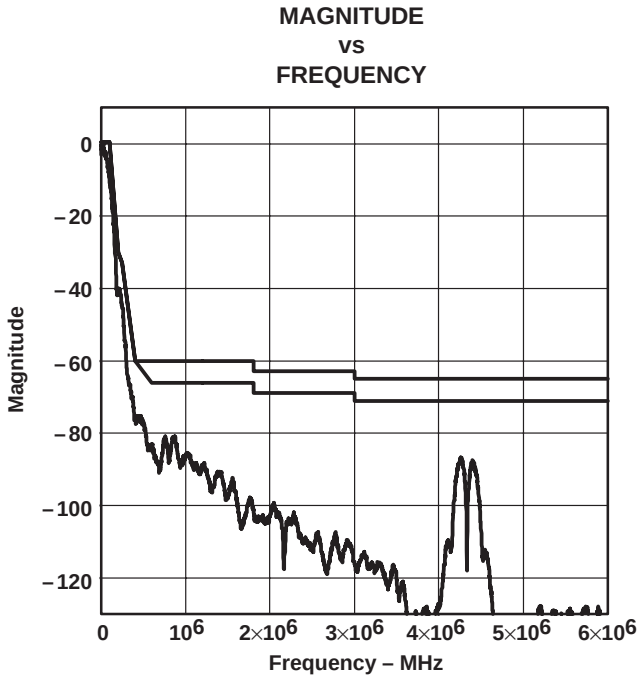
4 Principles of Operation

4.1 Baseband Uplink Path

Instead of the traditional transmit and receive terms, which can be confusing when describing a cellular telephone two-way communication, the terms uplink, which means from a user device to a remote station, and downlink, which means from a remote station, whether earthbound or satellite, are used to indicate the signal flow direction.

The modulator circuit in the baseband uplink path performs the Gaussian minimum shift keying (GMSK) in accordance with the GSM Specification, Section 05.04, Digital Cellular Telecommunication System; Modulation. The data to be modulated flows from the DSP through the serial interface. It is differentially encoded, and it is applied to the input of the GMSK modulator. The GMSK modulator is implemented with digital logic and a sin/cos look-up table in ROM, and it generates the I and Q components (words) with an interpolation ratio of 16.

These digital I and Q words are sampled at a 4.33-MHz rate and applied to the inputs of a pair of high-speed 8-bit DACs. The analog outputs are then processed by second-order Bessel filters to reduce image frequencies due to sampling and to obtain a spectrum consistent with GSM Specification, Section 05.05, Digital Cellular Telecommunications System (Phase 2+); Radio Transmission and Reception (see Figure 4–1).



NOTE: Conformance with GSM Specification, Section 05.5: simulated spectrum of an infinite modulation of random data with a Blackman Harris analysis window

Figure 4–1. Typical GSM Modulation Spectrum

Full-differential buffered signals are available at ULIP, ULIN, ULQP, and ULQN. These signals are suitable for use in the RF circuit for generating a phase-modulated signal of the form:

$$s(t) = A \cos (2 \pi fc\ t + Phi\ (t, alpha)) \quad (1)$$

where:

fc = the RF carrier frequency,
Phi (t, alpha) = the phase component generated by the GMSK modulator from the differential encoded data

Timing for power up, offset calibration, data transmission, and power ramp up are driven by control bits applied to BULON (base uplink on), BCAL (calibration), and BENA (enable) (see Figure 4–1). The entire content of a burst, including guard bits, tail bits, and data bits, is sent by the DSP using the DSP interface and then stored by the TCM4400 in a burst buffer. Transmission start is indicated by the control bit BENA when BULON is active. The transmission, sequencing, and power ramp up are then controlled by an on-chip burst timing control circuit having a one-quarter-bit timing accuracy (see Figure 4–2). All data related to a burst to be transmitted (such as bit data, ramp-up, and ramp-down delay programmation) have to be loaded before the rising edge of BENA.

The burst length is determined by the time during which the BENA signal is active. Effective burst length is equal to the duration of BENA plus 32 one-quarter bits. The tail of the burst is controlled internally, which means that the modulation is maintained for 32 one-quarter bits after BENA turns off to generate the ramp-down sequence and complete modulation.

For each burst, the power control level can be controlled by writing the power level value, using the serial interfaces, into the power register of the auxiliary RF power control circuitry. The power ramp-up and ramp-down sequences are controlled by the burst sequencer while the shape of the power control is generated internally by dedicated circuitry, which drives the power control 5-bit and 8-bit D/A converters.

To minimize phase error, the I and Q channel dc-offset can be minimized using offset calibration. Each channel includes an offset register in which a value corresponding to the required dc offset is stored, controlling the dc offset of the I channel and Q channel D/A converters. This value is set by a calibration sequence. Starting and stopping the calibration sequence is controlled by the control bit BCAL using the timing interface when BULON is active. During the calibration sequence, the digital value of I and Q is forced to zero so that only the offset register value drives the D/A converters and a low-offset comparator senses the dc level at the BULIP/BULIN and BULQP/BULQN outputs and modifies the content of the offset registers to minimize the dc offset (see Figure 4–2).

Gain imbalance can be introduced between I and Q channels to allow compensation of imperfections in RF circuits. This gain imbalance is controlled through the mean of three programmation bits (IQSEL, G1, and G0 of baseband uplink register BULCTL).

The power-down function is controlled with two bits. The first bit (BBULW of the PWDNRG1 register), determines whether the baseband uplink path can be powered down with external GSM transmit window activation (BULON). The second bit (BBULPD of the PWDNREG1 register) controls the activation of the baseband uplink path. For more information about power-down control, see Section 4.8 in this document.

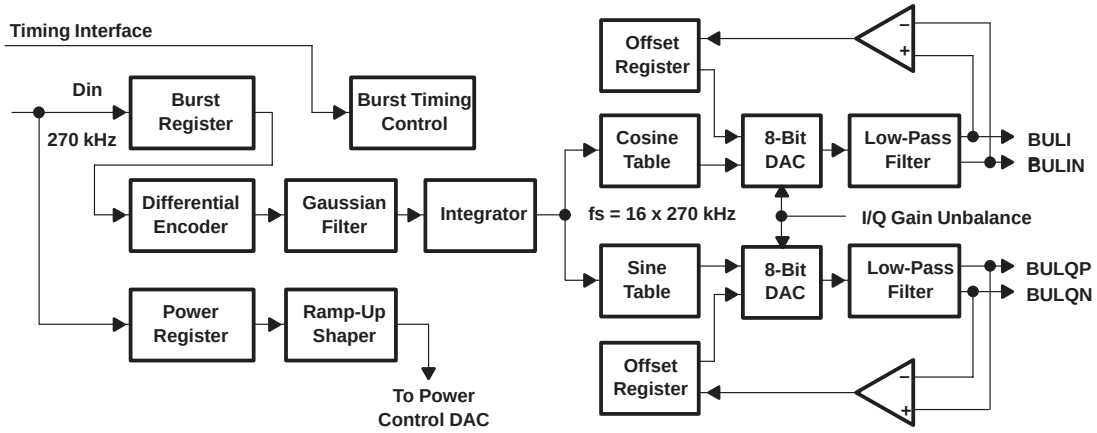


Figure 4–2. Functional Structure of The Baseband Uplink Path

4.2 Baseband Downlink Path

The baseband downlink path includes two identical circuits for processing the baseband I and Q components generated by the RF circuits. The first stage of the downlink path is a continuous-time second-order antialiasing filter (see Figure 4–3) that prevents aliasing due to sampling in the ADC. This filter also serves as an adaptation stage (input impedance and common-mode level) between external-world and on-chip circuitry.

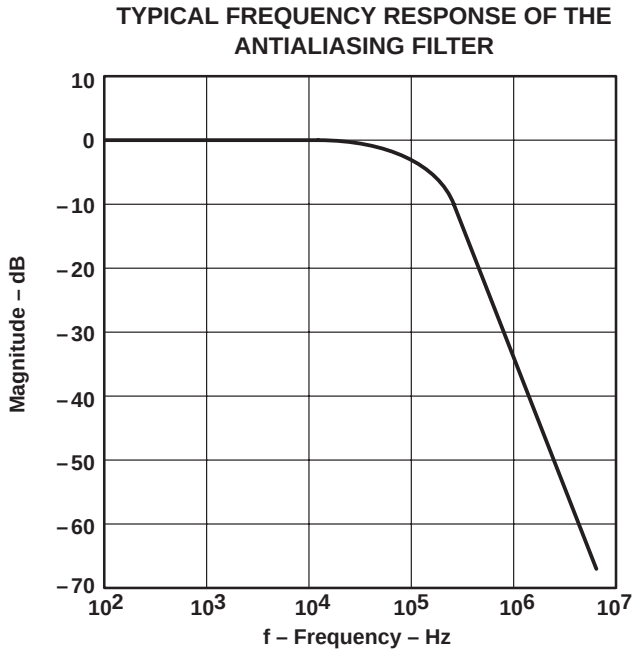


Figure 4–3. Antialiasing Filter

The antialiasing filter is followed by a third-order sigma-delta modulator that performs A/D conversion at a sampling rate of 6.5 MHz. The ADC provides 3-bit words that are fed to a digital filter (see Figure 4–4) that performs the decimation by a ratio of 24 to lower the sampling rate to 270.8 kHz and the channel separation by providing enough rejection of the adjacent channels to allow the demodulation performances required by the GSM Specification. Figure 4–5 shows the frequency response curve for the downlink digital filter and Figure 4–6 shows the in-band response curve for the same digital filter.

The baseband downlink path includes an offset register in which the value representing the channel dc offset is stored; this value is subtracted from the output of the digital filter before the digital samples are transmitted to the DSP using the serial interface. Upon reset, the offset register is loaded with 0 and updated with the BCAL calibrating signal (see Figure 3–2).

The content of the offset register results from a calibration sequence. The input BDLIP is shorted with the input BDLIN, and the input BDLQP is shorted with the input BDLQN. The digital outputs are evaluated and the values are stored in the corresponding offset registers in accordance with the dc offset of the GSM baseband and voice A/D and D/A downlink path. When the external autocalibration sequence is selected, the inputs BDLIP and BDLIN and the inputs BDLQP and BDLQN remain connected to the external circuitry. The digital outputs are evaluated, and the values stored in the corresponding offset registers take into account the dc offset of the external circuitry.

Timing control of the baseband downlink path is controlled by bits BDLON (downlink on), BCAL (calibration), and BENA (enable) when BDLON is active (see topic, timing and interface). BDLON controls the power up of the baseband downlink path; BCAL controls the start and duration of the autocalibration sequence (which can be internal or external depending on bit EXTCAL of PWDNRG1 register); and BENA controls the beginning and the duration of data transmission to the DSP by using the DSP serial interface. To avoid transmission of irrelevant data corresponding to the settling time of the digital filter. The first eight I and Q computed samples are not sent to the DSP. First, data are transmitted though the DSP interface about 30 μs after the BENA rising edge.

The power-down sequence is controlled with two bits. The first bit (BBDLW of PWDNRG1 register) determines whether the baseband downlink path can be powered down with external GSM receive window activation (BDLON). The second bit, BBDLPD of register PWDNRG1, controls the activation of the baseband downlink path. For more information about power-down control, see Section 4.8 in this document.

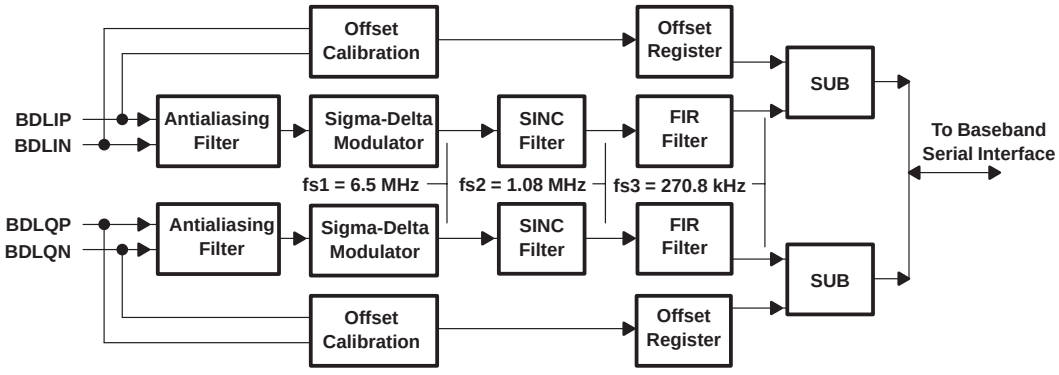


Figure 4–4. Functional Structure of the Baseband Downlink Path

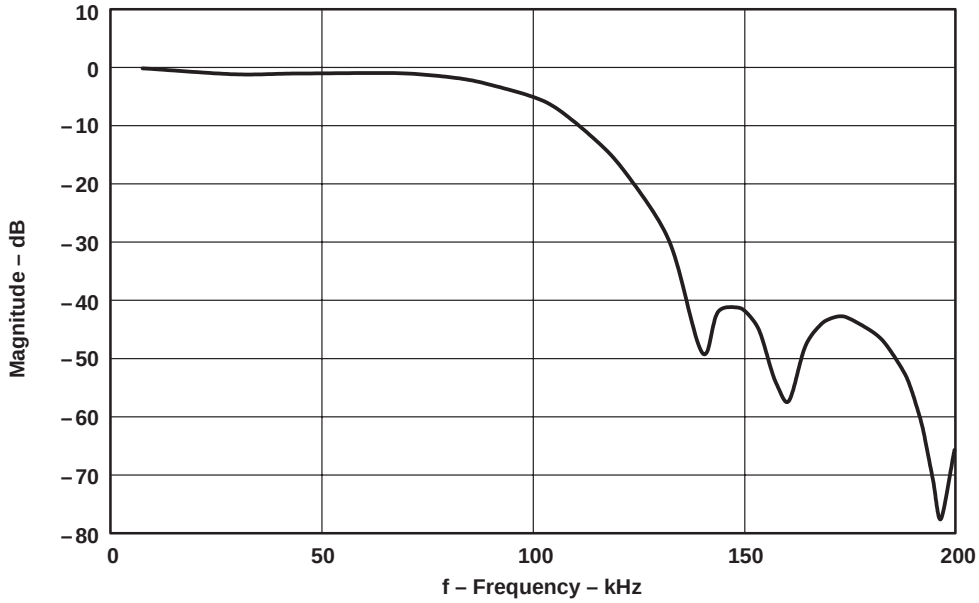


Figure 4–5. Downlink Digital Filter Frequency Response

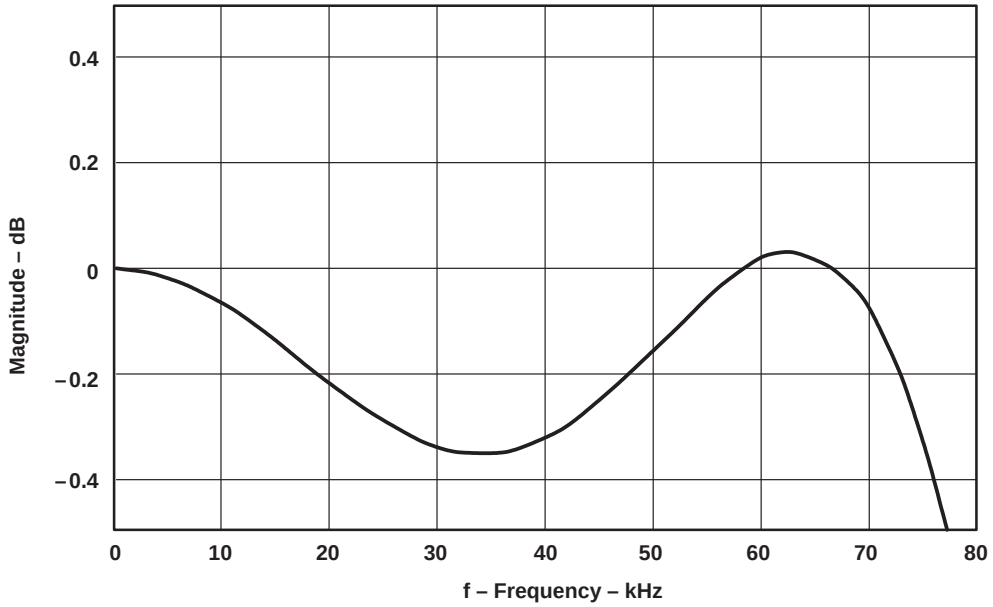


Figure 4–6. Downlink Digital Filter In-band Response

4.3 Auxiliary RF Functions

The auxiliary RF functions include the following:

- Automatic frequency control
- Auxiliary analog converter (automatic gain control)
- RF power control
- Monitoring

Each of these functions is discussed in the following paragraphs.

4.3.1 Automatic Frequency Control (AFC)

The automatic frequency control function consists of a DAC optimized for high-resolution dc conversion. The AFC digital interface includes two registers that can be written to using the serial interfaces. The content of these registers controls a 13-bit DAC whose purpose is to correct frequency shifts of the oscillator to maintain the master clock frequency in a 0.1 ppm range.

To optimize the AFC function depends on the type of oscillator used and whether its sampling frequency is programmable. This means that the lower the selected frequency, the lower the resolution and power consumption. Using a high-quality resonance oscillator filter permits the AFC circuit to operate at low frequency. Thus, a low-cost oscillator permits operation at a higher internal frequency to ensure 13-bit resolution.

The AFC value is programmed with registers AUXAFC1 (which contains the 10 LSBs) and AUXAFC2 (which contains the three MSBs). The three MSBs are sent to the DAC through a shadow register whose content is updated when LSBs are written in AUXAFC1. Proper operation of the AFC is ensured by writing the MSBs first and then the LSBs.

The internal resistance and output voltage swing selection is controlled with bit AFZ of the AUXCTL2 register. Power down is controlled with two bits: the first bit, AFCPN of the AUXCTL1 register, determines whether the AFC can be powered down from the external PWRDN terminal; the second bit, AFCPD of the AUXCTL1 register, controls the activation of the the AFC function. For more information about power-down control, see Section 4.8 in this document.

The auxiliary analog functions of the GSM baseband A/D and D/A conversions are independently powered from the $AV_{DD3/5}$ external terminal. The AFC output voltage swing is programmable to provide the largest possible voltage range. This configuration is programmed with bit AFCZ of the AUXCTRL2 register.

4.3.2 Auxiliary Analog Converter (Automatic Gain Control (AGC))

The auxiliary analog converter control function includes a register which can be written to using the serial interfaces and a 10-bit DAC that provides a control signal to set the gain of the RF section receive amplifier. The 10-bit DAC is accessed through the internal register AUXAGC.

Power down is controlled with two bits. The first bit (AGCW of the AUXCTL2 register) determines whether the AGC can be powered down with the external GSM receive window activation (BDLON). The second bit (AGCPD of the AUXCTL2 register) controls the activation of AGC function. For more information about power-down control, see Section 4.8 in this document.

The auxiliary analog functions of the GSM baseband A/D and D/A conversions are independently powered from the $AV_{DD3/5}$ external terminal. The AGC output voltage swing is programmable to provide the largest possible voltage range. This configuration is programmed with bit AGCSWG of the AUXCTL2 register.

4.3.3 RF Power Control

The RF power control section includes a register that is written to using the serial interfaces. An 8-bit DAC processes the content of this register, which determines the gain of the RF section power amplifier.

The reference of the 8-bit DAC (accessed by register AUXAPC) is provided by the ramp-up-shaper DAC which is a 5-bit DAC controlled by the APCRAM registers located in random-access memory (RAM). This area of RAM contains sixty-four 10-bit words which are read from address 0 through address 62 during the ramp-up sequence and from 63 through 1 during the ramp-down sequence at a rate of 4 MHz when bit APCSPD is at zero or at a rate of 2 MHz when bit APCSPD is at 1. The ramp-up parameters are obtained from the five least significant bits of the RAM words. The ramp-down parameters are obtained from the most significant bits of the RAM words. Content of address 0 must be identical with the content of address 1. The content of address 62 must be identical with the content of address 63.

This RAM is loaded once and its content determines the shape of the ramp-up and ramp-down control signal, which means these control signals can be adapted to the response of the power amplifier used in the RF section. The shape and timing of ramp-up and ramp-down waveforms are independent.

Timing of the ramp-up and ramp-down sequences is controlled internally; however, programming of the delay register allows adjusting the power-control start time in a 4-bit range in 1/4-bit steps. The contents of the delay register are referenced to the BENA signal, which determines the beginning of the burst-signal modulation. This feature allows adjusting the timing of the control signal versus the I and Q components within 1/4-bit accuracy, as defined in the specification GSM 05.05.

When APC is in power-down mode or when APC level is zero, the analog output is driven to V_{SS} (see Figure 4–7). During inactivity periods, the APC output is switched to V_{SS} to give low-current consumption to the power amplifier (drain cutoff current of the RF amplifier).

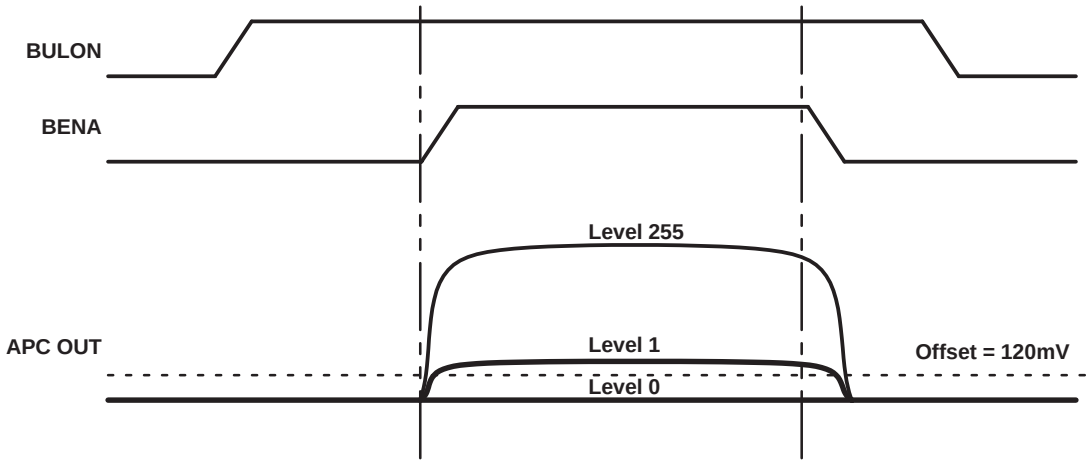


Figure 4–7. APC Output When APCMODE = 0

Typically, an offset of 120 mV (2-V swing) is added to the APC output to ensure level DAC linearity. Bit APCMODE controls how this offset is added. When APCMODE is zero, the APC output is given by

$$\text{APCout} = \text{Shape value} \times (\text{Level value} + \text{Offset}) \quad (2)$$

When APCMODE is one (see Figure 4–8), the APC output is given by formula

$$\text{APCout} = (\text{Shape value} \times \text{Level value}) + \text{Offset} \quad (3)$$

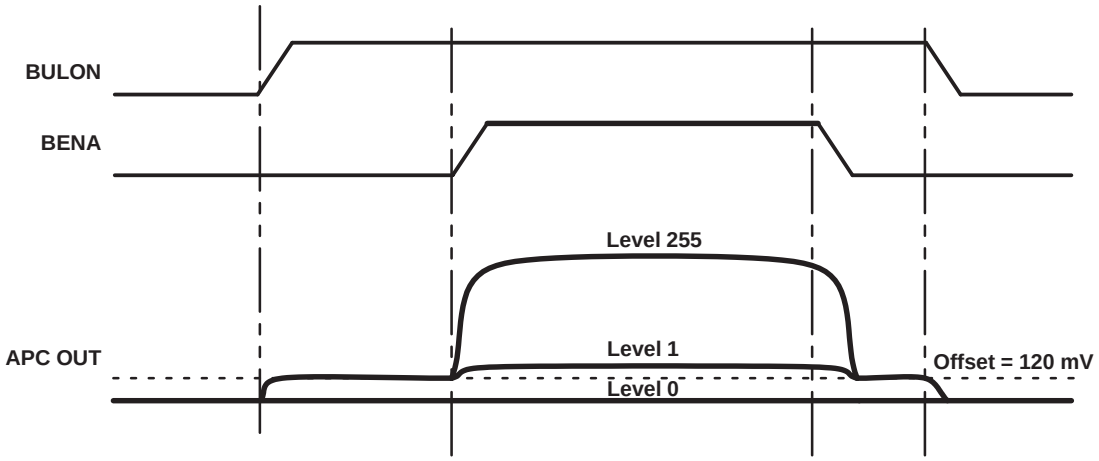


Figure 4–8. APC Output When APCMODE = 1

Power down is controlled with two bits. The first bit (APCW of the AUXCTL 2 register) determines whether the APC can be powered down by activating external GSM transmit window activation (BULON); the second bit (APCPD of the AUXCTL 2 register) controls the activation of APC function. For more information about power-down control, see Section 4.8 in this document. The auxiliary analog functions of the GSM baseband A/D and D/A conversions are independently powered from the $AV_{DD3/5}$ terminal. The APC output voltage swing is programmable to provide the largest voltage range. This configuration is programmed with bit APCSWG of the AUXCTRL 2 register.

4.3.4 Monitoring

The monitoring section includes a 10-bit A/D converter and one result register that allow monitoring of five external analog values, such as the temperature and the battery voltage. The selection of the input and reading of the control registers is done using the serial interfaces.

The selection of the input channel is done with the bits ADCCH0 – ADCCH2 of the AUXCTL1 register; the data is read from the AUXADC register. Power down is controlled with two bits. The first bit (ADCPN of the AUXCTL1 register) determines whether the A/D converter can be powered down from the external PWRDN terminal; the second bit (ADCPD of the AUXCTL1 register) controls the activation of the A/D conversion function. For more information about power-down control, see Section 4.8 in this document.

Conversion is started with a write access to the AUXCTL1 register. During the conversion, the ADCEOC bit of BSTATUS register stays at 1 and resets to 0 when the converted data is loaded into the AUXADC register. The power consumption of the main parts of the converter is limited to the useful part of the conversion time.

4.4 Voice Codec

The voice coder/decoder (codec) circuitry processes analog audio components in the uplink path and applies this signal to the voice signal interface for eventual baseband modulation. In the downlink path, the codec circuitry changes voice-component data received from the voice serial interface into analog audio. The following paragraphs describe these uplink/downlink functions in more detail.

4.4.1 Voice Uplink Path

The voice uplink path includes two input stages (see Figure 4–9). The first is a microphone amplifier compatible with an electret microphone containing an field-effect transistor (FET) buffer with open-drain output. It has a gain of typically 27 dB and provides an external voltage of 2 V to 2.5 V to bias the microphone. The auxiliary audio input can be used as an alternative source for a higher level speech signal. This stage performs single-ended-to-differential conversion and provides a gain of 6 dB. When auxiliary audio input is used, the microphone input is disabled and powered down. If both microphone and auxiliary amplifiers are powered up at the same time, only the signal of the microphone amplifier is transmitted to the voice uplink path.

The resulting fully differential signal is fed to a programmable gain amplifier that allows adjustment of the level of the speech signal to the dynamic range of the ADC, which is determined by the value of the internal voltage reference. Programmable gain can be set from –12 dB to 12 dB in 1-dB steps and is programmed with bits VULPG to VULPG4 of the VBCTL1 register.

Analog-to-digital conversion is made with a third-order sigma-delta modulator whose sampling rate is 1 MHz. Output of the A/D converter is fed to a speech digital filter which performs the decimation down to 8 kHz and limits the band of the signal with both low-pass and high-pass transfer functions. The speech samples are then transmitted to the DSP using the voice serial interface at a rate of 8 kHz.

Programmable functions of the voice uplink path, power up, input selection, and gain are controlled by the DSP or the MCU using the serial interfaces. The uplink voice path can be powered down with the bit VULON of the VBCTL1 internal register.

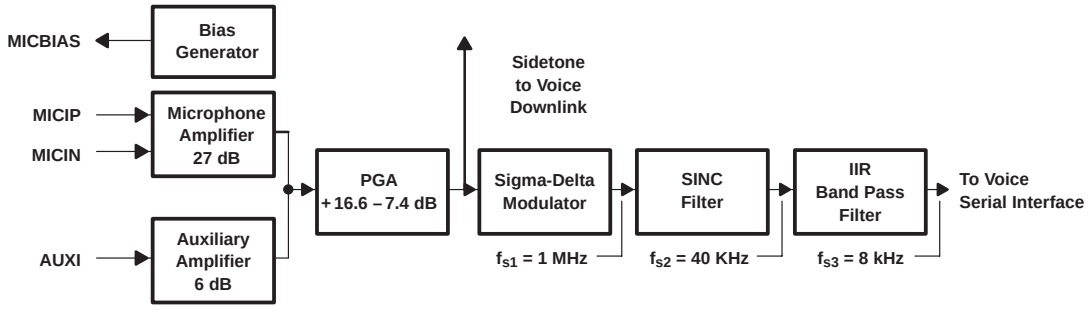


Figure 4–9. Uplink Path Block Diagram

4.4.2 Voice Downlink Path

The voice downlink path receives speech samples at an 8-kHz rate from the voice serial interface and converts them to analog signals to drive the external speech transducer.

The digital speech coming from the voice serial interface is first fed to a speech-digital infinite-duration impulse response (IIR) filter, which has two functions (see Figure 4–10). The first function is to interpolate the input signal and increase the sampling rate from 8 kHz up to 1 MHz to permit D/A conversion by an oversampling digital modulator. The second function is to limit the band of the speech signal using both low-pass and high-pass transfer functions.

The interpolated and band-limited signal is fed to a second-order sigma-delta modulator and sampled at 1 MHz to generate a 1-bit oversampled signal that drives a 1-bit DAC.

Due to the oversampling conversion, the analog signal obtained at the output of the one-bit DAC is mixed with high frequency noise. This noise is filtered by a switched-capacitor third-order low-pass filter and the remaining signal is fed to a programmable gain amplifier (PGA) to adjust the volume control. Volume control is done in 6-dB steps from 0 dB through –24 dB; in the mute state, attenuation is higher than 40 dB. A fine adjustment of gain is possible from –6 to 6 dB in 1-dB steps to calibrate the system, depending on the earphone characteristics. This configuration is programmed using the VBCTL2 register.

The PGA output is fed to two output stages: the earphone amplifier that provides a full differential signal on the terminals EARP/EARN, and an auxiliary amplifier that provides a single-ended signal on terminal AUXO. Both earphone and auxiliary amplifiers can be active at the same time. The downlink voice path can be powered down with bit VDLON of the VBCTL2 internal register.

A sidetone path is connected between the output of the voice uplink PGA and the input of the voice downlink PGA. This path provides seven programmable gains (1 dB, –2dB, – 5 dB, –8 dB, –11 dB, –14 dB, –17 dB, –20 dB, –23 dB) and one mute position. Sidetone path gain can be selected by programming bit at register address 23.

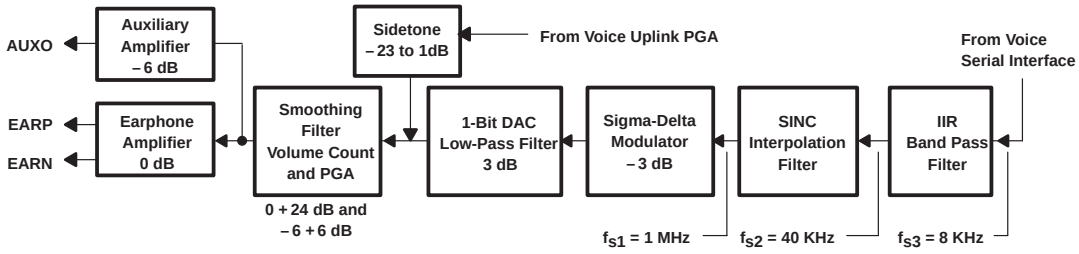


Figure 4–10. Downlink Path Block Diagram

4.5 DAI Interface

This digital audio interface (DAI) consists of four terminals: SSRST, SSCLK, SSDR, and SSDX. It is compatible with the digital audio interface described in the GSM Recommendation 11.10. This interface offers minimum CPU overhead during audio tests and speech transcoding tests, and minimizes the extra hardware and the number of external terminals of the mobile system (MS). With this interface, the DSP does not have to deal with rate adaptation. In normal operation, the DSP works with an 8-kHz sampling rate with a 16-bit word format and frame synchronization, but the DAI interface works with an 8-kHz sampling rate with a 13-bit word format without frame synchronization. The DSP (or the MCU) does not have real time constraints with SSRST because the reset of the internal transmitters is automatic.

The DAI is controlled with four internal bits of VBCTL3 register:

DAION: When 0, the DAI block is put in low power. When 1, the DAI block is active.

VDAI: This bit controls the start of the clock SSCLK. The falling edges of SSRST automatically reset the VDAI.

DAIMD 0/1: These two bits are used to switch the internal data path of the three types of DAI tests:
Tests of acoustic performance of the uplink/downlink voice path
Tests of speech decoder/DTX functions (downlink path)
Tests of speech encoder/DTX functions (uplink path)

In order to correctly execute these tests, the bits DAION/VULON/VDLON must be reset before starting the DAI test. In the case of acoustic tests, the following must be set in sequence: DAION, VDAI, VULON, and VDLON. In case of vocoder tests, when the speech samples are ready to be exchanged with the system simulator, the bits DAION and VDAI must be set at the same time.

4.6 JTAG Interface

TCM4400 provides a JTAG interface according to IEEE Std 1149.1. This interface uses five dedicated I/Os: TCK (test clock), TMS (test mode select), TDI (scan input), TDO (scan output), and TRST (test reset). Inputs TMS,TDI, and TRST contain a pullup device which makes their state high when they are not driven. Output TDO is a three-state output which is Hi-Z except when data are shifted between TDI and TDO. TRST input is intended for proper initialization of the state machine test access port (TAP) and boundary-scan cells. System RESET is sent into the device through a boundary-scan register which has to be initialized by TRST to allow the RESET signal to be propagated into the device; a good practice should be to connect RESET and TRST terminals together.

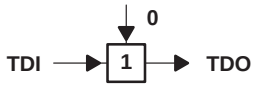
4.6.1 Standard User Instructions Available

NAME	OPCODE	DESCRIPTION
BYPASS	11111	Connects the bypass register between TDI and TDO.
SAMPLE/PRELOAD	00010	Connects the boundary-scan register between TDI and TDO. This mode captures a snapshot of the state of the digital I/Os of the device.
EXTEST	00000	Connects the boundary-scan register between TDI and TDO. This mode captures the state of the input terminals and forces the state of the output pins. This mode is for testing printed-circuit board connections between devices.
IDCODE	00001	Connects the identification register between TDI and TDO. This is the default configuration at reset.
INTEST	00011	Connects the boundary-scan register between TDI and TDO. This mode forces the internal system input signals via the parallel latches of the boundary-scan register and captures internal system outputs. The purpose of this mode is to perform internal device tests independently of the state of its input terminals. In this mode the internal system master clock is derived from TCK and is active in the run-test-idle state of the state machine to allow step-by-step operation of the device.

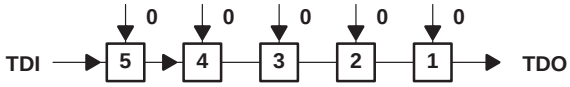
4.7 JTAG Interface Scan Chain Descriptions

The JTAG interface scan chains are described in the following sections.

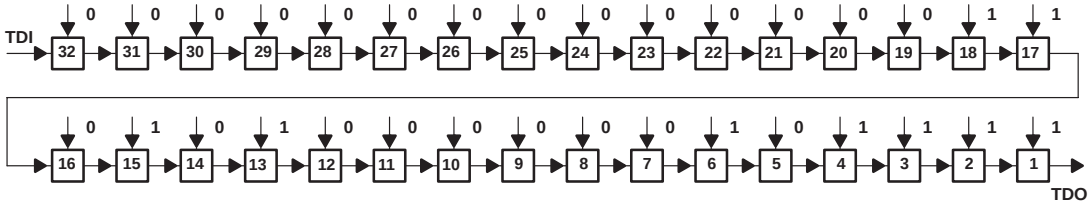
4.7.1 Bypass Register



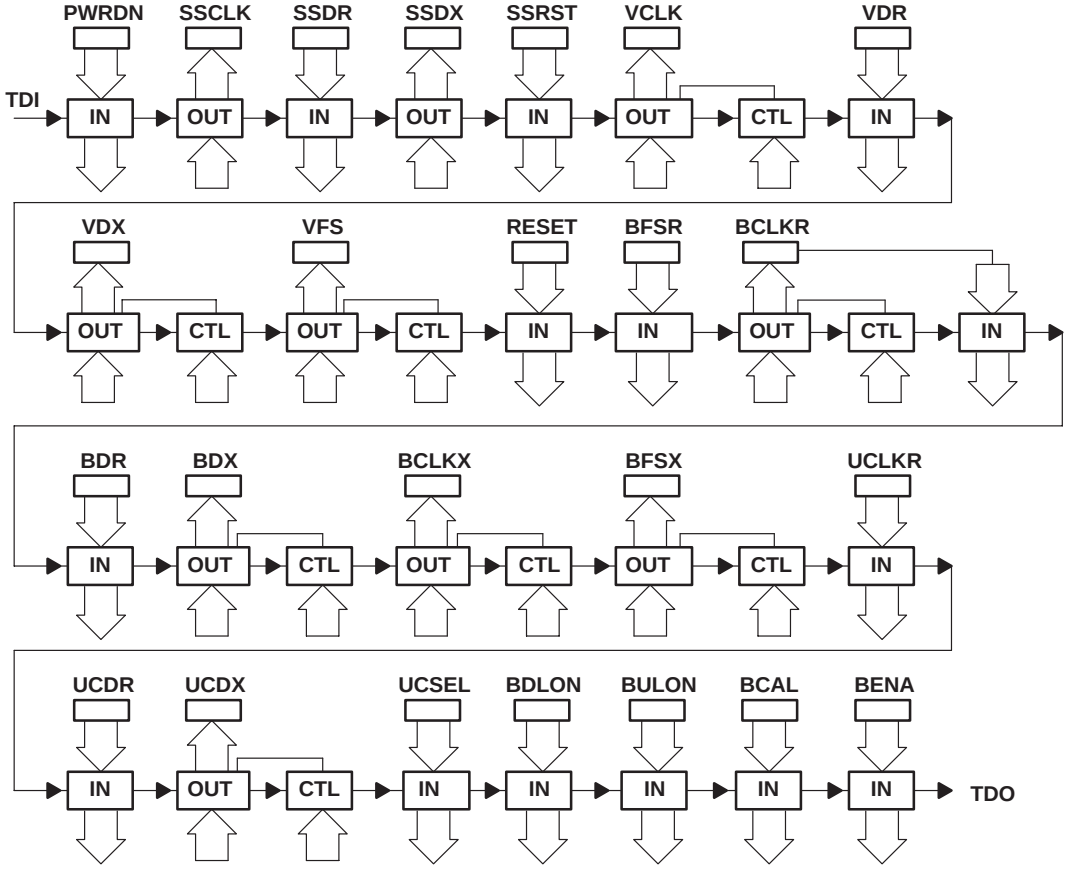
4.7.2 Instruction Register



4.7.3 Identification Register



4.7.4 Boundary-Scan Register



4.8 Power-Down Functional Description

During certain mobile activity (such as paging, conversation mode, or idle), it is possible to disable some TCM4400 functions in order to lower the power consumption. For example, it is possible to disable the internal functions dedicated to radio transmission during GSM-idle mode. It is also possible to disable the internal demodulator path during the transmit window.

There are three ways to control the power consumption of the internal blocks as described in the following paragraphs.

4.8.1 Direct Control with Internal Register

With this method, the following internal blocks are powered down:

- DAI GSM tests: bit DAION of register VBCTL3
- Transmit and receive voice path: bit VULON of register VBCTL1 and bit VDLON of register VBCTL2

4.8.2 Radio Window Activation Control

With this method, the following internal blocks are powered up with the control of two bits. The first bit enables the window control of the block activity; the second bit enables the power down.

First bit: If cleared to 0, the function is powered down with the control of the corresponding GSM window (BDLON/BULON terminal) and with the control of the second bit. If this first bit is set to 1, the power down is controlled only by the second bit.

Second bit: This bit is functionally associated with the first one. When this bit is 0, the function is in power down mode.

During transmit, the following windows are designated by the activity of the BULON terminal:

- Automatic power control (APC): bits APCW and APCPD of register AUXCTL2 are paired.
- Baseband uplink path: bits BBULW and BBULPD of register PWDNRG1 are paired.
- External reference voltage buffers VMID: bits VMIDW and VMIDPD are paired.

During receive, the following windows are designated by the activity of the BDLON terminal:

- Automatic gain control (AGC): bits AGCW and AGCPD of register AUXCTL2 are paired.
- Baseband downlink path: bits BBDLW and BBDLPD of register PWDNRG1 are paired.

4.8.3 External Terminal PWRDN Control

With this method, the internal blocks are powered under the control of two bits. The first bit enables the external terminal PWRDN control of the block activity. The second bit enables the power down. Terminal PWRDN is active high.

First bit: If cleared to 0, the function is powered down under the control of the PWRDN terminal and under the control of the second bit. If this first bit is set to 1, the power down is controlled only by the second bit.

Second bit: This bit is functionally associated with the first one. When this bit is loaded with 0, the function is in power down mode.

- For the digital serial interface to the DSP, bits BBSIPN and BBSIPD of register PWDNRG2 are paired.
- For the timing interface, bits TIMGPN and TIMGPD of register PWDNRG2 are paired.
- For the auxiliary A/D converters, bits ADCPN and ADCPD of register AUXCTL1 are paired.
- For the automatic frequency control (AFC) block, bits AFCPN and AFCPD of register AUXCTL1 are paired.
- For the external reference voltage buffers MICBIAS, bits VREFPN and VREFPD of register PWDNRG2 are paired.
- For the internal reference band gap buffers, bit VGAPPN determines whether the band gap power down is under control of the PWRDN bit.

4.9 DSP Voice Band Serial Interface

Voice band serial digital interface consists of a bidirectional serial port. Both receive and transmit operations are double buffered, which allows a continuous communication stream. The serial port is fully static and, thus, functions with any arbitrary low clocking frequency.

The transfer mode available on this port is:

Clock frequency	520 kHz	16-bit data packet	frame synchronization

VCLK is the output serial clock used to control the transmission or reception of the data, (see Figure 3–5). VCLK can run in burst mode or continuous mode, depending on the VCLKMODE bit. The transmitted serial data (VDX) is the serial data output; the frame synchronization (VFS) initiates the transfer of transmit and receive data. The received data (VDR) is the serial data input.

Each serial port includes four registers: the data transmit register (DXR), the data receive register (DRR), the transmit shift register (XSR), and the receive shift register (RSR).

The voice serial interface has the same structure and timing diagram as the serial interface. One extra cycle is generated before VFS, and two extra cycles are generated after the least significant bit (see Figure 3–5).

4.10 Voltage References

Voltage and current generators are integrated inside the GSM converter. Some additional components are required for the decoupling and regulation of the internal references. In addition, the internal buffers are automatically shut down with the corresponding functions being powered down.

The following six terminals are reserved for voltage references decoupling and use: VGAP, IBIAS, VREF, MICBIAS, and VMID (see Table 4–1):

VGAP: This terminal is connected to the internal band gap reference voltage. It must be externally connected to a 0.1-µF capacitor. The band gap drives the current generator and the voltage reference. This band gap may be powered down by the PWRDN pin, depending on bit VGAPPN of register PWDNRG2.

IBIAS: This terminal is connected to the current reference. It must be externally connected to a 100-kΩ resistor. Because this block is connected to the AFC function, the power down is controlled by similar means. The current generator is shut down with the same bits of the band gap: one bit for the power down selection of a hardware solution (with the external PWRDN terminal).

VREF: This terminal is connected to the internal reference voltage. It must be externally connected to a 0.1-µF capacitor. This band gap may be down powered under the control of bits VREFPN and VREFPD of register PWDNRG2. This voltage reference is internally connected to three buffers corresponding to the blocks of speech downlink, speech uplink, and GMSK downlink. The two first blocks are powered down with the inactivity of the corresponding speech blocks. This last block is shut down outside the radio downlink activations.

VMID: This buffer gives the $V_{DD}/2$- or 1.35-V common-mode output voltage of the baseband uplink path. This voltage value is selected with the SELVMID bit.

MICBIAS: This buffer is destined to drive an electret-type microphone. The output voltage can be chosen by software (bit MICBIAS of the VBCTL1 register) from 2 V to 2.5 V.

ADCMID: For decoupling purposes, the ADCMID terminal is connected to the internal comparison threshold of the ADC. Setup time before the ADC is powered on depends on the value of the external decoupling capacitor.

Table 4–1. Voltage References

REFERENCE	VOLTAGE	DEFINITION
VGAP	1.22 V	Band gap used for all other references
VREF	1.75 V	Voltage reference of GMSK internal ADC and DAC
VMID	$AV_{DD2}/2$	Common-mode reference for uplink/downlink GMSK
MICBIAS	2 V/2.5 V	Microphone-driving voltage
ADCMID	$A_{VDD3}/2$	Voltage dc biasing of the auxiliary ADCs

4.10.1 MCU Serial Baseband Digital Interface

The GSM baseband and voice A/D and D/A conversion provide two digital serial 16-bit interfaces for use with the DSP and a microcontroller device. Through this interface, a microcontroller can access all the internal registers that can be accessed through the DSP digital serial interface.

This option is for applications in which part of layer-1 software is implemented into the microcontroller and needs access to some functions implemented into the GSM baseband and voice A/D and D/A conversion circuitry.

4.10.2 Serial Interface

The microcontroller serial interface is compliant with 8-bit standard synchronous serial ports. This interface consists of four terminals (see Figure 3–4 for timing diagram).

UCLK: A clock provided by the microcontroller to GSM baseband and voice A/D and D/A conversion

UDR: An input terminal of the GSM baseband and voice A/D and D/A components for reception of data

UDX: An output terminal of the GSM baseband and voice A/D and D/A components for transmission of data

USEL: An input terminal of GSM baseband and voice A/D and D/A components for activation of the serial interface

When USEL = V_{DD}, the serial interface is deactivated and UDX is placed in a high-impedance state. A high level on USEL resets the internal serial interface; the 16-bit transfers must be completed with USEL = V_{SS}.

The external MCU initiates data transfer by driving the selection terminal and sending a clock signal. For both the GSM baseband and voice A/D and D/A components, the MCU data is shifted out of the shift registers on one edge of the clock and latched into the shift registers on the opposite clock edge.

As a result, both controllers send and receive data simultaneously. For the MCU portion, the software determines whether the data is meaningful or dummy data. On the GSM baseband and voice A/D and D/A conversion portion, dummy data is data with all zeroes.

The 16-bit word data format is identical to the DSP data format. After a read-register command, there is a sequential transfer delay between two 16-bit word acquisitions to let the internal sequencer extract the data going from internal registers to the serial shift register.

Three internal bits control the data serial flow as follows:

- UDIR determines whether data is transferred with MSB or LSB first.
- UPOL determines the polarity of the clock.
- UPHA determines the insertion of a half-clock period in the data serial flow.

With UPOL and UPHA, there are four clock schemes (see Table 4–2):

- Falling edge without delay. The MCU serial interface transmits data on the falling edge of the UCLK and receives data on the rising edge of the UCLK.
- Falling edge with delay. The MCU serial interface transmits data one half-cycle ahead of the falling edge of the UCLK and receives data on the falling edge of the UCLK.
- Rising edge without delay. The MCU serial interface transmits data on the rising edge of the UCLK and receives data on the falling edge of the UCLK.
- Rising edge with delay. The MCU serial interface transmits data one half-cycle ahead of the rising edge of the UCLK and receives data on the rising edge of the UCLK.

Table 4–2. Microcontroller Clocking Schemes

UPOL	UPHA	MCU Clocking Scheme
1	1	Falling edge without delay
1	0	Falling edge with delay
0	1	Rising edge without delay
0	0	Rising edge with delay

4.10.3 DSP/MCU Serial Interface

The DSP/MCU serial interface not only configures the GSM baseboard and voice A/D and D/A conversion but also transmits data to the DSP during downlink burst reactions. The following paragraphs describe the operation of the serial interface in more detail.

4.10.4 DSP Serial Digital Interface

The DSP serial digital interface (see Figure 4–11) transfers the baseband transmit and receive data, and also accesses all internal programming registers of the device (baseband codec, voice codec, and auxiliary RF functions). The format for the serial interface is 16 bits.

The baseband serial digital interface is a bidirectional (transmit/receive) serial port. Both receive and transmit operations are double buffered and permit a continuous communication stream (16-bit data packets). The serial port is fully static and functions with any arbitrary, low clocking frequency.

Six terminals are used for the serial port interface (see Figure 3–4 for timing diagram). BCLKR is an I/O port for the serial clock used to control the reception of the data BDR. At reset BCLKR is configured as an output and the clock frequency is set to MCLK/3 (4.333 MHz with MCLK = 13 MHz); the clock signal is running continuously. The port BCLKR can be reconfigured as an input by programming an internal register. In this case BCLKR is provided by the DSP and can run in burst mode to reduce power consumption. The receive frame synchronization (BFSR) is used to identify the beginning of a data packet transfer on port BDR.

The transmitted serial data (BDX) is the serial data input; the transmit frame synchronization (BFSX) initiates the transmission of data. The transmit clock (BCLKX) is provided by the GSM baseband and voice ADCs and DACs with a MCLK frequency. The clock signal BCLKX can run in burst mode or continuous mode, depending on the BCLKMODE bit. The downlink data bus (BFSX, BCLKX, BDX) can be driven to V_{SS} or placed in a high-impedance state when no data is to be transferred to the DSP. The BCLKDIR bit of the BCTLREG register controls the direction of the BCLKR clock.

As with the voice serial interface, one extra clock cycle must be generated because the last 16-bit word received on the DSP serial interface is latched on the next two falling BCLKR edges following the LSB. As for the voice serial interface, one extra clock period is generated on the BCLKX before the first synchronization BFSX of the downlink data sequence.

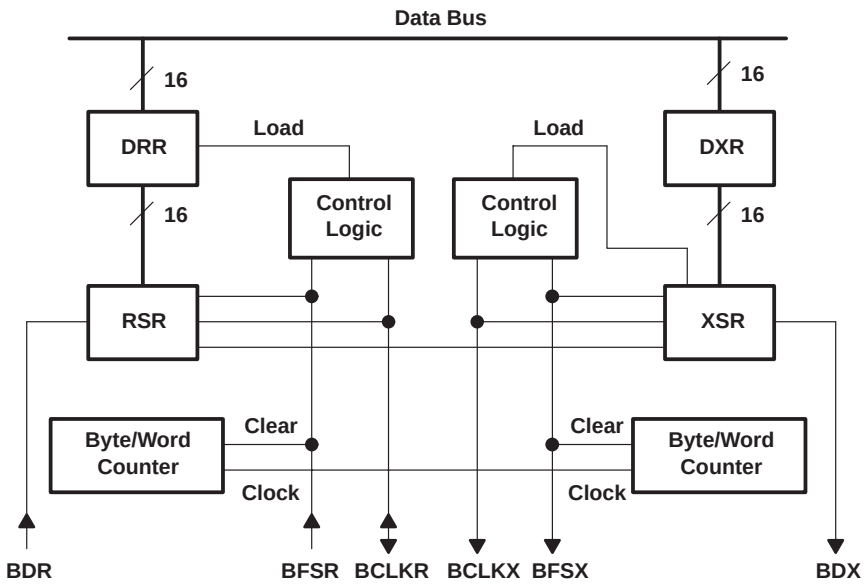


Figure 4–11. DSP Serial Digital Interface

4.10.5 DSP/MCU Serial Interface Operation and Format

The DSP/MCU serial interface configures the GSM baseband and voice ADCs and DACs (read and write operation in internal registers), and transmits RF data to the DSP during reception of a burst by the downlink path of the GSM baseband and voice A/D and D/A circuitry.

During reception of a burst (bit DLR of the status register is 1), the DSP serial interface and associated internal bus are dedicated to the transfer of RF data from the GSM baseband ADCs and DACs to the DSP. During this period, only a write operation of internal registers can be done through the DSP serial interface. However, all registers can be accessed by the MCU serial interface.

During transmission of a burst (bit ULX of the status register is 1), no read or write operation can be done in the registers of the baseband uplink part of the GSM baseband, APC RAM, and APC shape register.

Writing or reading registers using the serial interface is done by transferring 16-bit words to the serial interface. Each word is split into three fields as shown in Table 4–3.

Table 4–3. Read/Write Data Word

DATA										ADDRESS					R/W
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	1 / 0

When writing to internal registers observe the following convention:

Bit 0: This bit indicates a write operation at zero.

Bits 1 – 5: This field contains the address of the register to be accessed.

Bits 6 – 15: This field contains the data to be written into the internal register.

When reading from internal registers observe the following convention:

Bit 0: At 1, this bit indicates a read operation.

Bits 1 – 5: This field contains the address of the register to be accessed.

Bits 6 – 15: This field is an irrelevant status in a read request operation.

Read operation from the downlink baseband codec is done using the TX part of the DSP/MCU serial interface in the 16-bit word format defined in Table 4–4.

Table 4–4. 16-Bit Word Format

DATA										ADDRESS					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A4	A3	A2	A1	A0	0

During reception of a burst, transfer of RF data from the downlink baseband codec is done using the transmit part of the DSP serial interface in the 16-bit word format, defined in Table 4–5. Because the I and Q samples are coded with 16-bit words, the data rate is $270833 \times 16 \times 2$, which equals 8.66 Mbps. I and Q samples are differentiated by setting the LSB to zero for I samples and to one for Q samples. Because the digital clock MCLK is 13 MHz, transfer is done at 13 Mbps in burst mode. During burst reception, the DSP serial interface is idle about 33 percent of the time.

Table 4–5. Format of 16-Bit Word Transfer

DATA															I/Q
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

4.10.6 DSP/MCU Serial Interface Registers

The following internal register buffers are accessed using the DSP/MCU serial interface during manual operation of the TCM4400.

4.10.7 Baseband Uplink Ramp-delay Register

Each bit position of the baseband uplink ramp-delay register is defined in Table 4–6.

Table 4–6. Uplink Ramp-Delay Register

BULRUDEL: BASEBAND UPLINK RAMP-DELAY REGISTER										ADDRESS: 1					R/W
RESERVD	IBUFPTR	DELD 3	DELD 2	DELD 1	DELD 0	DELU 3	DELU 2	DELU 1	DELU 0	0	0	0	0	1	1 / 0
R = 0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	←ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	←VALUE AT RESET					

DELU0 to DELU3: Value of the delay of ramp-up start versus the rising edge of BENA

DELD0 to DELD3: Value of the delay of ramp-down start versus the falling edge of BENA

IBUFPTR: Writing a 1 in this bit initializes the pointer of the burst buffer to the base address. This is not a toggle bit and has to be set back to 0 to allow writing into the burst buffer.

RESERVD: Reserved bits for testing purposes

R/W: A 1 indicates a read operation; a 0 indicates a write operation.

4.10.8 Baseband Uplink Data Buffer

The baseband uplink data buffer is used to transmit the uplink burst data. The uplink data buffer contents are defined in Table 4–7.

Table 4–7. Uplink Data Buffer

BULDATA: BASEBAND UPLINK DATA BUFFER										ADDRESS: 2 (16 WORDS)					W
BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7	BIT8	BIT9	0	0	0	1	0	0
BIT10	BIT11	BIT12	BIT13	BIT14	BIT15	BIT16	BIT17	BIT18	BIT19	0	0	0	1	0	0
BIT20	BIT21	BIT22	BIT23	BIT24	BIT25	BIT26	BIT27	BIT28	BIT29	0	0	0	1	0	0
BIT30	BIT31	BIT32	BIT33	BIT34	BIT35	BIT36	BIT37	BIT38	BIT39	0	0	0	1	0	0
BIT40	BIT41	BIT42	BIT43	BIT44	BIT45	BIT46	BIT47	BIT48	BIT49	0	0	0	1	0	0
BIT50	BIT51	BIT52	BIT53	BIT54	BIT55	BIT56	BIT57	BIT58	BIT59	0	0	0	1	0	0
BIT60	BIT61	BIT62	BIT63	BIT64	BIT65	BIT66	BIT67	BIT68	BIT69	0	0	0	1	0	0
BIT70	BIT71	BIT72	BIT73	BIT74	BIT75	BIT76	BIT77	BIT78	BIT79	0	0	0	1	0	0
BIT80	BIT81	BIT82	BIT83	BIT84	BIT85	BIT86	BIT87	BIT88	BIT89	0	0	0	1	0	0
BIT90	BIT91	BIT92	BIT93	BIT94	BIT95	BIT96	BIT97	BIT98	BIT99	0	0	0	1	0	0
BIT100	BIT101	BIT102	BIT103	BIT104	BIT105	BIT106	BIT107	BIT108	BIT109	0	0	0	1	0	0
BIT110	BIT111	BIT112	BIT113	BIT114	BIT115	BIT116	BIT117	BIT118	BIT119	0	0	0	1	0	0
BIT120	BIT121	BIT122	BIT123	BIT124	BIT125	BIT126	BIT127	BIT128	BIT129	0	0	0	1	0	0
BIT130	BIT131	BIT132	BIT133	BIT134	BIT135	BIT136	BIT137	BIT138	BIT139	0	0	0	1	0	0
BIT140	BIT141	BIT142	BIT143	BIT144	BIT145	BIT146	BIT147	BIT148	BIT149	0	0	0	1	0	0
BIT150	BIT151	BIT152	BIT153	BIT154	BIT155	BIT156	BIT157	BIT158	BIT159	0	0	0	1	0	0
W	W	W	W	W	W	W	W	W	W	←ACCESS TYPE					
1	1	1	1	1	1	1	1	1	1	←VALUE AT RESET					

Bit 0 through Bit 159 are the bits composing the sequence of the transmitted burst. Bit 0 is transmitted first. For a normal burst, the uplink data buffer is loaded as follows:

Bits 0 to 3: 4 guard bits

Bits 4 to 6: 3 tail bits

Bits 7 to 66: 58 data bits

Bits 67 to 92: 26 training sequence bits

Bits 93 to 92: 58 training sequence bits

Bits 151 to 153: 3 tail bits

Bits 154 to 159: 8 guard bits

At reset and after each transmission, the burst buffer is reinitialized with guard bits (all bits = 1). An address pointer is incremented after each word written into the buffer so that the next write operation affects the next word of the buffer. This address pointer is set to the base address (word 0) by a RESET after transmission of a burst or by setting the IBUFPTR bit to 1. This bit has to be set back to zero to release the address pointer.

4.10.9 Baseband Uplink I and Q Offset Registers

The baseband uplink I and Q offset registers contain the offset values for the I and Q components, respectively, as given in Table 4–8 and Table 4–9.

Table 4–8. Uplink I Offset Register

BULIOFF: BASEBAND UPLINK I OFFSET REGISTER										ADDRESS: 3					R/W
RESERVD	ULI-OFF 8	ULI-OFF 7	ULI-OFF 6	ULI-OFF 5	ULI-OFF 4	ULI-OFF 3	ULI-OFF 2	ULI-OFF 1	ULI-OFF	0	0	0	1	1	1/0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	←ACCESS TYPE					
0	0	1	1	1	1	1	1	1	1	←VALUE AT RESET					

ULIOFF0 to ULIOFF1: Integration bits during calibration (to minimize sensitivity to noise)

ULIOFF2 to ULIOFF8: Value of the offset on I channel

RESERVD: Reserved bits for testing purposes

R/W: A 1 indicates a read operation; a 0 indicates a write operation.

Table 4–9. Uplink Q Offset Register

BULQOFF: BASEBAND UPLINK Q OFFSET REGISTER										ADDRESS: 4					R/W
RESERVD	ULQ OFF 8	ULQ OFF 7	ULQ OFF 6	ULQ OFF 5	ULQ OFF 4	ULQ OFF 3	ULQ OFF 2	ULQ OFF 1	ULQ OFF 0	0	0	1	0	0	1/0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	←ACCESS TYPE					
0	0	1	1	1	1	1	1	1	1	←VALUE AT RESET					

ULQOFF0 to ULQOFF1: Integration bits during calibration (to minimize sensitivity to noise)

ULQOFF2 to ULQOFF8: Value of the offset on Q channel

RESERVD: Reserved bits for testing purposes

R/W: A 1 indicates a read operation; a 0 indicates a write operation.

4.10.10 Baseband Uplink I and Q D/A Conversion Registers

The I and Q component values generated by the I and Q uplink DAC during the conversion of analog data are written to and read from the uplink I and Q DAC registers as defined in Table 4–10 and Table 4–11, respectively.

Table 4–10. Uplink I DAC Register

BULIDAC: BASEBAND UPLINK I DAC REGISTER										ADDRESS: 6					R/W
RESERVD	RESERVD	ULI-DAC 7	ULI-DAC 6	ULI-DAC 5	ULI-DAC 4	ULI-DAC 3	ULI-DAC 2	ULI-DAC 1	ULI-DAC 0	0	0	1	1	0	1/0
R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	←ACCESS TYPE					
0	0	1	1	1	1	1	1	1	1	←VALUE AT RESET					

ULIDAC0 to ULIDAC7: Data applies to the DAC of I channel.

RESERVD: Bits are reserved for testing purposes.

R/W: A 1 indicates a read operation; a 0 indicates a write operation.

Table 4–11. Uplink Q DAC Register

BULQDAC: BASEBAND UPLINK Q DAC REGISTER										ADDRESS: 5					R/W
RESERVD	RESERVD	ULD-DAC 7	ULQ-DAC 6	ULQ-DAC 5	ULQ-DAC 4	ULQ-DAC 3	ULQ-DAC 2	ULQ-DAC 1	ULQ-DAC 0	0	0	1	0	1	1/0
R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	←ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	←VALUE AT RESET					

ULQDAC0 to ULQDAC7: Data applies to D/A converter of I channel.

RESERVD: Bits are reserved for testing purposes.

R/W: A 1 indicates a read operation; a 0 indicates a write operation.

4.10.11 Power-Down Register 2

The values in each bit position of power-down register 2 are defined in Table 4–12.

Table 4–12. PWDNRG2 Register

PWDNRG2: REGISTER FOR POWERING DOWN										ADDRESS: 8					R/W
RESERVD	RESERVD	TIM GPN	TIM GPD	BBS IPN	BBS IPD	VGA PPN	CHG UP	VREF PN	VREF PD	0	1	0	0	0	1/0
R = 0	R = 0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	←ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	←VALUE AT RESET					

VREFPN: If this bit is cleared to 0, the internal reference voltage is powered down under the control of terminal PWRDN and bit VREFPD. If bit VREFPN is set to 1, the power down is controlled only by bit VREFPD.

VREFPD: This bit is functionally associated with bit VREFPN.

VGAPPN: If this bit is cleared to 0, the internal reference VGAP is powered down under the control of terminal PWRDN. If this bit is set to 1, the VGAP is not placed in power-down mode.

TIMGPN: If this bit is cleared to 0, the timing interface is powered down under the control of terminal PWRDN. If this bit is set to 1, the power down is controlled only by bit TIMPGD.

TIMGPD: This bit is functionally associated with bit TIMGPN.

BBSIPN: If this bit is cleared to 0, the baseband serial interface is powered down under the control of terminal PWRDN. If this bit is set to 1, the power down is controlled only by bit BBSIPD.

BBSIPD: This bit is functionally associated with bit BBSIPN. When this bit is set to 1, the baseband serial interface is in power-down mode.

CHGUP: This bit is used for testing purposes to accelerate the band gap settling time.

RESRVD: Bits are reserved for testing purpose.

4.10.12 Power-Down Register No. 1

The values in each bit position of power-down register 1 are defined in Table 4–13.

Table 4–13. PWDNRG1 Register

PWDNRG1: REGISTER FOR POWERING DOWN										ADDRESS: 7					R/W
SEL VMID	BA LOOP	VMID W	VMID PD	BBUL W	BBUL PD	BBDL W	BBDL PD	EXT CAL	BBR ST	0	0	1	1	1	1/0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	←ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	←VALUE AT RESET					

BBRST: This is the digital reset of the baseband codec (active at 1); the uplink burst buffer is loaded with all 1s, and the memory and registers of the downlink digital filter is cleared to 0. This is not a toggle bit; it has to be set to 0 to remove the reset condition.

EXTCAL: Downlink autocalibration mode (0 = autocalibration; 1 = external calibration)

BBULW: If this bit is cleared to 0, the baseband uplink path is powered down under the control of the GSM transmit window (BULON terminal). If this bit is set to 1, the power down is controlled only by bit BBULPD.

BBULPD: This bit is functionally associated with bit BBULW. When this bit is set to 1, the baseband uplink path is in power-down mode.

BBDLW: If this bit is cleared to 0, the baseband downlink path is powered down under the control of the GSM receive window (BDLON terminal). If this bit is set to 1, the power down is controlled only by bit BBDLPD.

BBDLPD: This bit is functionally associated with bit BBDLW. When this bit is set to 1, the baseband downlink path is in power-down mode.

VMIDW: If this bit is cleared to 0, the VMID output driver is powered down under the control of the GSM transmit window (BULON terminal). If this bit is set to 1, the power down is controlled only by bit VMIDPD.

VMIDPD: This bit is functionally associated with and paired with bit VMIDW. When VMIDW bit is set to 1, the VMID output driver is active. When VMIDPD bit is set to 1, the VMID output driver is in power-down mode.

BALOOP: When this bit is set to 1, the internal analog loop of I and Q uplink terminals are connected to I and Q downlink terminals.

SELVMID: When this bit is cleared to 0, this sets the common-mode voltage of the baseband uplink and VMID at $V_{DD}/2$; when set to 1, these voltages are set to 1.35 V.

4.10.13 Baseband Control Register

The values in the baseband control register bit positions determine whether the data is shifted left or right (see Table 4–14). Note that the MCU clocking scheme determines the edge of the clock on which that data is received or transmitted using the serial interface (see Table 4–15).

Table 4–14. Baseband Control Register

BCTLREG: BASEBAND CONTROL REGISTER										ADDRESS: 9					R/W
RE-SERVD	RE-SERVD	RE-SERVD	MCL KBP	BCLK MODE	BIZ-BUS	BCL KDIR	UDIR	UPHA	UPOL	0	1	0	0	1	1/0
R = 0	R = 0	R = 0	R /W	R /W	R/W	R/W	R/W	R/W	R/W	←ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	←VALUE AT RESET					

UDIR: This bit determines whether the data is shifted in from right (see serial register description) to left, MSB first (bit value 0), or from left to right, LSB first (bit value 1).

BCLKMODE: When this bit is cleared to 0, BLCKX runs in burst mode; when set to 1, BCLKX is continuous.

MCLKBP: When this bit is cleared to 0, the MCLK signal passes through the clock slicer; when set to 1, the clock slicer is bypassed (in this case, the signal at the MCLK terminal must be digital).

4.10.14 MCU Clocking Schemes

Falling edge without delay: The MCU serial interface transmits data on the falling edge of UCLK and receives data on the rising edge of UCLK.

Falling edge with delay: The MCU serial interface transmits data one half-cycle ahead of the falling edge of UCLK and receives data on the falling edge of UCLK.

Rising edge without delay: The MCU serial interface transmits data on the rising edge of UCLK and receives data on the falling edge of UCLK.

Rising edge with delay: The MCU serial interface transmits data one half-cycle ahead of the rising edge of the UCLK and receives data on the rising edge of UCLK.

Table 4–15. MCU Clocking Schemes

UPOL	UPHA	MCU CLOCKING SCHEME
1	1	Falling edge without delay
1	0	Falling edge with delay
0	1	Rising edge without delay
0	0	Rising edge with delay

BCLKDIR: Direction of the BCLKR port (0 → Output, 1 → Input).

BIZBUS: When this bit is set to 1, BDX, BCLKX, BFSX are in hi-Z when there is nothing to transfer to the DSP; when it is cleared to 0, DBX, BCLKX, and BFSX are set to V_{SS} when there is nothing to transfer to the DSP.

RESRVD: Bits are reserved for testing purpose.

4.10.15 Voice Band Uplink Control Register

The values in the voice band uplink control register bit positions control not only the power level of the audio in the uplink path but also set the gain of the PGA from –12 dB to 12 dB in 1-dB steps. Bit MICBIAS and VULMIC and VULAUX are shifted by one position to the left. This is defined in Table 4–16.

Table 4–16. Voice Band Uplink Control Register

VBCTL1: VOICE BAND UPLINK CONTROL REGISTER										ADDRESS: 10					R/W
RESERVD	MIC-BIAS	VUL MIC	VUL AUX	VUL PG4	VUL PG3	VUL PG2	VUL PG1	VUL PG0	VULON	0	1	0	1	0	1/0
R = 0	R /W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	←ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	←VALUE AT RESET					

VULON: Power on the uplink path of the audio codec

VULAUX: Enables the auxiliary input amplifier if bit VULON is 1

VULMICL: Enables the microphone input amplifier if bit VULON is 1

MICBIAS: When MICBIAS = 0, the analog bias for the electric microphone and external decoupling is driven to 2 V; when the value is 1, the bias is 2.5 V.

RESERVD: Reserved for testing

VULPG (0–4): Gain of the voice uplink programmable gain amplifier (–12 dB to 12 dB in 1 dB step). See Table 4–17.

Table 4–17. Uplink PGA Gain

VULPG 4	VULPG 3	VULPG 2	VULPG 1	VULPG 0	RELATIVE GAIN
1	0	0	0	0	–12 dB
1	0	1	1	1	–11 dB
1	1	0	0	0	–10 dB
1	1	0	0	1	–9 dB
1	1	0	1	0	–8 dB
1	1	0	1	1	–7 dB
0	0	0	0	0	–6 dB
0	0	0	0	1	–5 dB
0	0	0	1	0	–4 dB
0	0	0	1	1	–3 dB
0	0	1	0	0	–2 dB
0	0	1	0	1	–1 dB
0	0	1	1	0	0 dB
0	0	1	1	1	1 dB
0	1	0	0	0	2 dB
0	1	0	0	1	3 dB
0	1	0	1	0	4 dB
0	1	0	1	1	5 dB
0	1	1	0	0	6 dB
1	0	0	0	1	7 dB
1	0	0	1	0	8 dB
1	0	0	1	1	9 dB
1	0	1	0	0	10 dB
1	0	1	0	1	11 dB
1	0	1	1	0	12 dB

4.10.16 Voice Band Downlink Control Register

The values in the voice band downlink control register bit positions control the audio power level in the downlink path. Earphone volume is set (three bits VOLCTL0 –VOLCTL 2), and PGA gain is set from – 6 dB to 6 dB in 1-dB steps. This is defined in Table 4–18.

Table 4–18. Voice Band Downlink Control Register

VBCTL 2: VOICE BAND DOWNLINK CONTROL REGISTER										ADDRESS: 11					R/W
VDLAUX	VDLEAR	VOL CTL 2	VOL CTL1	VOL CTL0	VDLG 3	VDLG 2	VDLG 1	VDLG 0	VDL ON	0	1	0	1	1	1 / 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	←ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	←VALUE AT RESET					

VDLON: Power on of the downlink path of the audio codec

VDLEAR: Enables the earphone amplifier if the VDLON bit is 1

VDLAUX: Enables the auxiliary output amplifier if the VDLON bit is 1

VGLG (0 – 3) 1 dB: Gain of the voice downlink programmable gain amplifier (– 6 dB to 6 dB in 1-dB steps). See Table 4–19.

Table 4–19. Downlink PGA Gain

	VDLG3	VDLG2	VDLG1	VDLG0	RELATIVE GAIN
0	0	0	0	0	– 6 dB
1	0	0	0	1	– 5 dB
2	0	0	1	0	– 4 dB
3	0	0	1	1	– 3 dB
4	0	1	0	0	– 2 dB
5	0	1	0	1	– 1 dB
6	0	1	1	0	0 dB
7	0	1	1	1	1 dB
8	1	0	0	0	2 dB
9	1	0	0	1	3 dB
10	1	0	1	0	4 dB
11	1	0	1	1	5 dB
12	1	1	0	0	6 dB
13	1	1	0	1	– 6 dB
14	1	1	1	0	– 6 dB
15	1	1	1	1	– 6 dB

VOLCTL (0 – 2): Volume control (0, – 6 ,–12, 18, – 24, Mute). See Table 4–20.

Table 4–20. Volume Control Gain Settings

	VOLCTL2	VOLCTL1	VOLCTL0	RELATIVE GAIN
0	0	1	0	0 dB
1	1	1	0	–6 dB
2	0	0	0	–12 dB
3	1	0	0	–18 dB
4	0	1	1	–24 dB
5	1	0	1	Mute
6	0	0	1	Mute
7	1	1	1	Mute

4.10.17 Voice Band Control Register

The values in the voice band control register are defined in Table 4–21.

Table 4–21. Voice Band Control Register

VBCTL3: VOICE BAND CONTROL REGISTER										ADDRESS: 12					R/W
RESERVD	RESERVD	VCLK MODE	DAI MD1	DAI MD0	VDAI	DAI ON	VA LOOP	VIZ-BUS	VRST	0	1	1	0	0	1 / 0
R = 0	R = 0	R /W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	←ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	←VALUE AT RESET					

VALOOP: When this bit is set to 1, the internal analog loop of output samples is sent to the audio input terminal; standard audio paths are connected together; and auxiliary audio paths are connected together.

VIZBUS: When this bit is set to 1, VFS, VCLK, and VDX are put in a hi-Z state when there is nothing to transfer to the DSP. When it is cleared to 0, VFS and VCLK are put in V_{SS} when there is nothing to transfer to the DSP, and the VDX bus drives an undefined value (value depends on the previous serial data transfers).

VRST: When this bit is 1, resets the digital parts of the audio codec (digital filter and modulator). This is not a toggle bit and has to be set to 0 to remove the reset condition.

DAION: When this bit is cleared to 0, the DAI block is in power down; when it is set to 1, the DAI block is active.

VDAI: Writing a 1 to this bit starts the SSCLK (104 kHz DAI clock) on reception of the first sample. This bit is automatically reset to 0 by SSRST after reception of the last sample.

RESERVD: Reserved bits for testing

DAIMD (0–1): DAI mode selection as defined in Table 4–22.

VCLKMODE: When cleared to 0, this bit allows selection of VCLK in burst mode. When set to 1, this bit allows selection of VCLK in continuous mode.

Table 4–22. DAI Mode Selection

DAIMD1	DAIMD0	DAI MODE
0	0	Normal operation (no tested device using DAI)
0	1	Test of speech decoder / DTX functions (downlink)
1	0	Test of speech encoder / DTX functions (uplink)
1	1	Test of acoustic devices and A/D and D/A (voice path)

4.10.18 Auxiliary Functions Control Register 1

The bit values in the auxiliary functions control register 1 reset the APC generator or the AFC modulator, select the A/D counter input, and select the AFC sampling frequency. This is defined in Table 4–23.

Table 4–23. AUX Functions Control Register 1

UXCTL1: AUXILIARY FUNCTIONS CONTROL REGISTER 1										ADDRESS: 13					R/W
AFCPN	AFCPD	ADC PN	ADC PD	AFCC K1	AFCC K0	ADCC H2	ADCC H1	ADCC H0	ARST	0	1	1	0	1	1/0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	←ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	←VALUE AT RESET					

ARST: This bit resets the digital parts for the auxiliary function (APC generator and AFC modulator). This is not a toggle bit and has to be set to 0 to remove the reset condition.

ADCCH (0–2): This bit selects the input of the ADC (see Table 4–24).

Table 4–24. ADC Selection

ADCCH2	ADCCH1	ADCCH0	A/D CONVERTER INPUT SELECTION
0	0	0	A/D conversion of ADIN1
0	0	1	A/D conversion of ADIN2
0	1	0	A/D conversion of ADIN3
0	1	1	A/D conversion of ADIN4
1	0	0	A/D conversion of ADIN5
1	0	1	A/D conversion of ADIN5
1	1	0	A/D conversion of ADIN5
1	1	1	A/D conversion of ADIN5

AFCCK (0–1): This bit selects the sampling frequency of the AFC (see Table 4–25).

Table 4–25. AFC Selection

AFCCK1	AFCCK0	AFC INTERNAL FREQUENCY
0	0	0.25 MHz
0	1	0.50 MHz
1	0	1 MHz
1	1	2 MHz

AFCPN: If this bit is cleared to 0, the AFC block is powered down under the control of the PWRDN terminal. If this bit is set to 1, the power down is controlled only by bit AFCPD.

AFCPD: This bit is functionally associated with and paired with bit AFCPN. When the AFCPN bit is 1, the AFC block is active. When the AFCPD bit is set to 1, the AFCPD block is in power-down mode.

ADCPN: If this bit is cleared to 0, the auxiliary ADC block is powered down when under the control of PWRDN. If this bit is set to 1, the power down is controlled only by bit ADCPD.

ADCPD: This bit is functionally associated with and paired with bit ADCPN. When the ADCPN bit is set to 1, an auxiliary ADC is active. When the ADCPD bit is set to 1, the auxiliary ADCPD is in power-down mode.

4.10.19 Automatic Frequency Control Registers (1 and 2)

There are two AFC control registers; each is 10 bits wide. AFC control register 1 contains the least significant bit of the AFC D/A converter output. AFC control register 2 contains the most significant bit of the AFC DAC input. See Table 4–26 and Table 4–27. The AFC value is loaded after writing to the AFC MSB register (first) and then the LSB register (second).

Table 4–26. AFC Control Register 1

AUXAFC1: AUTOMATIC FREQUENCY CONTROL REG1										ADDRESS: 14					R/W
BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	0	1	1	1	0	1/0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	←ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	←VALUE AT RESET					

Bits 9–0: LSB input of the 13-bit AFC DAC in 2s complement

Table 4–27. AFC Control Register 2

AUXAFC2: AUTOMATIC FREQUENCY CONTROL REG2										ADDRESS: 15					R/W
RE SRVD	RE SRVD	RE SRVD	RE SRVD	RE SRVD	RE SRVD	RE SRVD	BIT12	BIT11	BIT10	0	1	1	1	1	1/0
R = 0	R = 0	R = 0	R = 0	R = 0	R = 0	R = 0	R/W	R/W	R/W	←ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	←VALUE AT RESET					

Bits 12–10: MSB input of the 13-bit AFC DAC in 2s complement

4.10.20 Automatic Power Control Register

The values in the automatic power control (APC) register set the operating conditions for the APC circuit (see Table 4–28).

Table 4–28. APC Register

AUXAPC: AUTOMATIC POWER CONTROL REGISTER										ADDRESS: 16					R/W
RESERVD	RESERVD	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	1	0	0	0	0	1/0
R = 0	R = 0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	←ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	←VALUE AT RESET					

Bits 7–0: Input of the 8-bit level APC DAC

RESERVD: Reserved bits for testing

4.11 Automatic Frequency Control Registers (1 and 2)

The content of the APC RAM describes the shape of the ramp-up and ramp-down control; as defined in Table 4–29.

Table 4–29. APC Ramp Control

APCRAM: AUTOMATIC POWER CONTROL RAM										ADDRESS: 17 (64 Words)					W
RDWN WORD0 (5 BIT)					RUP WORD0 (5 BIT)					1	0	0	0	1	0
RDWNWORD1 (5 BIT)					RUP WORD1 (5 BIT)					1	0	0	0	1	0
RDWNWORD2 TO 61 (5 BIT)					RUP WORD2 TO 61 (5 BIT)					1	0	0	0	1	0
RDWNWORD62 (5 BIT)					RUP WORD 62 (5 BIT)					1	0	0	0	1	0
RDWNWORD63 (5 BIT)					RUP WORD 63 (5 BIT)					1	0	0	0	1	0
W	W	W	W	W	W	W	W	W	W	←ACCESS TYPE					
X	X	X	X	X	X	X	X	X	X	←VALUE AT RESET					

Actual shape values (five bits long) are contained in the shape DAC input register, as defined in Table 4–30.

Table 4–30. Shape DAC Input Register

APCSHAP: SHAPE DAC INPUT REGISTER										ADDRESS: 18					R/W
RE SRVD	RE SRVD	RE SRVD	RE SRVD	RE SRVD	BIT4	BIT3	BIT2	BIT1	BIT0	1	0	0	1	0	1/0
R = 0	R = 0	R = 0	R = 0	R = 0	R/W	R/W	R/W	R/W	R/W	←ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	←VALUE AT RESET					

Bits 4 – 0: Input of the 5-bit APC DAC

RESERVD: Reserved bits for testing

4.11.1 AGC Control Register

The AGC control register is 10 bits wide and controls operations of the analog AGC circuit, as defined in Table 4–31.

Table 4–31. Analog AGC Gain Control Register

AUXAGC: AUTOMATIC GAIN CONTROL REGISTER										ADDRESS: 19					R/W
BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	1	0	0	1	1	1/0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	←ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	←VALUE AT RESET					

Bits 9 – 0: Input of the 10-bit AAGC DAC

RESERVD: Reserved bits for testing

4.11.2 Auxiliary Functions Control Register 2

The values in the auxiliary function control register 2 set the operation parameters as defined in Table 4–32.

AFCZ: This bit selects the internal resistance of the AFC driver. When AFCZ is 1, the resistance is 50 kΩ. When AFZ is 0, the resistance is 25 kΩ. The largest swing is obtained with 50 kΩ.

APCSPD: When this bit is cleared to 0, the APC clock is at 4 MHz; when set to 1, the APC clock is at 2 MHz.

AGCSWG: This bit selects the swing of the AGC output: 0 corresponds to a 0-V to 2.0-V swing; 1 corresponds to 0-V to 4-V swing.

APCSWG: This bit selects the swing of the APC output: 0 corresponds to a 0-V to 2-V swing; 1 corresponds to 0-V to 4-V swing.

IAPCPTR: Setting this bit to 1 initializes the pointer of the APC RAM to the base address. This is not a toggle bit and has to be set to 0 to set APC RAM operational.

APCMODE: This bit selects the equation used for APC waveform generation.

AGCW: If this bit is cleared to 0, the automatic gain control path is powered down with the control of the GSM receive window (BDLON terminal) and the AGCPD bit. If the AGCPD bit is set to 1, the power down is controlled by the AGCPD bit.

AGCPD: This bit is functionally associated with the AGCW bit. When this bit is set to 1, the automatic gain control path is in power-down mode.

APCW: If this bit is 0, the RF power control path is down powered with the control of the GSM transmit window (BULON) and with the control of the APCPD bit. If the APCPD bit is set to 1, power down is controlled only by the APCPD bit.

APCPD: This bit is functionally associated with the BBULW bit. When this bit is set to 1, the RF power control path is in power-down mode.

Table 4–32. AUX Functions Control Register 2

AUXCTL2: AUXILIARY FUNCTIONS CONTROL REGISTER 2										ADDRESS: 20					R/W
AGCW	AGCPD	APCW	APC PD	IAP CTR	APC MODE	APC SWG	AGC SWG	APC SPD	AFCZ	1	0	1	0	0	1/0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	←ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	←VALUE AT RESET					

4.11.3 Auxiliary A/D Converter Output Register

This register is read-only; however, if there is an attempt to write to it, an A/D conversion operation starts; see Table 4–33. When the A/D conversion is finished, the AUXADC register is loaded and the ADC is automatically powered down. During the conversion process, the ADCEOC bit of the BSTATUS register is set. This bit is reset automatically after AUXADC is loaded.

Table 4–33. AUX A/D Converter Output Register

AUXADC: AUXILIARY A/D CONVERTER OUTPUT REGISTER										ADDRESS: 21					R
BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	1	0	1	0	1	1/0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	←ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	←VALUE AT RESET					

Bits 9 – 0: Output of the 10-bit monitoring ADC

4.11.4 Baseband Status Register

The baseband status register stores the baseband status as defined in Table 4–34.

Table 4–34. Baseband Status Register

BSTATUS: BASEBAND STATUS REGISTER										ADDRESS: 22						R
RESERVD	ADCEOC	RAM PTR	BUF PTR	UL ON	UL CAL	ULX	DL ON	DL CAL	DLR	1	0	1	1	0	1
R = 0	R	R	R	R	R	R	R	R	R	←ACCESS TYPE						
0	0	1	1	0	0	0	0	0	0	←VALUE AT RESET						

DLR: This bit is set to 1 during conversion of a burst in the downlink path.

DLCAL: This bit is set to 1 during offset calibration of the downlink path.

DLON: When set to 1, it indicates that the downlink path is powered on.

ULX: This bit is set to 1 during transmission of the burst in the uplink path.

ULCAL: This bit is set to 1 during offset calibration of the uplink path.

ULON: When set to 1, it indicates that the uplink path is powered on.

BUFPTR: When set to 1, it indicates that the pointer of the burst buffer is at address zero.

RAMPTR: When set to 1, it indicates that the pointer of the APC RAM is at address zero.

ADCEOC: (ADC-end of conversion) When this bit is set to 1, an ADC conversion is in process.

4.11.5 Voice Band Control Register 4 (Address 23)

Voice band control register 4 (VBCTL4) is a read/write register (see Table 4–35) and contains the four programming bits of VDLST, as defined in Table 4–36.

Table 4–35. Voice Band Control Register 4

VBCTL4: VOICE BAND CONTROL REGISTER 4										ADDRESS: 23					R/W
RE SRVD	RE SRVD	RE SRVD	RE SRVD	RE SRVD	RE SRVD	VDLST 3	VDLST 2	VDLST 1	VDLST 0	1	0	1	1	1	1/0
R = 0	R = 0	R = 0	R = 0	R = 0	R = 0	R/W	R/W	R/W	R/W	←ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	←VALUE AT RESET					

Table 4–36. VDLST Status

VDLST3	VDLST2	VDLST1	VDLST0	SIDE TONE GAIN
1	0	0	0	Mute
1	1	0	1	–23 dB
1	1	0	0	–20 dB
0	1	1	0	–17 dB
0	0	1	0	–14 dB
0	1	1	1	–11 dB
0	0	1	1	–8 dB
0	0	0	0	–5 dB (nominal)
0	1	0	0	–2 dB
0	0	0	1	+1 dB
0	1	0	1	+1 dB

4.11.6 Baseband Uplink Register (Address 24)

The baseband uplink register (BULCTL) is a 3-bit register (see Table 4–37) that permits mismatch compensation in the RF transmit mixer. Gain mismatches of 0 dB, –0.25 dB, –0.5 dB, and –0.75 dB are permitted between the I and Q channel, as defined in Table 4–38.

Table 4–37. Uplink Register BULCTL

BULCTL: BASEBAND UPLINK CONTROL REGISTER										ADDRESS: 24					R/W
RE SRVD	RE SRVD	RE SRVD	RE SRVD	RE SRVD	RE SRVD	RE SRVD	IQSEL	G1	G0	1	1	0	0	0	1/0
R = 0	R = 0	R = 0	R = 0	R = 0	R = 0	R = 0	R/W	R/W	R/W	←ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	←VALUE AT RESET					

Table 4–38. BLKCTL Register

BIT2	BIT1	BIT0	GAIN I	GAIN Q
IQSEL	G1	G0		
0	0	0	0 dB	0 dB
0	0	1	–0.25 dB	0 dB
0	1	0	–0.50 dB	0 dB
0	1	1	–0.75 dB	0 dB
1	0	0	0 dB	0 dB
1	0	1	0 dB	–0.25 dB
1	1	0	0 dB	–0.50 dB
1	1	1	0 dB	–0.75 dB

4.11.7 Power-On Status Register (Address 25)

The power-on status register is a 9-bit, read-only register which displays the status power-on/power down of the functions having several power on/off controls as defined in Table 4–39. When the function is in power-on status, the corresponding bit is at 1.

Table 4–39. Power-On Status Register PWONCTL

PWONCTL: POWER-ON STATUS REGISTER										ADDRESS: 25					R/W
RESRVD	BGA P ON	VREF ON	BBIF ON	TIMIF ON	VMID ON	AFC ON	ADC ON	AGC ON	APC ON	1	1	0	0	1	1/0
R = 0	R	R	R	R	R	R	R	R	R	←ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	←VALUE AT RESET (See Note 1)					

NOTE 1: PWONCTL is the power-on status register value at reset when the PWRDN terminal is set high.

4.11.8 Timing and Interface

Accurate timing control of baseband uplink and downlink paths is performed using the timing serial interface. The timing interface is a parallel asynchronous port with four control signals (see Figure 4–12). The BDLON bit controls power on the downlink path of the baseband codec; the BULON bit controls power on the uplink path of the baseband codec; and the BCAL bit controls the calibration of the active parts of the baseband codec selected by BULON or BDLON.

The BENA bit controls the transmission of the reception of burst, depending on which part of the baseband codec is selected by the signals BULON or BDLON. These asynchronous inputs are internally synchronized with the uplink and downlink internal clocks and stored in timing register TR. The timing register, TR, is a 6-bit register containing the bits defined in Table 4–40.

Table 4–40. 6-Bit TR Register

BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ULON	ULCAL	ULSEND	DLON	DLCAL	DLREC

TR Bit Signification

ULON: If set to 1, this bit turns on the uplink path of the baseband codec; if cleared to 0, the uplink path is in power-down mode.

ULCAL: When this bit is set to 1, the uplink offset autocalibration is active.

ULSEND: A transition from 0 to 1 of ULSEND initiates the emission of a burst. The burst information data, burst length, and power level need to be loaded in the corresponding registers using the serial interface.

DLON: If set at 1, this bit turns on the downlink path of the baseband codec; if cleared to 0, the downlink path is in power-down mode.

DLCAL: When this bit is set at 1, the downlink offset autocalibration is active.

DLREC: A transition from 0 to 1 of DLREC initiates the transmission of data from the baseband codec to the DSP using the serial interface.

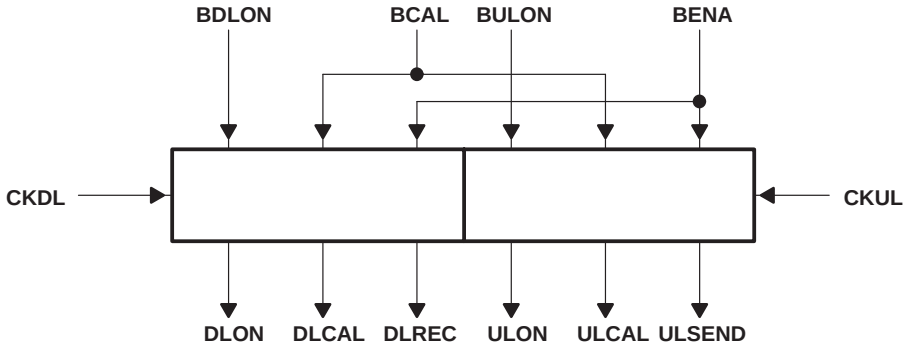
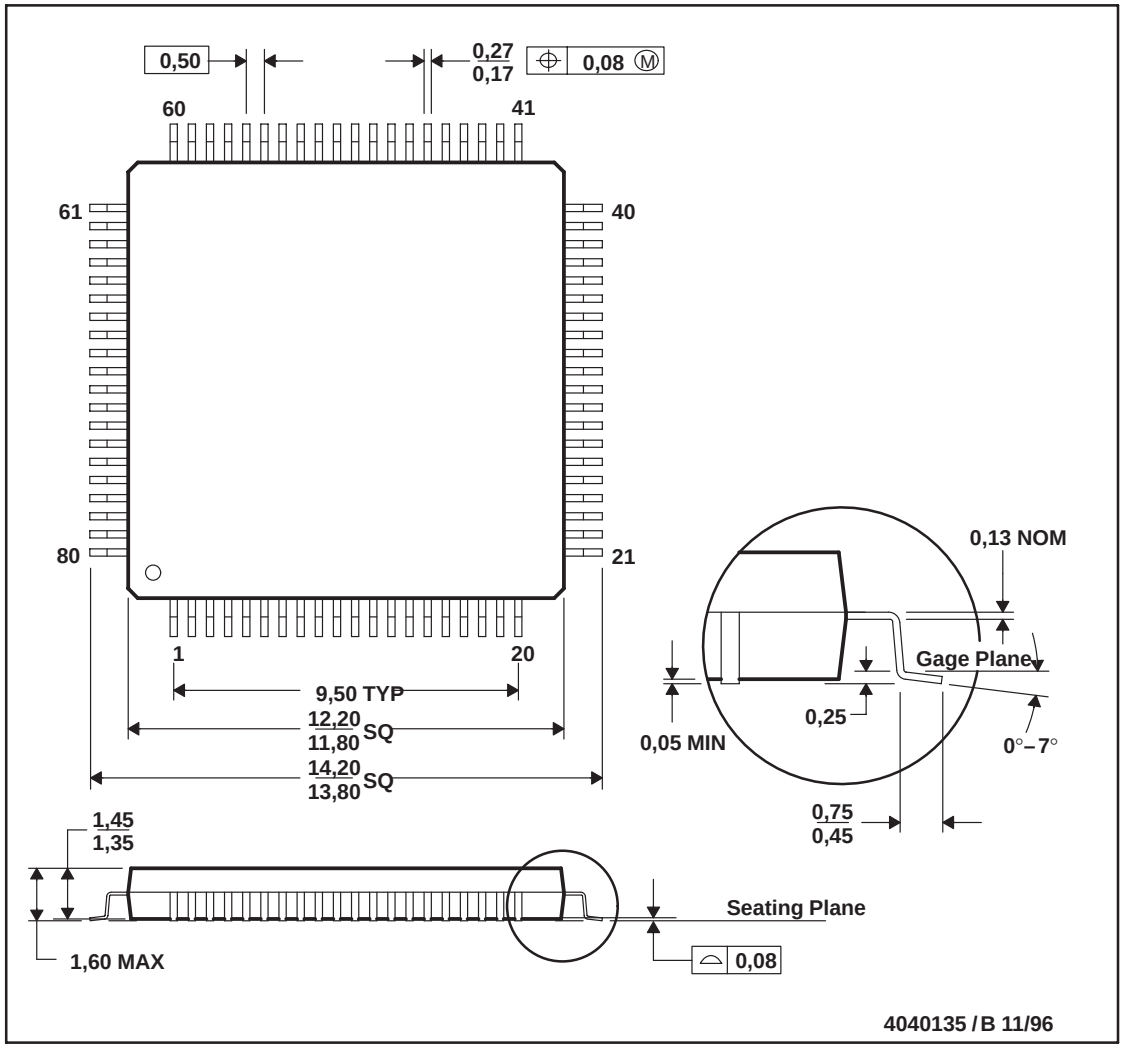


Figure 4–12. Timing Interface

5 MECHANICAL DATA

5.1 PN (S-PQFP-G80) PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026