TCC−103

PTIC Control IC

Introduction

ON Semiconductor's PTIC Controller IC is a three-output high voltage digital to analog control IC specifically designed to control and bias ON Semiconductor's Passive Tunable Integrated Circuits (PTICs).

These tunable capacitive circuits are intended for use in mobile phones and dedicated RF tuning applications. The implementation of ON Semiconductor's tunable circuits in mobile phones enables significant improvement in terms of antenna radiated performance.

The tunable capacitors are controlled through a bias voltage ranging from 2 V to 20 V. The TCC−103 high-voltage PTIC control IC has been specifically designed to cover this need, providing three independent high-voltage outputs that control up to three different tunable PTICs in parallel. The device is fully controlled through a multi-protocol digital interface.

Features

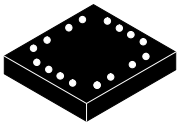
- Controls ON Semiconductor's PTIC Tunable Capacitors and RF Tuners
- Compliant with Timing Needs of Cellular and Other Wireless System Requirements
- Integrated Boost Converter with 3 Programmable Outputs (Up To 24 V)
- Low Power Consumption
- Auto-detection of SPI (30- or 32-bit) or MIPI RFFE Interfaces (1.2 V or 1.8 V)
- Available in WLCSP (Ball and Peripheral Arrays) and for Stand-alone or Module Integration

Typical Applications

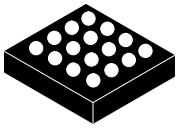
- Multi-band, Multi-standard, Advanced and Simple Mobile Phones
- Tunable Antenna Matching Networks
- Compatible with Closed Loop and Open-loop Antenna Tuner Applications

ON Semiconductor®

http://onsemi.com

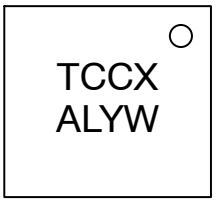


Peripheral Bump
CASE TBD



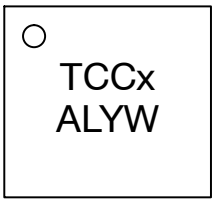
RDL Ball Array
CASE TBD

MARKING DIAGRAMS



Peripheral Bump

TCC = Product Code
X = MIPI ID
A = Assembly Location
L = Wafer Lot Code
Y = Year Code
W = Week Code
O = Pin 1 Marker



RDL

TCC = Product Code
x = MIPI ID
A = Assembly Location
L = Wafer Lot Code
Y = Year Code
W = Week Code
O = Pin 1 Marker

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 29 of this data sheet.

© Semiconductor Components Industries, LLC, 2013

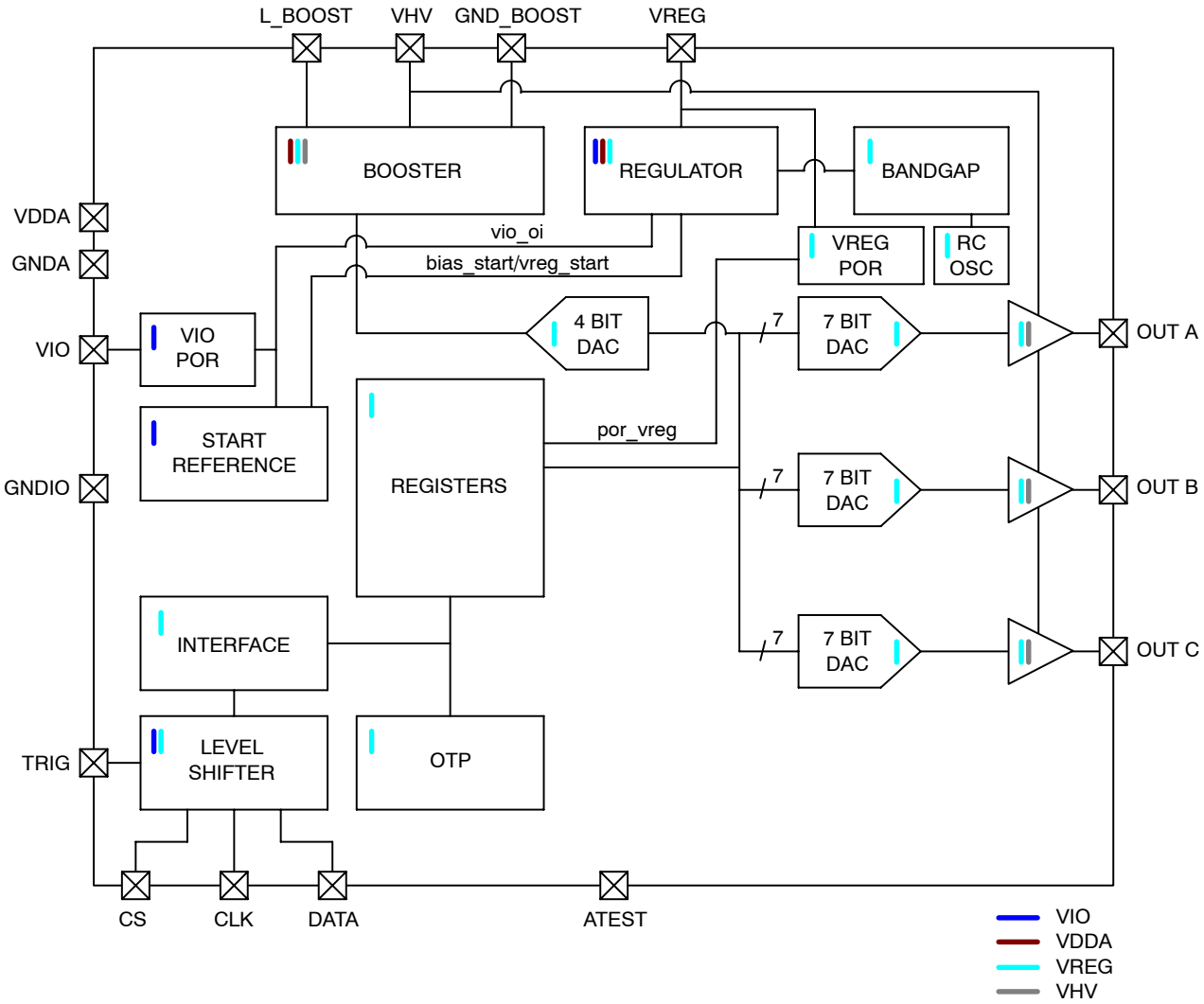


Figure 1. HVDAC Functional Block Diagram

Peripheral Bump Pin Out

Table 1. PIN FUNCTION DESCRIPTIONS

Bump	Name	Type	Description
1	L_BOOST	Analog HV Output	Boost Inductor
2	AVDD	Power	Analog Supply
3	GND_REF	Power	Analog Ground
4	TRIG	Digital I/O	Trigger Signal Input
5	CS	Digital Input	SPI_CS (Ground for MIPI RFFE)
6	CLK	Digital Input	RFFE SCLK/SPI CLK
7	DATA	Digital I/O	RFFE SDATA/SPI_DATA
8	VIO	Power	IO Reference Supply
9	GND_DIG	Power	Digital Ground
10	OUTA	Analog HV Output	High Voltage Output A
11	OUTB	Analog HV Output	High Voltage Output B
12	OUTC	Analog HV Output	High Voltage Output C
13	VREG	Analog Output	VREG Capacitor
14	ATEST	Analog Output	Test Pin (Ground in Application)
15	GND_BOOST	Power	Boost Ground
16	VHV	Analog HV I/O	Boost High Voltage Output

Peripheral Bump Package Footprint

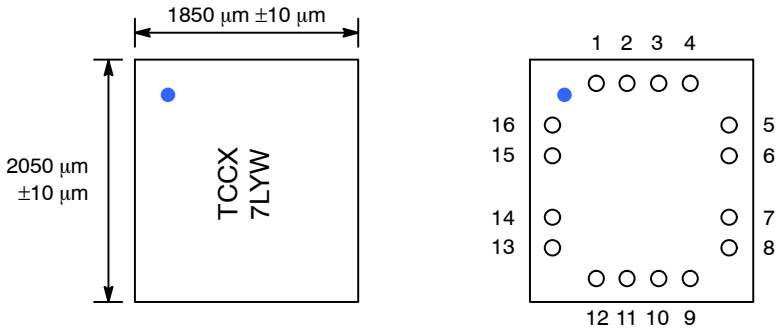


Figure 2. Peripheral Row Footprint − Top View

RDL Pin Out

Table 2. PIN FUNCTION DESCRIPTIONS

Bump	Name	Type	Description
A1	VREG	Analog Output	VREG Capacitor
A2	ATEST	Analog Output	Test Pin (Ground in Application)
A3	GND_BOOST	Power	Boost Ground
A4	VHV	Analog HV I/O	Boost High Voltage Output
B1	OUTB	Analog HV Output	High Voltage Output B
B2	OUTC	Analog HV Output	High Voltage Output C
B3	AVDD	Power	Analog Supply
B4	L_BOOST	Analog HV Output	Boost Inductor
C1	OUTA	Analog HV Output	High Voltage Output A
C2	GND_DIG	Power	Digital Ground
C3	TRIG	Digital I/O	Trigger Signal Input
C4	GND_REF	Power	Analog Ground
D1	VIO	Power	IO Reference Supply
D2	DATA	Digital I/O	RFFE SDATA/SPI_DATA
D3	CLK	Digital Input	RFFE SCLK/SPI CLK
D4	CS	Digital Input	SPI_CS (Ground for MIPI RFFE)

RDL Ball Array Package Footprint

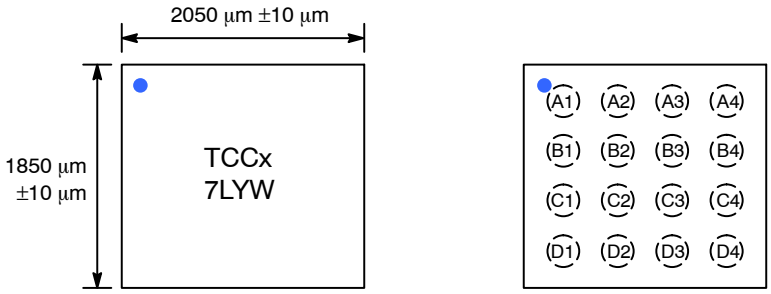


Figure 3. Ball Array Footprint − Top View

Electrical Performance Specifications

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
AVDD	Analog Supply Voltage	−0.3 to +6.0	V
VIO	IO Reference Supply Voltage	−0.3 to +3.6	V
$V_{I/O}$	Input Voltage Logic Lines (DATA, CLK, CS)	−0.3 to VIO	V
VHV	VHV Maximum Voltage	−0.3 to 30	V
$V_{ESD\ (HBM)}$	Human Body Model, JESD22-A114, All I/O	2,000	V
$V_{ESD\ (MM)}$	Machine Model, JESD22-A115	200	V
T_{STG}	Storage Temperature	−55 to +150	°C
$T_{AMB_OP_MAX}$	Max Operating Ambient Temperature without Damage	+110	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Rating			Unit
		Min	Typ	Max	
T_{AMB_OP}	Operating Ambient Temperature	−30	–	+85	°C
T_{J_OP}	Operating Junction Temperature	−30	–	+125	°C
AVDD	Analog Supply Voltage	2.3	–	5.5	V
VIO	IO Reference Supply Voltage	1.1	–	3.0	V

Table 5. DC CHARACTERISTICS

(T_A = −30 to +85°C; V_{OUTX} = 15 V for each output; 2.3 V < AVDD < 5.5 V; 1.1 V < VIO < 3.0 V; R_{LOAD} = equivalent series load of 5.6 kΩ and 2.7 nF; C_{HV} = 22 nF; L_{BOOST} = 15 μH; TRIG pin grounded; unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Comment
Shutdown Mode						
I_{AVDD}	AVDD Supply Current	–	–	0.8	μA	VIO Supply is Low
I_{L_BOOST}	L_BOOST Leakage	–	–	1	μA	VIO Supply is Low
I_{BATT}	Battery Current	–	–	1	μA	VIO Supply is Low
I_{VIO}	VIO Supply Current	−1	–	1	μA	VIO Supply is Low
I_{CLK}	CLK Leakage	−1	–	1	μA	VIO Supply is Low
I_{DATA}	DATA Leakage	−1	–	1	μA	VIO Supply is Low
Active Mode						
I_{BATT}	Average Battery Current, 3 Outputs Actively Switching 16 V for 1205 μs to 2 V for 1705 μs to 8V for 1705 μs	–	980	1,290	μA	At VHV = 20 V AVDD = 3.3 V
I_{BATT_SS0}	Average Battery Current, 3 Outputs @ 0 V Steady State	–	590	830	μA	At VHV = 20 V AVDD = 3.3 V
I_{BATT_SS2}	Average Battery Surrent, 3 Outputs @ 2 V Steady State	–	610	860	μA	At VHV = 20 V AVDD = 3.3 V
I_{BATT_SS16}	Average Battery Current, 3 Outputs @ 20 V Steady State	–	780	1,020	μA	At VHV = 20 V AVDD = 3.3 V
I_{L_BOOST}	Average Inductor Current, 3 Outputs Actively Switching 20 V for 1205 μs to 2 V for 1705 μs to 8 V for 1705 μs	–	730	1,000	μA	At VHV = 20 V AVDD = 3.3 V
$I_{L_BOOST_SS0}$	Average Inductor Current, 3 Outputs @ 0 V Steady State	–	350	550	μA	At VHV = 20 V AVDD = 3.3 V
$I_{L_BOOST_SS2}$	Average Inductor Current, 3 Outputs @ 2 V Steady State	–	380	570	μA	At VHV = 20 V AVDD = 3.3 V

Table 5. DC CHARACTERISTICS (continued)
(T_A = −30 to +85°C; V_{OUTX} = 15 V for each output; 2.3 V < AVDD < 5.5 V; 1.1 V < VIO < 3.0 V; R_{LOAD} = equivalent series load of 5.6 kΩ and 2.7 nF; C_{HV} = 22 nF; L_{BOOST} = 15 μH; TRIG pin grounded; unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Comment
Active Mode (continued)						
$I_{L_BOOST_SS16}$	Average Inductor Current, 3 Outputs @ 20 V Steady State	–	550	750	μA	At VHV = 20 V AVDD = 3.3 V
I_{VIO_INACT}	VIO Average Inactive Current	–	–	3	μA	VIO is High, No Bus Activity
I_{VIO_ACTIVE}	VIO Average Active Current	–	–	250	μA	VIO = 1.8 V, Master Sending Data at 26 MHz
V_{VREG}		2.05	–	2.3	V	No External Load Allowed
Low Power Mode						
I_{AVDD}	AVDD Supply Current	–	–	7	μA	
I_{L_BOOST}	L_BOOST Leakage	–	–	3	μA	
I_{BATT}	Battery Current	–	–	10	μA	I_{AVDD} + I_{L_BOOST}
I_{VIO}	VIO Supply Current	–	–	3	μA	No Bus Activity
V_{VREG}		2.0	–	3.3	V	No External Load Allowed

Table 6. BOOST CONVERTER CHARACTERISTICS
(AVDD from 2.3 V to 5.5 V; VIO from 1.1 V to 3.0 V; T_A = −30 to +85°C; C_{HV} = 22 nF; L_{BOOST} = 15 μH; unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VHV_min	Minimum Programmable Output Voltage (Average), DAC Boost = 0h	Active Mode	8.5	9	9.5	V
VHV_max	Maximum Programmable Output Voltage (Average), DAC Boost = Fh	Active Mode	22.8	24	25.2	V
Resolution	Boost Voltage Resolution	4 Bit DAC	–	1	–	V
$R_{DS(ON)}$	n-Channel MOSFET On-Resistance	I_{L_BOOST} = 10 mA	–	1.3	–	Ω
$I_{L_BOOST_LIMIT}$	Inductor Current Limit		–	100	–	mA

Table 7. ANALOG OUTPUTS (OUT A, OUT B, OUT C)
(AVDD from 2.3 V to 5.5 V; VIO from 1.1 V to 3.0 V; VHV = 24 V; T_A = −30 to +85°C; R_{LOAD} = ∞ unless otherwise specified)

Parameter	Description	Min	Typ	Max	Unit	Comment
Shutdown Mode						
Z_{OUT}	OUT A, OUT B, OUT C Output Impedance	7	–	–	MΩ	DAC Disabled
Active Mode						
V_{OH}	Maximum Output Voltage	22.0	–	–	V	DAC A, B or C = FFh, DAC Boost = Fh, I_{OH} < 10 μA
V_{OL}	Minimum Output Voltage	–	–	1	V	DAC A, B or C = 01h, DAC Boost = 0h to Fh, I_{OH} < 10 μA
Slew Rate		–	6.5	10	μs	2 V to 20 V Step, Measured at V_{OUT} = 15.2 V, R_{LOAD} = Equivalent Series Load of 5.6 kΩ and 2.7 nF, Turbo Enabled
R_{PD}	OUT A, OUT B, OUT C Set In Pull Down Mode	–	–	800	Ω	DAC A, B or C = 00h, DAC Boost = 0h to Fh, Selected Output(s) is Disabled
Resolution	Voltage Resolution (1 Bit)	–	188	–	mV	(1 LSB = 1 Bit)
V_{OFFSET}	Zero Scale, Least Squared Best Fit	-1	–	+1	LSB	
Error		-3.0	–	+3.0	$\%V_{OUT}$	Over 2 V – 18 V V_O Range
DNL	Differential Non-linearity Least Squared Best Fit	-0.9	–	+0.9	LSB	Over 2 V – 18 V V_O Range
INL	Integral Non-linearity Least Squared Best Fit	-1	–	+1	LSB	Over 2 V – 18 V V_O Range
I_{SC}	Over Current Protection	–	35	65	mA	Any DAC Output to Ground
V_{RIPPLE}	Output Ripple with All Outputs at Steady State	–	–	10	mV RMS	Over 2 V – 18 V V_O Range, VHV = 20 V

Theory of Operation

Overview

The control IC outputs are directly controlled by programming the three DACs (DAC A, DAC B, and DAC C) through the digital interface. The DACs are 8-bit DACs used in a 7-bit format.

The DAC stages are driven from a reference voltage, generating an analog output voltage driving a high-voltage amplifier supplied from the boost converter (see Control IC block diagram − Figure 1).

The control IC output voltages are scaled from 0 to 24 V, with 128 steps of 188 mV (2×24 V/255 = 0.188235 V). The nominal control IC output can be approximated to 188 mV × (DAC value).

For performance optimization the boost output voltage (VHV) can be programmed to levels between 9 V and 24 V via the DAC_boost register (4 bits with 1 V steps). The startup default level for the boosted voltage is VHV = 20 V.

For proper operation and to avoid saturation of the output devices and noise issues it is recommended to operate the boosted VHV voltage at least 2 V above the highest programmed V_{OUT} voltage of any of the three outputs.

When the DAC output value is set to 00h the corresponding output is disabled and the output is pulled to GND through an effective impedance of less than 800 Ω.

Operating Modes

The following operating modes are available:

1. **Shutdown Mode:** All circuit blocks are off, the DAC outputs are disabled and placed in high Z state and current consumption is limited to minimal leakage current. The shutdown mode is entered upon initial application of AVDD or upon VIO being placed in the low state. The contents of the registers are not maintained in shutdown mode.
2. **Startup Mode:** Startup is only a transitory mode. Startup mode is entered upon a VIO high state. In startup mode all registers are reset to their default states, the digital interface is functional, the boost converter is activated, outputs OUT A, OUT B, and OUT C are disabled and the DAC outputs are placed in a high Z state. Control software can request a full hardware and register reset of the TCC−103 by sending an appropriate PWR_MODE command to direct the chip from either the active mode or the low power mode to the startup mode. From the startup mode the device automatically proceeds to the Active mode.
3. **Active Mode:** All blocks of the TCC−103 are activated and the DAC outputs are fully controlled through the digital interface. The DAC settings can be dynamically modified and the HV outputs will be adjusted according to the specified timing diagrams. Each DAC can be individually controlled and/or switched off according to application requirements. Active mode is automatically entered from the startup mode. Active mode can also be entered from the low power mode under control software command.
4. **Low Power Mode**: In low power mode the serial interface is enabled, the DAC outputs are disabled and are placed in a high Z state and the boost voltage circuit is disabled. Control software can request to enter the low power mode from the active mode by sending an appropriate PWR_MODE command. The contents of all registers are maintained in the low power mode.

AVDD Power-On Reset

Upon application of AVDD the TCC−103 will be in shutdown mode. All circuit blocks are off and the chip draws only minimal leakage current.

VIO Power-On Reset and Startup Conditions

A high level on VIO places the chip in startup mode which provides a power on reset (POR) to the TCC−103. POR resets all registers to their default settings as described in Table 8. VIO POR also resets the serial interface circuitry. POR is **not** a brown-out detector and VIO needs to be brought back to a low level to enable the POR to trigger again.

Table 8. VIO POWER-ON RESET AND STARTUP

Register	Default State for VIO POR	Comment
DAC Boost	[1011]	VHV = 20 V
Power Mode	[01] > [00]	Transitions from SHUTDOWN to STARTUP and then Automatically to ACTIVE Mode
DAC Enable	[000]	V_{OUT} A, B and C Disabled
DAC A		Output in High-Z Mode
DAC B		Output in High-Z Mode
DAC C		Output in High-Z Mode

VIO Shutdown

A low level at any time on VIO places the chip in shutdown mode in which all circuit blocks are off. The contents of the registers are not maintained in shutdown mode.

Table 9. VIO THRESHOLDS
(AVDD from 2.3 V to 5.5 V; T_A = −30 to +85°C unless otherwise specified)

Parameter	Description	Min	Typ	Max	Unit	Comment
VIORST	VIO Low Threshold	−	−	0.2	V	When VIO is lowered below this threshold level the chip is reset and placed into the Shutdown state.

Power Supply Sequencing

The AVDD input is typically directly supplied from the battery and thus is the first on. After AVDD is applied and before VIO is applied to the chip all circuits are in the shutdown state and draw minimum leakage currents. Upon application of VIO the chip automatically starts up using default settings and is placed in the active state waiting for a command via the serial interface.

Table 10. TIMING
(AVDD from 2.3 V to 5.5 V; VIO from 1.1 V to 3.0 V; T_A = −30 to +85°C; OUT A, OUT B & OUT C; CHV = 22 nF; L_{BOOST} = 15 μH; VHV = 20 V; Turbo-Charge mode Off unless otherwise specified)

Parameter	Description	Min	Typ	Max	Unit	Comment
T_{POR_VREG}	Internal Bias settling time from Shutdown to Active mode	−	50	120	μs	For Info Only
T_{BOOST_START}	Time to charge CHV @ 95% of set VHV	−	130	−	μs	For Info Only
$T_{SD_TO_ACT}$	Startup time from Shutdown to Active mode	−	180	250	μs	
T_{SET+}	Output A, B, C Positive settling time to within 5% of the delta voltage, equivalent series load of 5.6 kΩ and 2.7 nF, V_{OUT} from 2 V to 20 V; 0Bh (11d) to 55h (85d)	−	50	60	μs	Voltage Settling Time Connected on V_{OUT} A, B, C
T_{SET-}	Output A, B, C Negative settling time to within 5% of the delta voltage, equivalent series load of 5.6 kΩ and 2.7 nF, V_{OUT} from 20 V to 2 V; 55h (85d) to 0Bh (11d)	−	50	60	μs	Voltage Cettling Time Connected on V_{OUT} A, B, C

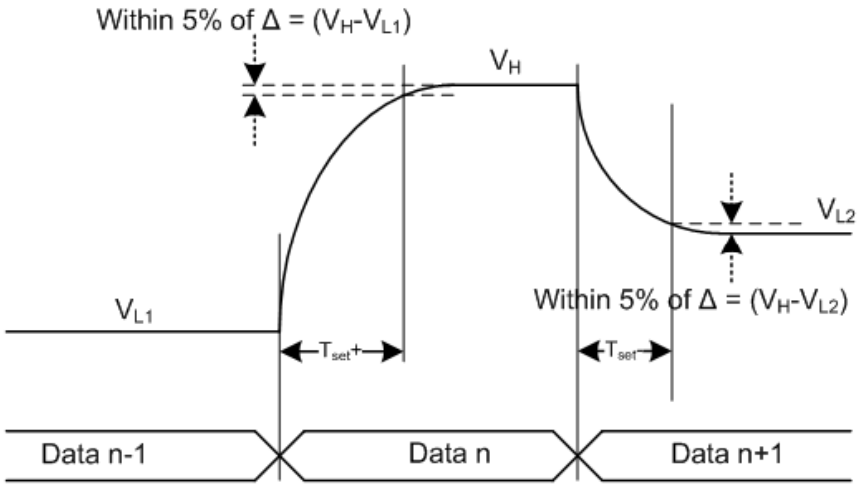


Figure 4. Output Setting Diagram

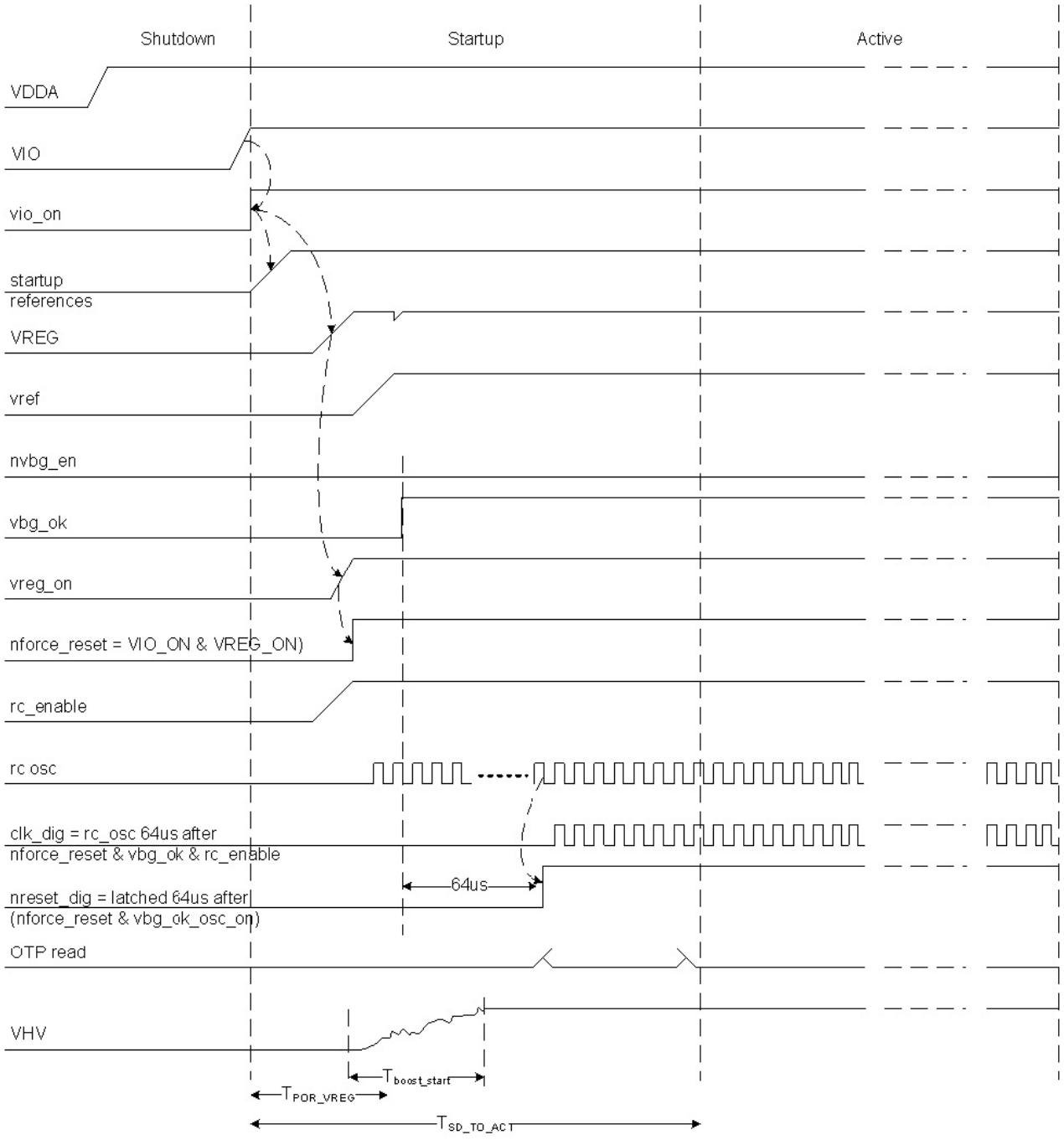


Figure 5. Startup Timing Diagram

Boost Control

The TCC−103 integrates an asynchronous current control boost converter. It operates in a discontinuous mode and features spread-spectrum circuitry for Electro-Magnetic Interference (EMI) reduction. The average boost clock is 2 MHz and the clock is spread between 0.8 MHz and 3.2 MHz.

Boost Output Voltage (VHV) Control Principle

The asynchronous control starts the boost converter as soon as the VHV voltage drops below the reference set by the 4-bit DAC and stops the boost converter when the VHV voltage rises above the reference again.

Due to the slow response time of the control loop, the VHV voltage may drop below the set voltage before the control loop compensates for it. In the same manner, VHV can rise higher than the set value. This effect may reduce the maximum output voltage available. Please refer to Figure 6 below.

The asynchronous control reduces switching losses and improves the output (VHV) regulation of the DC/DC converter under light load, particularly in the situation where the TCC−103 only maintains the output voltages to fixed values.

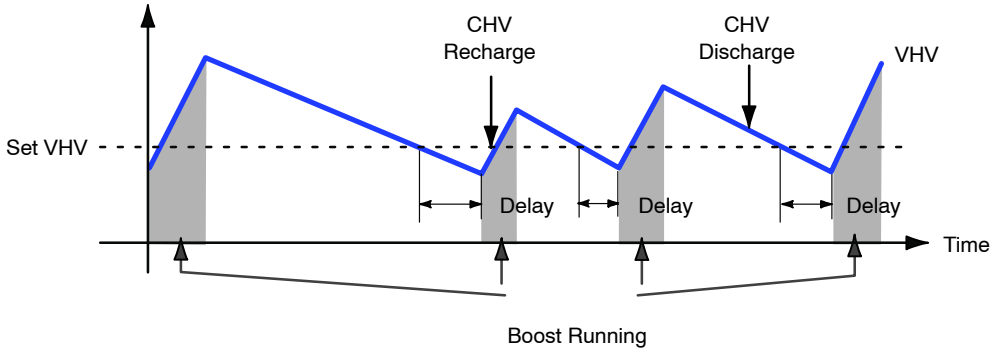


Figure 6. VHV Voltage Waveform

High Impedance (High Z) Feature

In Shutdown mode the OUT pins are set to a high impedance mode (high Z).

Following is the principle of operation for the control IC:

1. The output voltage V_{OUT} is defined by:

$$V_{OUT} = \frac{\text{DAC code}}{255} \times 24\ V \times 2 \qquad \text{(eq. 1)}$$

2. The voltage VHV defines the maximum supply voltage of the output regulator and is set by the 4 bit DAC.
3. The maximum DC output voltage V_{OUT} is limited to (VHV − 2 V).
4. The minimum output voltage V_{OUT} is 1.0 V MAX.

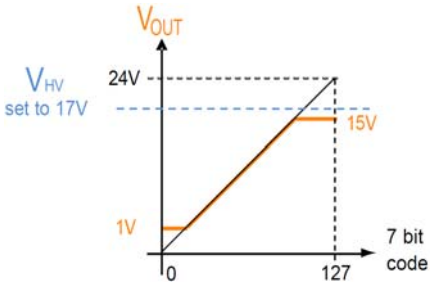


Figure 7. DAC Output Range Example A

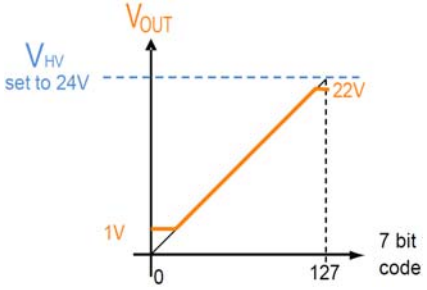


Figure 8. DAC Output Range Example B

Digital Interface

The control IC is fully controlled through a digital interface (DATA, CLK, CS). The digital interface automatically detects and responds to MIPI RFFE interface commands, 3-wire 30-bit Serial Interface commands or 3-wire 32-bit Serial Interface commands. Auto-detection is accomplished on a frame by frame basis. The digital interface is further described in the next sections of this document.

3-wire Serial Interface

The 3-wire serial interface operates in a synchronous write-only 3-wire slave mode. 30-bit or 32-bit message length is automatically detected for each frame. If CS changes state before all bits are received then all data bits are ignored. Data is transmitted most significant bit first and DATA is latched on the rising edge of CLK. Commands are latched on the falling edge of CS.

Table 11. 3-WIRE SERIAL INTERFACE SPECIFICATION

(T_A = −30 to +85°C; 2.3 V < AVDD < 5.5 V; 1.1 V < VIO < 3.0 V; unless otherwise specified)

Parameter	Description	Min	Typ	Max	Unit	Comment
F_{CLK}	Clock Frequency	–	–	26	MHz	
T_{CLK}	Clock Period	38.4	–	–	ns	
N_{BIT}	Bits Number	–	30/32	–	bits	Auto-detection 30-bit or 32-bit
T_{HIGH}	Clock High Time	13	–	–	ns	
T_{LOW}	Clock Low Time	13	–	–	ns	
TCS_{SETUP}	CS Set-up Time	5	–	–	ns	70% Rising Edge of CS to 30% Rising Edge of First Clock Cycle
TCS_{HOLD}	CS Hold Time	5	–	–	ns	30% Falling Edge of Last Clock Cycle to 70% Falling Edge of CS
TD_{SETUP}	Data Set-up Time	4	–	–	ns	Relative to 30% of CLK Rising Edge
TD_{HOLD}	Data Hold Time	4	–	–	ns	Relative to 70% of CLK Rising Edge
T_{SUCC}	CS Low Time between Successive Writes	38.4	–	–	ns	70% Falling Edge of CS to 70% Rising Edge of CS
T_{SUCC}	CS Low Time between Successive DAC Update Writes	1,500	–	–	ns	Time between Groups of DAC Update Reg [00000] & [00001] Writes
C_{CLK}	Input Capacitance	–	–	5	pF	CLK Pin
C_{DATA}	Input Capacitance	–	–	8.3	pF	DATA Pin
C_{CS}	Input Capacitance	–	–	5	pF	CS Pin
C_{TRIG}	Input Capacitance	–	–	10	pF	TRIG Pin
V_{IH}	Input Logic Level High	0.7 × VIO	–	VIO + 0.3	V	DATA, CLK, CS
V_{IL}	Input Logic Level Low	−0.3	–	0.3 × VIO	V	DATA, CLK, CS
I_{IH_DATA}	Input Current High	−2	–	10	μA	DATA
I_{IL_DATA}	Input Current Low	−2	–	1	μA	DATA
$I_{IH_CLK,CS}$	Input Current High	−1	–	10	μA	CLK, CS
$I_{IL_CLK,CS}$	Input Current Low	−1	–	1	μA	CLK, CS
V_{TP_TRIG}	Positive Going Threshold Voltage	0.4 × VIO	–	0.7 × VIO	V	TRIG
V_{TN_TRIG}	Negative Going Threshold Voltage	0.3 × VIO	–	0.6 × VIO	V	TRIG
V_{H_TRIG}	Hysteresis Voltage ($V_{TP} - V_{TN}$)	0.1 × VIO	–	0.4 × VIO	V	TRIG
I_{IH_TRIG}	TRIG Input Current High	−2	–	10	μA	TRIG = 0.8 × VIO
I_{IL_TRIG}	TRIG Input Current Low	−2	–	1	μA	TRIG = 0.2 × VIO

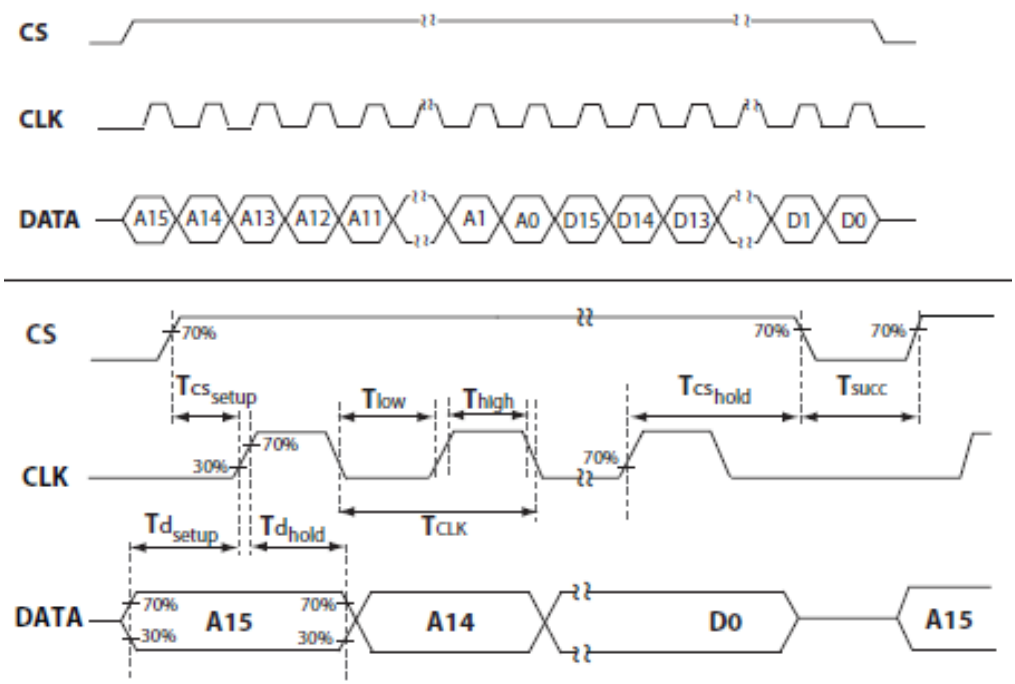


Figure 9. 3-wire Serial Interface Signal Timing

SPI Frame Length Decoding

30-bit or 32-bit frame length is automatically detected. The length of the frame is defined by the number of Clock rising edges while CS is kept high. The TCC−103 will not respond to a SPI command if the length of the frame is not exactly 30 bits or 32 bits. SPI registers are write only.

SPI Frame Structure

Table 12. 32 BITS FRAME: ADDRESS DECODING (1 OR 2 OR 3 OUTPUTS)

H0	H1	R/W	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	1	0	1	0	1	0	0	1	0	0	X	X	X	X	X
ON Semiconductor Header		R/W	Device ID			Specific Device ID					Register Address for Operation				

Table 13. 30 BITS FRAME: ADDRESS DECODING (1 OR 2 OR 3 OUTPUTS)

R/W	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	1	0	0	X	X	X	X	X
R/W	Device ID			Specific Device ID					Register Address for Operation				

Table 14. 3-WIRE SERIAL INTERFACE ADDRESS MAP

A4	A3	A2	A1	A0	Data [15:8]	Data [7:0]
0	0	0	0	0	Turbo Charge Settings for DAC A, B, C	DAC C
0	0	0	0	1	DAC B	DAC A
0	0	1	0	0	Turbo-Charge Delay Parameters for DAC A, B, C	Turbo Threshold Delay Settings for A, B, C
1	0	0	0	0	Mode Select + Control IC Setup	
1	0	0	1	0	Reserved	Reserved
To						
1	1	1	1	1		

Turbo-Charge Mode

The TCC−103A control IC has a Turbo-Charge mode that significantly shortens the system settling time when changing programming voltages. In Turbo-Charge mode the DAC output target voltage is temporarily set to either a delta voltage above or a delta voltage below the actual desired target for the TCDLY time. It is recommended that VHV be set to 24 V when using Turbo-Charge mode.

Table 15. DATA DECODING FOR DATA REGISTER [00000]

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TC_INDX[7:0]								TC_INDX[10]	DAC C						

Table 16. DATA DECODING FOR DATA REGISTER [00001]

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TC_INDX[9]	DAC B							TC_INDX[8]	DAC A						

Table 17. FIRST AND LAST 26 VALUES OF TURBO TIME ENCODED TABLE INTO TC_INDX [10:0] REGISTER

DAC A State	DAC B State	DAC C State	Encoded Value	
Dec	Dec	Dec	Dec	Hex
0	0	0	0	0
0	0	1	1	1
0	0	2	2	2
0	0	3	3	3
0	0	4	4	4
0	0	5	5	5
0	0	6	6	6
0	0	7	7	7
0	0	8	8	8
0	0	9	9	9
0	0	10	10	A
0	0	11	11	B
0	1	0	12	C
0	1	1	13	D
0	1	2	14	E
0	1	3	15	F
0	1	4	16	10
0	1	5	17	11
0	1	6	18	12
0	1	7	19	13
0	1	8	20	14
0	1	9	21	15
0	1	10	22	16
0	1	11	23	17
0	2	0	24	18
0	2	1	25	19
Last 25 Values				
11	9	11	1703	6A7
11	10	0	1704	6A8
11	10	1	1705	6A9
11	10	2	1706	6AA

Table 17. FIRST AND LAST 26 VALUES OF TURBO TIME ENCODED TABLE INTO TC_INDX [10:0] REGISTER (continued)

DAC A State	DAC B State	DAC C State	Encoded Value	
Dec	Dec	Dec	Dec	Hex
11	10	3	1707	6AB
11	10	4	1708	6AC
11	10	5	1709	6AD
11	10	6	1710	6AE
11	10	7	1711	6AF
11	10	8	1712	6B0
11	10	9	1713	6B1
11	10	10	1714	6B2
11	10	11	1715	6B3
11	11	0	1716	6B4
11	11	1	1717	6B5
11	11	2	1718	6B6
11	11	3	1719	6B7
11	11	4	1720	6B8
11	11	5	1721	6B9
11	11	6	1722	6BA
11	11	7	1723	6BB
11	11	8	1724	6BC
11	11	9	1725	6BD
11	11	10	1726	6BE
11	11	11	1727	6BF

The Turbo time is encoded into TC_INDX register, using the formula:

$$Index = State_A \times 144 + State_B \times 12 + State_C \quad \text{(eq. 2)}$$

TC_INDX [10:0] register mapping:

TC_INDX [7:0] = SPI_REG_0x00, bit [15:8]

TC_INDX [8] = SPI_REG_0x01, bit 7

TC_INDX [9] = SPI_REG_0x01, bit 15

TC_INDX [10] = SPI_REG_0x00, bit 7

Hardware extracts the state of each DAC from the encoded Turbo time table (Table 17), and applies the corresponding delay from Table 18.

Table 18. TUNING TCDLY STEPS [μS]

TURBO Steps [μS] {from Table 21}	DAC State											
	0	1	2	3	4	5	6	7	8	9	10	11
5	Turbo OFF	5	10	15	20	25	30	35	40	45	50	55
4	Turbo OFF	4	8	12	16	20	24	28	32	36	40	44
3	Turbo OFF	3	6	9	12	15	18	21	24	27	30	33
2	Turbo OFF	2	4	6	8	10	12	14	16	18	20	22

The value of Turbo time is deducted based on the hardware comparison of new DAC value in respect to old DAC value, as follows:

If DAC new > DAC old, then $\mathbf{T_{UP}}$ = TCDLY

If DAC new < DAC old, and DAC new > 21, then $\mathbf{T_{DOWN}}$ = TCDLY

If DAC new < DAC old, and DAC new = 21, then $\mathbf{T_{DOWN}}$ = TCDLY

If DAC new < DAC old, and DAC new < 21, then $\mathbf{T_{DOWN}}$ = TCDLY + TCM × (21 – DAC new)

Table 19. TURBO-CHARGE DELAY PARAMETERS REGISTER FOR A, B & C [00100]

D15	D14	D13	D12	D11	D10	D9	D8
Reserved		TCM_C_1	TCM_C_0	TCM_B_1	TCM_B_0	TCM_A_1	TCM_A_0

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		TCSTP_DAC _C_1	TCSTP_DAC _C_0	TCSTP_DAC _B_1	TCSTP_DAC _B_0	TCSTP_DAC _A_1	TCSTP_DAC _A_0

Table 20. TURBO-CHARGE MULTIPLICATION SETTINGS (TCM)

TCM_X_1	TCM_X_0	Multiplication Factor
0	0	4 (Default)
0	1	3
1	0	2
1	1	1

Table 21. TURBO-CHARGE DELAY STEP SETTINGS (TCSTP_DAC)

TCSTP_DAC_X_1	TCSTP_DAC_X_0	TURBO Steps [μS]
0	0	2
0	1	3
1	0	4
1	1	5 (Default)

The process of decoding TC_INDX is based on comparing the corresponding MSB or LSB bits, because the index is incremental. After the DAC states are extracted, the delay values are applied from Table 18, as start value for a count-down timer. Optional fine tuning of the Turbo time, is available through register shown in Table 21.

Configuration Message

(DAC Configuration - Enable Mask, HVDAC Boost and Trigger Pin Settings)

Table 22. DATA DECODING FOR DATA REGISTER [10000]

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SSE	TP	TE	1	DAC Boost				Power Mode		0	0	DAC A	DAC B	DAC C	X

SSE – Spread Spectrum Enable bit

TP – External Trigger Signal Polarity bit

TE – External Trigger Enable bit. When TE is enabled sending messages to data registers 0x00000 and 0x00001 (with SPI messages: 0xd4, 0x80,<TC_INDX>, <DAC C value> and 0xd4, 0x81, <DAC B value>, <DAC A value>) will load the registers but only after active edge on external TRIG pin will these settings be applied. When TE is disabled the DAC outputs change immediately when messages are sent to data registers 0x00000 and 0x00001.

Bits D5, D4 & D0 – Reserved

Table 23. DATA DECODING FOR DATA REGISTER [10000] FOR TRIGGER SETTINGS

D15	D14	D13	Description
0	–	–	Spread Spectrum Disabled
1	–	–	Spread Spectrum Enabled (Default)
–	0	–	External TRIG Polarity Active Low
–	1	–	External TRIG Polarity Active High (Default)
–	–	0	External TRIG Disabled (Default)
–	–	1	External TRIG Enabled

Table 24. BOOST DAC MODE SETUP

D11	D10	D9	D8	VHV (V)
0	0	0	0	9
0	0	0	1	10
0	0	1	0	11
0	0	1	1	12
0	1	0	0	13
0	1	0	1	14
0	1	1	0	15
0	1	1	1	16
1	0	0	0	17
1	0	0	1	18
1	0	1	0	19
1	0	1	1	20 (Default)
1	1	0	0	21
1	1	0	1	22
1	1	1	0	23
1	1	1	1	24

Table 25. POWER MODE SETUP

D7	D6	State	Description
0	0	ACTIVE	Boost Control active, VHV set by Digital Interface V_{OUT} A, B, C enabled and controlled by Digital Interface (default)
0	1	STARTUP	Boost Control active, VHV set by Digital Interface V_{OUT} A, B, C disabled
1	0	LOW POWER	Digital interface is active and all other circuits are in low power mode
1	1	Reserved	State of hardware does not change

Trig Pin Operation with SPI

The TRIG input pin can be used as an external synchronization signal to ensure that new DAC settings are applied to the outputs at appropriate times in an overall transceiver system.

The TRIG trigger function is enabled or disabled by Register [10000], bit D13 (TE, Trigger Enable).

The default for TE is disabled. The external TRIG input is referenced to VIO. The TRIG input is edge sensitive. The TRIG input signal width must be at least 1,500 ns, otherwise it will be ignored by the digital logic. To improve interfacing options the polarity of the TRIG signal is programmable via Register [10000], bit D14 (TP, Trigger Polarity). The default for TP is low-to-high transition of the TRIG signal.

When the TRIG input pin is enabled (D13 = TE set to 1 with a write to Register [10000]), the requested DAC voltage levels are set up in shadow registers and not transferred to the destination registers until the trigger condition is met. In this manner the change in DAC output voltage levels are synchronized with the external TRIG event (active edge). If multiple DAC voltage level requests are received before the TRIG event occurs, only the last fully received DAC output voltage level will be applied to the outputs.

If the external trigger function is not needed in the application, the TRIG pin should be grounded and the TRIG function disabled. When TRIG is disabled, the requested DAC voltage levels are immediately applied to the outputs and are not synchronized with the TRIG signal.

Table 26. DAC MODE SETUP: DAC ENABLE

D3	D2	D1	DAC A	DAC B	DAC C	
0	0	0	Off	Off	Off	(Default)*
0	0	1	Off	Off	Enabled	
0	1	0	Off	Enabled	Off	
0	1	1	Off	Enabled	Enabled	
1	0	0	Enabled	Off	Off	
1	0	1	Enabled	Off	Enabled	
1	1	0	Enabled	Enabled	Off	
1	1	1	Enabled	Enabled	Enabled	

*If all bits [3:1] are ‘0’, then incoming DAC messages will be ignored until at least one of [3:1] is set ‘1’.

RF Front-End Control Interface (MIPI RFFE Interface)

The TCC−103 is a write-only slave device which is fully compliant to the MIPI Alliance Specification for RF Front-End Control Interface (RFFE) Version 1.00.00 03 May 2010. This device is rated at Full-Speed operation for 1.65 V < VIO < 1.95 V and at Half-Speed operation for 1.1 V < VIO < 1.65 V. When using the MIPI RFFE interface the CS pin is grounded.

Table 27. MIPI RFFE INTERFACE SPECIFICATION

(T_A = −30 to +85°C; 2.3 V < AVDD < 5.5 V; 1.1 V < VIO < 1.95 V; unless otherwise specified)

Parameter	Description	Min	Typ	Max	Unit	Comment
F_{SCLK}	Clock Full-Speed Frequency	0.032	–	26	MHz	Full-Speed Operation: 1.65 V < VIO < 1.95 V
T_{SCLK}	Clock Full-Speed Period	0.038	–	32	μs	Full-Speed Operation: 1.65 V < VIO < 1.95 V
T_{SCLKIH}	CLK Input High Time	11.25	–	–	ns	Full-Speed
T_{SCLKIL}	CLK Input Low Time	11.25	–	–	ns	Full-Speed
F_{SCLK_HALF}	Clock Half-Speed Frequency	0.032	–	13	MHz	
T_{SCLK_HALF}	Clock Half-Speed Period	0.077	–	32	μs	
T_{SCLKIH}	CLK Input High Time	24	–	–	ns	Half-Speed
T_{SCLKIL}	CLK Input Low Time	24	–	–	ns	Half-Speed
V_{TP}	Positive Going Threshold Voltage	0.4 × VIO	–	0.7 × VIO	V	CLK, DATA, TRIG, 1.2 or 1.8 V Bus
V_{TN}	Negative Going Threshold Voltage	0.3 × VIO	–	0.6 × VIO	V	CLK, DATA, TRIG, 1.2 or 1.8 V Bus
V_H	Hysteresis Voltage ($V_{TP} - V_{TN}$)	0.1 × VIO	–	0.4 × VIO	V	CLK, DATA, TRIG, 1.2 or 1.8 V Bus
I_{IH}	Input Current High	−2	–	+10	μA	TRIG, SDATA = 0.8 × VIO
		−1	–	+10	μA	SCLK = 0.8 × VIO
I_{IL}	Input Current Low	−2	–	+1	μA	TRIG, SDATA = 0.2 × VIO
		−1	–	+1	μA	SCLK = 0.2 × VIO
C_{CLK}	Input Capacitance	–	–	5	pF	CLK Pin
C_{DATA}	Input Capacitance	–	–	8.3	pF	DATA Pin
C_{TRIG}	Input Capacitance	–	–	10	pF	TRIG Pin
TD_{SETUP}	DATA Setup Time	–	–	1	ns	Full-Speed
TD_{HOLD}	DATA Hold Time	–	–	5	ns	Full-Speed
TD_{SETUP}	DATA Setup Time	–	–	2	ns	Half-Speed
TD_{HOLD}	DATA Hold Time	–	–	5	ns	Half-Speed
T_{SUCC}	Time between Successive DAC Update Writes	1,500	–	–	ns	

The HVDAC contains twenty-four 8 bit registers. Register content is described in Table 35. Some additional registers, implement as provision, are not described in this document.

Table 28. MIPI RFFE ADDRESS MAP

Register Address	Description	Purpose	Access Type	Size (Bits)
0x00	DAC Configuration (Enable Mask)	High Voltage Output Enable Mask	Write	7
0x01	Turbo Register DAC A, B & C	Turbo-Charge Configuration DAC A, B & C	Write	8
0x02	DAC A Register	Used to Set Up OUT A	Write	8
0x03	DAC B Register	Used to Set Up OUT B	Write	8
0x04	DAC C Register	Used to Set Up OUT C	Write	8
0x10	DAC Boost (VHV)	Settings for the Boost High Voltage	Write	8
0x11	Trigger Register	Trigger Configuration	Write	8
0x12	Turbo-Charge Delay DAC A, B, C	Turbo-Charge Delay Steps DAC A, B, C	Write	8
0x13	Turbo-Charge Delay DAC A, B, C	Turbo-Charge Delay Multiplication DAC A, B, C	Write	8
0x1C	Power Mode and Trigger Register	Power Mode & Trigger Control PWR_MODE [7:6] TRIG_REG [5:0]	Write	8
0x1D	Product ID Register	Product Number * Hard Coded into ASIC	(Write)	8
0x1E	Manufacturer ID Register	MN (10 Bits Long) Manufacturer ID[7:0] Hard Coded into ASIC	(Write)	8
0x1F	Unique Slave Identifier Register (USID)	Spare [7:6] [5,4] = Manufacturer ID [9:8] USID [3:0]	Write	8

*The two least significant bits are programmed in OTP during manufacture.

Configuration Settings

Table 29. DAC CONFIGURATION (ENABLE MASK) AT [0x00]

Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SSE	0 Reserved	0 Reserved	DAC A	DAC B	DAC C	0 Reserved

SSE = 0 Spread Spectrum disabled, SSE = 1 Spread Spectrum enabled (default)

DAC A, B, C = 1 when output is enabled

DAC A, B, C = 0 when output is off (default); If all three DAC A, DAC B, and DAC C bits are set to “0” then incoming DAC messages will be ignored until at least one is set to “1”.

Table 30. BOOST DAC MODE SETUP (VHV) AT [0x10] (Note 1)

Bit 7*	Bit 6*	Bit 5*	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	VHV (V)
0	0	0	1	0	0	0	0	9
0	0	0	1	0	0	0	1	10
0	0	0	1	0	0	1	0	11
0	0	0	1	0	0	1	1	12
0	0	0	1	0	1	0	0	13
0	0	0	1	0	1	0	1	14
0	0	0	1	0	1	1	0	15
0	0	0	1	0	1	1	1	16
0	0	0	1	1	0	0	0	17
0	0	0	1	1	0	0	1	18
0	0	0	1	1	0	1	0	19
0	0	0	1	1	0	1	1	20 (Default)
0	0	0	1	1	1	0	0	21
0	0	0	1	1	1	0	1	22
0	0	0	1	1	1	1	0	23
0	0	0	1	1	1	1	1	24

1. Bit 4 is fixed at logic 1 for reverse SW compatibility.
*Indicates reserved bits.

MIPI RFFE TRIG Operation

The MIPI RFFE Trigger Mode can be used as a synchronization signal to ensure that new DAC settings are applied to the outputs at appropriate times in the overall transceiver system. When the MIPI RFFE TRIG function is enabled via [0x11] bit 4 the requested DAC voltage levels are set up in the shadow registers and not transferred to the destination registers until the trigger condition is met. In this manner the change in output voltage levels are synchronized with the MIPI RFFE TRIG command. If multiple DAC voltage level requests are received before the TRIG event occurs, only the last fully received DAC output voltage level will be applied to the outputs.

The trigger configuration also provides for an additional external TRIG pin to be used as a synchronization signal. The external TRIG is independent from the built-in triggers available within the MIPI RFFE interface. When the TRIG input pin is enabled via [0x11] bit 4 the requested DAC voltage levels are set up in the shadow registers and are not transferred to the destination registers until the external trigger condition is met. In this manner the change in output voltage levels are synchronized with the external TRIG event. The external TRIG input is referenced to VIO. To improve interfacing options the polarity of external TRIG is programmable via [0x11] bit 1.

If the external trigger function is not needed in the application, the TRIG pin should be grounded and the TRIG function disabled. When MIPI RFFE trigger and the external TRIG input are disabled, the requested DAC voltage levels are immediately applied to the outputs and are not synchronized with the MIPI RFFE Trigger Modes or the external TRIG signal.

Table 31. TRIGGER CONFIGURATION AT [0x11]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved 0	Reserved 0	Reserved 0	TRIG Select 0 = Ext TRIG Pin 1 = RFFE Trigger	Reserved 0		TRIG Edge 0 = Active Falling 1 = Active Rising	Mask Ext TRIG 1 = Mask

Table 32. EXTERNAL TRIGGER CONFIGURATION BIT SETTINGS AT [0x11]

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description
0	–	–	–	–	External trigger pin is enabled. Sending the RFFE message will load a ‘shadow’ registers only. Only upon an active signal on external TRIG pin are the output registers loaded with the new voltage settings which are then applied to the outputs.
1	–	–	–	–	The MIPI RFFE Trigger Is Enabled. (Default)
–	–	–	0	–	External TRIG Pin Signal Is Active Falling.
–	–	–	1	–	External TRIG Pin Signal Is Active Rising. (Default)
–	–	–	–	0	External Trigger Pin Is Not Masked
–	–	–	–	1	Mask External Trigger Pin (Default)

Table 33. POWER MODE AND TRIGGER REGISTER [0x1C]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PM1	PM0	Trigger Mask 2	Trigger Mask 1	Trigger Mask 0	Trigger 2	Trigger 1	Trigger 0

Writing a logic one (‘1’) to the bits 0, 1 or 2 (Trigger 0, 1 or 2) moves data from the shadow registers into the destination registers. Default for bit 0, 1 & 2 is logic low.

If Trigger Mask 0, 1 or 2 bit is set (‘1’) the Trigger 0, 1 or 2 are disabled respectively and the data goes directly to the destination register. Default for bit 3, 4 & 5 is logic low.

All three triggers behave in the same way as the external pin TRIG. When each of these triggers is set using the MIPI RFFE interface the results are the same as when an active edge is applied to the TRIG pin when External pin TRIG is selected.

Table 34. POWER MODE BIT SETTINGS IN REGISTER [0x1C]

PM1	PM0	State	Description
0	0	Active	Boost Control Active, VHV Set by Digital Interface V_{OUT} A, B, C Enabled and Controlled by Digital Interface (Default)
0	1	Startup	Boost Control Active, VHV Set by Digital Interface V_{OUT} A, B, C Disabled
1	0	Low Power	Digital Interface is Active While All Other Circuits are in Low Power Mode
1	1	Reserved	State of Hardware Does Not Change

Table 35. PRODUCT_ID REGISTER AT [0x1D]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1*	Bit 0*
PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0
0	0	0	0	0	1	0	0

*Programmed in OTP during manufacture (4 combinations of Product ID possible).

Table 36. MANUFACTURER_ID REGISTER AT [0x1E]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MPN7	MPN6	MPN5	MPN4	MPN3	MPN2	MPN1	MPN0
0	0	1	0	1	1	1	0

Table 37. SPARE(1:0), MANUFACTURER_ID(9:8), USID(3:0) REGISTER AT [0x1F]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3*	Bit 2*	Bit 1*	Bit 0*
Reserved	Reserved	MPN9	MPN8	USID3	USID2	USID1	USID0
0	0	0	1	0	1	1	1

*Changes to the USID are not retained during SHUTDOWN power mode.

DAC Output Register Setting

The control IC output voltages are scaled from 0 to 24 V, with 128 steps of 188 mV ((24 V/255) × 2 = 0.188 V). The nominal control IC output can be approximated to 188 mV × (DAC value). The DAC output voltage settings are stored in registers [0x02], [0x03] & [0x04] in 7-bit binary form:

Table 38. TURBO-CHARGE DAC A, B & C REGISTER [0x01]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC_INDX [7:0]							

Table 39. DAC A REGISTER [0x02]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC_INDX [8]	DAC A Value (Default = 0000000)						

Table 40. DAC B REGISTER [0x03]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC_INDX [9]	DAC B Value (Default = 0000000)						

Table 41. DAC C REGISTER [0x04]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC_INDX[10]	DAC C Value (Default = 0000000)						

The Turbo time is encoded into TC_INDX register, using the formula:

$$\text{Index} = \text{State_A} \times 144 + \text{State_B} \times 12 + \text{State_C} \quad \text{(eq. 3)}$$

TC_INDX [10:0] register mapping:

TC_INDX [7:0] = RFFE_REG_0x01, bit [7:0]

TC_INDX [8] = RFFE_REG_0x02, bit 7

TC_INDX [9] = RFFE_REG_0x03, bit 7

TC_INDX [10] = RFFE_REG_0x04, bit 7

See Table 17.

Turbo-Charge Mode

Table 42. TURBO-CHARGE DELAY STEPS [0x12]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		TC_STP_ DAC_C1	TC_STP_ DAC_C0	TC_STP_ DAC_B1	TC_STP_ DAC_B0	TC_STP_ DAC_A1	TC_STP_ DAC_A0

NOTE: TC_STP_DAC_X is defined in the Table 21.

Table 43. TURBO-CHARGE DELAY MULTIPLICATION [0x13]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		TCM_C1	TCM_C0	TCM_B1	TCM_B0	TCM_A1	TCM_A0

NOTE: TCM_X is defined in the Table 20.

Command Sequences

- **Register 0 Write** (used to access the Register 0 DAC Configuration - Enable Mask). Register 0 can be also be accessed using Register Write or/and Extended Register Write.
- **Register Write** (used to access only one register at the time)
- **Extended Register Write** (used to access a group of contiguous registers with one command)

Register 0 Write Command Sequence

The Command Sequence starts with a Sequence Start Condition (SSC) which is followed by the Register 0 Write Command Frame. This Frame contains the Slave address, a logic one, and the seven bit word that will be written to Register 0. The Command Sequence is depicted below.

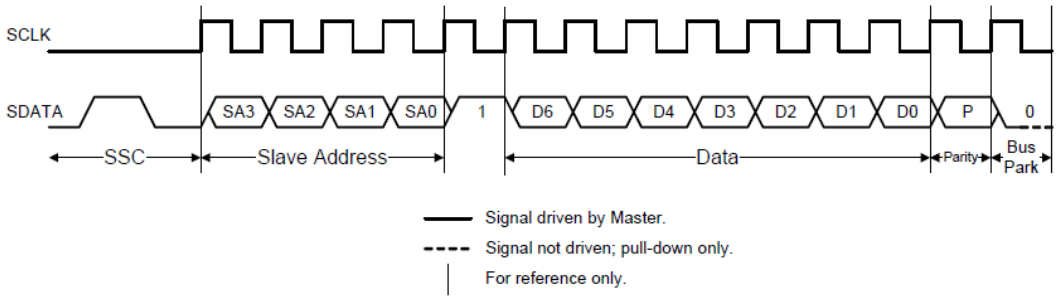


Figure 10. Register 0 Write Command Sequence

Table 44. MIPI RFFE COMMAND FRAME FOR REGISTER 0 WRITE COMMAND SEQUENCE

Description	SSC		Command Frame										BP
SSE & DAC Configuration	1	0	SA [3,0]	1	SSE	0	0	DAC_A	DAC_B	DAC_C	0	P	BP

Register Write Command Sequence

The Write Register command sequence may be used to access each register (addresses 0-31).

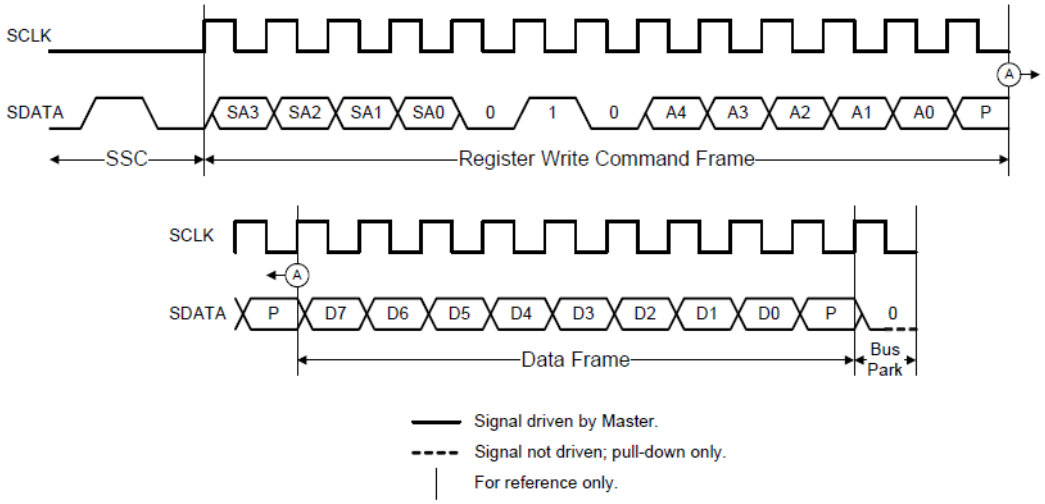


Figure 11. Register Write Command Sequence

Table 45. MIPI RFFE COMMAND FRAME FOR REGISTER 0 WRITE COMMAND SEQUENCE

Description	SSC		Command Frame										Data Frame		BP
Turbo Charge Settings	1	0	SA [3,0]	0	1	0	0	0	0	0	1	P	Turbo Charge [7:0]	P	BP
Register Write DAC A	1	0	SA [3,0]	0	1	0	0	0	0	1	0	P	TC [8] & DAC_A [6:0]	P	BP
Register Write DAC B	1	0	SA [3,0]	0	1	0	0	0	0	1	1	P	TC [9] & DAC_B [6:0]	P	BP
Register Write DAC C	1	0	SA [3,0]	0	1	0	0	0	1	0	0	P	TC [10] & DAC_C [6:0]	P	BP

Extended Register Write Command Sequence

In order to access more than one register in one sequence this message could be used. Most commonly it will be used for loading three DAC registers at the same time. The four LSBs of the Extended Register Write Command Frame determine the number of bytes that will be written by the Command Sequence. A value of 0b0000 would write one byte and a value of 0b1111 would write sixteen bytes.

If more than one byte is to be written, the register address in the Command Sequence contains the address of the first extended register that will be written to and the Slave's local extended register address shall be automatically incremented by one for each byte written up to address 0x1F, starting from the address indicated in the Address Frame.

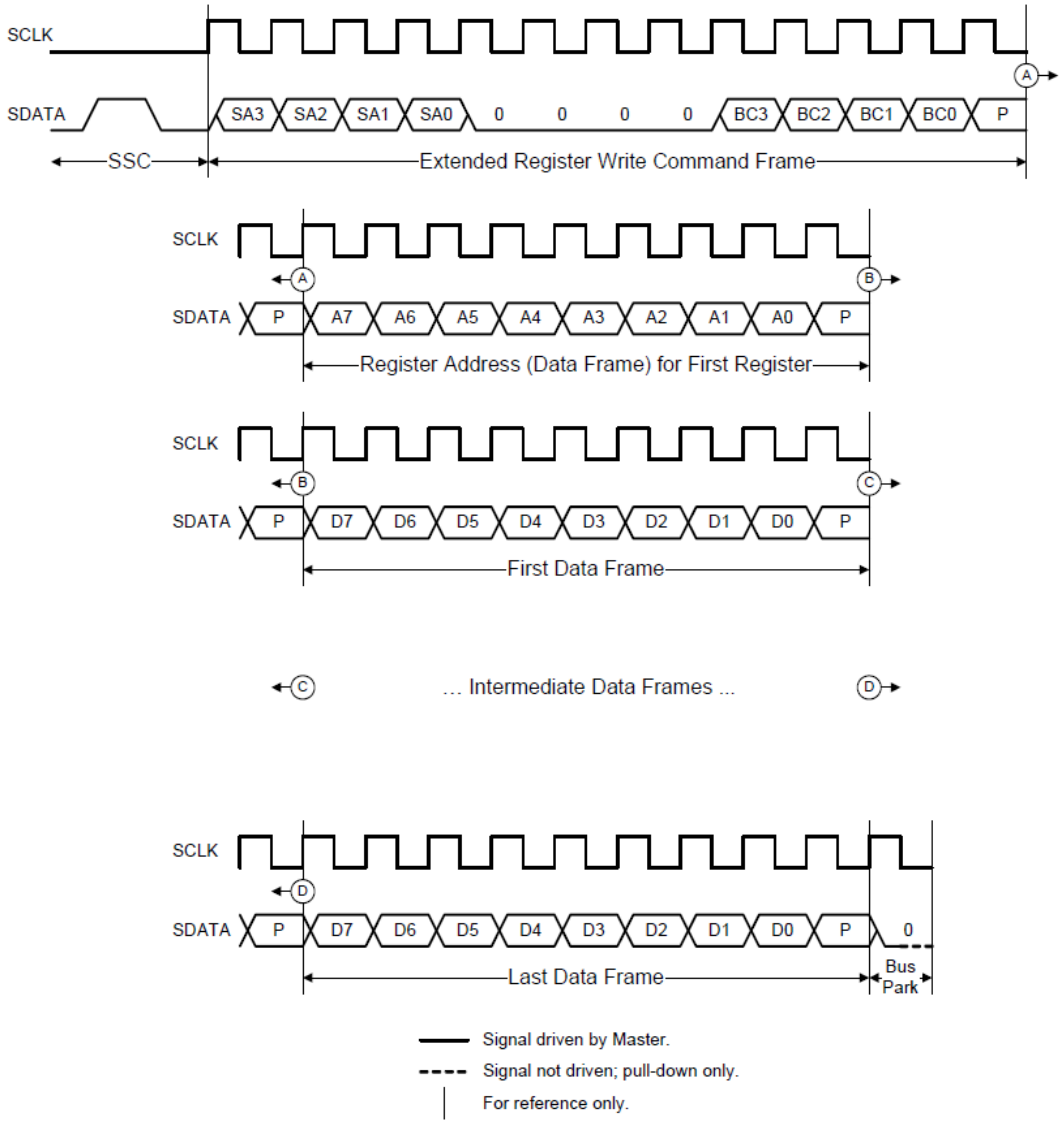


Figure 12. Extended Register Write Command Sequence

Table 46. EXTENDED REGISTER WRITE

Description	SSC		Command Frame										Address Frame								
Extended Register Write Turbo Charge & DAC							Op Code		<Byte Count>			P	<Starting Address>								P
	1	0	SA [3,0]				0	0	0	0	0	0	1	1	P	0	0	0	0	0	0	0	1	P

Data Frame		Data Frame		Data Frame		Data Frame		BP
<Data-8 Bit>	P	<Data-8 Bit>	P	<Data-8 Bit>	P	<Data-8 Bit>	P	BP
Turbo Charge	P	DAC_A [7,0]	P	DAC_B [7,0]	P	DAC_C [7,0]	P	BP

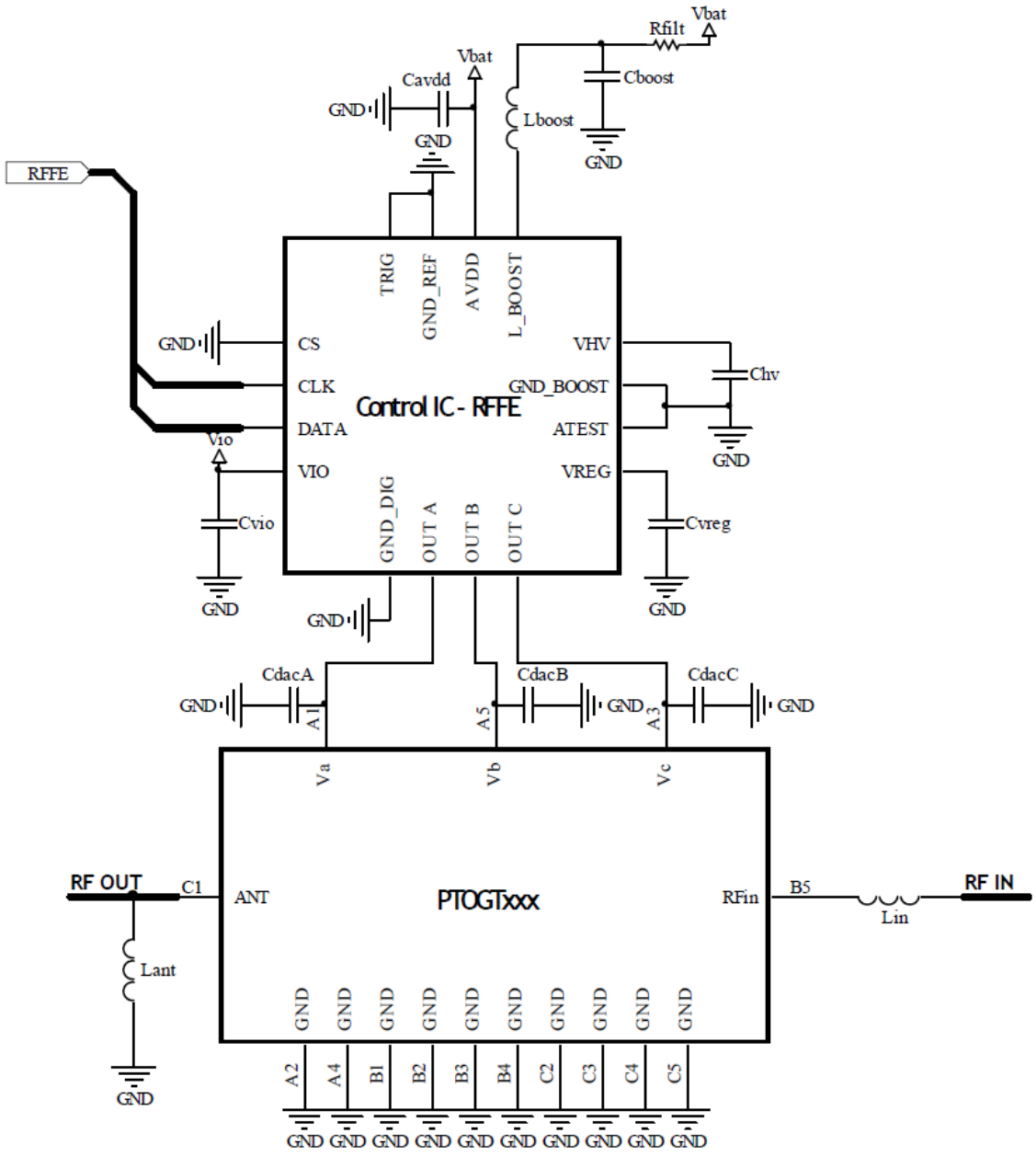


Figure 13. Recommended MIPI RFFE Interface Application Schematic

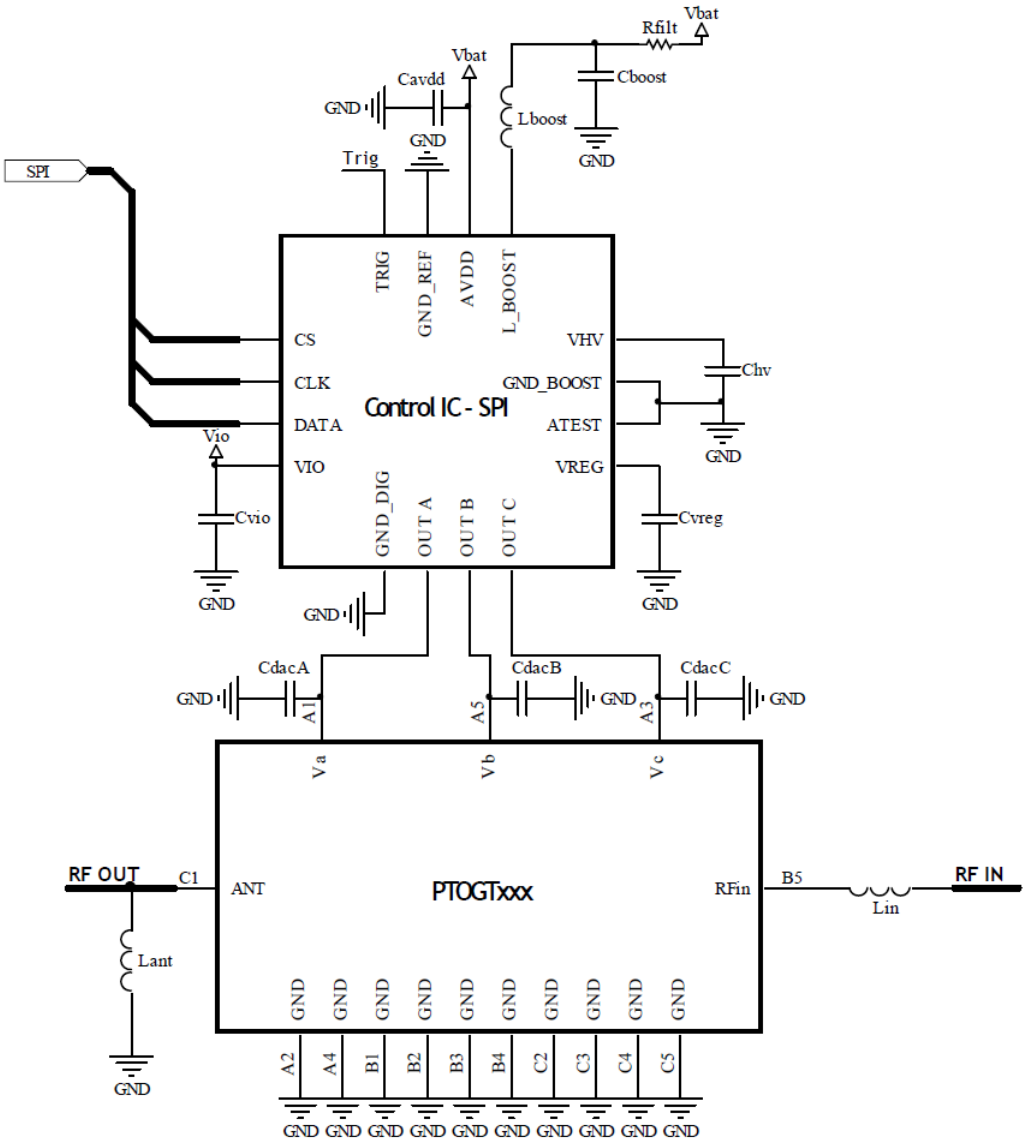


Figure 14. Recommended 3-wire Serial Interface Application Schematic

Table 47. RECOMMENDED EXTERNAL BOM

Component	Description	Nominal Value	Package (Inch)	Recommended P/N
C_{BOOST}	Boost Supply Capacitor, 10 V	1 μF	0402	TDK: C1005X5R1A105K
L_{BOOST}	Boost Inductor	15 μH	0603	Coilcraft: 0603LS-153X_L ABCO: LPS181210T-150M Others: TDK: VLS2010ET-150M Sumida: CDH20D11DLDNP-150MC
R_{FILT}	Decoupling Resistor, 5%	3.3 Ω	0402	Vishay: CRCW04023R30JNED
C_{VIO}	V_{IO} Supply Decoupling, 10 V	100 nF	0201	Murata: GRM033R61A104ME15D
C_{AVDD}	V_{AVDD} Supply Decoupling, 10 V	1 μF	0402	TDK: C1005X5R1A105K
C_{VREG}	V_{VREG} Supply Decoupling, 10 V	220 nF	0201	TDK: C0603X5R1A224M
C_{HV}	Boost Output Capacitor, 50 V	22 nF	0402	Murata: GRM155R71H223KA12
C_{dacA} C_{dacB} C_{dacC}	Decoupling Capacitor, 50 V	100 pF	0201	Murata: GRM0335C1H101JD01D

MECHANICAL DESCRIPTION

TCC = Product Code
X = MIPI ID
(see MIPI Version Table)
7 = Assembly Location
L = Wafer Lot Code
Y = Year Code
W = Week Code
• = Pin 1 Marker

Pb-Free (Sn/Ag/Cu SAC351)

MIPI VERSION
A = 00
B = 01
C = 10
D = 11

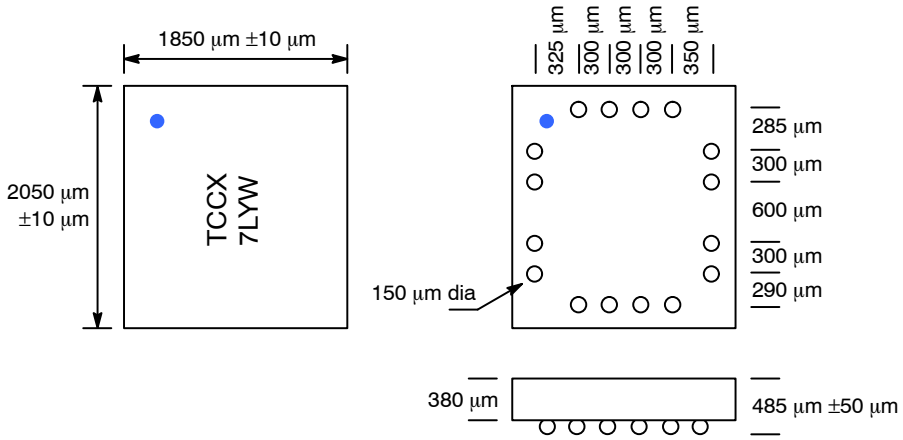
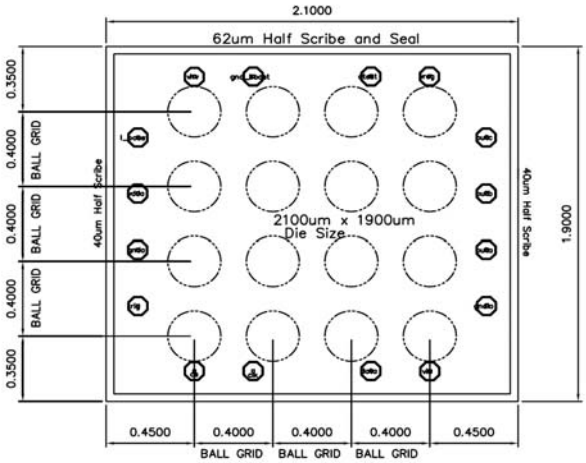


Figure 15. Peripheral Row Package



TCC = Product Code
x = MIPI ID
(see MIPI Version Table)
7 = Assembly Location
L = Wafer Lot Code
Y = Year Code
W = Week Code
• = Pin 1 Marker

Pb-Free (96.8% Sn/2.6% Ag/0.6% Cu)

MIPI VERSION
a = 00
b = 01
c = 10
d = 11

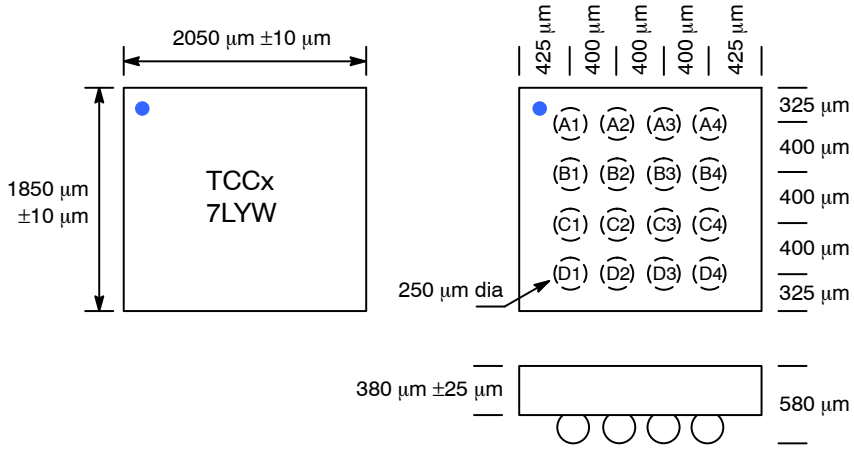
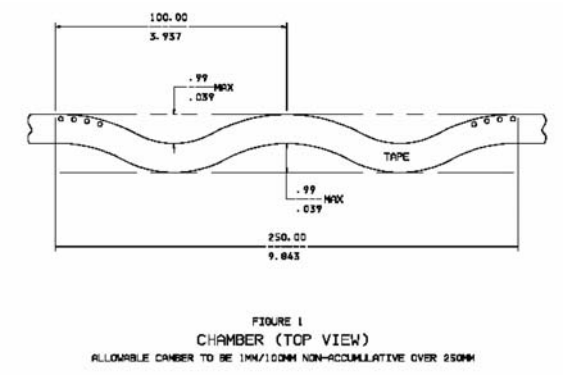
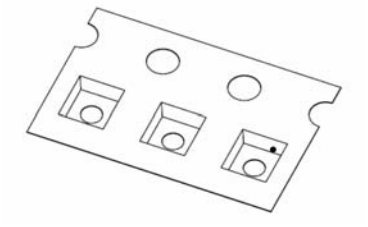
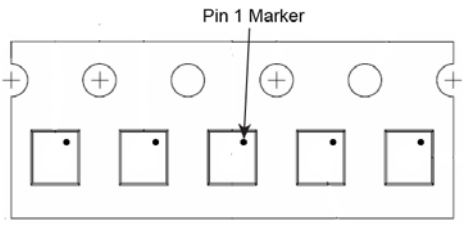


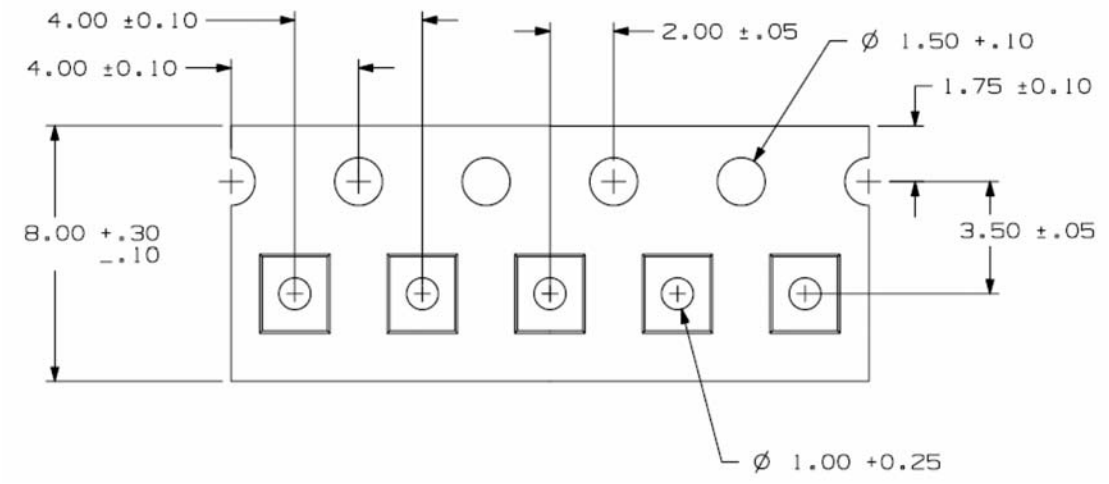
Figure 16. Ball Array Package

TAPE & REEL DIMENSIONS









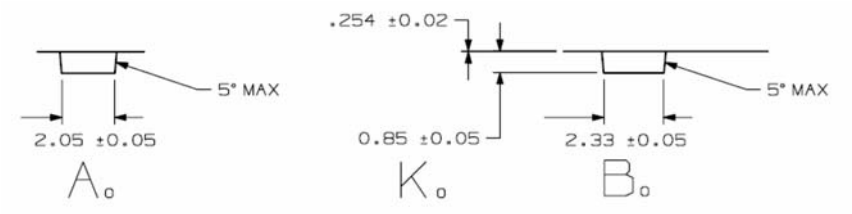


Figure 17. WLCSP Carrier Tape Drawings

Table 48. ORDERING INFORMATION

Device	Package	Shipping†
TCC−103A−PT	Peripheral Bump (Pb-Free)	3,000 Units/Reel
TCC−103A−RT	RDL (Pb-Free)	3,000 Units/Reel
TCC−103B−PT	Peripheral Bump (Pb-Free)	3,000 Units/Reel
TCC−103B−RT	RDL (Pb-Free)	3,000 Units/Reel
TCC−103C−PT	Peripheral Bump (Pb-Free)	3,000 Units/Reel
TCC−103C−RT	RDL (Pb-Free)	3,000 Units/Reel
TCC−103D−PT	Peripheral Bump (Pb-Free)	3,000 Units/Reel
TCC−103D−RT	RDL (Pb-Free)	3,000 Units/Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative