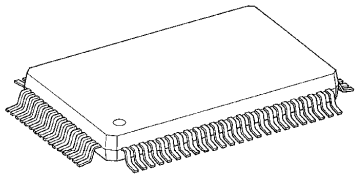
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9331F

AUDIO DIGITAL SIGNAL PROCESSOR

The TC9331F digital integrated circuit facilitates real time processing of digital signals in audio equipment for digital filters such as equalizers, dynamic range controllers for compressors and expanders, as well as acoustic field simulators that produce concert hall effects. The TC9331F is a-high speed, high-definition audio digital processor.



QFP80-P-1420-0.80A

Weight : 1.57g (Typ.)

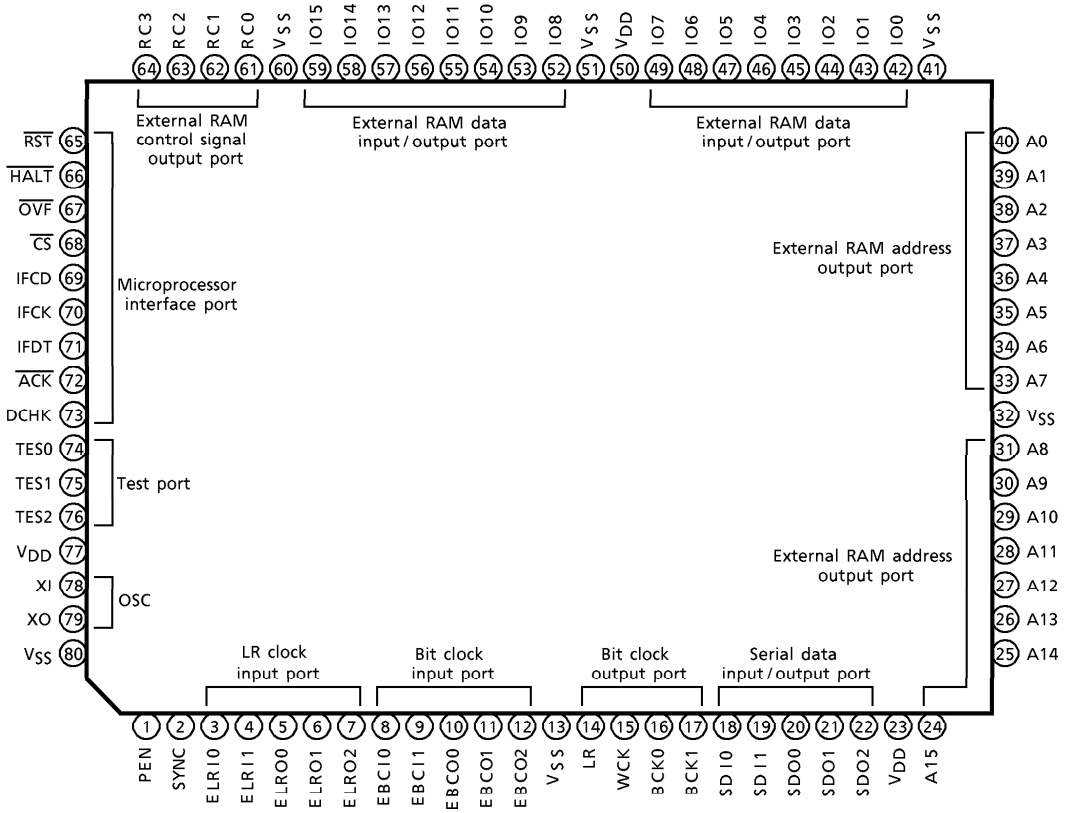
FEATURES

- The TC9331F features a 32bit main bus.
- The TC9331F is capable of both reading from and writing to external sources of RAM data and allows for the simultaneous accumulation, operation, and integration of the data that needs to be processed.
  - Multiplier / adder : 32bit × 16bit + 51bit → 51bit
  - Shifter : + 4, + 1bit shift
  - Accumulator : 51bit (code extension 4bit)
  - Work register : 2 registers (32 and 47bit)
  - Program RAM : 320 words × 32bit
  - Data RAM : 128 words × 32bit [Mode 1], (128 words × 16bit) × 2 [Mode 2]
  - Coefficient RAM : 320 words x 16bit
  - Offset address RAM : 64 words x 16bit
- The interface parameters for external RAM sources are as follows:
  - Data word length : Both 16bit and 32bit
  - External RAM : 1M DRAM, 256K DRAM, 256K pseudo-static RAM (PSRAM)
- The following five ports have been made available for use as serial data ports.
  - Serial data input ports : 2 ports (SDI0, SDI1)
  - Serial data output ports : 3 ports (SDO0, SDO1, SDO2)
  - Data word length : Both 16 and 32bit
  - Data format : 2's complement, MSB first
- The program's settings, coefficient data, and offset data can be made converted through the microprocessor interface.
- The CMOS construction of the TC9331F makes high-speed processing possible.
- The TC9331F features a flat, 80 pin package design.

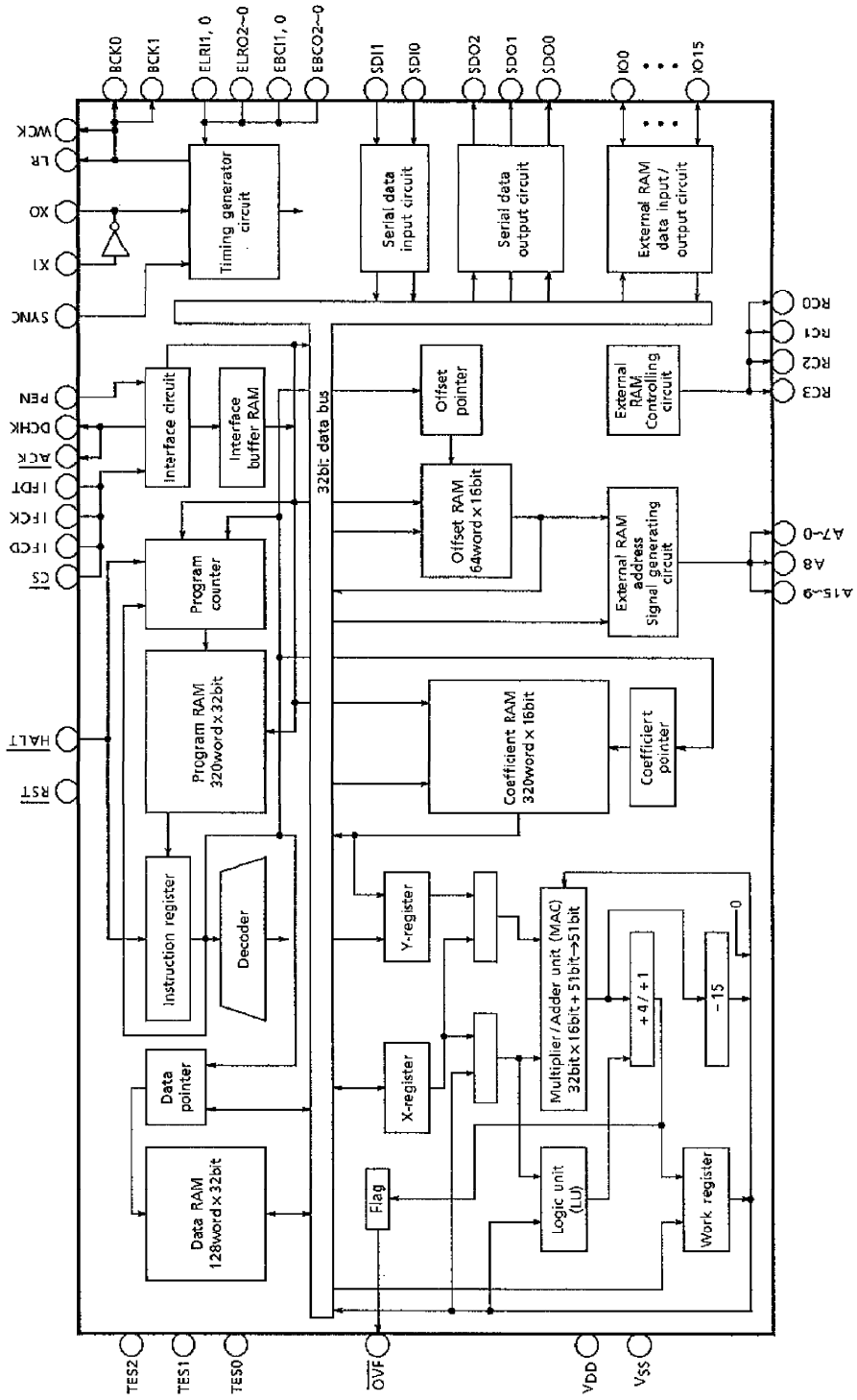
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PIN CONNECTION



BLOCK DIAGRAM

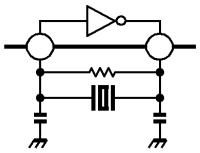


TC9331F-3

DESCRIPTION OF PIN FUNCTIONS

PIN No.	SYMBOL	I / O	DESCRIPTION OF PIN FUNCTION		REMARK
1	PEN	I	Parity-check-function-enabling terminal. (H = enable, L = disable) Sets up the execution of the interface data parity check (odd parity) .		Pull-up resistor
2	SYNC	I	Synchronous signal input terminal. The synchronous signal forcibly resets the program counter to "zero", and the polarity is set by the microcomputer controller.		Schmidt input Pull-up resistor
3	ELRI0	I	LR clock input terminal. Input terminal for the SDI0 / 1 data processing LR clock.	For SDI0 data input	—
4	ELRI1			For SDI1 data input	
5	ELRO0	I	LR clock input terminal. Input terminal for the SDO0 / 1 / 2 data processing LR clock.	For SDO0 data output	—
6	ELRO1			For SDO1 data output	
7	ELRO2			For SDO2 data output	
8	EBCI0	I	Bit clock input terminal. Input terminal for the SDI0 / 1 data processing shift clock.	For SDI0 data input	—
9	EBCI1			For SDI1 data input	
10	EBCO0	I	Bit clock input terminal. Input terminal for the SDO0 / 1 / 2 data processing shift clock.	For SDO0 data output	—
11	EBCO1			For SDO1 data output	
12	EBCO2			For SDO2 data output	
14	LR	O	LR clock output terminal. (1fs)		—
15	WCK	O	Word clock output terminal. (2fs)		—
16	BCK0	O	Bit clock output terminal. (32fs)		—
17	BCK1	O	Bit clock output terminal. (64fs)		—
18	SDI0	I	Serial data input terminals. The microcomputer controller allows 32bit or 16bit input data lengths to be selected.		—
19	SDI1				
20	SDO0	O	Serial data output terminals. The microcomputer controller allows 32bit or 16bit output data lengths to be selected.		—
21	SDO1				
22	SDO2	O	Serial data output terminal. Outputs 16bit data.		—
24 ~ 31	A15 ~ A8	O	External RAM address output terminals. Generally used when in the pseudo-static RAM mode. In the dynamic RAM mode, this terminal is set at "L". Note, however, that A8 is used for output addressing purposes in the 1 M Dram (4bit × 256K) mode.		—
33 ~ 40	A7 ~ A0	O	External RAM address output terminals. In the dynamic RAM mode, both the low and column addresses are output from these terminals.		—

<table>
<tr><th>PIN No.</th><th>SYMBOL</th><th>I/O</th><th>DESCRIPTION OF PIN FUNCTION</th><th>REMARK</th></tr>
<tr><td>42
~
49</td><td>IO0
~
IO7</td><td rowspan="2">I/O</td><td rowspan="2">Data input/output to and from the external RAM source.<table><tr><th>DATA LENGTH</th><th>I/O0~I/O7</th><th>I/O8~I/O15</th></tr><tr><td>16bit</td><td>Low priority 8bit (D_7-D_0)</td><td>High priority 8bit (D_{15}-D_8)</td></tr><tr><td>32bit</td><td>Low priority 16bit (D_{23}-D_{16})/(D_7-D_0)</td><td>High priority 16bit (D_{31}-D_{24})/(D_{15}-D_8)</td></tr></table></td><td rowspan="2">Pull-up resistor</td></tr>
<tr><td>52
~
59</td><td>IO8
~
IO15</td></tr>
<tr><td colspan="2">RC0~RC3</td><td></td><td>〔Pseudo-static RAM mode〕</td><td>〔Dynamic RAM mode〕</td><td>—</td></tr>
<tr><td>61</td><td>RC0</td><td>O</td><td>$\overline{CE}$: Chip enable signal output terminal.</td><td>$\overline{RAS}$: Low address strobe output terminal.</td><td>—</td></tr>
<tr><td>62</td><td>RC1</td><td>O</td><td>Not in use.</td><td>$\overline{CAS}$: Column address strobe output terminal.</td><td>—</td></tr>
<tr><td>63</td><td>RC2</td><td>O</td><td>$\overline{OE}$/$\overline{RFSH}$: Output enable/refresh signal output terminal.</td><td>$\overline{OE}$: Output enabling signal output terminal.</td><td>—</td></tr>
<tr><td>64</td><td>RC3</td><td>O</td><td>R/$\overline{W}$: Read/write signal output terminal.</td><td>$\overline{WTITE}$: Read/write signal output terminal.</td><td>—</td></tr>
<tr><td>65</td><td>$\overline{RST}$</td><td>I</td><td colspan="2">Reset signal input terminal.</td><td>Pull-up resistor</td></tr>
<tr><td>66</td><td>$\overline{HALT}$</td><td>I</td><td colspan="2">Halt signal input terminal.
When “L” is active, the program counter is stopped and instructions are rendered as NOP.
Generally used in the emulation mode.</td><td>Schmidt input
Pull-up resistor</td></tr>
<tr><td>67</td><td>$\overline{OVF}$</td><td>O</td><td colspan="2">Overflow output terminal.
Activates “L” when an overflow occurs during operations.</td><td>Open drain output.</td></tr>
<tr><td>68</td><td>$\overline{CS}$</td><td>I</td><td colspan="2">Chip selection signal terminal.
When the “$\overline{CS}$” is in an “L” 's active, data can be transferred from the CPU.</td><td>Schmidt input.</td></tr>
<tr><td>69</td><td>IFCD</td><td>I</td><td colspan="2">Microcomputer command or data input mode selection terminal. When “H” is active, the terminal acts as a command selection terminal; when “L” is active, it acts as a data input selection terminal.</td><td>Schmidt input.</td></tr>
<tr><td>70</td><td>IFCK</td><td>I</td><td colspan="2">Shift clock input terminal for microcomputer data processing.</td><td>Schmidt input.</td></tr>
<tr><td>71</td><td>IFDT</td><td>I</td><td colspan="2">Microcomputer data processing input terminal.
Receives commands and data to which one parity bit has been added at the LSB first.</td><td>Schmidt input.</td></tr>
<tr><td>72</td><td>$\overline{ACK}$</td><td>O</td><td colspan="2">Acknowledge output terminal for the microcomputer.
Outputs an acknowledge signal when the command and data parity are acceptable.</td><td>Open drain output.
Pull-up resistor</td></tr>
</table>

PIN No.	SYMBOL	I / O	DESCRIPTION OF PIN FUNCTION	REMARK
73	DCHK	O	Microcomputer return output terminal. At the same time that the IFCK is initiated, the terminal outputs the received data. In the emulation mode, the terminal also sends out an "L", the break acknowledge signal.	Open drain output. Pull-up resistor
74 ʃ 76	TES0 ʃ TES2	I	Test terminal. Usually used in an " H", or open, position.	Pull-up resistor
78	XI	I	Crystal oscillator connection terminal.	
79	XO	O		
23 50 77	V_{DD}	—	Power supply terminal.	—
13 32 41 51 60 80	V_{SS}	—	Ground terminal.	—

OPERATING INSTRUCTIONS

1. Timing sequence generating circuit.

   (1) Crystal-controlled oscillator circuit

   An internal operations clock can be created by connecting a crystal-controlled oscillator (30.72 MHz), condenser, and resistor in the manner shown in Figure 1 below.
   An alternative method would be to connect a external clock to the XI terminal as shown in Figure 2 below.

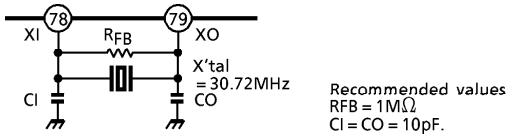
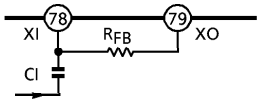


Fig.1(a) Self excited crystal oscillator

For external clock purposes, a crystal with a good starting potential and low CI value is recommended.



Recommended values
RFB = 1MΩ
CI = 0.001-0.01μF

Fig.1(b) External clock Input.

(2) The generating circuit for the audio data input / output clock (channel clock and bit clock)

Both internal generating and external input modes are available for 16 / 32bit serial data input / output channel (LR, ELRI0-1, and ELRO0-2) and bit (BCK0, EBCI0-1, EBCO0-2) clocks.
As shown in Figure 1(b), the channel clock is selected by LROS0-2 and LRIS0-1, and the bit clock by BCOS0-1, BCIS0-1, and BCKS of control register 2, respectively.
Both 16bit and 32bit outputs are available in internal clock generation mode (SDO2 is bypassed). The mode setup is accomplished through the microcomputer interface (control register 2).
(For further details please refer to the Explanation of the Microcomputer Interface Control Register Functions.)
The data input (SDI1 and SDI0) channel clock and bit clock are selected by LRIS1 and LRIS0, and BCIS1 and BCIS0 of control register 2, respectively.
Tables 1. (a) and 1. (b) below provide details regarding the data input (SDI1 and SDI0) modes.

Table 1. (a) The (SDI1) data input channel clock and bit clock modes

CONTROL REGISTER 2 (CNT-R2)		DATA INPUT APPLICATIONS (SDI1)	
LRIS1	BCIS1	CHANNEL CLOCK / BIT CLOCK	DATA BIT COUNT
0	0	Internally generated TGLR / (TG32 / TG64)	16bit
0	1	Internally generated TGLR / (TG32 / TG64)	32bit
1	X	External input ELRI1 / EBCI1	—

Table 1. (b) The (SDI0) data input channel clock and bit clock modes

CONTROL REGISTER 2 (CNT-R2)		DATA INPUT APPLICATIONS (SDI0)	
LRIS0	BCIS0	CHANNEL CLOCK / BIT CLOCK	DATA BIT COUNT
0	0	Internally generated TGLR / (TG32 / TG64)	16bit
0	1	Internally generated TGLR / (TG32 / TG64)	32bit
1	X	External input ELRI0 / EBCI0	—

The data output (SDO1 and SDO0) channel clock and bit clock are selected by LROS1 and LROS0, and BCOS1 and BCOS0 of control register 2, respectively.
Tables 2. (a) and 2. (b) below provide details regarding the data output (SDO1 and SDO0) modes.

Table 2. (a) The (SDO1) data output channel clock and bit clock modes

CONTROL REGISTER 2 (CNT-R2)		DATA INPUT APPLICATIONS (SDO1)	
LROS1	BCOS1	CHANNEL CLOCK / BIT CLOCK	DATA BIT COUNT
0	0	Internally generated TGLR / TG32	16bit
0	1	Internally generated TGLR / TG64	32bit
1	X	External input ELRO1 / EBCO1	—

Table 2. (b) The (SDO0) data output channel clock and bit clock modes

CONTROL REGISTER 2 (CNT-R2)		DATA INPUT APPLICATIONS (SDO0)	
LROS0	BCOS0	CHANNEL CLOCK / BIT CLOCK	DATA BIT COUNT
0	0	Internally generated TGLR / TG32	16bit
0	1	Internally generated TGLR / TG64	32bit
1	X	External input ELRO0 / EBCO0	—

The LR and BCK terminals as well as the SDO2 channel clock and bit clock are selected from BCKS, TOS, and LROS2 of control register 2.
The data output (SDO2), LR, and BCK terminal output modes are shown in Table 3 below.

Table 3. LR and BCK terminal output, and (SDO2) data channel clock and bit clock modes

CONTROL REGISTER 2 (CNT-R2)			LR TERMINAL OUTPUT / BCKO TERMINAL OUTPUT	DATA OUTPUT (SDO2)
BCKS	TOS	LROS2	CHANNEL CLOCK / BIT CLOCK	
0	0	0	Internally generated TGLR / TG32	Internally generated TGLR / TG32
0	0	1	Internally generated TGLR / TG32	External input ELRO2 / EBCO2
0	1	0	External input ELRO2 / EBCO2	Internally generated TGLR / TG32
0	1	1	External input ELRO2 / EBCO2	External input ELRO2 / EBCO2
1	0	0	Internally generated TGLR / 1 / 2 frequency of EBCO2	Internally generated TGLR / 1 / 2 frequency of EBCO2
1	0	1	Internally generated TGLR / 1 / 2 frequency of EBCO2	External input ELRO2 / 1 / 2 frequency of EBCO2
1	1	0	External input ELRO2 / 1 / 2 frequency of EBCO2	Internally generated TGLR / 1 / 2 frequency of EBCO2
1	1	1	External input ELRO2 / 1 / 2 frequency of EBCO2	External input ELRO2 / 1 / 2 frequency of EBCO2

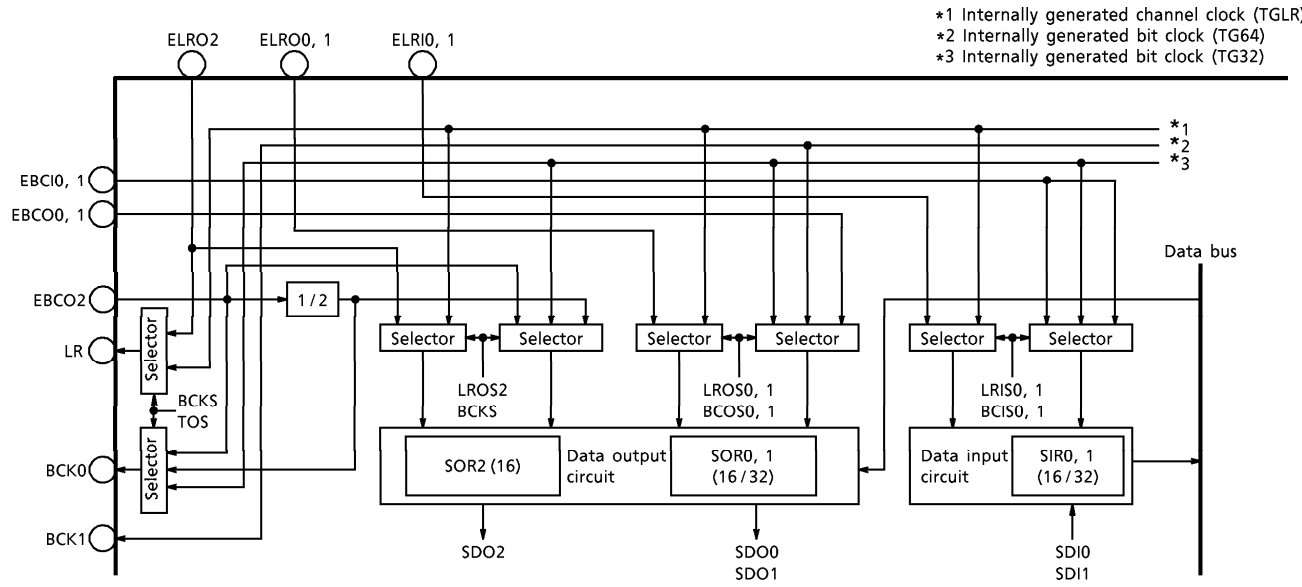


Fig.2 The data input / output clock selection circuit

2. The Data Input And Data Output Circuits

(1) Data Input Circuit

(1-1) Data input circuit

The input data is conveyed as a 2's complement expression and corresponds to the padding following the MSB first. The SIR1 and SIR0 input register can be selected for 16 or 32bit data count applications. The timing signals of the SDI1 and SDI0 input data can be input both independently and externally to the channel clock (LRCK) and bit clock (BCK). Note that internally generated modes are also available for the LRCK and BCK. The rising and falling of the LRCK trailing edge is first detected and then the input data is received internally.

(1-2) Data input format

- Refer to Figures 3 and 4 (a) when the input data is 16bit / ch.

  When the BCK is at least 32fs but not more than 64fs, the data is received later from the padding.

- When the input data is at least 17bit but not more than 32bit, refer to Figures 4 (b) and 4 (c).

  The input register should be set up for 32bit processing. As shown in Figures 4 (b) and 4 (c), data is put into the padding and the priority bit modified before inputting. In order to input data before it is put into the padding, the input register must be set for 32bit and, as shown in Figure 5, the remaining data must be reset to "zero".

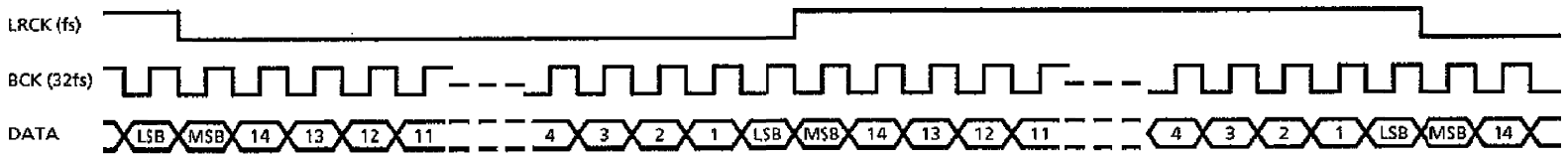


Fig.3 Serial data input timing (16bit)

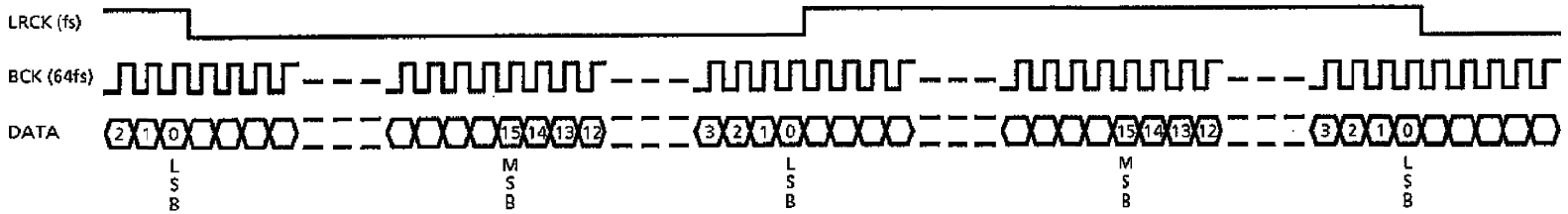


Fig.4 (a) Serial data input timing (32bit)

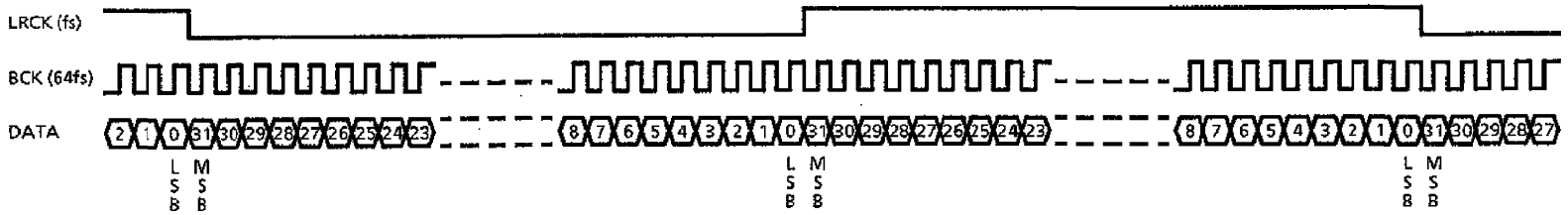


Fig.4 (b) Serial data input timing (32bit)

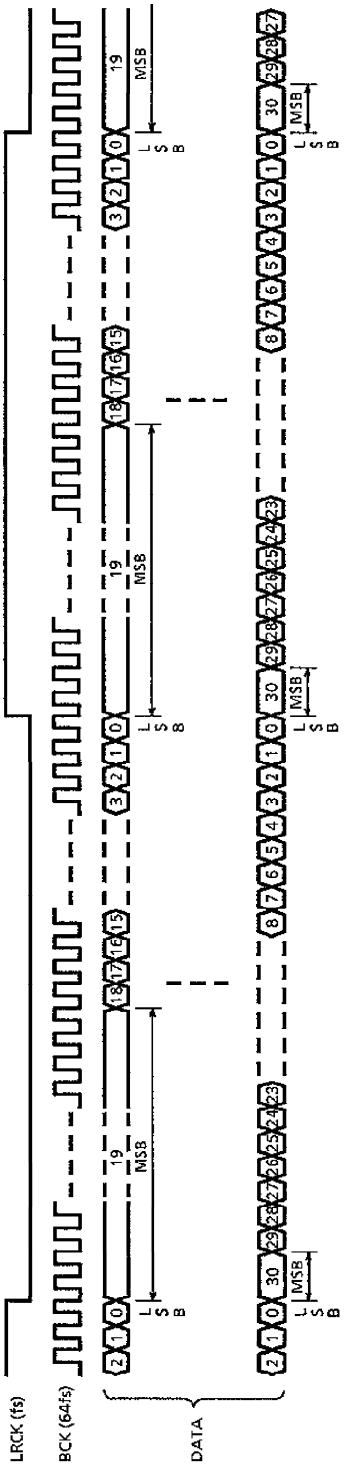


Fig.4 (c) Serial data input timing (32bit)

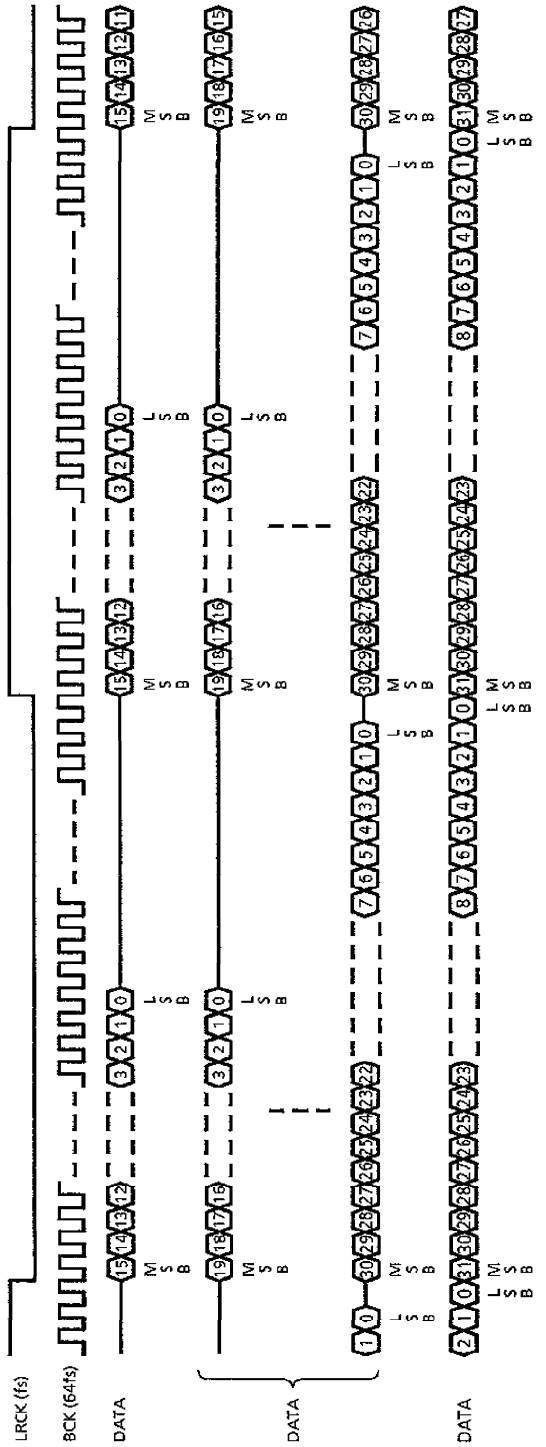


Fig.5 Serial data input timing (32bit)

TC9331F-11

(2) Data Output Circuit

(2-1) Data output circuit

The output data is conveyed as a 2's complement expression and is the pre-padded data of the MSB first. The SOR2 is a 16bit fixed register while the SOR1 and SOR0 can be selected as either 16bit or 32bit registers. The timing signals of the SDO2, SDO1 and SDO0 output data can be input both independently and externally to the channel clock (LRCK) and bit clock (BCK). Note that internally generated modes are also available for the LRCK and BCK. The rising and falling of the LRCK trailing edge is first detected and then the data is output to the PISO register.

(2-2) Data output format

The output data from the MSB database is either 16 or 32bit. When the BCK is equal to 32fs, the output data is in the format shown in Figure 6. When the BCK is 64fs, as shown in Figure 7(a), data past the 16th bit of SDO2 is first modified then output by the LSB. Note that the data past the 16th bit may also be modified and output by the secondary channel data LSB, depending on the program's processing content. When the BCK input (EBCO2) of the SDO2 is set to 64s, a clock may be set to one half the value in the BCK. In this instance, the output format will be as shown in Figure 6. The output formats for SDO1 and SDO0 are as shown in Figure 7(b). The output for the LR and BCK0 terminals can be selected for either internally generated signals or externally inputted signals. Consequently, the LR and BCK0 output can be used as A/D and D/A converter timing signals.

When the DIR (digital audio I/F receiver) is in use, the LR and BCK0 are set up to receive external input signals (ELRO2 and EBCO2) and to provide the D/A converter timing signals.

When the BCK of the DIR is 64fs, and an applicable BCK of 32fs is desired, the mode setting and BCK input are externally output from the BCK0 at 1/2 the clock rate. This BCK0 output can be used as a D/A converter timing signal by inputting the BCK0 output to the EBCO1 and EBCO0.

When an A/D converter is use, the internally generated signals are used as D/A converter timing signals.

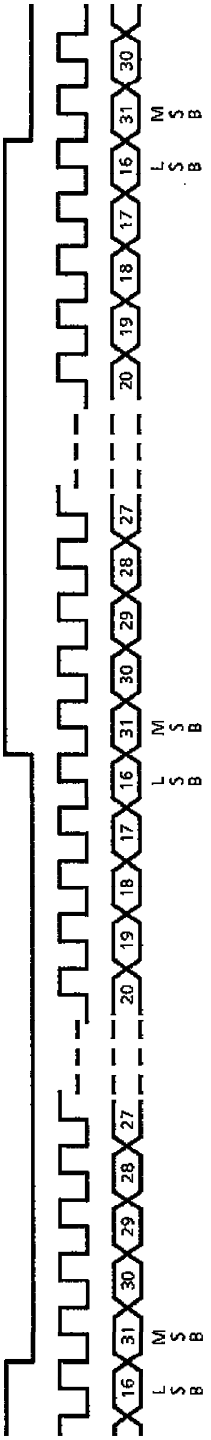


Fig.6 Serial data output timing (16bit)

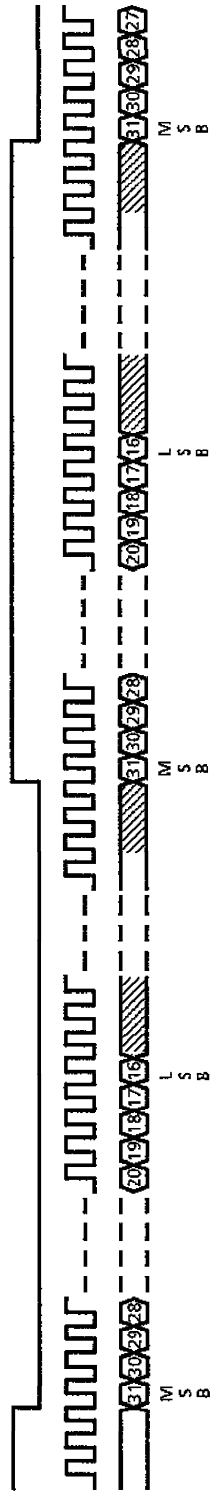


Fig.7 (a) Serial data output timing (32bit)

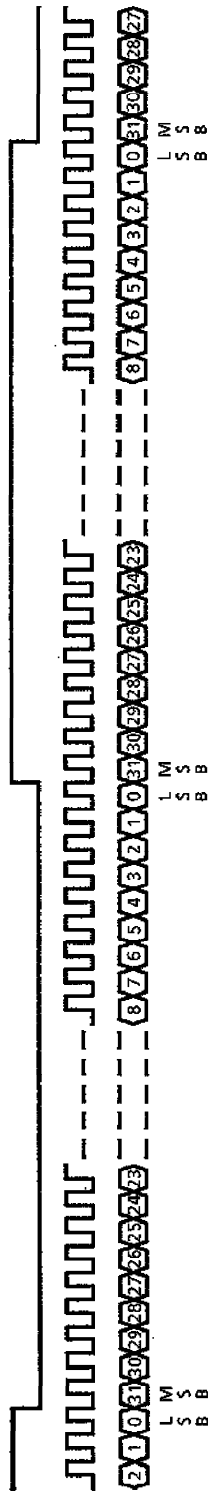


Fig.7 (b) Serial data output timing (32bit)

3. Microcomputer Interface Circuit

Through the $\overline{CS}$, IFCD, IFCK, IFDT, and ($\overline{ACK}$ and DCHK) terminals, the TC9331F transfers synchronized serial data between itself and the host microcomputer.

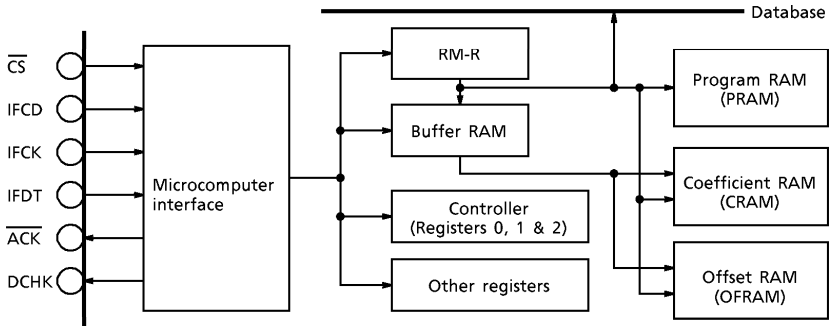


Fig.8 Microcomputer Interface Block Structure

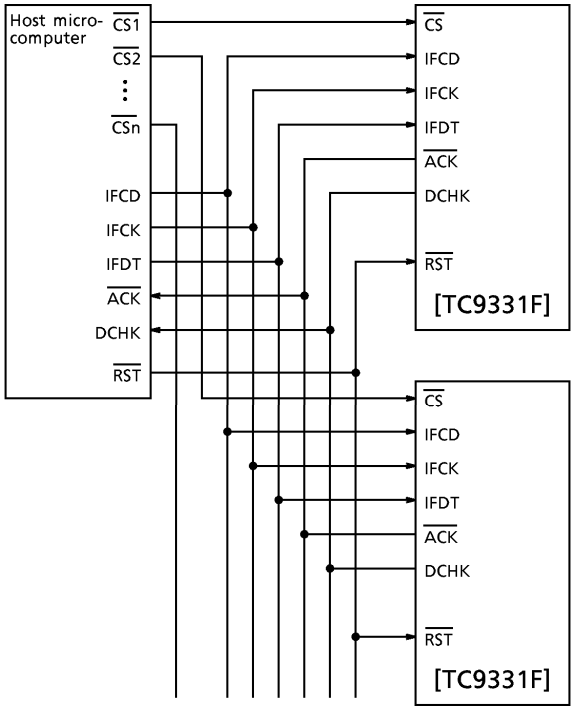


Fig.9 The relationship between the host microcomputer and the TC9331F

(1) Data Transfer Format

When idle, the $\overline{CS}$, IFCD, IFCK, and IFDT signals are set to "H". The standard unit of data transferred from the host microcomputer is an 8bit (1byte) unit to which an odd, 1bit parity has been added. However, when a parity check is not conducted, a dummy bit is substituted. There are two types of transfer data: single-byte command words and one to four-byte data words. The number of data word bytes depends on the command byte. The data is transferred from the LSB first and the dummy bit at the MSB end of the transferred data is set to "0". The microcomputer interface terminal signals and their functions are listed below.

$\overline{CS}$ signal (input)	: Activation signal for TC9331F data reception
IFCD signal (input)	: Signal used to differentiate command words from data words.
IFCK signal (input)	: Shift clock for the data signal.
IFDT signal (input)	: Data signal.
$\overline{ACK}$ signal (output)	: The acknowledge signal for the results of the parity check.
DCHK signal (output)	: Synchronizes the data signal with the TC9331F system clock and outputs the data at the rise of the IFCK trailing edge.

The host microcomputer is able to check for data transfer errors using the $\overline{ACK}$ and DCHK signals.
The 12 different (write) commands that may be used by the host microcomputer to control the TC9331F are listed in Table 4 below.

Table 4. Command Words

COMMAND WORD (HEX)	DATA WORD (EXCLUDE PARITY)		DATA IS WRITTEN TO THE FOLLOWING ADDRESS
	LENGTH OF BIT USED	TRANSFER BYTE LENGTH	
0F	15	2	CNT-R2
0E	8	1	CNT-R1
0D	8	1	CNT-R0
0C	9	2	STAD-R
0B	5	1	TXW-R
0A	32	4	PRAM
09	16	2	CRAM
08	16	2	OFRAM
07	32	4	RM-R
06	3	1	XINT-R
05	5	1	XRMD-R
04	9	2	BRKA-R
03 02 01 00	—	—	Not assigned

(2) The Control Register and the I/F Dedicated Register

(2-1) Control register 2 (CNT-R2)

(* = Default value)

BIT	SYMBOL	FUNCTION					
14	LRIS1	Selects the channel clock and bit clock for the audio serial data input from the SDI1 terminal.				0*	Internally generated
						1	Externally generated
13	BCIS1	Selects the bit count for the audio serial data input from the SDI1 terminal.				0*	16bit
						1	32bit
12	LRIS0	Selects the channel clock and bit clock for the audio serial data input from the SDI0 terminal.				0*	Internally generated
						1	Externally generated
11	BCIS0	Selects the bit count for the audio serial data input from the SDI0 terminal.				0*	16bit
						1	32bit
10	LROS2	Selects the channel clock and bit clock for the audio serial data output from the SDO2 terminal.				0*	Internally generated
						1	Externally input
9	LROS1	Selects the channel clock and bit clock for the audio serial data output from the SDO1 terminal.				0*	Internally generated
						1	Externally input
8	BCOS1	Selects the bit clock for the audio serial data output from the SDO1 terminal.				0*	16bit (TG32)
						1	32bit (TG64)
7	LROS0	Selects the channel clock and bit clock for the audio serial data output from the SDO0 terminal.				0*	Internally generated
						1	Externally input
6	BCOS0	Selects the bit clock for the audio serial data output from the SDO0 terminal.				0*	16bit (TG32)
						1	32bit (TG64)
5 4	BCKS TOS	Selects the mode for the SDO2 terminal bit clock output for the LR terminal and BCK terminal output.					
		BCKS	TOS	LR terminal output	BCK terminal output	SDO2 bit clock	
		0*	0*	Internally generated (TGLR)	Internally generated (TG32)	Selection made at LROS2	
		0	1	ELRO2 input signal	EBCO2 input signal	Selection made at LROS2	
		1	0	Internally generated (TGLR)	1/2 frequency of EBCO2 input signal	1/2 frequency of EBCO2 input signal	
		1	1	ELRO2 input signal	1/2 frequency of EBCO2 input signal	1/2 frequency of EBCO2 input signal	
3	SYNCS	Used to select either an internally generated or externally input (SYNC terminal) mode.				0*	Internally generated (TGLR)
						1	External input
2	SYNCP	Selects the SYNC signal polarity.				0*	Rise
						1	Fall
1	SYNCR1	Resets the coefficient pointer (CP) at each SYNC signal.				0*	Run
						1	Prohibit
0	SYNCR0	Resets the offset address pointer (OFP) at each SYNC signal.				0*	Run
						1	Prohibit

(2-2) Control register 1 (CNT-R1)

(* = Default value)

BIT	SYMBOL	FUNCTION		
7	PCMON	The program counter values are output at terminals IO15~IO7. (The external RAM is placed on standby.)	0*	Prohibit
			1	Run
6	ACMP	When the CRAM or OFRAM pointer values coincide with the rewrite counter address, data in both RAM are rewritten.	0*	Prohibit
			1	Run
5	CKSL	Selects the XI oscillation (input) clock frequency.	0*	XI = 640fs
			1	XI = 512fs
4	PS	Selects the externally attached RAM type (PSRAM or DRAM).	0*	PSRAM
			1	DRAM
3	—	Not assigned.	—	—
			—	—
2	DSL	Selects the internal DBUS data that will access the externally attached RAM source (high priority 16 / 32bit).	0*	High priority 16bit (DB16)
			1	32bit (DB32)
1	IOS	Selects an 8bit or a 16bit access mode for the external RAM source.	0*	16bit / access (IO16)
			1	8bit / access (IO8)
0	XSEP	Partitions the externally attached RAM into delay and data table domains.	0*	Prohibit
			1	Run

(2-3) Control register 0 (CNT- R0)

(* = Default value)

BIT	SYMBOL	FUNCTION		
7	PRGALL	The active switch is turned to the "on" position when the program is loaded. During this active state, instructions are placed in an NOP condition. When the switch is turned from the "on" position to the "off" position, the XINT and RMRF ignore flags are reset.	0*	On
			1	Off
6	BRKRQ	Once the program break address (BRKA) has been established, setting BRKRQ to "1" will activate the break.	0*	Off
			1	On
5	INMT	Sets the SDI0 and SDI1 terminal input to "0" mute.	0	Mute off
			1*	Mute on
4	OUTMT2	Sets the SDO2 terminal output to "0" mute.	0	Mute off
			1*	Mute on
3	OUTMT1	Sets the SDO1 terminal output to "0" mute.	0	Mute off
			1*	Mute on
2	OUTMT0	Sets the SDO0 terminal output to "0" mute.	0	Mute off
			1*	Mute on

(* = Default value)

BIT	SYMBOL	FUNCTION		
1	XCLR	Trigger bit that clears the externally attached RAM delay domain to "0". Once the clearing operation has been initiated, the bit is reset to a trigger "off" position (XCLR = 0).	0*	Trigger off
			1	Trigger on
0	XSTBY	Places the externally attached RAM on standby.	0	Standby off
			1*	Standby on

※ The CNT-RO data is latched via a SYNC signal.

(2-4) The I/F dedicated register

SYMBOL	FUNCTION
STAD	The STAD is a presentable up-counter used in setting the starting address for writing data and programs in the PRAM, CRAM, and OFRAM. (9bit)
TXW	The TXW register is responsible for setting the rewrite data count (max. 32 words) for the CRAM and OFRAM when ACMP is in the 1 (CNT-R1) mode. (5bit)
RMR	The RMR register temporarily retains data to be written to the PRAM, CRAM, OFRAM until it receives subsequent data (32bit). The RMR also acts as the source register for the data bus.
XINT	The XINT register sets up the IFF2~0, which act as conditional field flags. (3bit)
XRMD	The XRMD register sets the following: (1) In the XSEP mode, sets the domains for the delay and table data partitions in the externally attached RAM. (2) Sets the access frequency for the externally attached RAM. (3) Sets set to use or not use the×4bit 1M DRAM (5bit) to active or inactive.

※ The RMR and XINT data are latched via a SYNC signal.

(3) The Data Transmission Process.

When the $\overline{CS}$ signal is set to "L" or activated, data is transmitted in command word (1 byte) and data word (1 to 4 byte) sets. Somewhat similar to the program, coefficient, and offset address processes, the command word becomes unnecessary when data bits using the same command word are transmitted successively; only the data word needs to be transmitted. In these situations, the IFCD signal is set to "L" prior to the $\overline{CS}$ signal.

(4) The Internal RAM (PRAM, CRAM, OFRAM) Data Transmission Process

The STAD-R, which sets the starting address for the writing process, adds a +1 increment to the address after writing each data unit. The internal RAM units that can utilize the buffer RAM (32 words × 16bits) are the CRAM and OFRAM. For them to do so, the coefficient and offset addresses must be rewritten in successively increasing increments of +1. For example, the coefficient address of the secondary IIR in the equalizer must be successively arranged from 5 single-precision units to 10 multiple-precision units. The buffer RAM is used when altering the individual characteristics of the filter. These coefficients can be rewritten within a single sampling period.

Ex. Rewriting the offset data coefficient in the buffer RAM

When the targeted rewrite coefficient addresses are set at 30, 31, 32, 33, and 34, the following takes place.

When the targeted coefficient RAM addresses are arranged in succession, as shown in the example below, the buffer RAM can be rewritten.
. . . , 29, 30, 31, 32, 33, 34, 35, 36, . . . (or)
. . . , 29, 30, 36, 31, 32, 28, 29, 33, 34, 35, 36, . . .

When the targeted coefficient RAM addresses are randomly arranged, as shown in the example below, the buffer RAM cannot be rewritten.
. . . , 29, 30, 31, 34, 33, 32, 35, 36, . . .

- Setting up the data in the PRAM (Program RAM)
  - ① The write starting address is set in the STAD-R (command: 0CH).
  - ② An "0AH" command is transmitted and the PRAM write-to flag is triggered.
  - ③ Only the 32bit program code data is continued and the necessary steps are transmitted.
- Setting up the data in the CRAM (coefficient RAM) and OFRAM (offset RAM)
  - (a) The buffer RAM is not in use (The ACMP of the CNT-R1 is set to "0").
    - ① The write starting address is set in the STAD-R (command: 0CH).
    - ② An "09H" or "08H" command is transmitted and the CRAM or OFRAM write-to flag is triggered.
    - ③ Only the 16bit coefficient or offset data is continued and the necessary steps are transmitted.
  - (b) The buffer RAM is in use (the ACMP of the CNT-R1 is set to "1").
    - ① The write starting address is set in the STAD-R (command: 0CH).
    - ② The data coefficient-1 stored in the buffer RAM is set to the TXW-R.
    - ③ An "09H" or "08H" command is transmitted and the CRAM or OFRAM write-to flag is triggered.
    - ④ Only the 16bit coefficient or offset data is continued and the necessary steps are transmitted.

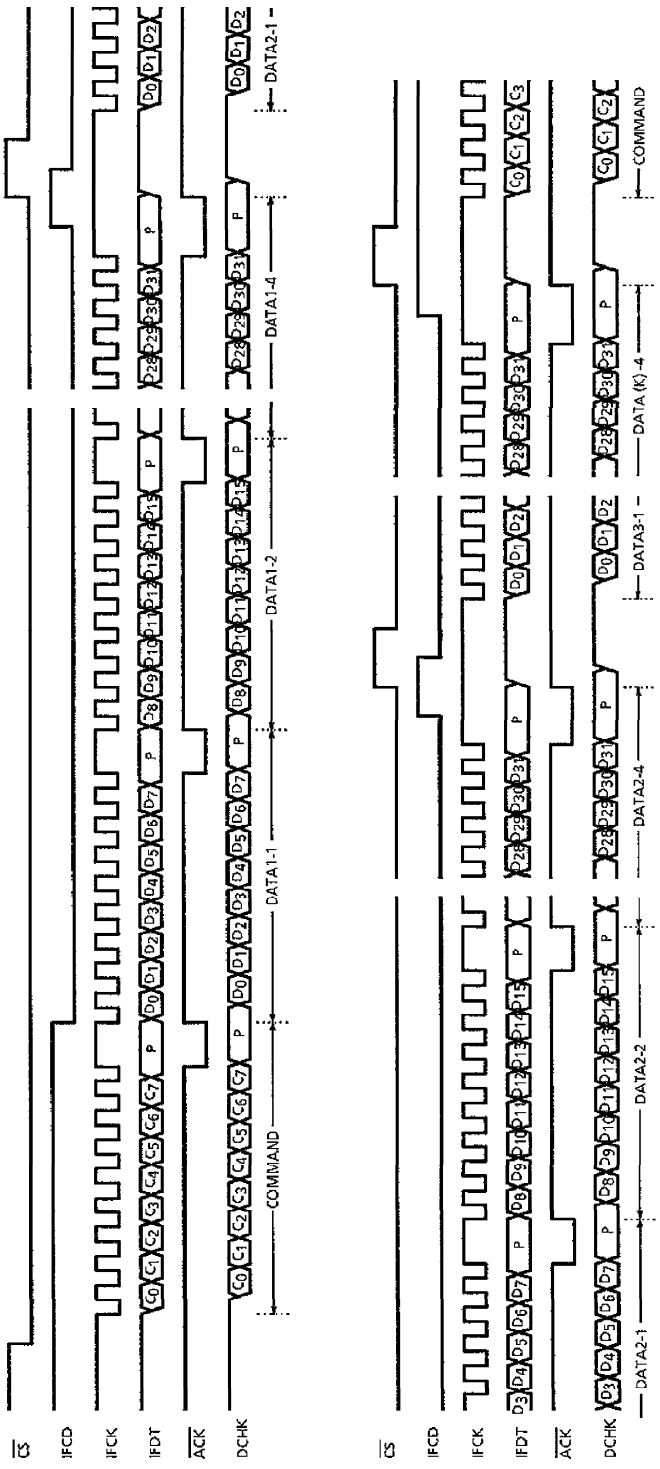
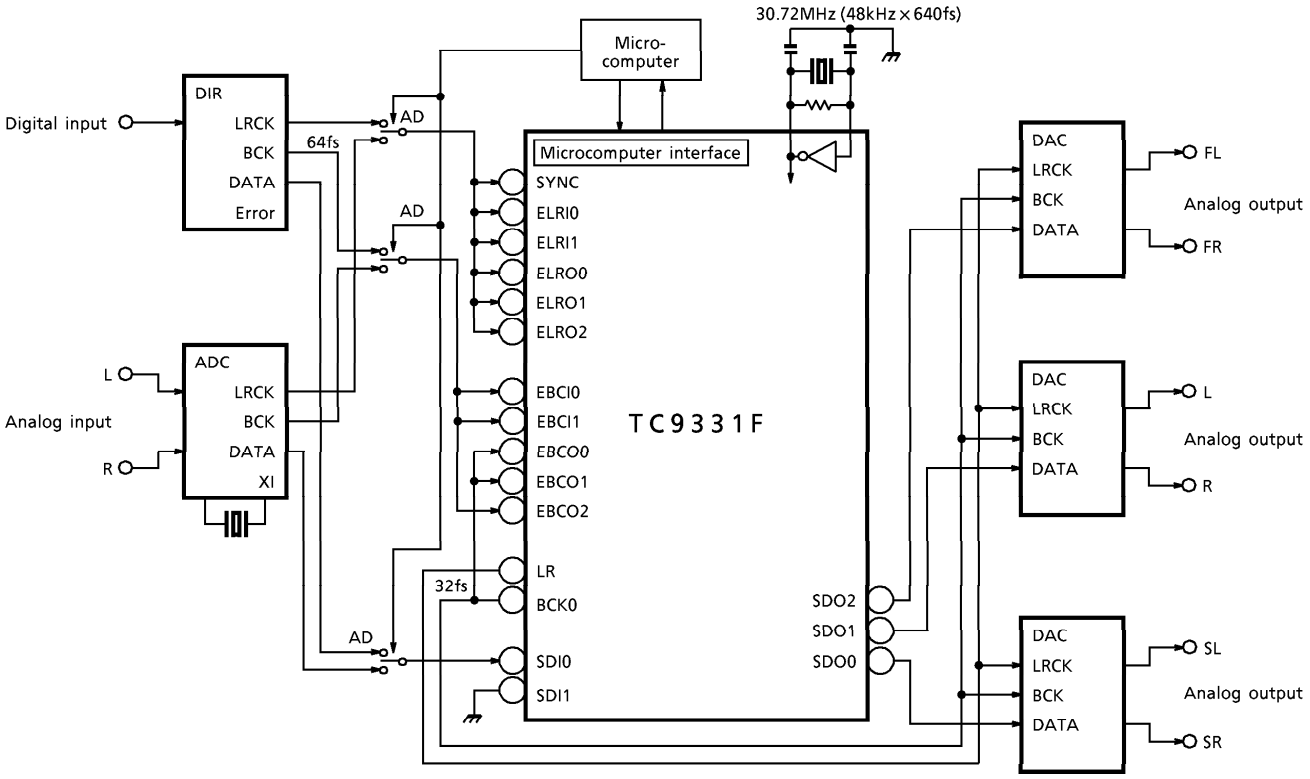


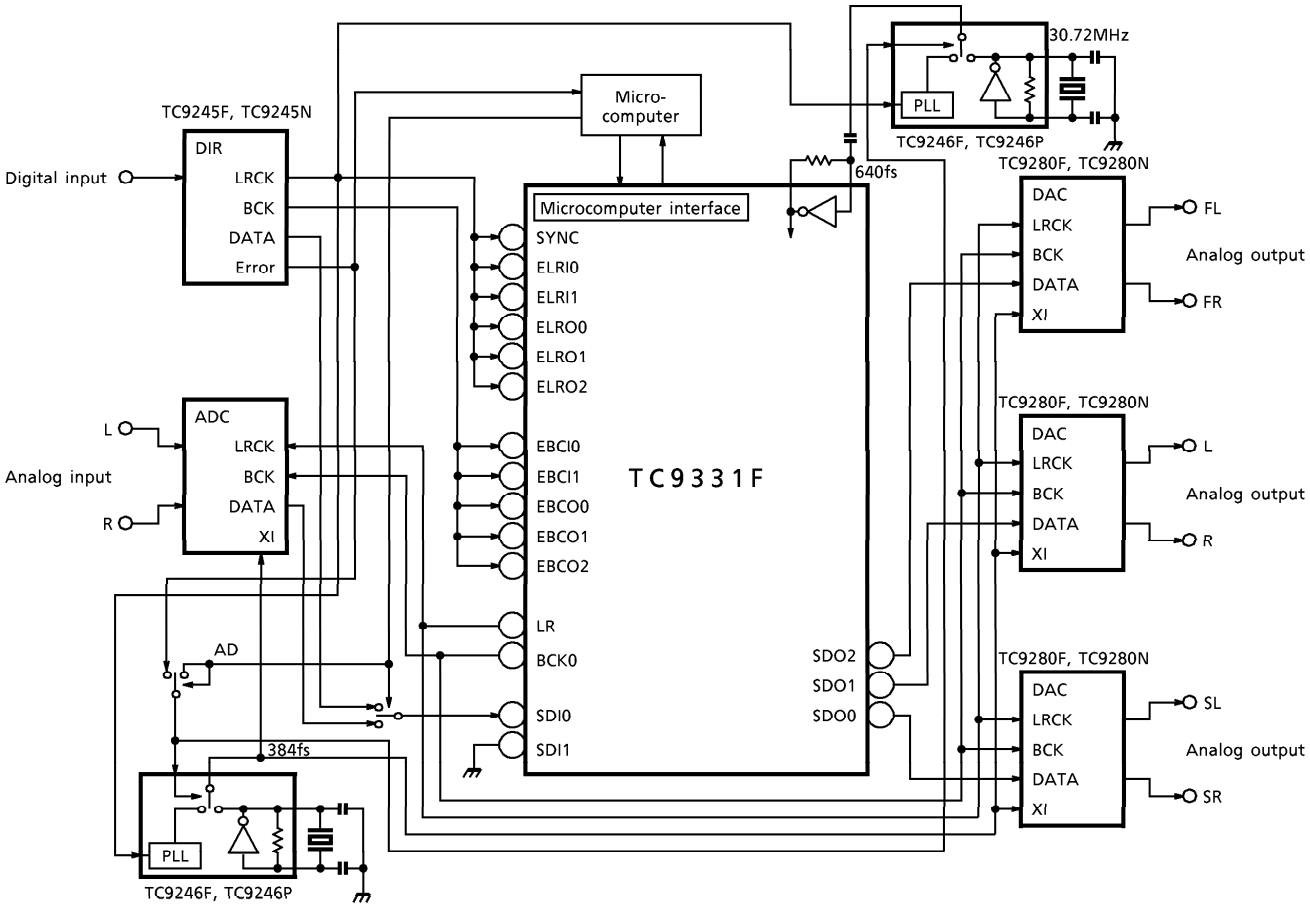
Fig.10 A sample of the microcomputer timing control

REGISTER	COMMAND WORD (HEX)	BIT LENGTH USED	TRANSMITTED BIT LENGTH
CNT-R2	0F	15	2
CNT-R1	0E	8	1
CNT-R0	0D	8	1
STAD-R	0C	9	2
TXW-R	0B	5	1
PRAM	0A	32	4
CRAM	09	16	2
OFRAM	08	16	2
RM-R	07	32	4
XINT-R	06	3	1
XRMD-R	05	5	1
BRKA-R	04	9	2

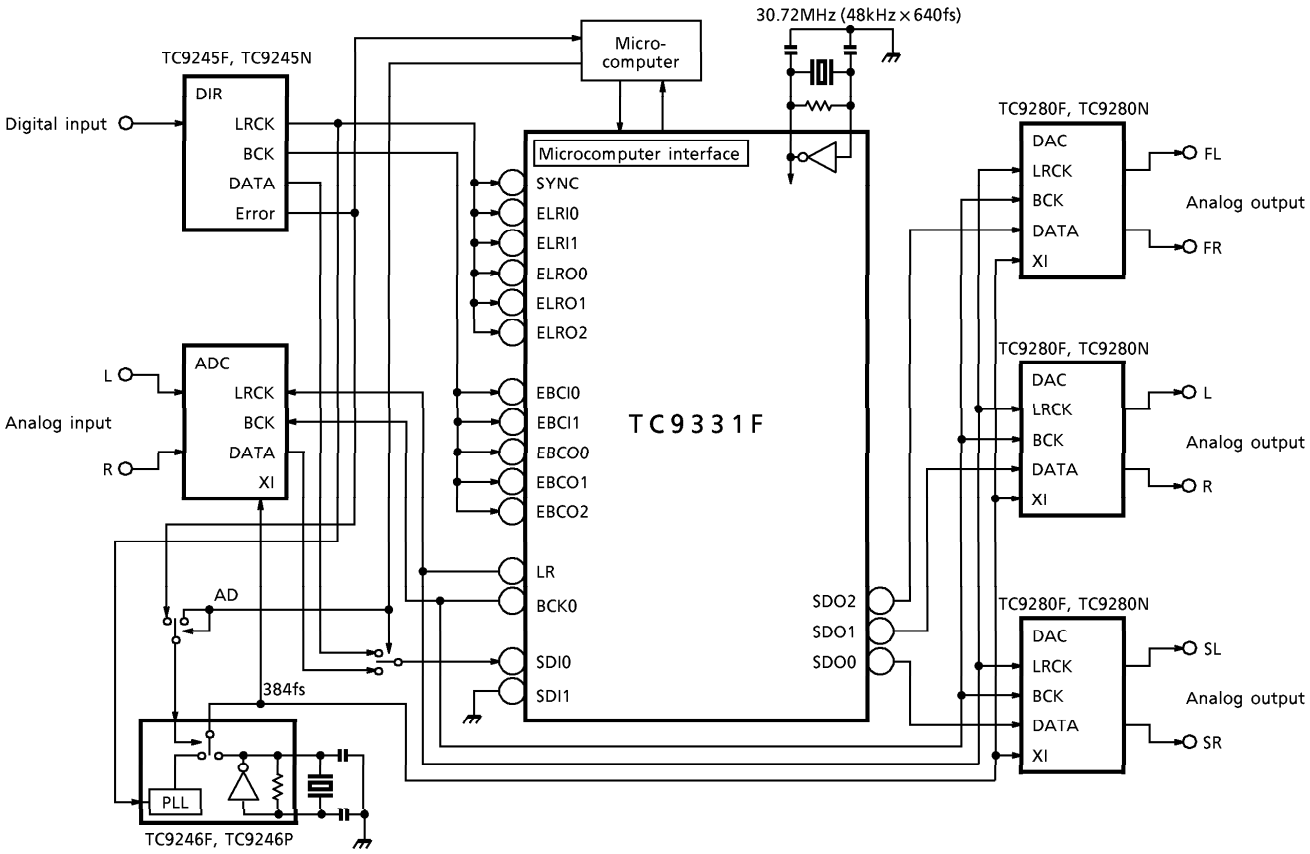
SYSTEM DESIGN, EXAMPLE 1.



SYSTEM DESIGN, EXAMPLE 2.



SYSTEM DESIGN, EXAMPLE 3.



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Source Voltage	V_{DD}	−0.3~6.0	V
Input Voltage	V_{IN}	−0.3~V_{DD} +0.3	V
Allowable Loss	P_D	1250	mW
Operating Temperature	T_{opr}	−35~85	°C
Storage Temperature	T_{stg}	−55~150	°C

ELECTRICAL CHARACTERISTICS (1) (Unless otherwise specified, Ta = 25°C, V_{DD} = 5V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Source Voltage	V_{DD}	—	Ta = −35~85°C	4.5	5.0	5.5	V
Operating Source Current (No-Load, During The Crystal Oscillation Period)	I_{DD}	—	f_{opr} = 30.72MHz (48kHz × 640fs)	—	60	100	mA
			f_{opr} = 24.576MHz (48kHz × 512fs)	—	50	90	
Operating Frequency Range	f_{opr}	—	—	4.0	—	32.0	MHz

CLOCK TERMINALS (XI, XO)

Input Voltage	"H" Level	V_{IH1}	—	XI terminal		3.5	—	—	V
	"L" Level	V_{IL1}	—			—	—	1.5	
Output Voltage	"H" Level	V_{OH1}	—	I_{OH} = −2.5mA	XO terminal	2.4	—	—	
	"L" Level	V_{OL1}	—	I_{OL} = 2.5mA		—	—	0.4	

INPUT TERMINAL

Input Voltage	"H" Level	V_{IH2}	—	(*1)		3.5	—	—	V
	"L" Level	V_{IL2}	—			—	—	1.5	
Threshold Voltage	"H" Level	V_P	—	(*2)		—	2.7	—	
	"L" Level	V_N	—			—	1.6	—	
Input Leakage Current	"H" Level	I_{IH1}	—	$V_{IN} = V_{DD}$	(*1, 2)	—	—	1.0	μA
	"L" Level	I_{IL1}	—	V_{IN} = 0V		−1.0	—	—	

(*1) ELRI0~1, ELRO0~2, EBCI0~1, EBCO0~2, SDI0~1, TES0~2
(*2) SYNC, $\overline{RST}$, $\overline{HALT}$, PEN, $\overline{CS}$, IFCD, IFCK, IFDT (Schmidt input terminal)

ELECTRICAL CHARACTERISTICS (2) (Unless otherwise specified, Ta = 25°C, V_{DD} = 5V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT

OUTPUT TERMINAL

Output Voltage	"H" Level	V_{OH2}	—	I_{OH} = −1mA	(*3)	2.4	—	—	V
	"L" Level	V_{OL2}	—	I_{OL} = 1mA		—	—	0.4	
Output Voltage	"H" Level	V_{OH3}	—	I_{OH} = −2mA	(*4)	2.4	—	—	
	"L" Level	V_{OL3}	—	I_{OL} = 2mA		—	—	0.4	

(*3) LR, WCK, BCK0~1, SDO0~2
(*4) A0~A15, RC0~RC3

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
THREE STATE INPUT / OUTPUT TERMINAL (IO0 - IO15)								
Input Voltage	"H" Level	V_{IH4}	—	—	3.5	—	—	V
	"L" Level	V_{IL4}	—	—	—	—	1.5	
Output Voltage	"H" Level	V_{OH4}	—	I_{OH} = −2mA	2.4	—	—	
	"L" Level	V_{OL4}	—	I_{OL} = 2mA	—	—	0.4	
Output "Off" Leakage Current	"H" Level	I_{OFH}	—	$V_{OH} = V_{DD}$	—	—	5.0	μA
	"L" Level	I_{OFL}	—	V_{OL} = 0V	−5.0	—	—	
OPEN DRAIN OUTPUT TERMINAL ($\overline{OVF}$, $\overline{ACK}$, DCHK)								
"L" Level Output Voltage		V_{OL5}	—	I_{OL} = 1mA	—	—	0.4	V
Output Open Leakage Current		I_{OF}	—	$V_{OH} = V_{DD}$	—	—	5.0	μA
PULL-UP TERMINAL								
Pull-Up Resistor		RUP	—	(*5)	—	100	—	kΩ

(*5) IO0~IO15, $\overline{RST}$, $\overline{HALT}$, $\overline{OVF}$, PEN, $\overline{ACK}$, DCHK

AC CHARACTERISTICS (1) (Unless otherwise specified, Ta = 25°C, V_{DD} = 5V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
EXTERNAL CLOCK INPUT TERMINAL (XI)							
XI Clock Periodicity	t_{XI}	—	—	32	36	250	ns
XI Clock "H" Period Length	t_{XIH}	—	—	16	18	125	
XI Clock "L" Period Length	t_{XIL}	—	—	16	18	125	
Reset Terminal ($\overline{RST}$)							
Stand-By Time	t_{ST}	—	—	500	—	—	μs
Reset Pulse Length	t_{RS}	—	—	10	—	—	μs

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
AUDIO SERIAL INTERFACE							
XI-BCK1 Transfer Time (1)	t_{CK1}	—	C_L = 10pF	—	25	—	ns
XI-BCK1 Transfer Time (2)	t_{CK2}	—	C_L = 10pF	—	25	—	
XI-BCK0 Transfer Time (1)	t_{CK3}	—	C_L = 10pF	—	25	—	
XI-BCK0 Transfer Time (2)	t_{CK4}	—	C_L = 10pF	—	25	—	
BCK0-WCK Transfer Time (1)	t_{CK5}	—	C_L = 10pF	—	5	—	
BCK0-WCK Transfer Time (2)	t_{CK6}	—	C_L = 10pF	—	5	—	
BCK0-LR Transfer Time (1)	t_{CK7}	—	C_L = 10pF	—	5	—	
BCK0-LR Transfer Time (2)	t_{CK8}	—	C_L = 10pF	—	5	—	
LR-SDO Lag Time (1)	t_{SO1}	—	C_L = 10pF	0	—	40	
BCKO-SDO Transfer Time	t_{SO2}	—	C_L = 10pF	0	—	40	
ELRI-EBCI Lag Time	t_{EB1}	—	C_L = 10pF	−55	—	55	
ELRO-EBCO Lag Time	t_{EB2}	—	C_L = 10pF	−55	—	55	
EBCI/O Clock Period	t_{EBC}	—	C_L = 10pF	—	350	—	
EBCI/O Clock "H" Period Length	t_{EBH}	—	C_L = 10pF	100	—	—	
EBCI/O Clock "L" Period Length	t_{EBL}	—	C_L = 10pF	100	—	—	
SDI Data Set Up Time	t_{SIS}	—	C_L = 10pF	100	—	—	
SDI Data Holding Time	t_{SIH}	—	C_L = 10pF	100	—	—	

AC CHARACTERISTICS (2) (Unless otherwise specified, Ta = 25°C, V_{DD} = 5V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
EXTERNAL RAM INTERFACE							
Read/Write Cycling Time	t_{RC}	—	XI = 30.72MHz C_L = 20pF	170	330	—	ns
$\overline{RAS}$ Pulse Length	t_{RAS}	—	XI = 30.72MHz C_L = 20pF	100	200	—	
$\overline{RAS}$ Precharging Time	t_{RP}	—	XI = 30.72MHz C_L = 20pF	60	130	—	
$\overline{CAS}$-$\overline{RAS}$ Precharging Time	t_{CRP}	—	XI = 30.72MHz C_L = 20pF	5	60	—	
$\overline{CAS}$ Holding Time	t_{CSH}	—	XI = 30.72MHz C_L = 20pF	100	260	—	

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$\overline{RAS}$ Holding Time	t_{RSH}	—	XI = 30.72MHz C_L = 20pF	40	130	—	ns
$\overline{CAS}$ Pulse Length	t_{CAS}	—	XI = 30.72MHz C_L = 20pF	40	190	—	
Low Address Setup Time	t_{ASR}	—	XI = 30.72MHz C_L = 20pF	0	60	—	
Low Address Holding Time	t_{RAH}	—	XI = 30.72MHz C_L = 20pF	10	30	—	
Column Address Setup Time	t_{ASC}	—	XI = 30.72MHz C_L = 20pF	0	30	—	
Column Address Holding Time	t_{CAH}	—	XI = 30.72MHz C_L = 20pF	15	190	—	
$\overline{CE}$ Address Setup Time	t_{ASE}	—	XI = 30.72MHz C_L = 20pF	0	60	—	
$\overline{CE}$ Holding Time	t_{AHC}	—	XI = 30.72MHz C_L = 20pF	30	260	—	
$\overline{RAS}$ Holding Time ($\overline{OE}$ Standard)	t_{ROH}	—	XI = 30.72MHz C_L = 20pF	20	130	—	
$\overline{OE}$ Pulse Length	t_{OE}	—	XI = 30.72MHz C_L = 20pF	—	190	—	
Write Command Pulse Length	t_{WP}	—	XI = 30.72MHz C_L = 20pF	15	190	—	
Write Command Holding Time	t_{WCH}	—	XI = 30.72MHz C_L = 20pF	15	130	—	
Data Input Setup Time	t_{DS}	—	XI = 30.72MHz C_L = 20pF	0	30	—	
Data Input Holding Time	t_{DH}	—	XI = 30.72MHz C_L = 20pF	15	290	—	

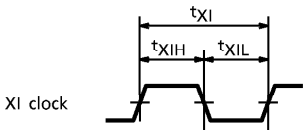
AC CHARACTERISTICS (3) (Unless otherwise specified, Ta = 25°C, V_{DD} = 5V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
MICROCOMPUTER INTERFACE							
$\overline{CS}$-IFCK Delay Time	t_1	—	C_L = 10pF	2.0	2.5	—	μs
I/F Clock Periodity	t_2	—	C_L = 10pF	4.0	5.0	—	
I/F Clock "L" Period Length	t_3	—	C_L = 10pF	2.0	2.5	—	
I/F Clock "H" Period Length	t_4	—	C_L = 10pF	2.0	2.5	—	
CHK Data Transfer Time	t_5	—	C_L = 10pF	—	0.5	—	
IFDT Data Setup Time	t_6	—	C_L = 10pF	0.5	1.0	—	
$\overline{ACK}$ Transfer Time (1)	t_7	—	C_L = 10pF	—	—	0.5	
$\overline{ACK}$ Transfer Time (2)	t_8	—	C_L = 10pF	—	—	0.5	
IFCD-IFCK Delay Time	t_9	—	C_L = 10pF	0.0	—	—	
IFCK-IFCD Delay Time	t_{10}	—	C_L = 10pF	0.5	1.0	—	
IFCD-$\overline{CS}$ Delay Time	t_{11}	—	C_L = 10pF	2.0	2.5	—	
IFDT-"H" Level Transition Time	t_{12}	—	C_L = 10pF	0.0	—	—	
$\overline{CS}$-DCHK Transfer Time	t_{13}	—	C_L = 10pF	—	—	0.5	
$\overline{CS}$-$\overline{ACK}$ Transfer Time	t_{14}	—	C_L = 10pF	—	—	0.5	
IFCD-CS Transfer Time	t_{15}	—	C_L = 10pF	2.0	2.5	—	
Rising Time (tr) Falling Time (tf)	t_{r1}	—	LR, WCK, BCK0 BCK1, SDO0~SDO2 C_L = 10pF	—	—	20	ns
	t_{f1}	—		—	—	10	
	t_{r2}	—	A0~A15, IO0~IO15 RC0~RC3 C_L = 20pF	—	—	20	
	t_{f2}	—		—	—	10	
	t_{r3}	—	$\overline{OVF}$, $\overline{ACK}$, DCHK C_L = 10pF	—	—	5	
	t_{f3}	—		—	—	60	

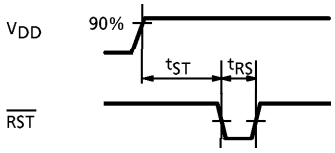
CAUTION! An AC timing measurement of (VIH, VIL) (VOH, VOL) has been used as a standard.

AC Special Measurement Points

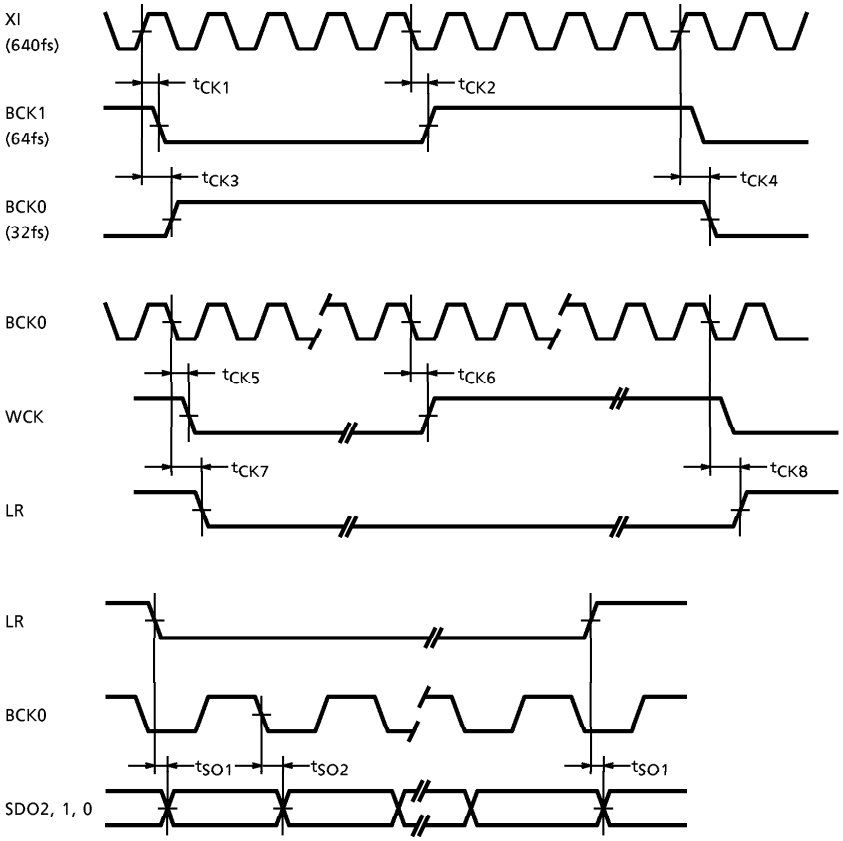
(1) External clock input terminal

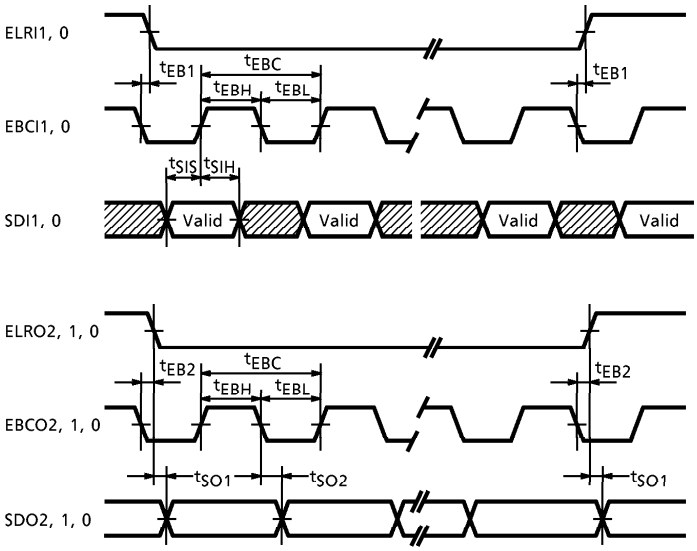


(2) Reset terminal



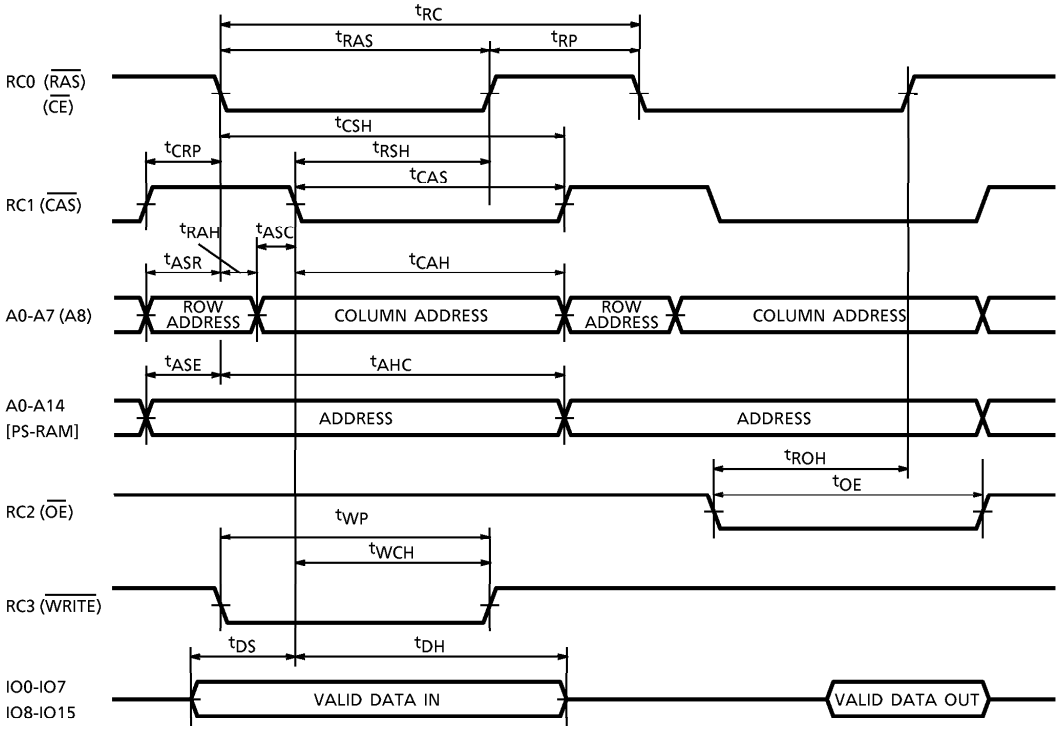
(3) Audio serial interface



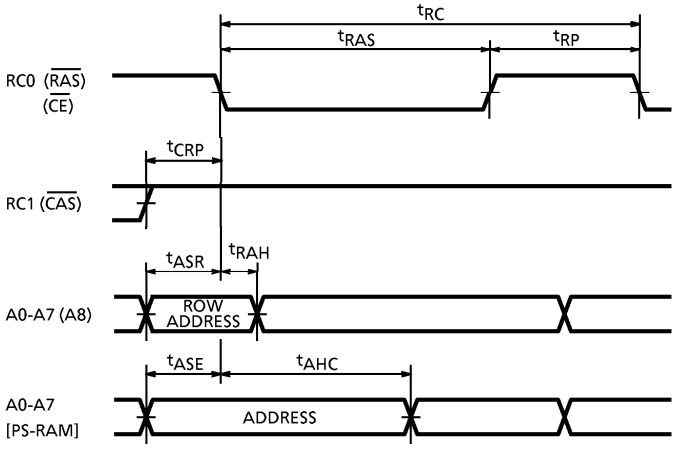


(4) External RAM interface

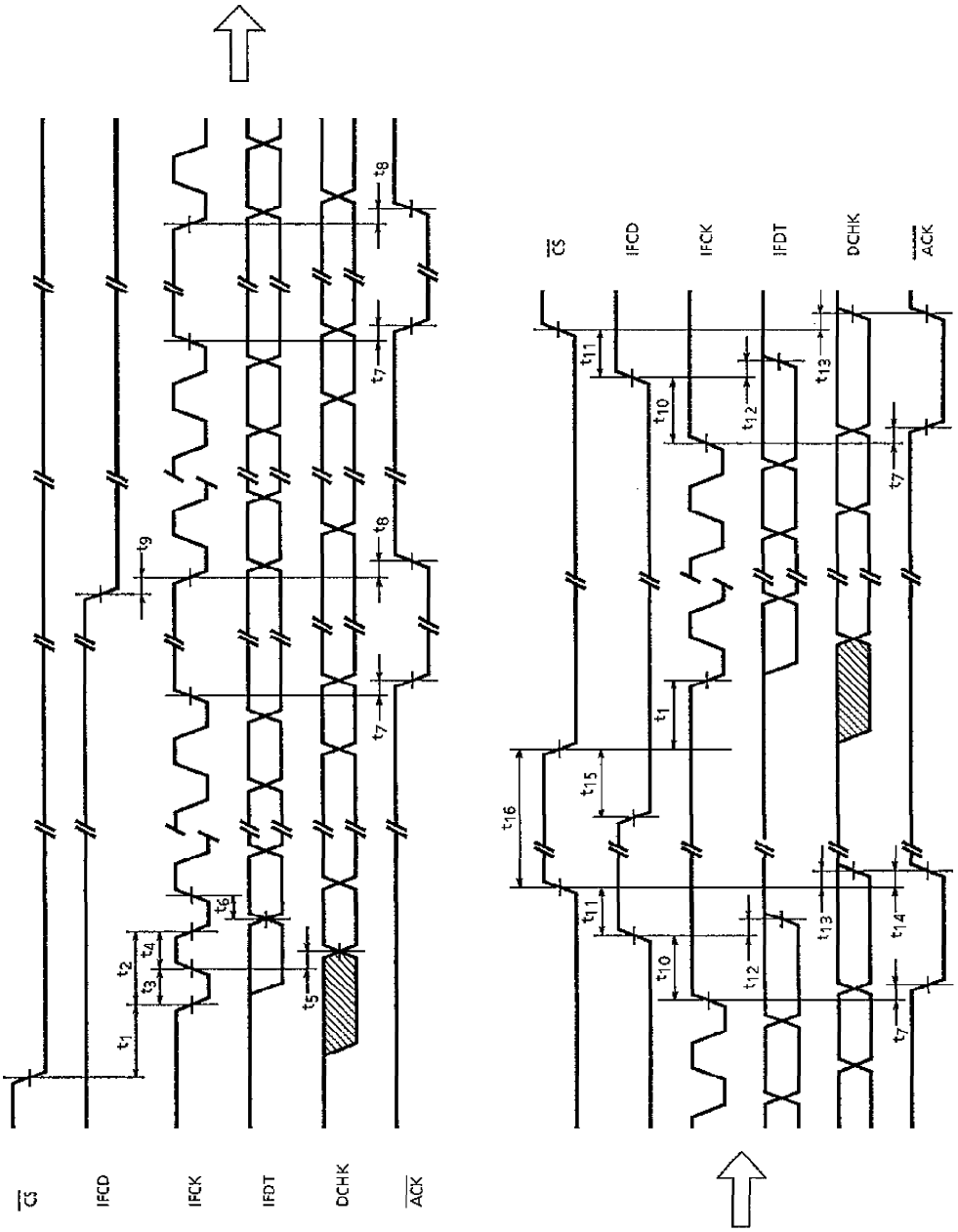
① READ / WRITE CYCLE TIMING



② RAS ($\overline{CE}$) REFRESH CYCLE TIMING ONLY



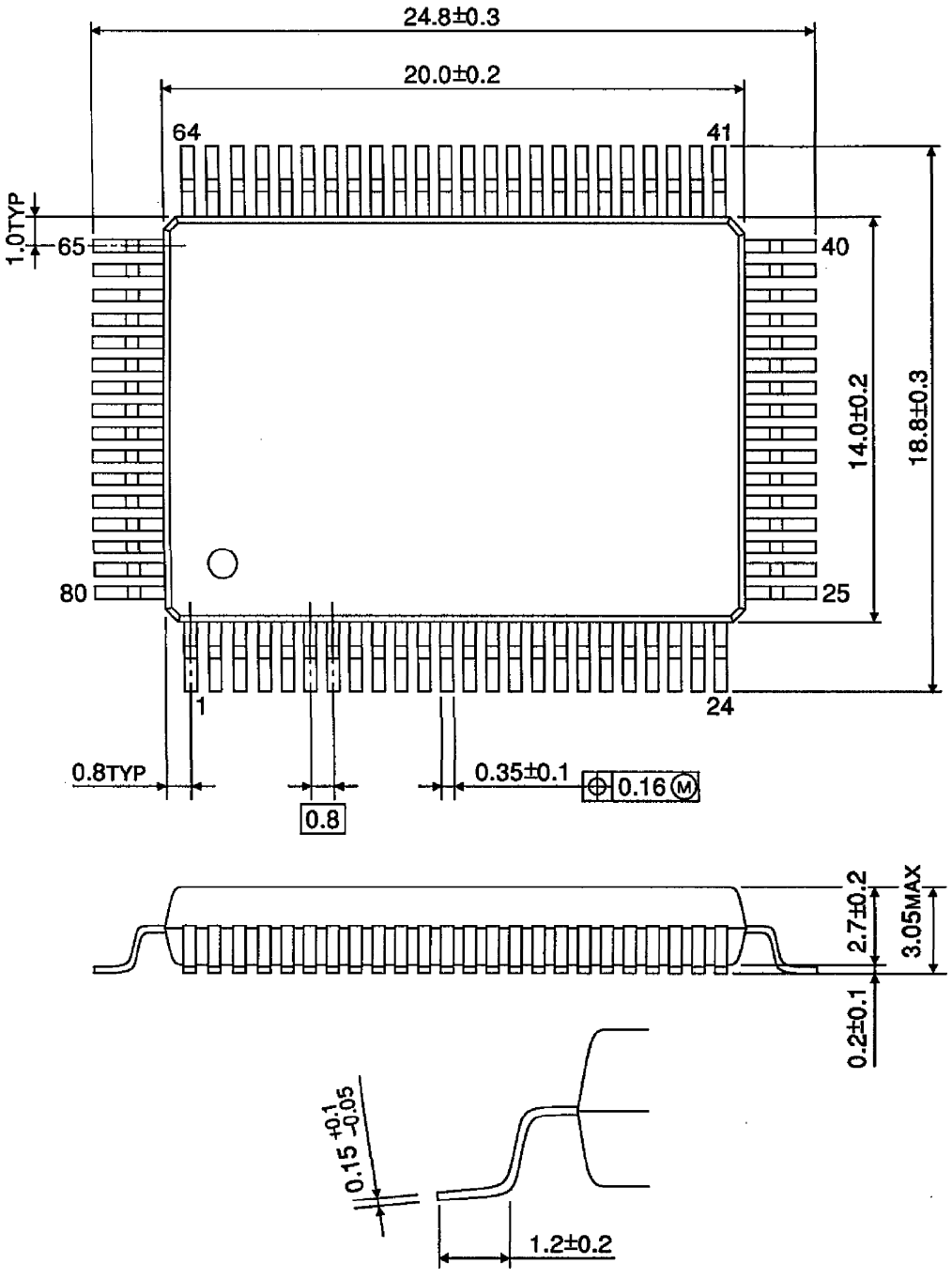
(5) MICROCOMPUTER INTERFACE



TC9331F-32

OUTLINE DRAWING

QFP80-P-1420-0.80A Unit : mm



Weight : 1.57g (Typ.)