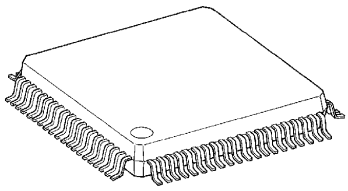
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9327F

DTS MICROCONTROLLER (DTS-21)

The TC9327F is a 4-bit CMOS microcontroller for single-chip digital tuning systems, featuring a built-in 230-MHz prescaler, PLL, and LCD drivers.
The CPU has 4-bit parallel addition and subtraction instructions (e.g., AI, SI), logic operation instructions (e.g., OR, AN), composite decision and comparison instructions (e.g., TM, SL), and time-base functions.
The package is an 80-pin, 0.5mm-pitch compact package.
In addition to various input / output ports and a dedicated key-input port, which are controlled by powerful input / output instructions (IN1 to 3, OUT1 to 3), there are many dedicated LCD pins, a PWM output port, a BUZR port, a 6-bit A / D converter, a serial interface, and an IF counter, etc.
Low-voltage and low-current consumption make this microcontroller suitable for portable DTS equipment.



LQFP80-P-1212-0.50A

Weight : 0.45g (Typ.)

FEATURES

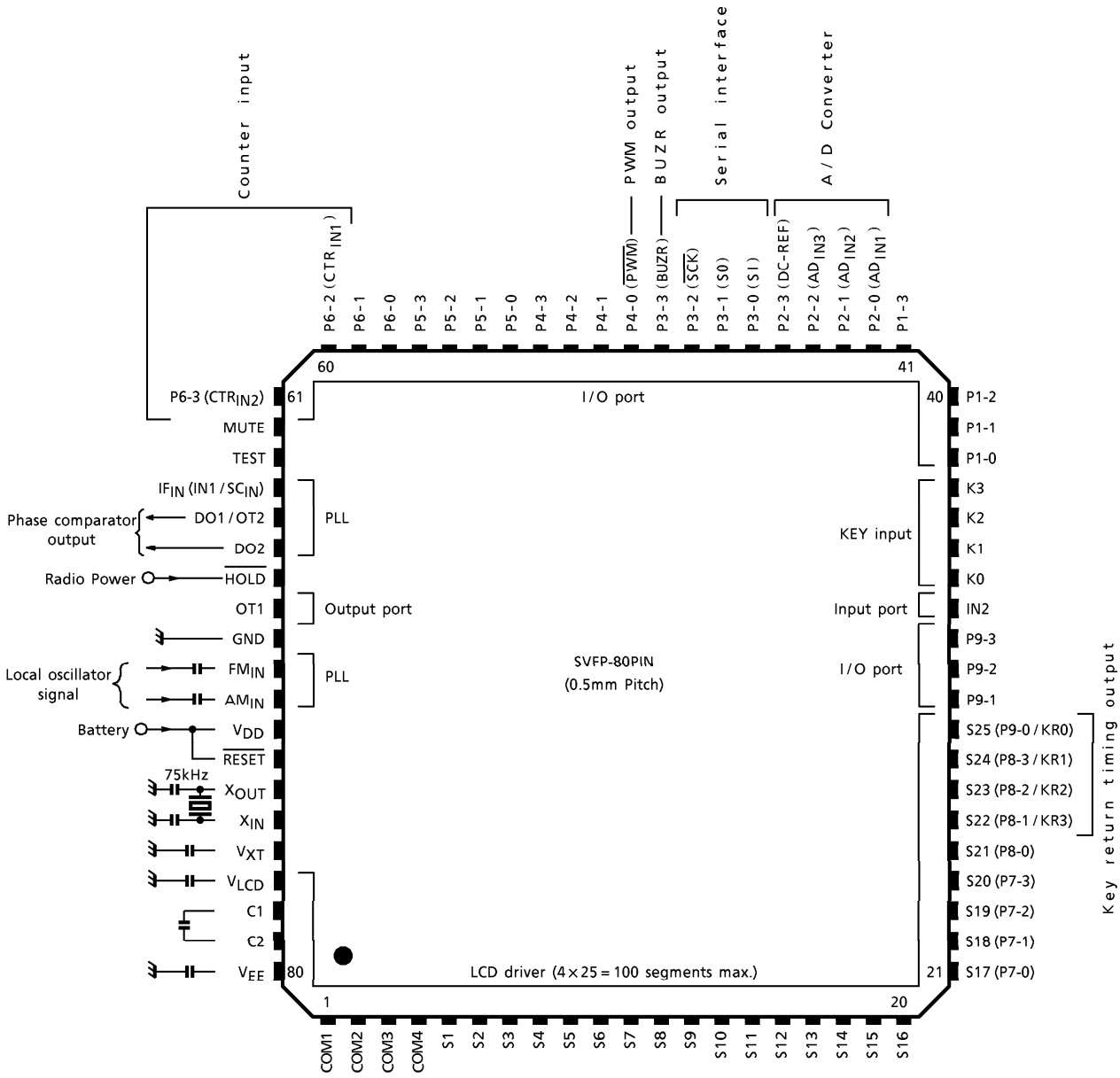
- 4-bit microcontroller for single-chip digital tuning systems.
- Operating voltage V_{DD} = 1.8 to 3.6V, with low current consumption due to CMOS circuitry (with only the CPU operating when V_{DD} = 3V, I_{DD} = 100μA Max.)
- Built-in prescaler (1 / 2 fixed divider + 2 modulus prescaler : fmax$\geqq$230MHz)
- Features built-in 1 / 4-duty, 1 / 2-bias LCD drivers and a built-in 3V booster circuit for the display.
- Data memory (RAM) and ports are easily backed up.
- Program memory (ROM) : 16bit × 7168 steps
- Data memory (RAM) : 4bit × 256 words

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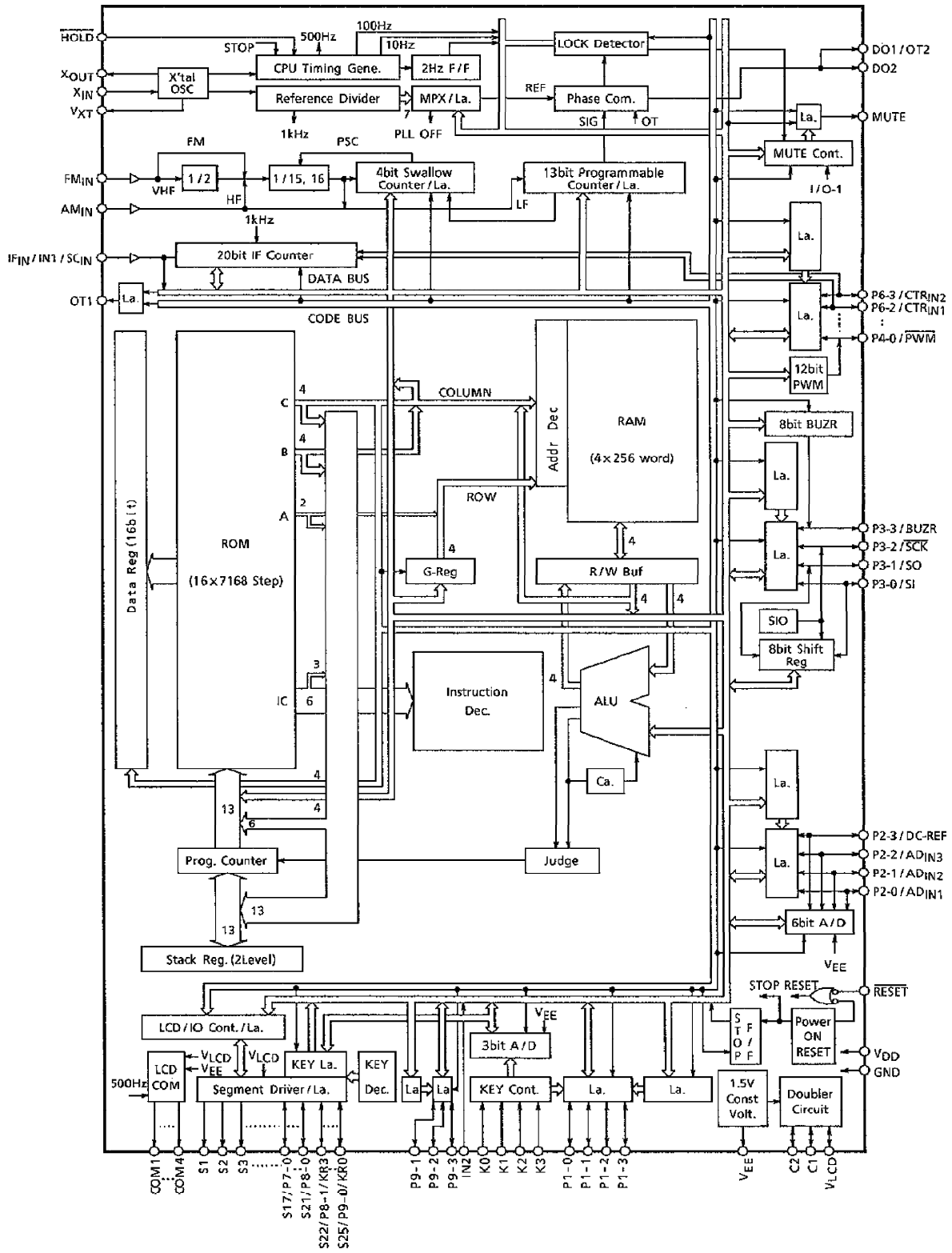
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- 62-instruction set (all one-word instructions)
- Instruction execution time : 40μs (with 75-kHz crystal) (MVGS, DAL instructions : 80μs)
- Many addition and subtraction instructions (12 types each addition and subtraction)
- Powerful composite decision instructions (TMTR, TMFR, TMT, TMF, TMTN, TMFN)
- Data can be transmitted between addresses on the same row.
- Register indirect transfer available (MVGD, MVGS instructions).
- 16 powerful general registers (located in RAM)
- Stack levels : 2
- Free branching (JUMP instructions) is allowed in the 7168 steps of program memory (ROM) as there are no pages or fields.
- 16 bits of any address in the 1024 program memory steps (ROM) can be referenced (DAL instructions).
- Features independent frequency input pins (FM_{IN} and AM_{IN}) and two (DO1 and DO2) phase comparator outputs for FM / VHF and AM.
- Seven kinds of reference frequencies can be selected via software.
- Powerful input / output instructions (IN1 to 3, OUT1 to 3).
- Dedicated input ports (K0 to K3) for key input, 29 LCD drive pins (100 segments maximum) available.
- 29 I / O ports : 27 input / output programmable in 1-bit units, 1 output-only port, and 1 input-only port. The 2 IF_{IN}, and DO1 pins can be switched by instruction to IN1 (input-only) or OT2 (output-only). In addition, 9 output LCD output pins for S17 to S25 can be switched to I / O port in 1-bit units.
- Three backup modes available by instruction : only CPU operation, crystal oscillation only, clock stop.
- Features a built-in 2-Hz timer F / F and a built-in 10 / 100Hz interval pulse outputs (internal port for time base).
- Allows PLL lock status detection.
- Four of the LCD segment outputs (S22 to S25) can also operate as key return timing outputs (KR0 to KR3). The I / O ports are not dedicated for key return timing outputs but can have other uses as well.
- Built-in 20-bit, general-purpose IF counters can detect stations during auto-tuning by counting the intermediate frequencies of each band.
- Built-in buzzer output circuit can output 8 kinds of frequencies in 4 modes : continuous output, single-shot output, 10-Hz intermittent output, and 10-Hz intermittent 1-Hz interval output.
- Features built-in 12-bit PWM circuit usable for easy-to-use D / A converter.
- Features a built-in 3-channel, 6-bit A / D converter.
- To prevent CPU malfunction, a built-in supply voltage drop detection circuit shuts down the CPU when the voltage falls below 1.55V.

PIN-ASSIGNMENT

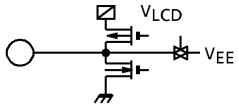
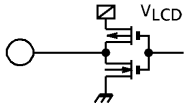
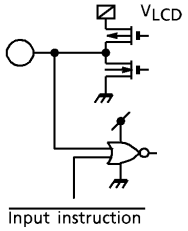
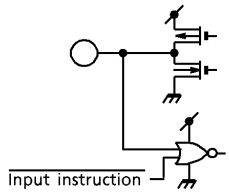
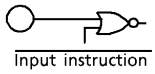


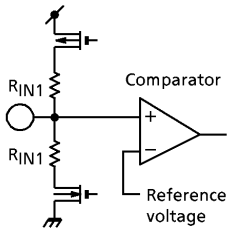
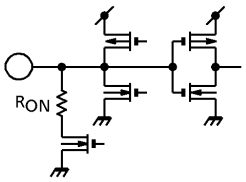
BLOCK DIAGRAM

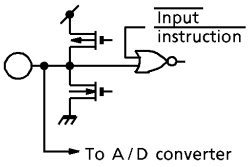


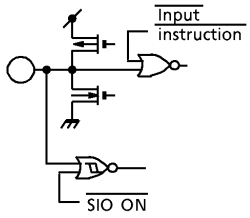
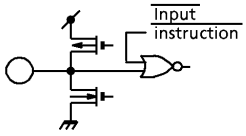
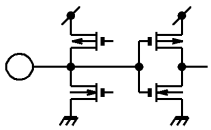
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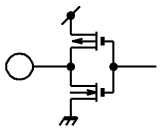
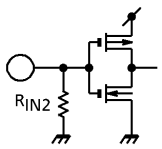
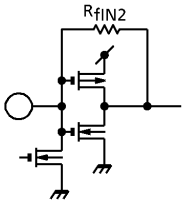
DESCRIPTION OF PIN FUNCTION

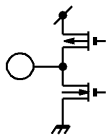
PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
1	COM1	LCD common output	Output common signals to LCD panels. Through a matrix with pins S1 to S25, a maximum 100 segments can be displayed. Three levels, V_{LCD}, V_{EE}, and GND, are output at 62.5Hz every 2ms. V_{EE} is output after system reset and CLOCK STOP are released, and a common signal is output after the DISP OFF bit is set to "0".	
2	COM2			
3	COM3			
4	COM4			
5~20	S1~S16	LCD segment output	Segment signal output terminals for LCD panel. Together with COM1 to COM4, a matrix is formed that can display a maximum of 100 segments. S17 to S25 are usable as I/O port by program. Signals for key matrix and the segment signals from pins S22/KR3 to S25/KR0 are output on a time sharing basis. 4×4=16 key matrix can be created in conjunction with key inport ports K0 to K3.	
21~25	S17/P7-0 ~ S21/P8-0	LCD segment output/I/O port		
26~29	S22/P8-1/KR3 ~ S25/P9-0/KR0	LCD segment output/I/O port/key return timing output		
30~32	P9-1~P9-3	I/O port 9	3-bit I/O port, capable of input/output setup for each bit via software.	
33	IN2	Input port 2	1-bit input port	

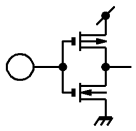
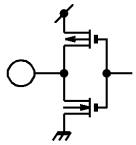
PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
34~37	K0~K3	Key input port	4-bit input port for key matrix input, capable of inputting a maximum of 4×4=16 key data in combination with the key return timing outputs (KR0 to KR3) of an LCD segment pin. Comprises an A/D comparator making it possible to select high impedance with pull-down and pull-up pins for inputs, and to perform programming with a 3-bit input threshold. This allows various key matrices to be formed. Also usable as a 4-channel 3-bit A/D converter with a successive comparison formula via software. When an "H" level is applied in key input ports set to pull-down mode, WAIT mode is canceled.	
38~41	P1-0~P1-3	I/O port 1	The input and output of these 4-bit I/O ports can be programmed in 1-bit units. This pin is capable of outputting timing signals for the key matrix by program. It contains load resistance in N-ch, and can form the matrix for a push-key needing no diode for the key matrix. By altering the input of I/O ports set to input, the CLOCK STOP mode or the WAIT mode can be released, and the MUTE bit of the MUTE pin can be set to "1".	

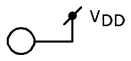
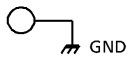
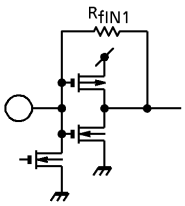
PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
42~45	P2-0 / AD_{IN1} P2-1 / AD_{IN2} P2-2 / AD_{IN3} P2-3 / DC-REF	I/O port 2 / AD analog voltage input / AD analog voltage input / AD analog voltage input / Reference voltage input	4-bit I/O ports, allowing input and output to be programmed in 1-bit units. Pins P2-0 to P2-2 can also be used for analog input to the built-in 6-bit, 3-channel A/D converter. The conversion time of the built-in A/D converter using the successive comparison method is 280μs. The necessary pin can be programmed to AD analog input in 1-bit units, and P2-3 can be set to the reference voltage input. Internal power supply (V_{DD}) or constant voltage (V_{EE}) can be used as the reference voltage. So battery voltage, etc., can be easily detected. The reference voltage input, for which a built-in operational amp. is used, has high impedance. The A/D converter and all associated controls are performed via sortware.	

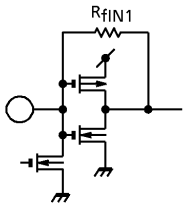
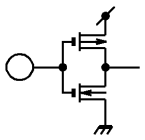
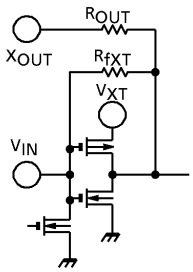
PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
46~49	P3-0 / SI P3-1 / SO P3-2 / $\overline{SCK}$ P3-3 / BUZR	I / O port 3 / Serial data input / Serial data output / Serial clock I / O / Buzzer output	4-bit I / O ports, allowing input and output to be programmed in 1-bit units. Pins P3-0 to P3-2 can also be used for the I / O terminals of serial interface circuits (SIO). SIO functions for 4-bit or 8-bit serial data inputs from the SI pin and outputs from the SO pin at the $\overline{SCK}$ pin clock edge. The clock for serial operation ($\overline{SCK}$) is capable of internal / external options and rise / fall shift options. The SO pin is also capable of switching to serial inputs (SI), facilitating the control of various LSI's and communication between controllers. All SIO inputs use built-in Schmitt circuits. P3-3 pins also functions as the output for a built-in buzzer. The buzzer output can select 8 kinds of 0.625 to 3kHz frequencies with 4modes: continuous output, single-shot output, 10-Hz intermittent output, and 10-Hz intermittent 1-Hz interval output. SIO, buzzer, and all associated controls can be programmed.	 (excluding P3-3 pins)
50~61	P4-0 / $\overline{PWM}$ P4-1 ≀ P6-2 / CTR_{IN1} P6-3 / CTR_{IN2}	I / O port 4 / PWM output I / O port 4 ≀ I / O port 6 / Counter input	16-bit I / O ports, allowing input and output to be programmed in 1-bit units. The P4-0 pin is also used for built-in 12-bit PWM outputs. The PWM outputs pulse continuously at 73.26Hz, and can change the duty of the pulses to 256 steps (8 bits), causing the added pulses to be output using 4 bits for 16 cycles (218.5ms). The P6-2 and P6-3 pins are also used for input purposes when using 20-bit IF counters as 12-bit and 8-bit binary counters. The P6-2 pin can be used for 12-bit binary counter inputs, and the P6-3 pin for 8-bit binary counter inputs. PWM outputs, counter inputs, and all associated controls can be programmed.	 (P4-0~P6-1)  (P6-2, P6-3)

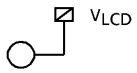
PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
62	MUTE	Muting output port	1-bit output port, normally used for muting control signal output. This pin can set the internal MUTE bit to "1" according to a change in the input of I/O port 1. MUTE bit output logic can be changed: PLL phase difference can also be output using this pin.	
63	TEST	Test mode control input	Input pin used for controlling TEST mode. "H" (high) level indicates TEST mode, while "L" (low) indicates normal operation. The pin is normally used at low level or in NC (no connection) state. (A pull-down resistor is builtin).	
64	IF_{IN} / IN1 / SC_{IN}	IF signal input / Input port / Cycle measurement input	IF signal input pin for the IF counter to count the IF signals of the FM and AM bands and to detect the automatic stop position. The input frequency is between 0.35 to 12MHz ($0.2V_{p\text{-}pmin}$). A built-in input amp. and C coupling allow operation at low-level input. The IF counter is a 20bit counter with optional gate times of 1, 4, 16 and 64ms. 20 bits of data can be readily stored in memory. This counter is used as a timer when the IF counter is not used. The input pin can be programmed for use as an input port (IN port). CMOS input is used when the pin is set as an IN port. (Note) To set SC_{IN}, use the pin with DC coupling and rectangular wave input.	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
65 66	DO1 / OT2 DO2	Phase comparator output / Output port Phase comparator output	PLL phase comparator output pins. When the prescaler output of the programmable counter is higher than the reference frequency, output is at high level. When output is lower than the reference frequency, output is at low level. When output equals the reference frequency, high impedance output is obtained. Because DO1 and DO2 are output in parallel, optional filter constants can be designed for the FM / VHF and AM bands. Pin DO1 can be programmed to high impedance or programmed as an output port (OT2). Thus, the pins can be used to improve lock-up time or used as output ports.	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
67	$\overline{\text{HOLD}}$	Hold mode control input	Input pin for request / release hold mode. Normally, this pin is used to input radio mode selection signals or battery detection signals. Hold mode includes CLOCK STOP mode (stops crystal oscillation) and WAIT mode (halts CPU). Setting is implemented with the CKSTP instruction or the WAIT instruction. When the CKSTP instruction is executed, request / release of the hold mode depends on the internal MODE bit. If the MODE bit is "0" (MODE-0), executing the CKSTP instruction while the $\overline{\text{HOLD}}$ pin is at low level stops the generator and the CPU and changes to memory back-up mode. If the MODE bit is "1" (MODE-1), executing the CKSTP instruction enters memory back-up mode regardless of the level of the $\overline{\text{HOLD}}$ pin. Memory back-up is released when the $\overline{\text{HOLD}}$ pin goes high in MODE-0, or when the $\overline{\text{HOLD}}$ pin input changes in MODE-1. When memory back-up mode is entered by executing a WAIT instruction, any change in the $\overline{\text{HOLD}}$ pin input releases the mode. In memory back-up mode, current consumption is low (below 10μA), and all the output pins (e.g., display output, output ports) are automatically set to low level.	
68	OT1	Output port	1-bit output port. (Note) This output goes high after reset, and internal latch data is output as is even when CLOCK STOP is being executed.	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
72	V_{DD}	Power-supply pins	Pins to which power is applied. Normally, V_{DD} = 1.8 to 3.6V is applied. In back-up mode (when CKSTP instructions are being executed), voltage can be lowered to 1.0V. If voltage falls below 1.55V while the CPU is operating, the CPU stops to prevent malfunction (STOP mode). When the voltage rises above 1.55V, the CPU restarts. STOP mode can be detected by checking the STOP F/F bit. If necessary, execute initialization or adjust clock by program. When detecting or preventing CPU malfunctions using an external circuit, STOP mode can be invalidated and rendered non-operative by program. In that case, all four bits of the internal TEST port should be set to "1". If more than 1.8V is applied when the pin voltage is 0, the device system is reset and the program starts from address "0". (Power on reset) (Note) To operate the power on reset, the power supply should start up in 10 to 100ms.	
69	GND			
70	FM_{IN}	FM local oscillator signal input	Using programmable counter input pins for FM, VHF band. The 1/2 + pulse swallow system (VHF mode) and the pulse swallow system (FM mode) are freely selectable by program. At the VHF mode, local oscillation output (VCO output) of 50 to 230MHz [$0.3V_{p-p}$ (Min)] is input, and at the FM mode, that of 40 to 130MHz [$0.2V_{p-p}$ (Min)] is input. A built-in input amp. and C coupling allow operation at low-level input. (Note) When in the PLL OFF mode or when set to AM_{IN} input, the input is pulled down.	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
71	AM_{IN}	AM local oscillator signal input	Programmable counter input pin for AM band. The pulse swallow system (HF mode) and direct dividing system (LF mode) are freely selectable by program. At the HF mode, local oscillation output (VCO output) of 1 to 45MHz [$0.2V_{p-p}$ (Min)] is input, and at the LF mode, 0.5 to 12MHz [$0.2V_{p-p}$ (Min)] is input. Built-in input amp. operates with low-level input using a C coupling. (Note) When in PLL OFF mode or when set to FM_{IN} input, the input is pulled down.	
73	$\overline{RESET}$	Reset input	Input pin for system reset signals. $\overline{RESET}$ takes place while at low level; at high level, the program starts from address "0". Normally, if more than 1.8V is supplied to V_{DD} when the voltage is 0, the system is reset (power on reset). Accordingly, this pin should be set to high level during operation.	
74	X_{OUT}	Crystal oscillator pin	Crystal oscillator pins. A reference 75-kHz crystal resonator is connected to the X_{IN} and X_{OUT} pins. The oscillator stops oscillating during CKSTP instruction execution. The V_{XT} pin is the power supply for the crystal oscillator. A stabilizing capacitor (0.47μF typ.) is connected.	
75	X_{IN}			
76	V_{XT}			

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
77	V_{LCD}	Voltage doubler boosting pin	Voltage doubler boosting pin to drive the LCD. A capacitor (0.1 to 3.3μF typ.) is connected to boost the voltage. The V_{LCD} pin outputs voltage (3.1V), which has been doubled from the constant voltage (V_{EE} : 1.55V) using the capacitor connected between C1 and C2. This potential is supplied to the LCD driver. If the internal V_{LCD} OFF bit is set to "1" by program, an external supply can be input through the V_{LCD} pin to drive the LCD. At this time, the $V_{LCD}/2$ potential, whose V_{LCD} voltage divided using resisters, is output from the C2 pin.	
78	C1			
79	C2			
80	V_{EE}	Constant voltage supply pin	1.55V constant voltage supply pin to drive the LCD. A stabilizing capacitor (0.47μF Typ.) is connected. This is a reference voltage for the A/D converter, key input, and the bias potential of the LCD common output.	—

(Note 1) When the device is reset (V_{DD} = 0V→1.8V or higher or $\overline{RESET}$ = "L"→"H") I/O ports are set to input, the pins for both LCD output and I/O ports and additional functions (e.g., SIO, A/D converter) are set to I/O port input pins, while the IF_{IN}/IN1/SC_{IN} pins become IF input pins.

(Note 2) When in PLL OFF mode (when the four bits in the internal reference ports are all set to "1"), the IF_{IN}/SC_{IN} and FM_{IN}, AM_{IN} pins are pulled down, and DO1 and DO2 are at high impedance.

(Note 3) When in CLOCK STOP mode (during execution of CKSTP instruction), the output ports (excluding OT1 output) and LCD output pins are all at low level, while the constant voltage circuit (V_{EE}), the voltage doubler circuit (V_{LCD}), and the power supply for the crystal oscillator (V_{XT}) are at V_{DD} level.

(Note 4) When the device is being reset, the contents of the output ports and internal ports are undefined and must be initialized via software.

(Note 5) When the pins for both LCD output and I/O ports are set to the I/O port, V_{LCD} potential is used as the power supply for the output, so the V_{LCD} level is output at "H" level. In addition, the input power supply is at V_{DD} level, so it can be used in the same way as for the other I/O port inputs.

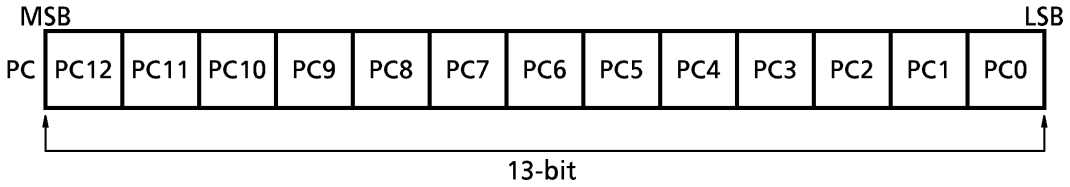
DESCRIPTION OF OPERATIONS

○ CPU

The CPU consists of a program counter, a stack register, ALU, a program memory, a data memory, a G-register, a data register, a carry F/F and a judgment circuit.

1. Program Counter (PC)

   The program counter consists of a 13-bit binary up-counter and addresses the program memory (ROM). The counter is cleared when the system is reset and the programs start from the 0 address.
   Under normal conditions, the counter is increased in increments of one whenever an instruction is executed, but the address specified in the instruction operand is loaded when a JUMP instruction or CALL instruction is executed.
   Also, when an instruction that is equipped with the skip function (AIS, SLTI, TMT, RNS instructions, etc.) is executed and the result of this includes a skip condition, the program counter is increased in increments of two and the subsequent instruction is skipped.



2. Stack Register (STACK)

   A register consisting of 2 × 13 bits which stores the contents of the program counter + 1 (the return address) when a sub-routine call instruction is executed. The contents of the stack register are loaded into the program counter when the return instruction (RN or RNS instruction) is executed.
   There are two stack levels available and nesting occurs with both levels.

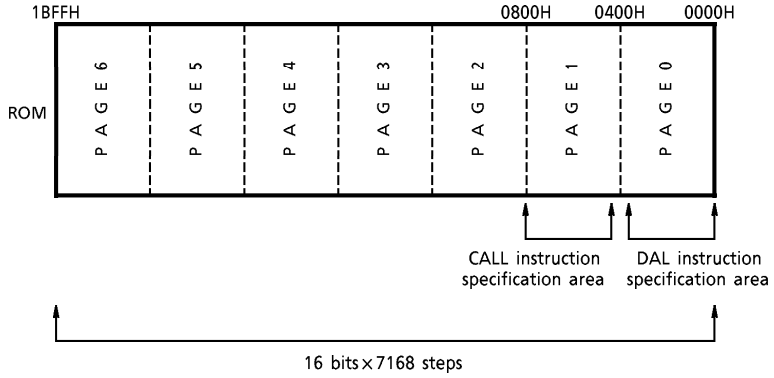
3. ALU

   ALU is equipped with binary 4-bit parallel add/subtract functions, logical operation, comparison and multiple bit judgment functions.
   This CPU is not equipped with an accumulator, and all operations are handled directly within the data memory.

4. Program Memory (ROM)

The program memory consists of 16 bits × 7168 steps and is used for storing programs. The usable address range consists of 7168 steps between address 0000H and address 1BFFH.
The program memory is divided into 7168 separate steps and consists of pages 0 to 6. The JUMP instruction can be freely used throughout all 7168 steps. However, the range of use for the CALL instruction is limited to addresses 400H to 7FFH (page 1). It is also possible to use address 000H to 3FFH (page 0) in the program memory as a data area, and the 16-bit contents of this can be loaded into the data register by executing the DAL instruction.

(Note) An address outside of the program loop must be set when establishing a data area within the program memory.

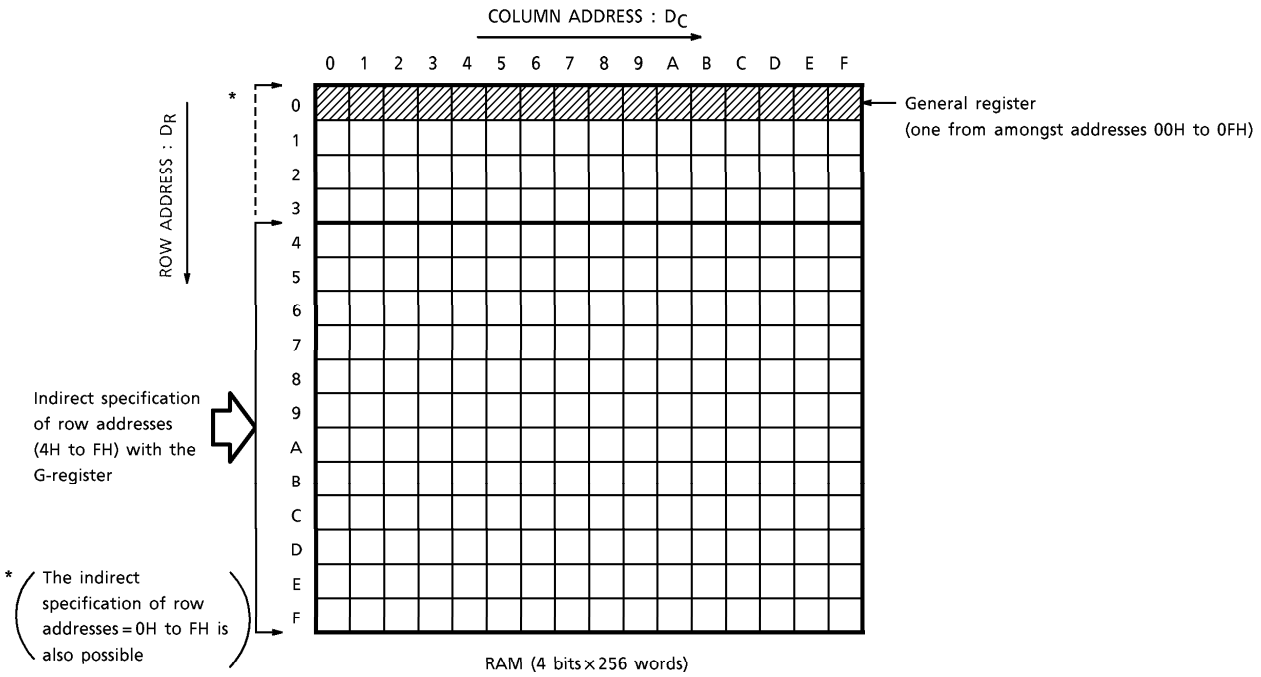


5. Data Memory (RAM)

The data memory consists of 4 bits × 256 words and is used for storing data. These 256 words are expressed in row addresses (4 bits) and column addresses (4 bits). 192 words (row address = addresses 4H to FH) within the data memory are addressed indirectly by the G-register. Owing to this, it is necessary to specify the row address with the G-register before the data in this area can be processed.
The addresses 00H to 0FH within the data memory are known as general registers, and these can be used simply by specifying the relevant column addresses (4 bit). These sixteen general registers can be used for operations and transfers with the data memory, and may also be used as normal data memories.

(Note) The column address (4 bit) that specifies the general register is the register number of the general register.

(Note) All row addresses (addresses 0H to FH) can be specified indirectly with the G-register.



6. G-Register (G-REG)

   The G-register is a 4 bit register used for addressing the row addresses (D_R = 4H to FH addresses) of the data memory's 192 words.
   The contents of this register are validated when the MVGD instruction or MVGS instruction are executed, and are not affected through the execution of any other instructions. This register is used as one of the ports, and the contents are set when the OUT1 instruction from amongst the I/O instructions is executed. (→ Refer to section #1 in Register Ports.)

7. Data Register (DATA REG)

   The data register consists of 1 × 16 bits and loads 16 bits of optional address data from amongst addresses 000H to 3FFH in the program memory when the DAL instruction is executed. This register is used as one of the ports, and the contents are loaded into the data memory in units of 4 bits when the IN1 instruction from amongst the I/O instructions is executed. (→ Refer to section #2 in Register Ports.)

8. Carry F/F (CF/F)

   This is set when either CARRY or BORROW are issued in the result of calculation instruction execution and is reset if neither of these are issued.
   The contents of carry F/F can only be amended through the execution of addition or subtraction instructions and are not affected by the execution of any other instruction.

9. Judgment circuit (J)

This circuit judges the skip conditions when an instruction equipped with the skip function is executed. The program counter is increased in increments of two when the skip conditions are satisfied, and the subsequent instruction is skipped.
There are 29 instructions equipped with a wide variety of skip functions available. (→ Refer to the items marked with a "*" symbol in the Table of Instruction Functions and Operational Instructions in section 11.)

10. Instruction Set Table

A total of 62 instruction sets are available, and all of these are single-word instructions. These instructions are expressed with 6-bit instruction codes.

High order 2-bit / Low order 4-bit		00	01	10	11
		0	1	2	3
0000	0	AI M, I	AD r, M	TMTR r, M	SLTI M, I
0001	1	AIS M, I	ADS r, M	TMFR r, M	SGEI M, I
0010	2	AIN M, I	ADN r, M	SEQ r, M	SEQI M, I
0011	3	AIC M, I	AC r, M	SNE r, M	SNEI M, I
0100	4	AICS M, I	ACS r, M	LD r, M	TMTN M, N
0101	5	AICN M, I	ACN r, M	ST M, r	TMT M, N
0110	6	ORIM M, I	ORR r, M	MVGD r, M	TMFN M, N
0111	7	ANIM M, I	ANDR r, M	MVGS M, r	TMF M, N
1000	8	SI M, I	SU r, M	JUMP ADDR1	IN1 M, C
1001	9	SIS M, I	SUS r, M		IN2 M, C
1010	A	SIN M, I	SUN r, M		IN3 M, C
1011	B	SIB M, I	SB r, M		OUT1 C, M
1100	C	SIBS M, I	SBS r, M		OUT2 C, M
1101	D	SIBN M, I	SBN r, M		OUT3 C, M
1110	E	XORI M, I	XORR r, M		DAL ADDR3, r
1111	F	MVIM M, I	MVSR M1, M2	CALL ADDR2	RN, RNS, WAIT CKSTP, NOOP

11. Table of Instruction Functions and Operational Instructions
(Description of the symbols used in the table)

M	:	Data memory address. Generally one of the addresses from amongst addresses 00H to 3FH in the data memory.
r	:	General register One of the addresses from amongst addresses 00H to 0FH in the data memory.
PC	:	Program counter (13 bits)
STACK	:	Stack register (13 bits)
G	:	G-register (4 bits)
DATA	:	Data register (16 bits)
I	:	Immediate data (4 bits)
N	:	Bit position (4 bits)
—	:	ALL "0"
C	:	Port code No. (4 bits)
C_N	:	Port code No. (4 bits)
R_N	:	General register No. (4 bits)
ADDR1	:	Program memory address (13 bits)
ADDR2	:	Program memory address within page 1 (10 bits)
ADDR3	:	High order 6 bit of the program memory address within page 0
Ca	:	Carry
b	:	Borrow
IN1-IN3	:	The ports used during the execution of instructions IN1 to IN3
OUT1-OUT3	:	The ports used during the execution of instructions OUT1 to OUT3
( )	:	Contents of the register or data memory
$[\ ]_C$	:	Contents of the port indicating code No.C (4 bits)
[ ]	:	Contents of the data memory indicating the contents of the register or data memory
$[\ ]_P$	:	Contents of the program memory (16 bits)
IC	:	Instruction code (6 bits)
*	:	Commands equipped with the skip function
D_C	:	Data memory column address (4 bits)
D_R	:	Data memory row address (2 bits)

INSTRUCTION GROUP	MNEMONIC	SKIP FUNC-TION	FUNCTION DESCRIPTION	OPERATION DESCRIPTION	MACHINE LANGUAGE (16 BITS) IC (6 BITS)	A (2 BITS)	B (4 BITS)	C (4 BITS)
ADDITION INSTRUCTIONS	AI M, I	—	Add immediate data to memory	M←(M) + I	000000	D_R	D_C	I
	AIS M, I	*	Add immediate data to memory, then skip if carry	M←(M) + I Skip if carry	000001	D_R	D_C	I
	AIN M, I	*	Add immediate data to memory, then skip if not carry	M←(M) + I Skip if not carry	000010	D_R	D_C	I
	AIC M, I	—	Add immediate data to memory with carry	M←(M) + I + ca	000011	D_R	D_C	I
	AICS M, I	*	Add immediate data to memory with carry, then skip if carry	M←(M) + I + ca Skip if carry	000100	D_R	D_C	I
	AICN M, I	*	Add immediate data to memory with carry, then skip if not carry	M←(M) + I + ca Skip if not carry	000101	D_R	D_C	I
	AD r, M	—	Add memory to general register	r←(r) + (M)	010000	D_R	D_C	R_N
	ADS r, M	*	Add memory to general register, then skip if carry	r←(r) + (M) Skip if carry	010001	D_R	D_C	R_N
	ADN r, M	*	Add memory to general register, then skip if not carry	r←(r) + (M) Skip if not carry	010010	D_R	D_C	R_N
	AC r, M	—	Add memory to general register with carry	r←(r) + (M) + ca	010011	D_R	D_C	R_N
	ACS r, M	*	Add memory to general register with carry,then skip if carry	r←(r) + (M) + ca Skip if carry	010100	D_R	D_C	R_N
	ACN r, M	*	Add memory to general register with carry, then skip if not carry	r←(r) + (M) + ca Skip if not carry	010101	D_R	D_C	R_N

INSTRUCTION GROUP	MNEMONIC	SKIP FUNC-TION	FUNCTION DESCRIPTION	OPERATION DESCRIPTION	MACHINE LANGUAGE (16 BITS) IC (6 BITS)	A (2 BITS)	B (4 BITS)	C (4 BITS)
SUBTRACTION INSTRUCTIONS	SI M, I	—	Subtract immediate data from memory	M←(M) – I	001000	D_R	D_C	I
	SIS M, I	*	Subtract immediate data from memory, then skip if borrow	M←(M) – I Skip if borrow	001001	D_R	D_C	I
	SIN M, I	*	Subtract immediate data from memory, then skip if not borrow	M←(M) – I Skip if not borrow	001010	D_R	D_C	I
	SIB M, I	—	Subtract immediate data from memory with borrow	M←(M) – I – b	001011	D_R	D_C	I
	SIBS M, I	*	Subtract immediate data from memory with borrow, then skip if borrow	M←(M) – I – b Skip if borrow	001100	D_R	D_C	I
	SIBN M, I	*	Subtract immediate data from memory with borrow, then skip if not borrow	M←(M) – I – b Skip if not borrow	001101	D_R	D_C	I
	SU r, M	—	Subtract memory from general register	r←(r) – (M)	011000	D_R	D_C	R_N
	SUS r, M	*	Subtract memory from general register, then skip if borrow	r←(r) – (M) Skip if borrow	011001	D_R	D_C	R_N
	SUN r, M	*	Subtract memory from general register, then skip if not borrow	r←(r) – (M) Skip if not borrow	011010	D_R	D_C	R_N
	SB r, M	—	Subtract memory from general register with borrow	r←(r) – (M) – b	011011	D_R	D_C	R_N
	SBS r, M	*	Subtract memory from general register with borrow, then skip if borrow	r←(r) – (M) – b Skip if borrow	011100	D_R	D_C	R_N
	SBN r, M	*	Subtract memory from general register with borrow, then skip if not borrow	r←(r) – (M) – b Skip if not borrow	011101	D_R	D_C	R_N

INSTRUCTION GROUP	MNEMONIC	SKIP FUNC-TION	FUNCTION DESCRIPTION	OPERATION DESCRIPTION	MACHINE LANGUAGE (16 BITS) IC (6 BITS)	A (2 BITS)	B (4 BITS)	C (4 BITS)
COMPARISON INSTRUCTIONS	SLTI M, I	*	Skip if memory is less than immediate data	Skip if (M)<I	110000	D_R	D_C	I
	SGEI M, I	*	Skip if memory is greater than or equal to immediate data	Skip if (M)≧I	110001	D_R	D_C	I
	SEQI M, I	*	Skip if memory is equal to immediate data	Skip if (M)=I	110010	D_R	D_C	I
	SNEI M, I	*	Skip if memory is not equal to immediate data	Skip if (M)≠I	110011	D_R	D_C	I
	SEQ r, M	*	Skip if general register is equal to memory	Skip if (r)=(M)	100010	D_R	D_C	R_N
	SNE r, M	*	Skip if general register is not equal to memory	Skip if (r)≠(M)	100011	D_R	D_C	R_N
TRANSFER INSTRUCTIONS	LD r, M	—	Load memory to general register	r←(M)	100100	D_R	D_C	R_N
	ST M, r	—	Store general register to memory	M←(r)	100101	D_R	D_C	R_N
	MVSR M1, M2	—	Move memory to memory in the same row	(D_R, D_{C1})←(D_R, D_{C2})	011111	D_R	D_{C1}	D_{C2}
	MVIM M, I	—	Move immediate data to memory	M←I	001111	D_R	D_C	I
	MVGD r, M	—	Move memory to destination memory referring to G-register and general register	[(G), (r)]←(M)	100110	D_R	D_C	R_N
	MVGS M, r	—	Move source memory referring to G-register and general register to memory	M←[(G), (r)]	100111	D_R	D_C	R_N
I/O INSTRUCTIONS	IN1 M, C	—	Input IN1 port data to memory	M←$[IN1]_C$	111000	D_R	D_C	C_N
	OUT1 C, M	—	Output contents of memory to OUT1 port	$[OUT1]_C$←(M)	111011	D_R	D_C	C_N

INSTRUCTION GROUP	MNEMONIC	SKIP FUNC-TION	FUNCTION DESCRIPTION	OPERATION DESCRIPTION	MACHINE LANGUAGE (16 BITS)			
					IC (6 BITS)	A (2 BITS)	B (4 BITS)	C (4 BITS)
I/O INSTRUCTIONS	IN2 M, C	—	Input IN2 port data to memory	M←[IN2] C	111001	D_R	D_C	C_N
	OUT2 C, M	—	Output contents of memory to OUT2 port	[OUT2] C←(M)	111100	D_R	D_C	C_N
	IN3 M, C	—	Input IN3 port data to memory	M←[IN3] C	111010	D_R	D_C	C_N
	OUT3 C, M	—	Output contents of memory to OUT3 port	[OUT3] C←(M)	111101	D_R	D_C	C_N
LOGICAL OPERATION INSTRUCTIONS	ORR r, M	—	Logical OR of general register and memory	r←(r)∨(M)	010110	D_R	D_C	R_N
	ANDR r, M	—	Logical AND of general register and memory	r←(r)∧(M)	010111	D_R	D_C	R_N
	ORIM M, I	—	Logical OR of memory and immediate data	M←(M)∨I	000110	D_R	D_C	I
	ANIM M, I	—	Logical AND of memory and immediate data	M←(M)∧I	000111	D_R	D_C	I
	XORIM M, I	—	Logical exclusive OR of memory and immediate data	M←(M)⊕I	001110	D_R	D_C	I
	XORR r, M	—	Logical exclusive OR of general register and memory	r←(r)⊕(M)	011110	D_R	D_C	R_N
BIT JUDGMENT INSTRUCTIONS	TMTR r, M	*	Test general register bits by memory bits, then skip if all bits specified are true	Skip if r [N (M)] = all "1"	100000	D_R	D_C	R_N
	TMFR r, M	*	Test general register bits by memory bits, then skip if all bits specified are false	Skip if r [N (M)] = all "0"	100001	D_R	D_C	R_N
	TMT M, N	*	Test memory bits, then skip if all bits specified are true	Skip if M (N) = all "1"	110101	D_R	D_C	N

INSTRUCTION GROUP	MNEMONIC	SKIP FUNC-TION	FUNCTION DESCRIPTION	OPERATION DESCRIPTION	MACHINE LANGUAGE (16 BITS) IC (6 BITS)	A (2 BITS)	B (4 BITS)	C (4 BITS)
BIT JUDGMENT INSTRUCTIONS	TMF M, N	*	Test memory bits, then skip if all bits specified are false	Skip if M (N) = all "0"	110111	D_R	D_C	N
	TMTN M, N	*	Test memory bits, then not skip if all bits specified are true	Skip if M (N) = not all "1"	110100	D_R	D_C	N
	TMFN M, N	*	Test memory bits, then not skip if all bits specified are false	Skip if M (N) = not all "0"	110110	D_R	D_C	N
SUB-ROUTINE INSTRUCTIONS	CALL ADDR2	—	Call subroutine	STACK← (PC) + 1 and PC←ADDR2 + 400H	101111	ADDR2 (10 bits)		
	RN	—	Return to main routine	PC← (STACK)	111111	00	—	—
	RNS	*	Return to main routine and skip unconditionally	PC← (STACK) and skip	111111	01	—	—
JUMP INSTRUCTIONS	JUMP ADDR1	—	Jump to the address specified	PC←ADDR1	101	ADDR1 (13 bits)		
OTHER INSTRUCTIONS	DAL ADDR3, r	—	Load program memory in page 0 to DATA register	DATA← [ADDR3 + (r)] P in page 0	111110	ADDR3 (6 bits)		R_N
	WAIT P	—	At P = "0" H, the condition is CPU waiting (Soft wait mode) At P = "1" H, except for clock generator, all function is waiting (Hard wait mode)	Wait at condition P	111111	10	0000	P
	CKSTP	—	Clock generator stop	Stop clock generator in $\overline{HOLD}$ = "0"	111111	10	1000	—
	NOOP	—	No operation	—	111111	11	—	—

(Note 1) The four low order bits of the program memory's 10-bit address specified with the DAL instruction are addressed indirectly with the contents of the general register. The execution time for the DAL instruction is 80μs (two machine cycles).

(Note 2) The execution time for the MVGS instruction is 80μs (two machine cycles).

○ I/O map

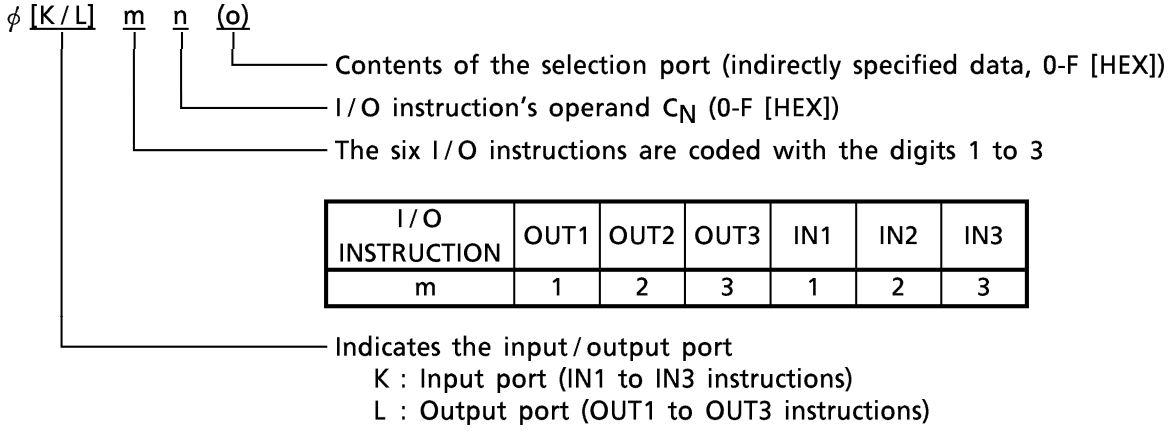
All of the ports within the device are expressed with a matrix of six I/O instructions (OUT 1 to 3 instructions and IN 1 to 3 instructions) and a 4-bit code number.
The allocation of these ports is shown on the following page in the form of an I/O map. The ports used in the execution of the various I/O instructions on the horizontal axis of the I/O map are allocated to the port code numbers indicated on the vertical axis. The G-register and data register are also used as ports.
The OUT 1 to 3 instructions are specified as output ports and the IN 1 to 3 instructions are specified as input ports.

(Note 1) The ports indicated by the angled lines on the I/O map do not actually exist within the device.
The contents of other ports and data memories are not affected when data is output to a non-existent output port with the execution of the output instruction. The data loaded from data memories when a non-existent input port has been specified with the execution of an input instruction becomes '1'.

(Note 2) The output ports marked with an asterisk (*) on the I/O map are not used. Data output to these ports assume the 'don't care' status.

(Note 3) The Y1 contents of the ports expressed in 4 bits correspond to the data memory data's low order bits and the Y8 contents correspond to the high order bits.

The ports specified with the six I/O instructions and code No.C are coded in the following manner:



I/O INSTRUCTION	OUT1	OUT2	OUT3	IN1	IN2	IN3
m	1	2	3	1	2	3

(Example) The setting for the G-register is allocated to code 'F' in the OUT1 instruction. The encoded expression at this time becomes 'φL1F'.

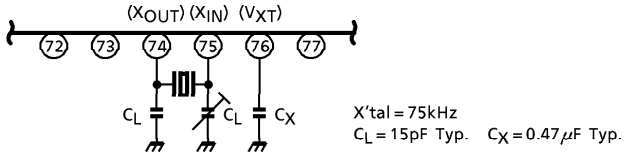
I/O map

I/O	φL1				φL2				φL3				φK1				φK2				φK3			
	OUT1 INSTRUCTION				OUT2 INSTRUCTION				OUT3 INSTRUCTION				IN1 INSTRUCTION				IN2 INSTRUCTION				IN3 INSTRUCTION			
CODE	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
0	HF	IF offset +1	IF offset −1	FM	A/D control AD SEL0	A/D control AD SEL1	A/D control REF SEL0	A/D control REF SEL1	I/O-1 data −0	I/O-1 data −1	I/O-1 data −2	I/O-1 data −3	IF control data BUSY	IF control data Manual	IF control data OVER	1	A/D data AD0	A/D data AD1	A/D data AD2	A/D data AD3	I/O-1 data −0	I/O-1 data −1	I/O-1 data −2	I/O-1 data −3
1	Programmable counter selection #1	Programmable counter selection #2	*		A/D control STA	A/D control *			I/O-2 data −0	I/O-2 data −1	I/O-2 data −2	I/O-2 data −3	IF data f0	IF data f1	IF data f2	IF data f3	A/D data AD4	A/D data AD5	A/D data BUSY	1	I/O-2 data −0	I/O-2 data −1	I/O-2 data −2	I/O-2 data −3
2	Programmable counter PA	Programmable counter PB	Programmable counter PC	Programmable counter PD	SIO control edge	SIO control SCK-INV	SIO control SCK-I/O	SIO control SIO-ON	I/O-3 data −0	I/O-3 data −1	I/O-3 data −2	I/O-3 data −3	IF data f4	IF data f5	IF data f6	IF data f7					I/O-3 data −0	I/O-3 data −1	I/O-3 data −2	I/O-3 data −3
3	Reference port R0	Reference port R1	Reference port R2	* P16	SIO control STA	SIO control SO-I/O	SIO control 8/4 bit	*	I/O-4 data −0	I/O-4 data −1	I/O-4 data −2	I/O-4 data −3	IF data f8	IF data f9	IF data f10	IF data f11	SIO control data BUSY	SIO control data COUNT	SIO control data SIO F/F	1	I/O-4 data −0	I/O-4 data −1	I/O-4 data −2	I/O-4 data −3
4	IF counter control OT1	IF counter control SC ON	IF counter control IF/IN1	IF counter control Split	SIO output data SO0	SIO output data SO1	SIO output data SO2	SIO output data SO3	I/O-5 data −0	I/O-5 data −1	I/O-5 data −2	I/O-5 data −3	IF data f12	IF data f13	IF data f14	IF data f15	SIO input data SI0	SIO input data SI1	SIO input data SI2	SIO input data SI3	I/O-5 data −0	I/O-5 data −1	I/O-5 data −2	I/O-5 data −3
5	IF counter control STA/STP	IF counter control Manual	IF counter control G0	IF counter control G1	SIO output data SO4	SIO output data SO5	SIO output data SO6	SIO output data SO7	I/O-6 data −0	I/O-6 data −1	I/O-6 data −2	I/O-6 data −3	IF data f16	IF data f17	IF data f18	IF data f19	SIO input data SI4	SIO input data SI5	SIO input data SI6	SIO input data SI7	I/O-6 data −0	I/O-6 data −1	I/O-6 data −2	I/O-6 data −3
6	MUTE OUT MUTE	MUTE OUT I/O	MUTE OUT POL	MUTE OUT UNLOCK	Timer reset 2Hz F/F	Timer reset Timer	Test data #4	Test data #5									Timer 2Hz F/F	Timer 10Hz	Timer 100Hz	STOP F/F				
7	UNLOCK RESET	DO1 control OTC	DO1 control OT2	DO1 control Hz									UNLOCK F/F	UNLOCK ENABLE	IN1	1	Key scan digit KR1	Key scan digit KR2	Key scan digit 1	Key scan digit 1				
8	PWM/BUZR data PW0/BM0	PWM/BUZR data PW1/BM1	PWM/BUZR data PW2/*	PWM/BUZR data PW3/*													Key input data K0	Key input data K1	Key input data K2	Key input data K3				
9	PWM/BUZR data PW4/BF0	PWM/BUZR data PW5/BF1	PWM/BUZR data PW6/BF2	PWM/BUZR data PW7/BEN	Key scan control KC0	Key scan control KC1	Key scan control KC2	Key scan control KC3									Key scan data K0	Key scan data K1	Key scan data K2	Key scan data K3				
A	PWM data PW8	PWM data PW9	PWM data PW10	PWM data PW11	Key scan data selection KSD1	Key scan data selection KSD2	Key scan data selection KSD4	Key scan data selection KSD8																
B	PWM ON	BUZR ON	PWM/BUZR	Buffer transfer/*					I/O-7 data −0	I/O-7 data −1	I/O-7 data −2	I/O-7 data −3	HOLD	1	1	1					I/O-7 data −0	I/O-7 data −1	I/O-7 data −2	I/O-7 data −3
C	Test data #0	Test data #1	Test data #2	Test data #3					I/O-8 data −0	I/O-8 data −1	I/O-8 data −2	I/O-8 data −3	DATA-reg d0	DATA-reg d1	DATA-reg d2	DATA-reg d3					I/O-8 data −0	I/O-8 data −1	I/O-8 data −2	I/O-8 data −3
D					SEG data selection S1	SEG data selection S2	SEG data selection S4	SEG data selection S8	I/O-9 data −0	I/O-9 data −1	I/O-9 data −2	I/O-9 data −3	DATA-reg d4	DATA-reg d5	DATA-reg d6	DATA-reg d7					I/O-9 data −0	I/O-9 data −1	I/O-9 data −2	I/O-9 data −3
E				CKSTP MODE	SEG-1 data COM1	SEG-1 data COM2	SEG-1 data COM3	SEG-1 data COM4	I/O control selection I/O1	I/O control selection I/O2	I/O control selection I/O4	I/O control selection I/O8	DATA-reg d8	DATA-reg d9	DATA-reg d10	DATA-reg d11					IN2	1	1	1
F	G-reg #0	G-reg #1	G-reg #2	G-reg #3	SEG-2 data COM1	SEG-2 data COM2	SEG-2 data COM3	SEG-2 data COM4	I/O control data IO-0	I/O control data IO-1	I/O control data IO-2	I/O control data IO-3	DATA-reg d12	DATA-reg d13	DATA-reg d14	DATA-reg d15								

* Programmable counter

○ Crystal resonator connection

A 75kHz crystal resonator is connected to the device's crystal resonator terminal (X_{IN}, X_{OUT}) as indicated below.
The oscillation signal is supplied to the clock generator, the reference frequency divider and other elements, and generates the various CPU timing signals and reference frequencies. The crystal resonator circuit is powered by the voltage supplied from a built-in rated voltage circuit (V_{XT} = 1.4V Typ.). This enables the stable operation of the crystal resonator and reduces current consumption.



(Note) It is necessary to use a crystal resonator with a low CI value and favorable start-up characteristics.

○ System reset

The device's system will be reset when the $\overline{RESET}$ terminal is subject to the 'L' level or when a voltage of 0V→1.8V or more is supplied to the V_{DD} terminal (power-on reset). The program will start from the 0 address immediately after the 100ms stand-by time has passed following system reset.
The $\overline{RESET}$ terminal should be fixed at the 'H' level as the power-on reset function is used under normal conditions.

(Note 1) The LCD common output and the segment output will be fixed at the 'L' level during system reset and during the subsequent stand-by period.

(Note 2) The internal ports outlined in the table below will be fixed after system reset, but all other ports will become unstable. It is therefore advisable to initialize the ports with a program in accordance with necessity.

Fixed Internal Ports

PORTS FIXED AT '0'	PORTS FIXED AT '1'
SC ON, Split bit (ϕL14), manual bit (ϕL15)	Reference port (ϕL13)
IO, POL, UNLOCK bit (ϕL16)	MUTE bit (ϕL16)
DO1 control port (ϕL17)	IF / $\overline{\text{IN1}}$ (ϕL14)
BUZR control ports (ϕL18, ϕL19)	
PWM ON, BUZR ON, PWM / BUZR, transfer bit (ϕL1B)	
Test ports (ϕL26, ϕL2FF)	Test port (ϕL1C)
CKSTP MODE bit (ϕL1E)	
AD control port (ϕL20)	
SIO control ports (ϕL22, ϕL23)	
Timer port (ϕK26)	
Key scan control ports (ϕL290, ϕL292 to ϕL294)	
V_{LCD} OFF bit (ϕL2FF)	DISP OFF bit (ϕL2FF)
IO-1 to IO-6 and IO9 IO control ports (ϕL3F0 to ϕL3F5, ϕL3FD)	SEG port (SEG / IO control ports: ϕL3F8 to ϕL3FA)

○ Back-up Mode

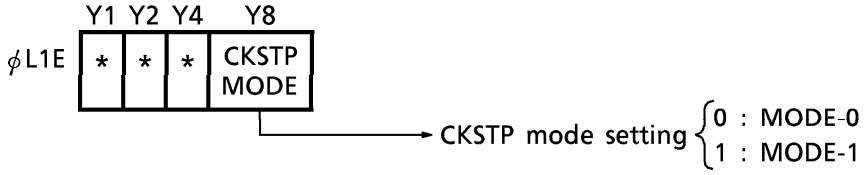
Three different types of back-up mode can be activated through the execution of the CKSTP instruction and WAIT instruction.

1. Clock Stop Mode

The clock stop mode is a function that suspends system operations and maintains the internal status immediately prior to suspension at a low level of current consumption (10μA or less at V_{DD} = 3.0V). Crystal oscillations are suspended simultaneously and all output terminals and output ports for LCD display purposes are automatically fixed at the 'L' level or at the OFF status. The mains power voltage can be reduced to 1.0V with the clock stop mode.
Suspension is activated at the CKSTP instruction execution address when the CKSTP instruction is executed. The next address is executed after approximately 100ms of stand-by time when the clock stop mode is cancelled.

(1) Clock stop mode setting

There are two types of mode setting for the clock stop mode. The required setting is selected with the CKSTP MODE bit. This bit is accessed with the OUT1 instruction for which [C_N = EH] has been specified in the operand.



① MODE-0

By setting this mode, the clock stop mode is assumed if the CKSTP instruction is executed when the $\overline{HOLD}$ terminal is in the 'L' level. The same operations as the NOOP instruction will be assumed if the CKSTP instruction is executed when the $\overline{HOLD}$ terminal is in the 'H' level.

② MODE-1

By setting this mode, the clock stop mode is assumed when the CKSTP instruction is executed regardless of the $\overline{HOLD}$ terminal level.

(Note) PLL will assume the off status during CKSTP instruction execution.

(2) Cancelling the clock stop mode

① MODE-0

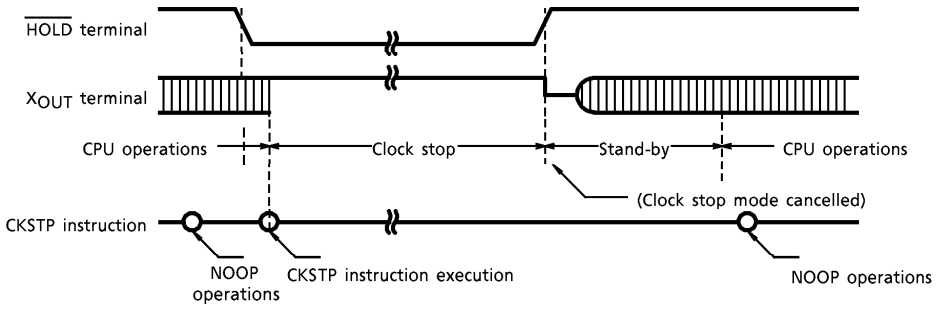
The clock stop mode is cancelled when specified in this mode by changing the 'H' level of the $\overline{\text{HOLD}}$ terminal or the input status of I/O port 1 (P1-0 to P1-3) specified in the input port.

② MODE-1

The clock stop mode is cancelled when specified in this mode by changing the $\overline{\text{HOLD}}$ terminal or the input status of I/O port 1 (P1-0 to P1-3) specified in the input port.

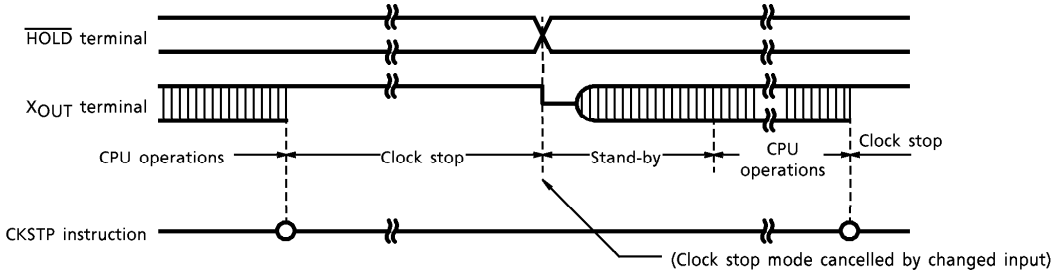
(3) Clock stop mode timing

① MODE-0



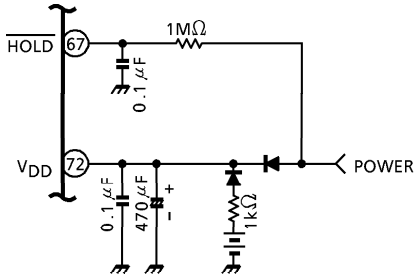
(The clock stop mode is assumed when the CKSTP instruction is executed when the $\overline{\text{HOLD}}$ input is in the 'L' level.)

② MODE-1

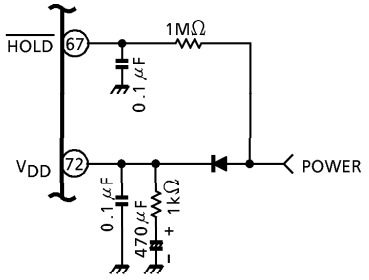


(The clock stop mode is assumed whenever the CKSTP instruction is executed.)

(4) Example of a circuit (example of a MODE-0 circuit)



Example of a battery back-up circuit



Example of a condenser back-up circuit

2. Wait mode

The wait mode suspends system operations, maintains the internal status immediately prior to suspension and reduces current consumption. There are two types of wait mode available; the SOFT WAIT mode and the HARD WAIT mode. Operations are suspended at the address where the WAIT instruction was executed when the wait mode is activated. The next address is executed immediately after the wait mode is cancelled without entering a stand-by status.

(1) SOFT WAIT mode

Only the CPU operations within the device are suspended when the WAIT instruction in which [P = 0H] has been specified in the operand is executed. The crystal resonator, display circuit and other elements will continue to operate normally at this time. The SOFT WAIT mode is efficient in reducing current consumption during clock operations when used in programs that include clock functions.

(Note) Current consumption will differ in accordance with the program.

(2) HARD WAIT mode

The operations of all elements, with the exception of the crystal resonator, can be suspended by the execution of The WAIT instruction in which [P = 1H] has been specified in the operand. This enables even greater levels of current consumption reduction than the SOFT WAIT mode. It suspends the CPU and the display circuit and all LCD display output terminals are automatically fixed at the 'L' level. (20μA Typ. at V_{DD} = 3V)

(3) Wait mode setting

The wait status is assumed whenever the WAIT instruction is executed.

(Note) The PLL OFF status will be assumed when in the HARD WAIT mode, but the PLL OFF status will not be assumed when in the SOFT WAIT mode. It is therefore necessary to set the PLL OFF status in the program prior to executing the SOFT WAIT function.

(4) Wait mode cancellation conditions

The wait mode is cancelled when the following conditions are satisfied:

① When the input status of the $\overline{\text{HOLD}}$ terminal changes.
② When the 'H' level is input for the key input terminals (K0 to K3). (However, only in the key input mode.)
③ When the 2Hz timer F/F is set as '1' (only with the SOFT WAIT mode.)
④ When the input status of the I/O port specified in the input port (P1-0 to P1-3) changes.

3. $\overline{\text{HOLD}}$ input port

	Y1	Y2	Y4	Y8
ϕK1B	$\overline{\text{HOLD}}$	1	1	1

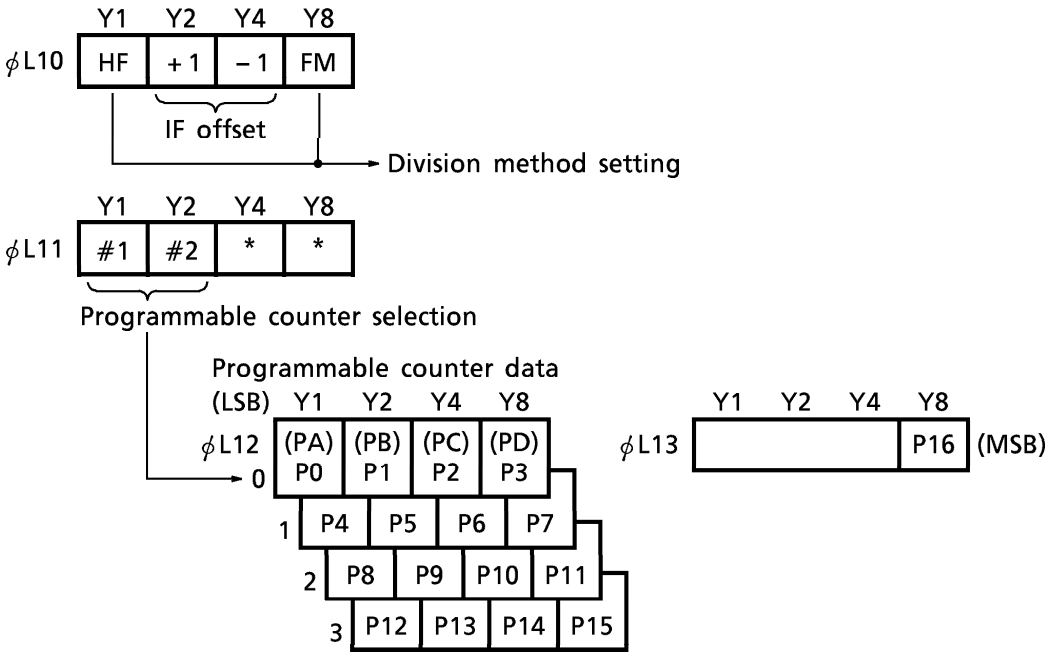
The $\overline{\text{HOLD}}$ terminal can be used as an input port. This bit loads data input with the IN1 instruction for which [C_N = BH] has been specified in the operand into the data memory.
It is necessary to access this port prior to the execution of the CKSTP instruction when the clock stop mode has been set. It is necessary to note that there are cases when the clock stop mode will not be activated if the CKSTP instruction is executed without this port being accessed.

○ Programmable counter

The programmable counter consists of two modulus pre-scalers, a 4-bit + 13-bit programmable counter and a port to control these elements.
The programmable counter controls the ON / OFF functions for the contents of the reference port.

1. Programmable counter control port

A port for controlling frequencies, division methods and IF correction (IF offset) when in the FM band.



(Note) '1' is added to the φL11 data whenever φL12 is accessed.

The division method and offset are accessed with the OUT1 instruction for which [C_N = 0H] has been specified in the operand.
Frequency setting is accessed with the OUT1 instruction for which [C_N = 1H, 2H] has been specified in the operand, and setting is performed by writing in the PA-PD bit (φL12). This port is divided with the programmable counter selection port (φL11), and a corresponding programmable counter is set up by setting data in the selection port.
Only the MSB P16 is accessed with the OUT1 instruction for which [C_N = 3H] has been specified in the operand, and setting is performed by writing in the P16 bit (φL13). All data between P0 and P16 are updated when P16 is set. It is therefore necessary to access P16 without fail even when updating only certain items of data and to perform setting as the final process.
'1' is added to the programmable counter selection whenever the programmable counter data (φL12) is accessed. Setting can easily be carried out by setting '0' in the programmable counter selection port and continually accessing the programmable counter data.

2. Division method setting

The pulse swallow method or direct division method are selected with the HF and FM ports. The direct division method is selected when in the AM band. The following four methods are available and should be selected in accordance with the frequency band being used.

MODE	HF	FM	DIVISION METHOD	EXAMPLE OF RECEIVING BAND	OPERATION FREQUENCY RANGE	INPUT TERMINAL	DIVISION NUMBER (NOTE)
LF	0	0	Direct division method	MW / LW	0.5~12MHz	AM_{IN}	n
HF	1	0	(1 / 15 or 1 / 16) Pulse swallow method	SW	1~45MHz		
FM	0	1		FM	40~130MHz	FM_{IN}	
VHF	1	1	1 / 2 × (1 / 15 or 1 / 16) Pulse swallow method	VHF	50~230MHz		2n

(Note) 'n' represents the number of divisions programmed.

3. IF correction function when in the FM band

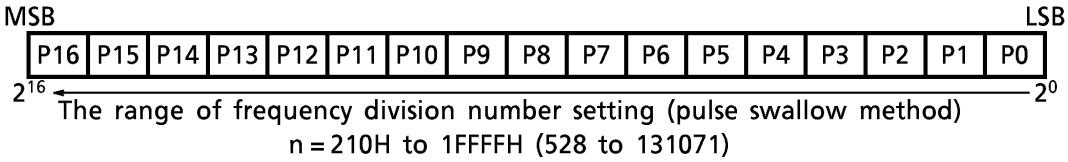
It is possible to add or subtract '1' from the frequency without modifying the number of divisions programmed when the pulse swallow method has been selected with the IF offset ±1 port, and IF offset can be used when in the FM band.
The IF offset function will not operate when the direct division method has been selected.

+1	−1	DIVISION NUMBER (During VHF)	DIVISION NUMBER (During FM and HF)
0	0	2·n	n
0	1	2· (n − 1)	n − 1
1	0	2· (n + 1)	n + 1
1	1	Inhibited	Inhibited

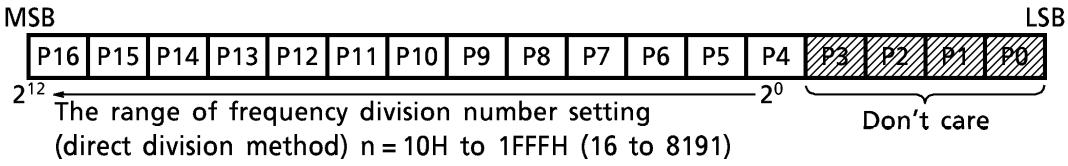
4. Frequency division number setting

The frequency division number for the programmable counter is set in bits P0 to P16 in binary.

- Pulse swallow method (17-bits)



- Direct division method (13-bits)

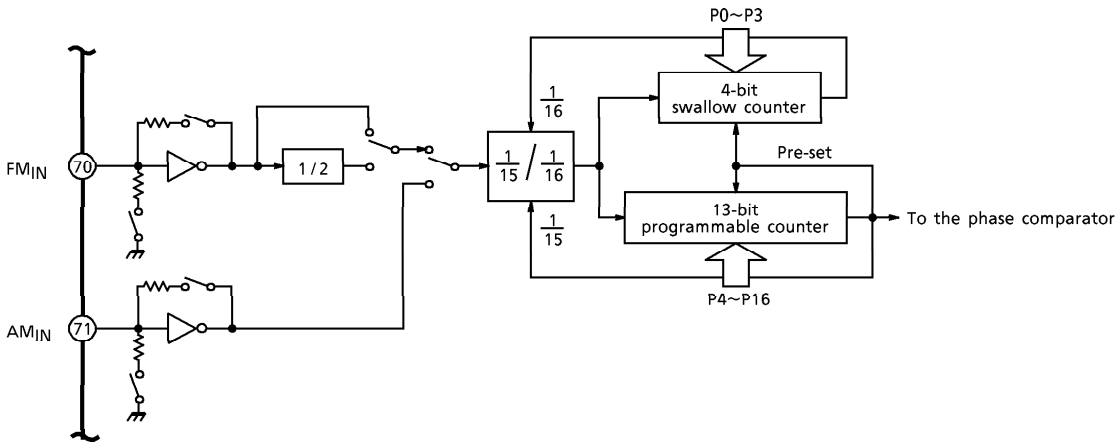


(Note 1) The data in ports P0 to P3 is of no concern with the direct division method, and port P4 becomes LSB.
(Note 2) The program value will become a two-fold frequency division number when in the VHF mode.

5. Programmable counter circuit configuration

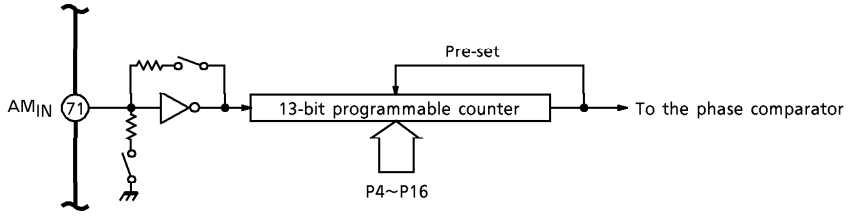
- Pulse swallow method circuit configuration

This circuit consists of two $\frac{1}{15}$ / $\frac{1}{16}$ modulus pre-scalers, the 4-bit swallow counter and a 13-bit binary programmable counter. A 1/2 frequency divider is added to the front stage of the pre-scaler when in the VHF mode.



- Direct division method circuit configuration

  The pre-scaler is not required if this is selected, and instead, the 13-bit programmable counter is used.



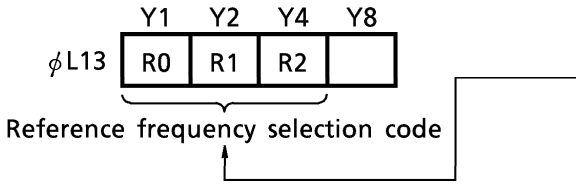
(Note) Both FM_{IN} and AM_{IN} terminals have been fitted into the amplifier, and small amplitude is possible by linking them to a condenser. The input is pull-down for input terminals which were not selected with the division method and when the PLL is in the off mode (set with the reference port).

○ Reference frequency divider

The reference frequency divider divides the oscillation frequencies of the external 75kHz crystal and generates the following seven types of PLL reference frequency signals; 1kHz, 3kHz, 3.125kHz, 5kHz, 6.25kHz, 12.5kHz and 25kHz. These signals are selected with reference port data.
The selected signal is supplied as a reference frequency for the phase comparator as described below. Also, the PLL is switched on and off with the contents of the reference port.

1. Reference port

   The reference port is an internal port for selecting the seven reference frequency signals. This port is accessed with the OUT1 instruction for which [C_N = 3H] has been specified in the operand (ϕL13). Operations for the programmable counter, the IF counter and the reference counter are suspended and the PLL assumes the off mode when the contents of the reference port are all '1'. As the frequency division setting data for the programmable counter is updated when the reference port is set, it is necessary to set the frequency division number of the programmable counter prior to setting the reference port.

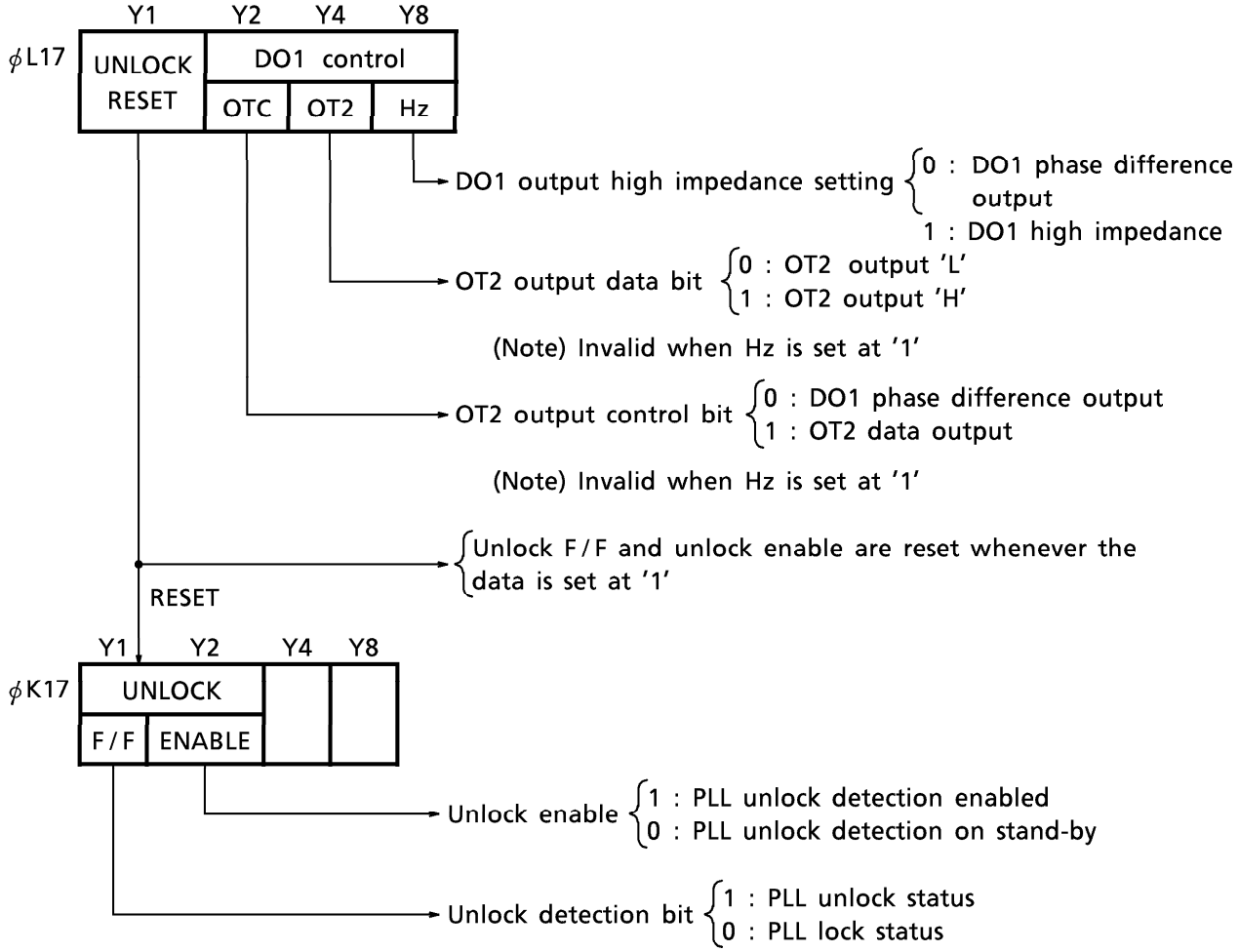


R2	R1	R0	/	REFERENCE FREQUENCY
0	0	0	0	1kHz
0	0	1	1	3kHz
0	1	0	2	3.125kHz
0	1	1	3	5kHz
1	0	0	4	6.25kHz
1	0	1	5	12.5kHz
1	1	0	6	25kHz
1	1	1	7	PLL off mode

○ Phase comparator and lock detection port

The phase comparator compares the difference in phasing between the reference frequency signal supplied from the reference frequency divider and the frequency division output of the programmable counter and outputs the result. It then controls the VCO via a low pass filter in order to ensure that the two frequency signals and the phase difference match.
As the phase comparator outputs both the DO1 and DO2 tri-state buffer terminals in parallel, it is possible to ensure the optimum filter constants for the FM / VHF and AM bands during design.
The DO1 terminal can also be used as a general-purpose output with the DO1 control port. In addition to this, the DO1 terminal can be set at high impedance, which enables PLL loop lock-up types and other character improvements with the use of the DO1 and DO2 terminals.
The lock detection port enables the lock status of the PLL system to be detected.

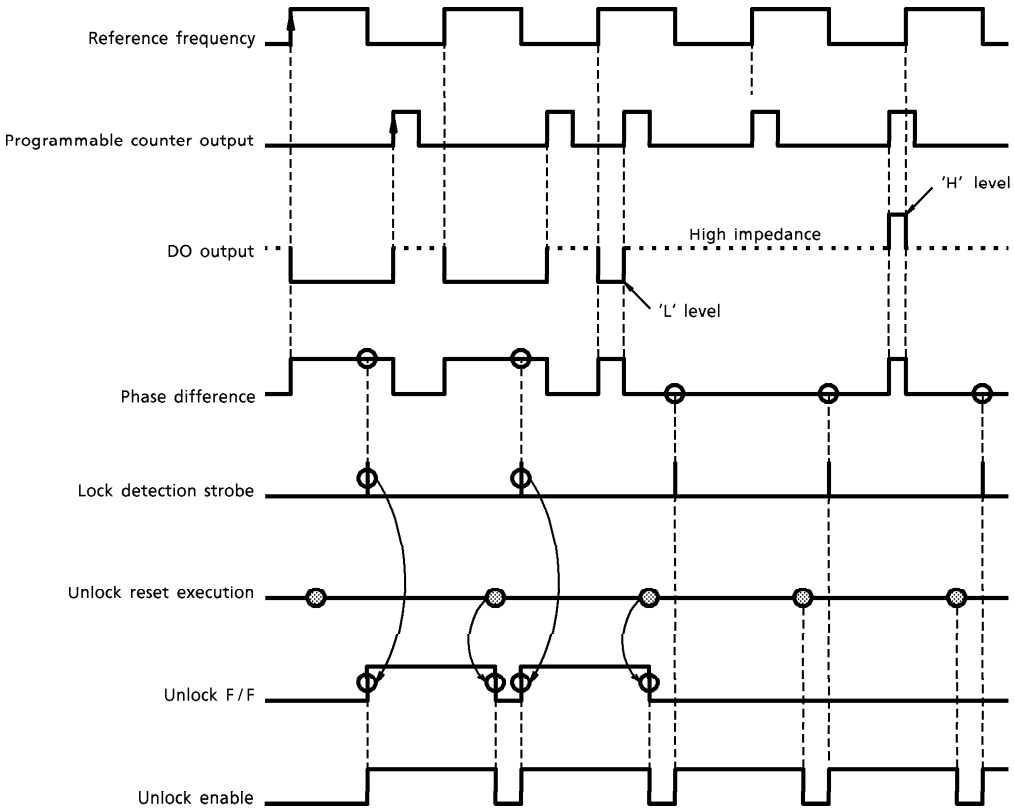
1. DO1 control port and the unlock detection port



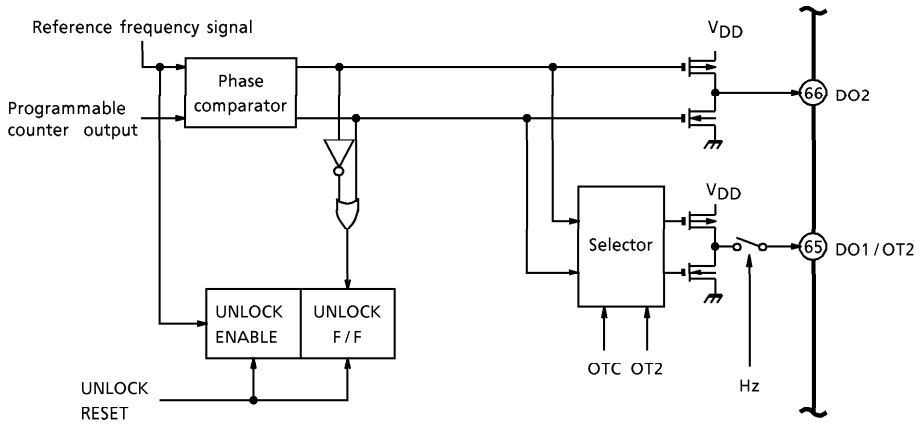
OTC, OT2 and each Hz bit of the DO1 control port use the DO1 output as a general-purpose output port and control the high impedance status without having to output the DO1 output phase difference. This can be set in the program depending on the specifications.
The UNLOCK F/F bit detects the phase difference between the programmable counter frequency division output and the reference frequency when the phasing is misaligned by approximately 180°. The UNLOCK F/F is set when the phase difference does not match (when in the unlock status). The UNLOCK F/F status is reset whenever the UNLOCK RESET bit is set as '1'.
It is necessary to access to UNLOCK F/F after establishing more time than is required for the reference frequency cycle after the unlock F/F has been reset in order to detect the phase difference with the reference frequency cycle. It is for this purpose that the enable bit has been made available, but the unlock F/F must not be accessed until after it has been confirmed that the unlock enable has been set at '1'.
The unlock enable bit will be reset whenever the UNLOCK RESET bit is set at '1'.
The control of these ports and data loading are performed with the OUT1/IN1 instructions for which [C_N = 7H] has been set in the operand.

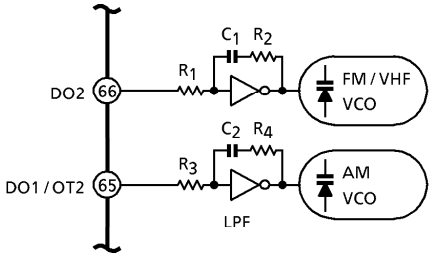
(Note) The DO output will enter a high impedance status when the PLL is in the off mode. However, the output data will be output without modification when DO1 has been set as the output port (OT2 output).

2. Phase comparator and unlock port timing

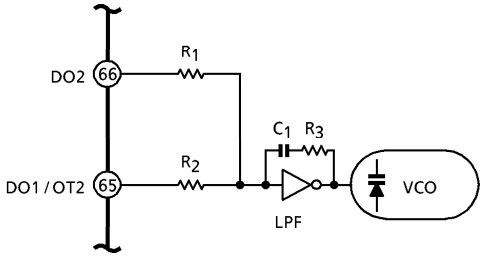


3. Phase comparator and the unlock port circuit configuration

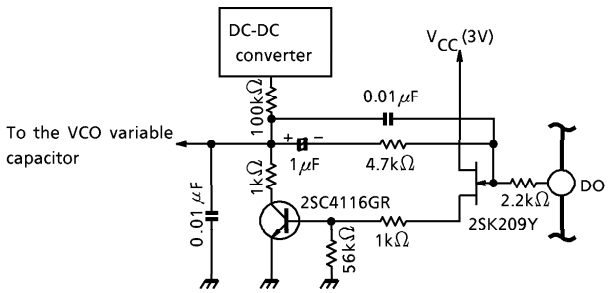




When a filter constant has been set for each band



When the LPF is shared (Sets DO1 at high impedance and switches the filter constants)



Example of an active low pass filter circuit (for reference purposes)

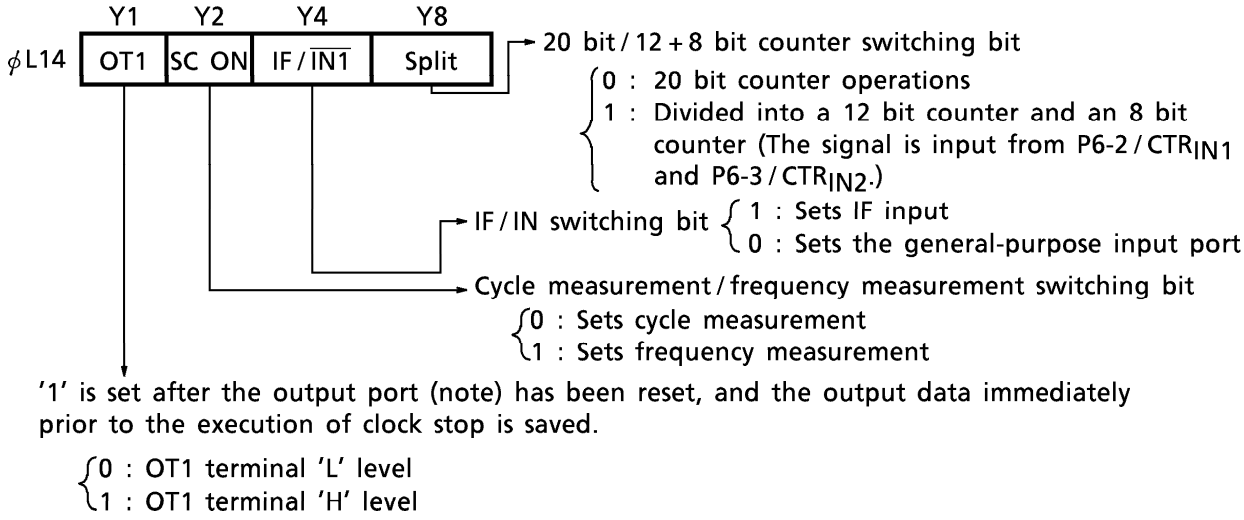
(Note) The filter circuits illustrated in the above diagrams are for reference purposes only. It is necessary to examine the system band configuration and characteristics and design actual circuits in accordance with requirements.

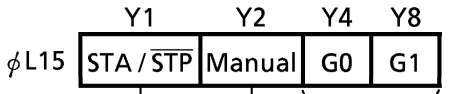
○ IF counter

The IF counter is a 20-bit general-purpose IF counter that calculates FM and AM intermediate frequencies (IF) during auto-tuning and can be used for detecting auto-stop signals, etc. It is also equipped with a cycle measurement function to measure the cycle of low frequency pilot signals. In addition to this, it is also possible to use the general-purpose IF counter as a timer function when it is not being used for calculation purposes.

The IF counter consists of a 20-bit binary counter and a control port.

1. IF counter control port and data port





Selection of the gate time for frequency measurements (measurement time)

G1	G0	GATE TIME
0	0	1ms
0	1	4ms
1	0	16ms
1	1	64ms

Frequency measurements automatic / manual mode switching bit

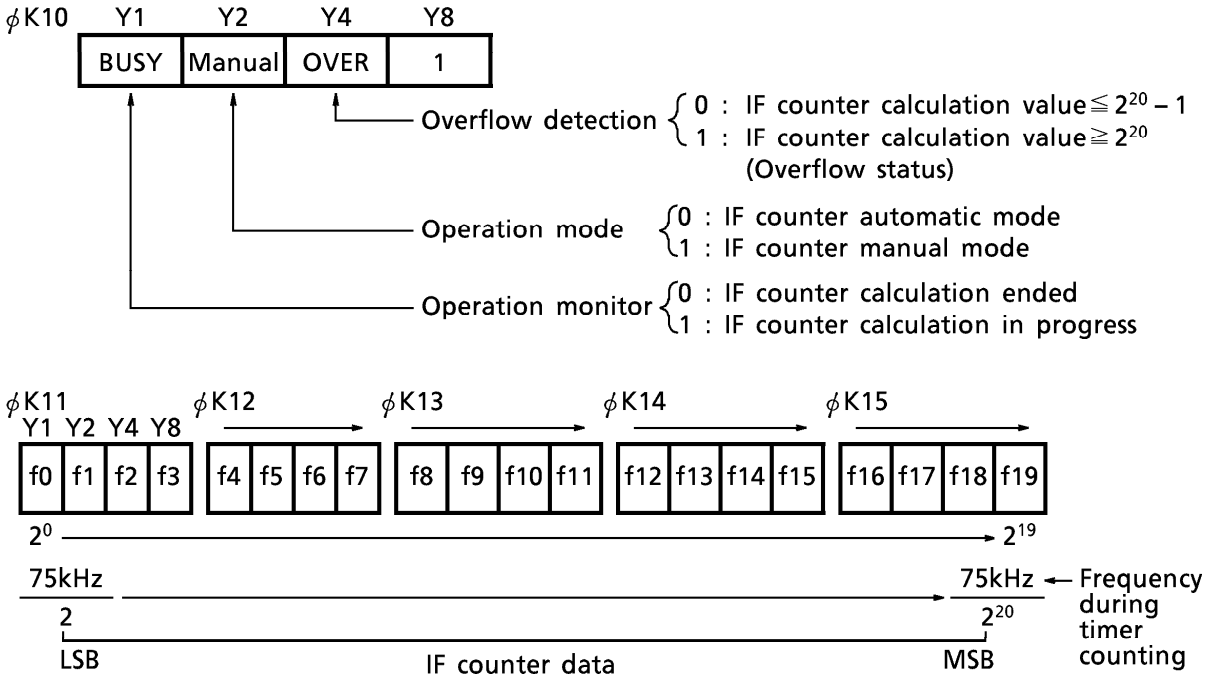
0 : Automatic mode
(Measurement is performed with the above-mentioned gate time when in the automatic mode)
1 : Manual mode
(Starts / stops measurements with the STA / $\overline{\text{STP}}$ bits)

Manual	G1	G0	
1	1	1	Operated as a binary timer counter

(The timer counter is reset when '1' is set in STA / $\overline{\text{STP}}$)

IF counter start / stop control bit

0 : Counter stop
1 : Counter start
(counter reset when the timer counter is set)



(Note) The IF_{IN} input amplifier is disabled in the PLL off mode when the IF input is set.

(Note) The IF counter can be operated in any mode regardless of the PLL mode when the IN1 input (general input port) is set.
Signals are input at the logic level in this event.

(1) IF counter automatic mode (frequency measurement)

In order to use the IF counter automatic mode, the IF terminal for which input is required is set in the IF input with the IF / $\overline{IN1}$ switching bit, and the SC_{ON} bit is set at the frequency measurements mode's '0'.

The IF counter is operated by setting the gate time with the IF input frequency band, setting '0' for the manual bit and setting '1' for the STA / $\overline{STP}$ bit.

This inputs the clock from the IF terminal to the 20-bit binary counter during the set gate time, and the input pulse is counted and then finished. The point for finishing IF counter calculation is determined by referencing the BUSY bit. Also, the OVER bit is set at '1' if the calculation value reaches a pulse count of 2^{20} or more.

By determining that the BUSY bit and the OVER bit are set at '0', the frequency input to the IF input terminal is calculated by loading the IF data in f0 to f19.

(2) IF counter manual mode (frequency measurement)

The manual mode is used to control the gate time with the internal time base (10Hz, etc) and measurement the IF frequency.
This method is activated by setting the IF counter in the same way as explained for the automatic mode and then setting the G0 / G1 bit data at anything other than '1'. Calculation is then started by setting the Manual bit to '1' and setting the STA / $\overline{STP}$ bit to '1'.
Calculations are terminated by setting the STA / $\overline{STP}$ bit to '0', and the data is loaded in binary.

(3) IF counter cycle mode (cycle measurement)

This mode is used to measure the low frequencies that cannot be measured with the frequency measurement method.
Measurement is performed by entering the reference clock (75kHz) for the duration of one cycle of the input signal into the 20-bit binary counter and measuring the cycle through the judgment of the pulse count.
This input terminal is also used as the IF input terminal, it is possible to switch across to the SC_{IN} terminal by setting '1' in the SC_{ON} bit.
The Manual bit, the G0 bit and the G1 bit are set at '0' during SC_{IN} setting.
Cycle measurement is started in the same way as the frequency measurement method, and the calculation data is loaded after the operational status of the BUSY bit has been confirmed.

(Note) The rectangular waveform must be input to the SC_{IN} terminal with the DC coupling at the logic level.

(Note) Note that the BUSY bit will not become '0' unless the clock has been input to SC_{IN}.

(4) Timer counter mode

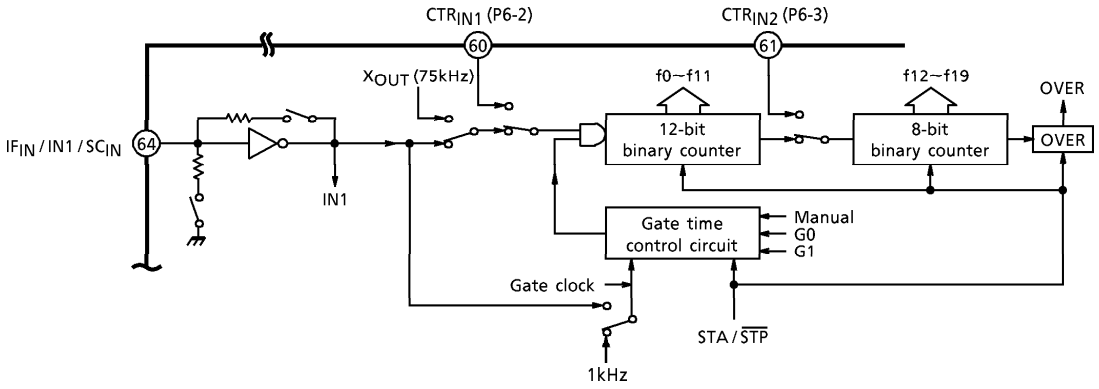
The IF counter may be used as a timer binary counter when it is not in use. The Manual bit, the G0 bit and the G1 bit are set at '1' to enable the counter to be used as a 75kHz reference clock in binary.
This counter is reset whenever the ST / $\overline{STP}$ bit is set at '1'.

(5) Counter division mode

The 20-bit binary counter can also be divided into a 12-bit and an 8-bit binary counter. This mode is set by setting the Split bit (ϕL14) and the Manual bit (ϕL15) at '1'. The CTRIN1 terminal is used for input into the 12-bit binary counter, and the CTRIN2 terminal is used for input into the 8-bit binary counter. Both of these terminals are also used as the P6-2 and P6-3 terminals, so it is necessary to establish the required setting. The data loaded into the 12-bit counter is the bits between f0 and f11 (ϕK11 to ϕK13) and the data loaded into the 8-bit counter is the bits between f12 and f19 (ϕK14 and ϕK15). These counters are reset when the STA / $\overline{STP}$ bit for both are set at '1'.

(Note) The rectangular waveform must be input to the CTR_{IN1} and CTR_{IN2} terminals with the DC coupling at the logic level.

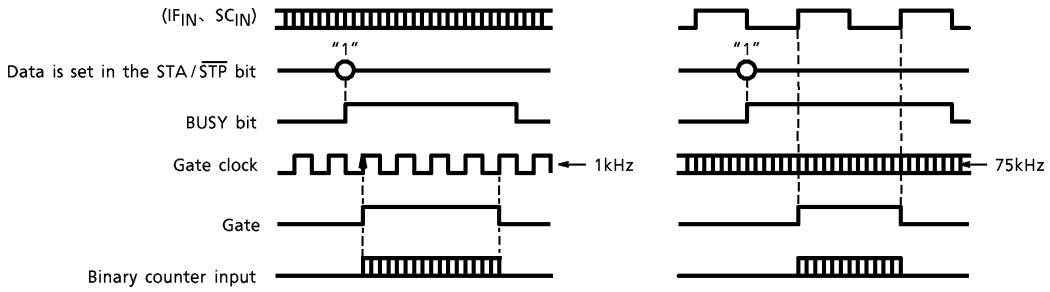
2. IF counter circuit configuration



The IF counter consists of the input amplifier, the gate time control circuit and the 12 + 8 bit binary counter.

The IF_{IN} input amplifier will enter the off mode when the PLL is in the off mode, but counter operations that do not require the input amplifier may still be carried out.

(Note) The IF_{IN} terminal is equipped with an amplifier, so small amplitude operations are possible with the condenser coupling.

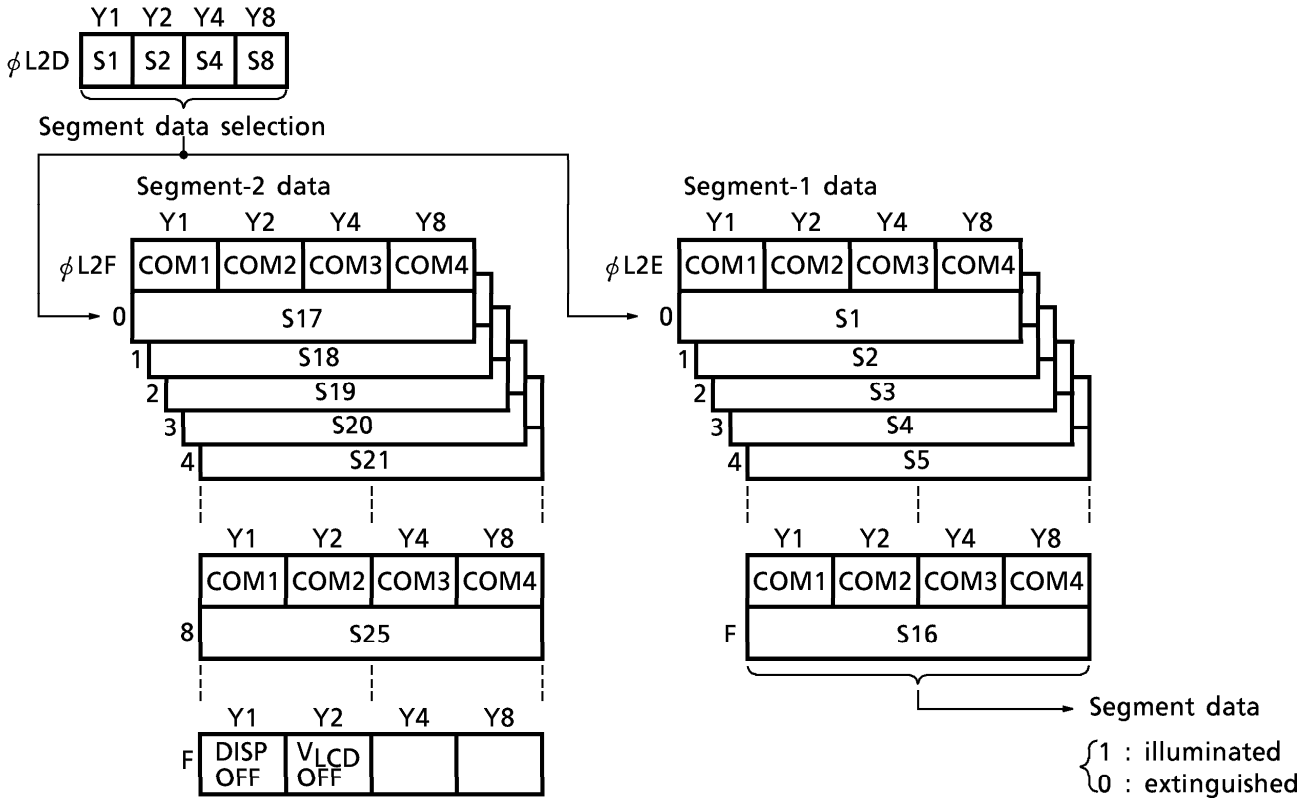


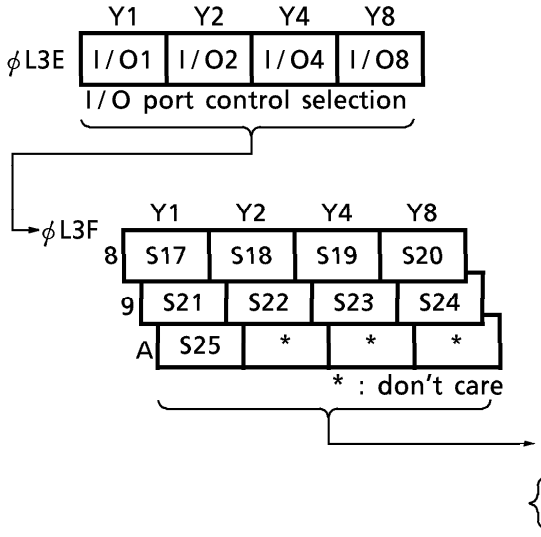
Frequency measurement automatic mode Cycle measurement mode

○ LCD driver

The LCD driver uses the 1/4 duty and 1/2 bias drive method (125Hz frame frequency).
The common output outputs the V_{LCD}, the $V_{LCD}/2$ (V_{EE}) and the GND electrical potential, and the segment output outputs the V_{LCD} and GND electrical potential.
A combination of four common outputs and 25 segment outputs enables a maximum of 100 segments to be illuminated.
The S22 to S25 segment output for the LCD driver are also used as the key return output for loading key matrix data.
The LCD driver is equipped with a constant voltage circuit (V_{EE} = 1.55V) for display purposes and a voltage doubler circuit (V_{LCD} = 3.1V) to increase this two-fold, and is a system that prevents contrast fluctuations in the LCD display even during voltage fluctuations.
It is also possible to switch to the I/O ports in units of one bit between S17 and S25, and this allows for programming that are perfectly matched to the system.

1. LCD driver port





(Note) The segment data controls illuminate / extinguish for the segments that correspond with the common output and segment output.

(Note) The DISP OFF bit is set at '1' when the system is reset and when the clock stop mode is cancelled.

(Note) The contents of the V_{LCD} OFF bit are reset at '0' when the system is reset.

SEG I/O control data (1: Segment output, 0: I/O port)

{ 1 : Segment output
0 : I/O port

The LCD driver control port consists of the segment data selection port and the segment data port. These ports are accessed with the OUT2 instruction for which [C_N = DH-FH] has been specified in the operand.

The segment data for the LCD driver is set with the segment data ports (ϕL2E and ϕL2F). The LCD display will be extinguished when the segment data port is set at '0' and will be illuminated when set at '1'. Also, the segment-2 data (ϕL2FF) specified with FH in the segment selection port becomes the DISP OFF bit and the V_{LCD} OFF bit. It is possible to extinguish all LCD displays with the DISP OFF bit without setting the segment data.

The common output enters a non-selected wave status when this bit is set at '1' and all LCD displays are extinguished. The contents of the segment is saved at this point, and the LCDs return to the previous display status when the DISP OFF bit is set at '0'.

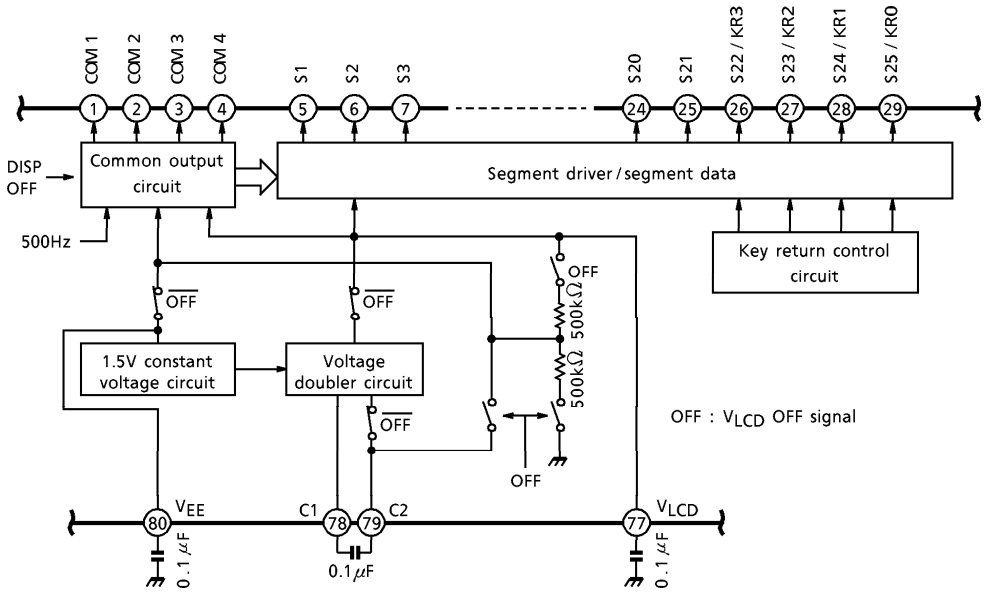
Segment data can be re-written when the DISP OFF status is in effect. The DISP OFF bit will also be set at '1' after resetting and after the execution of the CKSTP instruction.

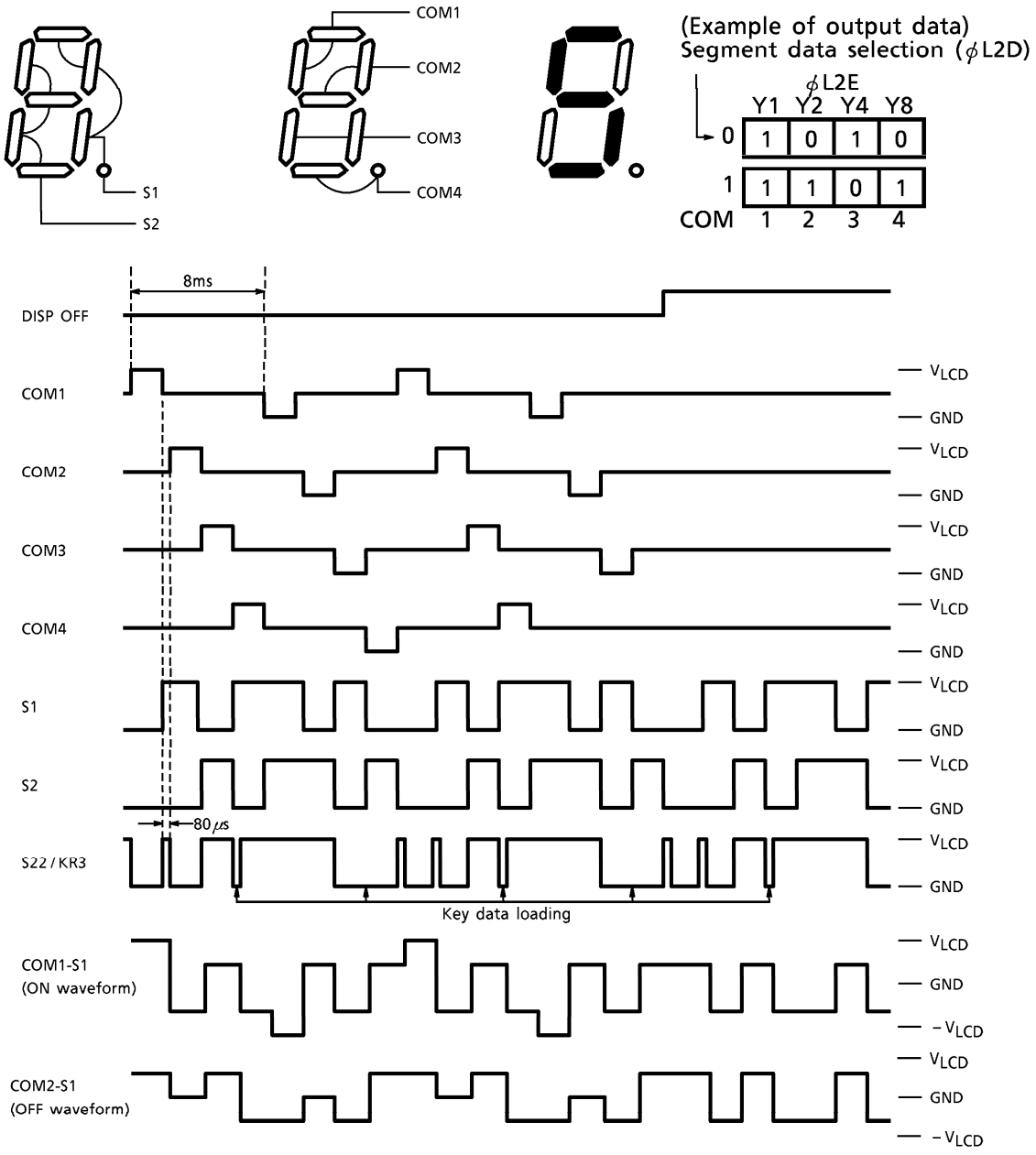
S17-S25 can be switched across to the I/O port, and control for this is performed with the SEG/IO control ports (ϕL3F8 to ϕL3FA). It becomes the segment output port when this port is set at '1' and the I/O port when set at '0'. It is necessary to pre-set the I/O port control selection (ϕL3E) in order to access this port.

In addition to this, it is also possible to use an external power source with the V_{LCD} OFF bit. This is effective when changing over to the crystal drive voltage.

This data is divided and set with the segment data selection port (ϕL2D). The S22 to S25 segment output terminals are also used as a key return timing signal for loading key matrix data. The segment output enters the GND level during key loading with this setting.

2. LCD driver circuit configuration





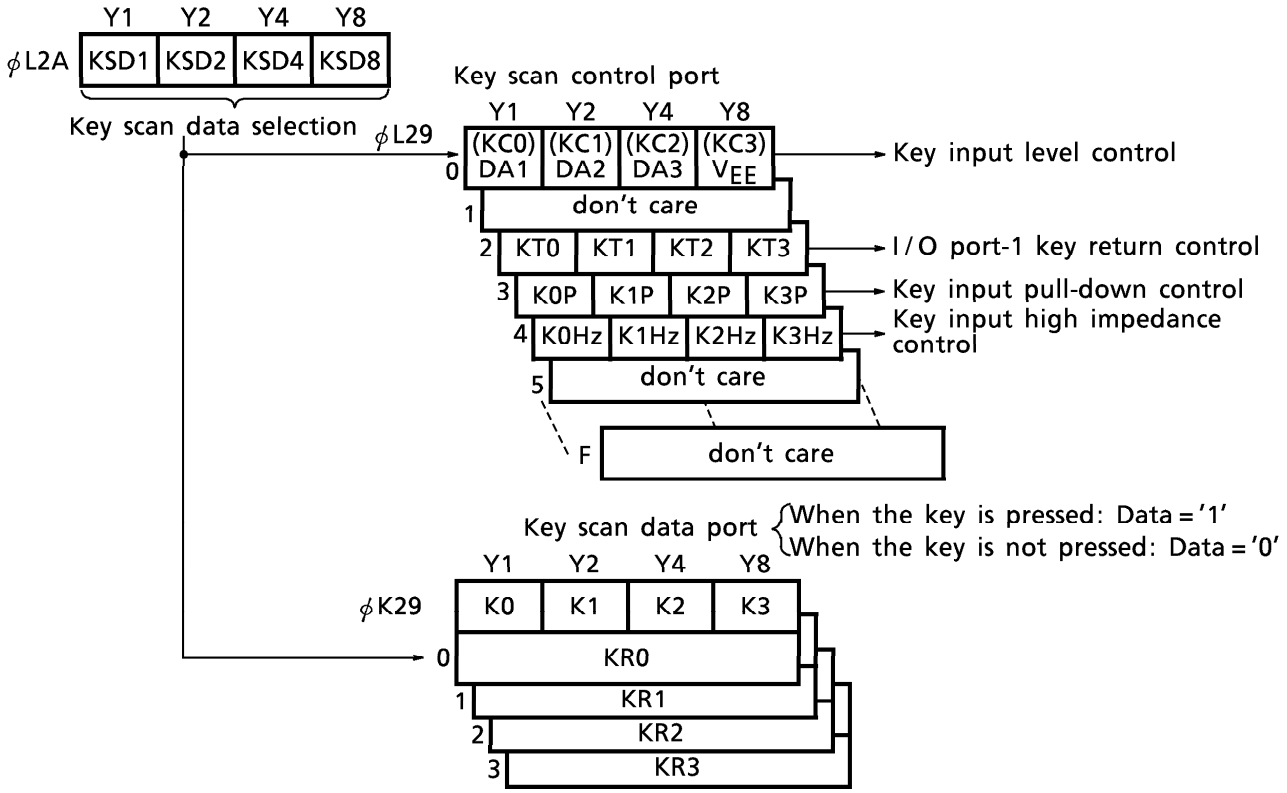
The electrical potential of the LCD driver waveform outputs V_{LCD} and GND potentials and half of the intermediate level potential of these potentials. S22-S25 also output key return signals during the switching. The 'L' level is entered when the segment output is 80μs during key return data loading.

(Note) The common and segment terminals enter the 'L' level during execution of the CKSTP instruction and during initialization.

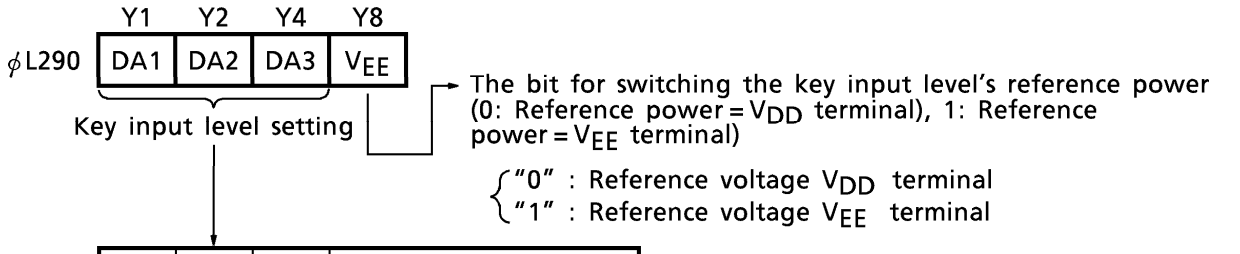
○ Key input and key return timing

There are three methods available for loading keys. The correct configuration should be selected for the system in use.

1. Key control port and key scan data port



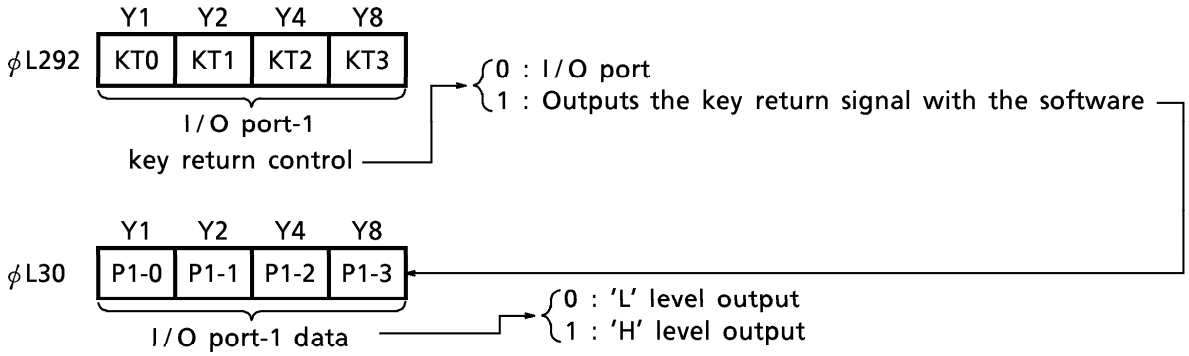
The key scan control port is used for setting the input level of the key input, the output format of I/O port-1 (P1-0 to P1-3) and the input format for key input.
The key data for when hardware key scans are performed is input into the key scan data port (φK29), and the key data is loaded into the data memory when this port is accessed.
This port is divided by the key scan data selection port (φL2A), and this enables the ports that correspond with the data set in this port to be accessed. '1' is added to the data in the key scan data selection port (φL2A) whenever the key scan control port (φL29) and the key scan data port (φK29) are accessed.



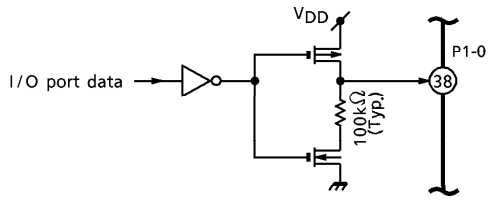
DA3	DA2	DA1	KEY INPUT LEVEL (VKREF)
0	0	0	1/9×V
0	0	1	2/9×V
0	1	0	3/9×V
0	1	1	4/9×V
1	0	0	5/9×V
1	0	1	6/9×V
1	1	0	7/9×V
1	1	1	8/9×V

V : When the V_{EE} bit = '1': 1.55 constant voltage (V_{EE})
When the V_{EE} bit = '0': Mains power voltage applied (V_{DD})

This port is for setting the key input level. The V_{EE} bit enables the reference power to be switched between the V_{EE} terminal and the mains power voltage (V_{DD} terminal). As indicated in the table above, the level of the divided reference power with DA bit and the key input terminal level are compared, and the result of this is output to the key scan data port and the key input data port.

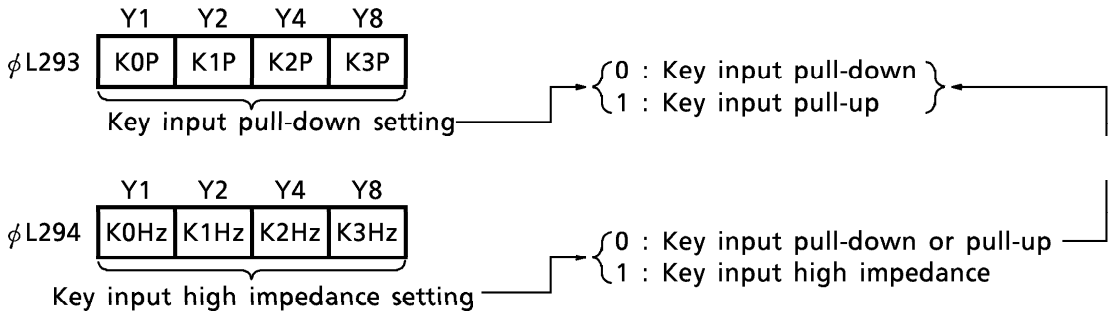


The following output format is assumed when '1' is set in the I/O port-1 key return control port, and the 'H' level and 'L' level setting for this output is controlled by the I/O port-1 data.



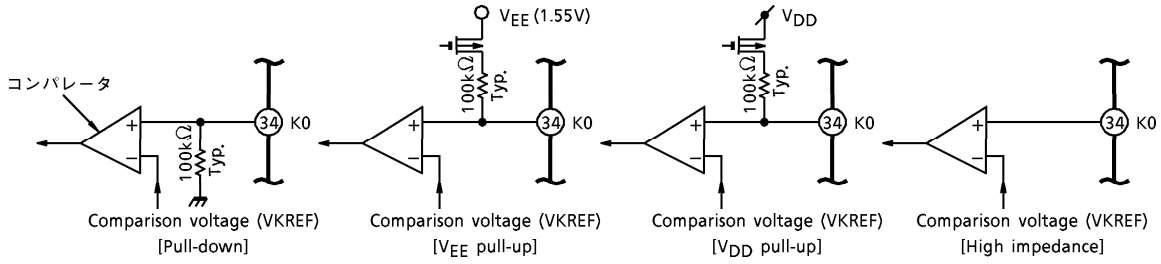
Output circuit when '1' is set in the KT0 bit

The bits between KT0 and KT3 correspond to the terminals between P1-0 and P1-3. These bits become I/O ports when set at '0'.
It is necessary to set the bits which correspond to the ports which operate key scanning within the I/O-1 control port to '1' (output port, [ϕL3F0]) when key scanning is operated from the I/O port-1 key return control port.

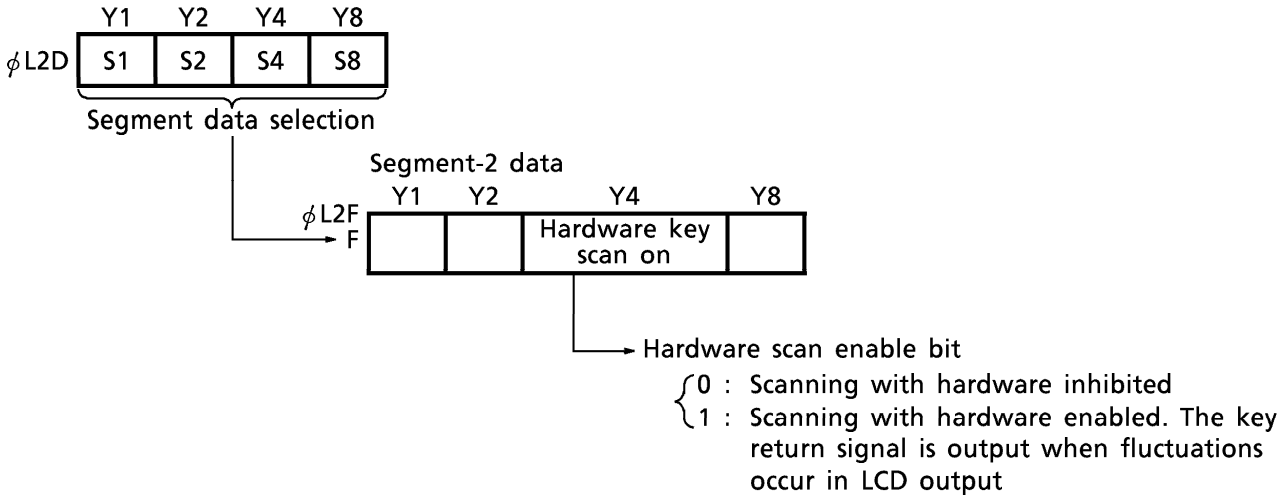


These ports are used for setting the input format of the key input. The input format can be set with the following conditions.

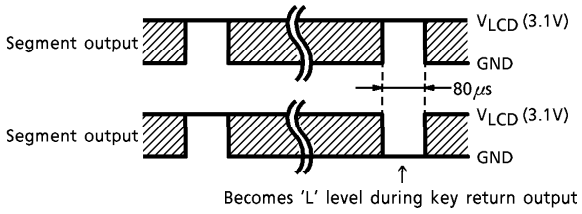
K0Hz	K0P	INPUT FORMAT
0	0	Pull-down
0	1	V_{EE} pull-up
1	0	V_{DD} pull-up
1	1	High impedance

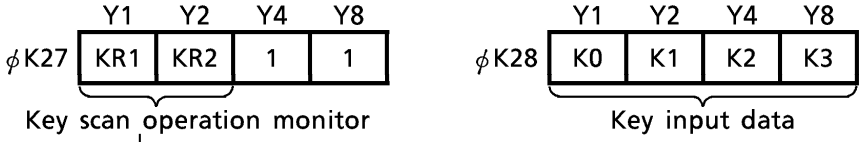


Pull-down is usually set during pull-down setting. Pull-up is only set when fluctuations exist with the LCD segment output, otherwise high impedance is set.
The key matrix is configured with a combination of the key input terminal and the key return output signal during pull-down and pull-up setting. This can also be used by the software as a sequential comparison method 3-bit A/D converter during high impedance setting.
The K0P to K3P bits and K0Hz to K3Hz bits correspond with the K0 to K3 terminals.
Execution of the WAIT instruction can be cancelled and CPU operations re-started by applying the 'H' level ($V_{DD} \times 0.6V$ or more) to key input terminals set with pull-down when in the wait mode. The CPU can only be re-started when in the 'H' level, and it should be noted that this operation is not possible during pull-up and high impedance setting.



The segment output is output with the timing outlined below when the hardware key scan enable bit is set as '1'. The key return signal is not output when this is set at '0'.

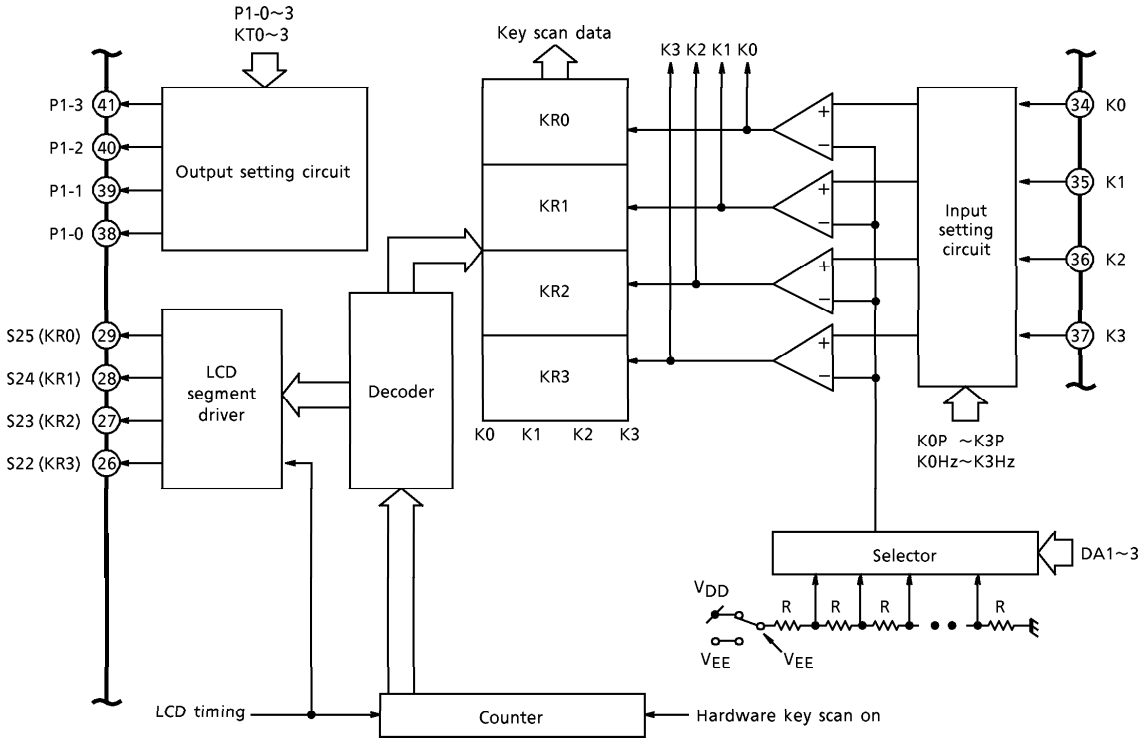




KR2	KR1	Scanning position
0	0	KR0 (S25)
0	1	KR1 (S24)
1	0	KR2 (S23)
1	1	KR3 (S22)

It is possible to reference the key scan monitor to determine which key line is currently being loaded when the hardware key scan is in operation.
Data loading during the hardware key scan is performed by accessing the key scan data ports (φL290 to φK293). On the other hand, each of the key input data port (φK28) digits are accessed during software key scans, and the result is loaded into the data memory. The input voltage becomes '1' when it is higher than the comparison voltage, and '0' when it is lower.

2. Key scan circuit configuration

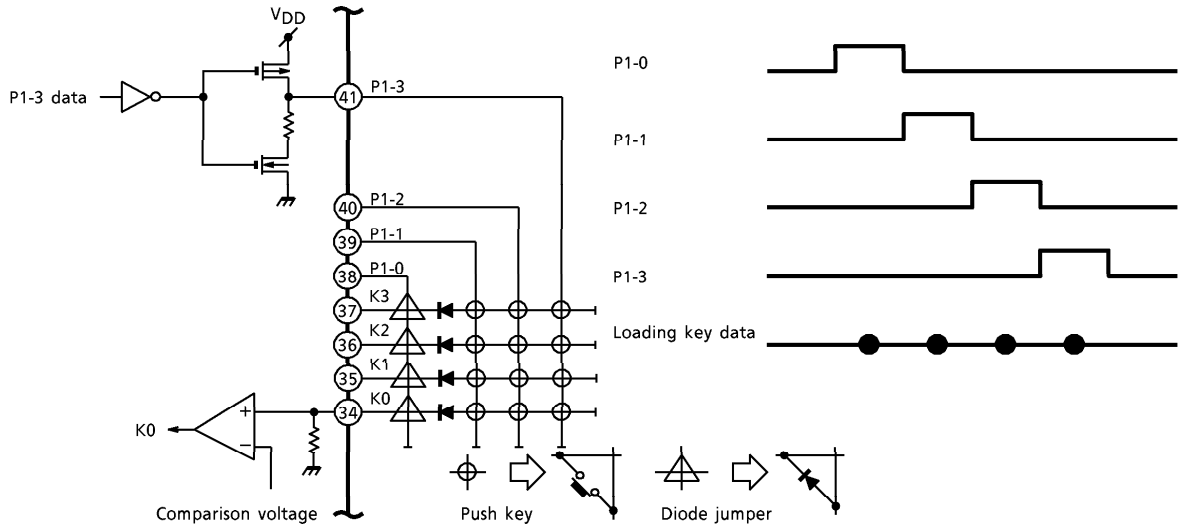


A key input area of the key scan circuit consists of, an input setting circuit, a 3-bit D/A converter, a comparator and a latch circuit for loading key data. The key return timing output area consists of an LCD segment driver, a counter and a decoder.

3. Key matrix configuration

The key matrix can be configured into the following three styles:

(1) Loading key data with software



The key matrix outlined above is configured when loading keys from programs. This method sets the key line I/O port-1 data (ϕL30) for which loading is required at the 'H' level and determines whether the key for loading the key input port data (ϕK28) into the data memory is valid or not. The I/O port-1 data for which loading is not required is set at the 'L' level at this point. The key input port data becomes '1' if the key is pressed, '0' if the key is not pressed, and the data is loaded into the data memory.

This method can only be used with a 4×4=16 key matrix, but as the key data is loaded at high speed and high resistance is entered into the P1-0 to P1-3 N channel FET areas, it is not necessary to fit a diode to the I/O for preventing reverse current flows caused by the key being pressed more than once.

The following data must be set in the relevant ports in order to use the method of loading data with software.

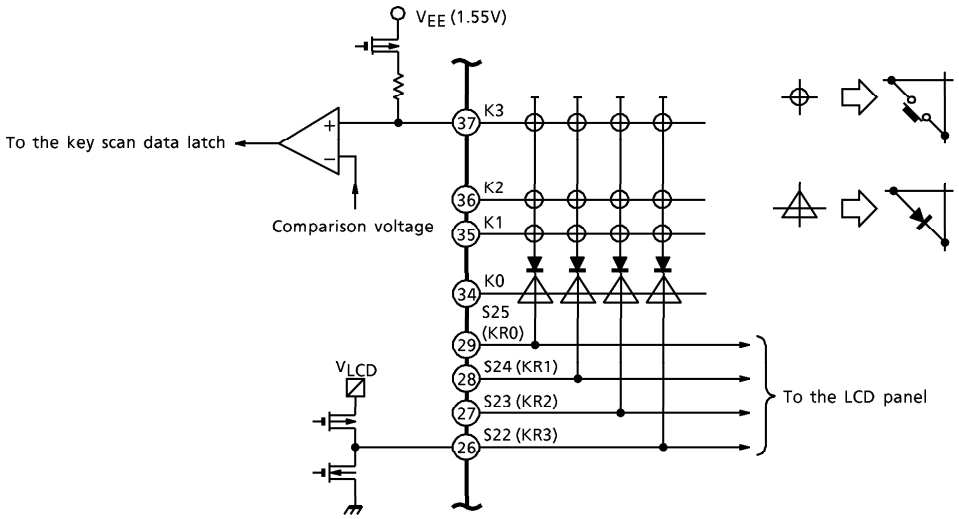
	DA1~DA3	V_{EE}	HARDWARE KEY SCAN ON	KT3~KT0	K0P~K3P	K0Hz~K3Hz
Without jumper	4/9 V_{DD}	0	0	All "1"	All "0"	All "0"
With jumper	3/9 V_{DD}	0	0	All "1"	All "0"	All "0"

(Note) Set the bits which corresponds with KT0 to KT3 at '0' when the I/O port-1 is to be used for I/O output.

(Note) The key input voltage applies a low voltage only to the diode's VF ($\simeq$0.6V) when a diode jumper is configured. For this reason, the threshold value of the key input is set at a low value. A diode to prevent reverse current flows caused by pressing the key more than once is also required, as indicated in the diagram above. This diode is not required in a diode jumper is not configured into the matrix.

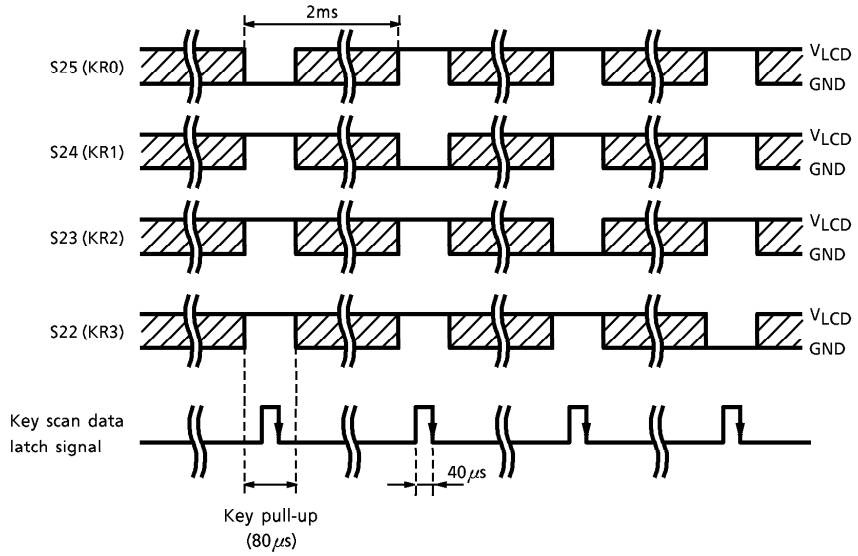
By setting the mode in this manner, the execution of the WAIT instruction is cancelled when the 'H' level ($V_{DD} \times 0.6V$ or more) is applied during the wait mode, and the CPU re-starts operations. (The 'H' level does not affect the DA1 to DA3 bit settings at this time.)

(2) Loading key data with LCD segment output



(Note) Configure of a maximum of $4 \times 4 = 16$ matrix is possible.

(Note) Push keys and diode jumpers cannot be combined in the same key line. Also, the diode jumper is to be located on the key return signal output.



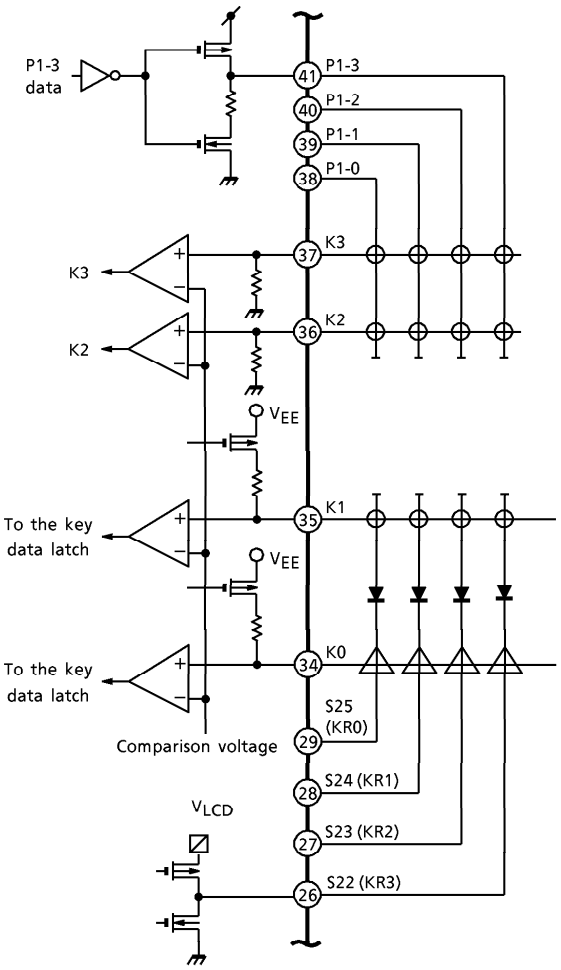
The key matrix outlined in the previous diagram is configured when loading data with LCD segment output. A diode to prevent reverse current is necessary with this key matrix, and care must be taken over the direction of the diode and the diode jumper.
With this matrix, the V_{LCD} (3.1V) electrical potential and the GND potential are output from the segment terminal when fluctuations occur with the LCD output. The segment signal to be loaded during key data loading becomes the GND potential when fluctuations occur in the LCD output, and the key input terminal is pulled up to the V_{EE} electrical potential. The V_{EE} level is input to the key input terminal when the key is not being pressed (or when no jumper diode exists), and the voltage for one diode ($\simeq$0.6V) is input from the GND potential when the key is being pressed (or when a jumper diode does exist).
The electrical potential that has been input is compared with the D/A output level, which is the V_{EE} electrical potential divided into nine, and the compared signal is latched onto the key scan data port that corresponds with the key loading segment's output line.
The key data is '1' when a key has been pressed and '0' when a key has not been pressed.
The following data must be set in the relevant ports in order to use the method of loading data with LCD segment output.

DA1~DA3	V_{EE}	HARDWARE KEY SCAN ON	KT0~KT3	K0P~K3P	K0Hz~K3Hz
6/9 V_{EE}	1	1	All "0"	All "1"	All "0"

The amount of time required for loading one line of key data is 2ms. Owing to this, the key scan data (ϕK29) is loaded into the data memory while referring to the key scan operation monitor.

(Note) As the diode jumper data is stored within the latch, it is possible to make the most effective use of data memory space by not loading the data into the data memory, but referring to the contents of the latch when necessary.

(3) Loading key data with LCD segment output and I/O ports



This method utilizes a combination of loading key data with software and loading key data with LCD segment output. (Refer to 3-(1), (2))
The main features of this method include the fact that high-speed key loading can be performed with the I/O ports, and the fact that the keys can be expanded by distributing the keys for which high-speed loading is not necessary to the LCD segment output area.
Key loading is performed by the key input data port (ϕK28) for the I/O ports and by the key scan data port (ϕK29) for the segment output.
Key input data port access is performed by switching across to the key input comparison voltage.
The settings for this method are as follows:

I/O port settings

KT0	KT1	KT2	KT3
1	1	1	1

Key input settings

K0P	K1P	K2P	K3P	K0Hz	K1Hz	K2Hz	K3Hz
1	1	0	0	0	0	0	0

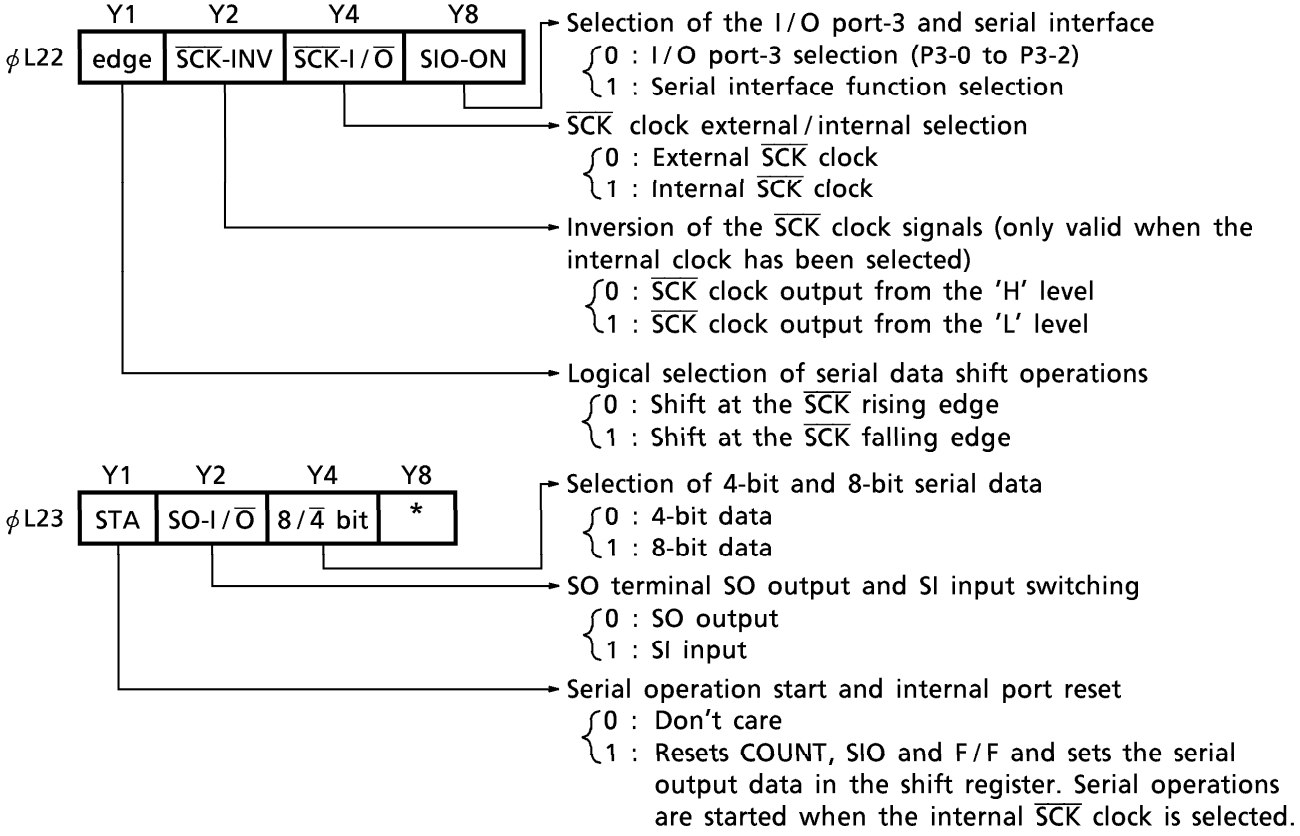
It is possible to make the settings for both the I/O ports and the LCD segment output in single bit units.

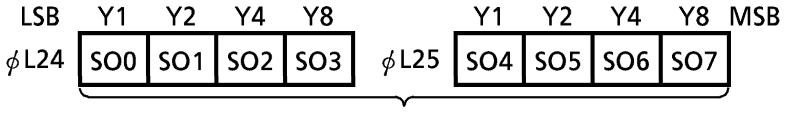
(Note) The execution of the WAIT instruction is cancelled when the 'H' level ($V_{DD} \times 0.6$ or more) is applied to the key input terminals for which pull-down has been set (the K2 and K3 terminals in the above diagram) during the wait mode, and the CPU re-starts operations.
(Note) As the segment key data is loaded when fluctuations occur in the LCD segment, the threshold value of the key input is different when the I/O port data is loaded simultaneously and the segment data will be loaded erroneously.
It is therefore necessary to control the situation with the key scan operation monitor.
(Note) Set all contents of the I/O port-1 control port (ϕL3F0) to '1' (output setting).

○ Serial interface

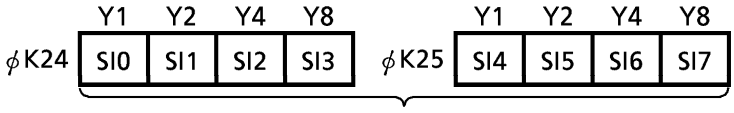
The serial interface is a serial I/O port that synchronizes the internal and external serial clocks and sends/receives 4-bit and 8-bit data. The data for LSIs for expansion purposes, micro-computers and other elements are sent and received by the SI, SO and $\overline{SCK}$ terminals.

1. The serial interface's control port and data port





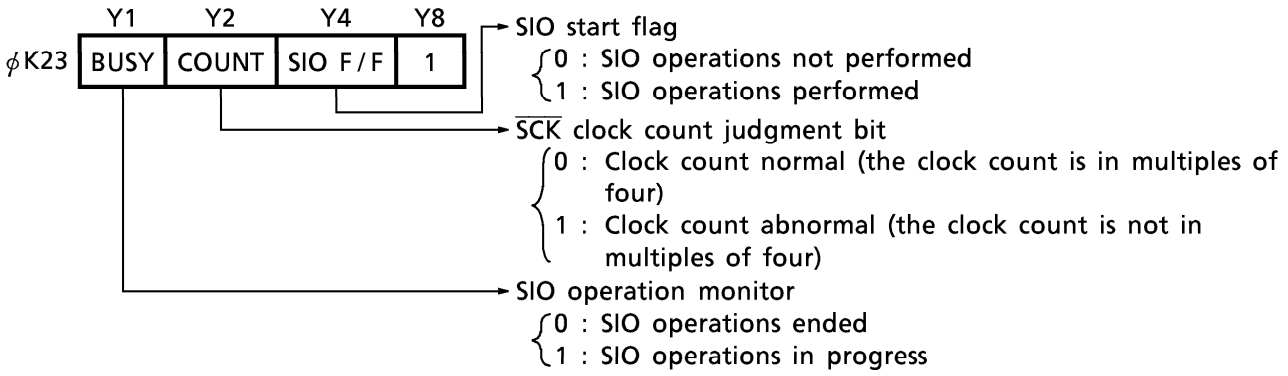
Serial output data: The data set in these ports is output in the serial format



Serial input data: It is possible to load data input in the serial format into the data memory

(Note) Serial input data can be accessed by directly accessing the contents of the shift register.

(Note) The contents of the serial interface control ports (ϕL22, ϕL23) will be set at '0' when the system is reset.



Serial interface control and serial data are accessed with the OUT2 and IN2 instructions for which [C_N = 2H-5H] has been specified in the operand.
The serial interface terminal is used together with the I/O port-3 P3-0, P3-1 and P3-2 terminals, and each of the I/O port-3 terminals are switched across to the SI, SO and $\overline{SCK}$ terminals by setting '1' in the SIOON bit.

(1) $\overline{SCK}$-INV and $\overline{SCK}$-I/O bits

The $\overline{SCK}$-INV and $\overline{SCK}$-I/O bits set the input waveform for the $\overline{SCK}$ terminal. The following modes are set with this bit data.

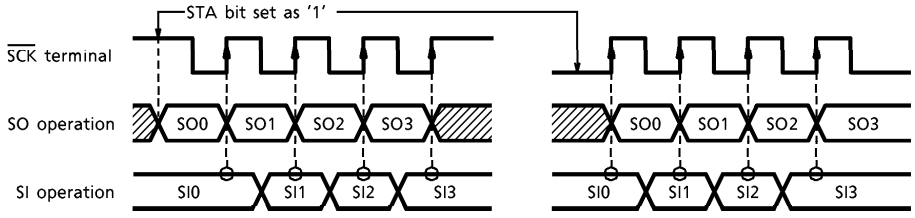
$\overline{SCK}$ terminal modes

INV	I/$\overline{O}$	I/O	$\overline{SCK}$ CLOCK WAVEFORM
0	1	Output	
1	1	Output	
*	0	Input	—

(2) edge bit

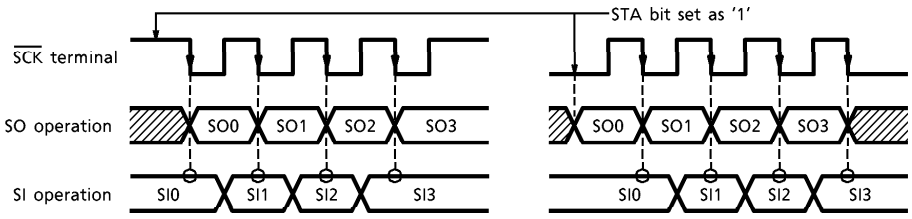
The edge bit sets the shift logic for the serial data. This data performs the following data shifting.

- When edge = '0'



The SO output is output with the rising edge of the $\overline{SCK}$ clock when the edge bit is set at '0', and the SI input is input to the shift register with the same rising edge.

- When edge = '1'

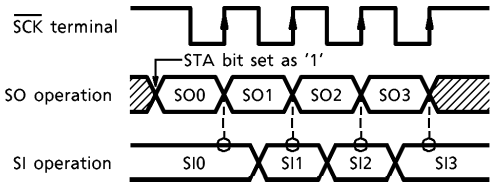


The SO output is output with the falling edge of the $\overline{SCK}$ clock when the edge bit is set at '1', and the SI input is input to the shift register with the same falling edge.

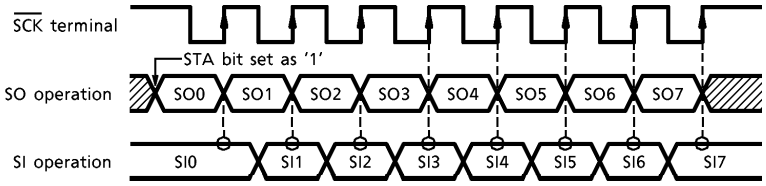
(3) 8 / $\overline{4}$ bit

The 8 / $\overline{4}$ bit selects the length of the serial data. The length of the serial data is set at 4 bits when this bit is '0', and at 8 bits when this bit is '1'. The $\overline{SCK}$ clock outputs four clocks when 4 bits are selected for the internal clock, and eight clocks when 8 bits are selected.

- When the 8 / $\overline{4}$ bit is '0' (however, edge = '0' and $\overline{SCK}$-INV = '0')

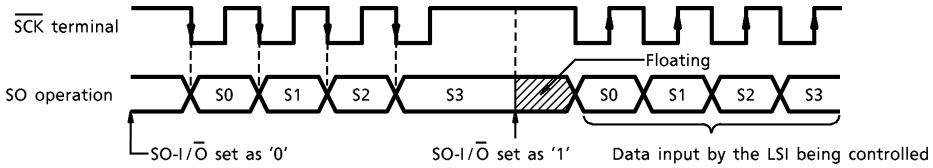


- When the 8 / $\overline{4}$ bit is '1' (however, edge = '0' and $\overline{SCK}$-INV = '0')



(4) SO-I/$\overline{O}$ bit

The SO-I/$\overline{O}$ bit sets the serial I/$\overline{O}$ for the SO terminal.
The SO terminal outputs serial data when the SO-I/$\overline{O}$ bit is set at '0', and the SO terminal is used for serial data input when this bit is set at '1'. The control of this bit enables T-BUS and other serial bus-type LSIs for performing data I/O with single terminals to be easily controlled.



(Note) It is necessary to pull up the SO terminal in the case of the above as a certain timing exists for floating.

This method sets the data in the serial output data port and performs SIO operations during sending, and performs SIO operations after the input setting of the SO terminal and loads the contents of the serial input data port into the data memory during receiving. The SI terminal can also be controlled as an I/O port (P3-0) when the serial interface has been selected. The I/O output (P3-0) can be used as the strobe pulse terminal for T-BUS and other elements.

(Note) The I/O control port's P3-0 bit that corresponds with the I/O port-3 must be set at '0' during SI terminal serial data input.

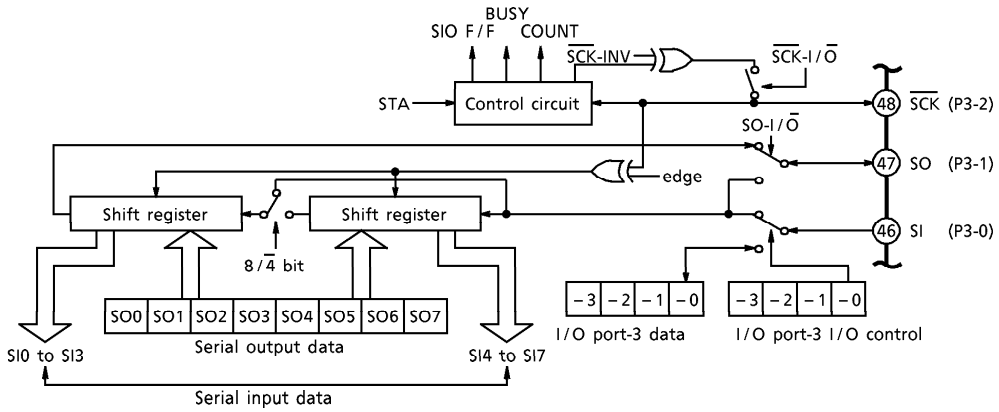
(5) Serial interface operation monitor

The operational status of the serial interface is determined by referencing the BUSY, COUNT and SIO F/F bits.
As the BUSY bit becomes '1' during SIO operations, control data switching and serial data access is performed when the BUSY bit is '0'.
The COUNT bit determines if data sending/receiving has been performed in units of 4 bits or not. This bit outputs '0' when shift operations are performed in multiples of four, and '1' when not performed in multiples of four.
'1' is set in the SIO F/F bit when the $\overline{SCK}$ terminal commences clock operations.
Both the COUNT bit and SIO F/F bit are reset to '0' when '1' is set in the STA bit. These two bits are mostly used when the $\overline{SCK}$ terminal sets external clocks. Normal operations are determined to exist when the external clock has been input and serial data has been sent or received.

(6) STA bit

The serial output data is set in the shift register whenever the STA bit is set at '1' during the $\overline{SCK}$ internal clock setting, the clock is output from the $\overline{SCK}$ terminal and shift operations are commenced. The COUNT bit and the SIO F/F bit are simultaneously reset at '0'.

2. Serial interface configuration



The serial interface consists of a control circuit, a shift register and an I/O port.

(Note) The SI terminal can be used as the I/O port-3 (P3-0) without modification.

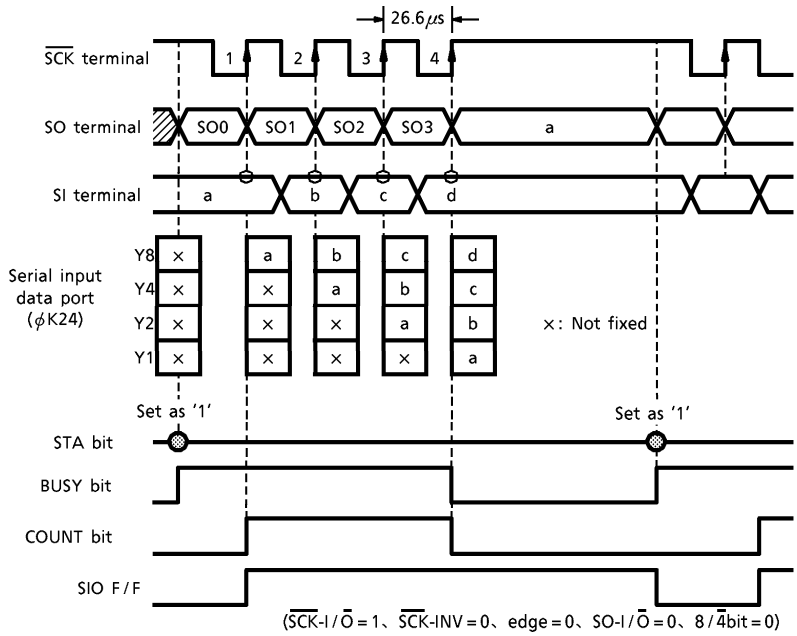
(Note) The data set in the serial output data area and the contents of the serial input data do not match.

(Note) The SI terminal set up for SI input, the $\overline{SCK}$ terminal set up for $\overline{SCK}$ input and the SO terminal set up for input will all follow the Schmidt input method.

3. Serial interface timing

The frequency of the clock output by the $\overline{SCK}$ terminal when the internal clock is set within the $\overline{SCK}$ clock is 37.5kHz (duty 50%).

The following is an example of the timing for the serial interface:

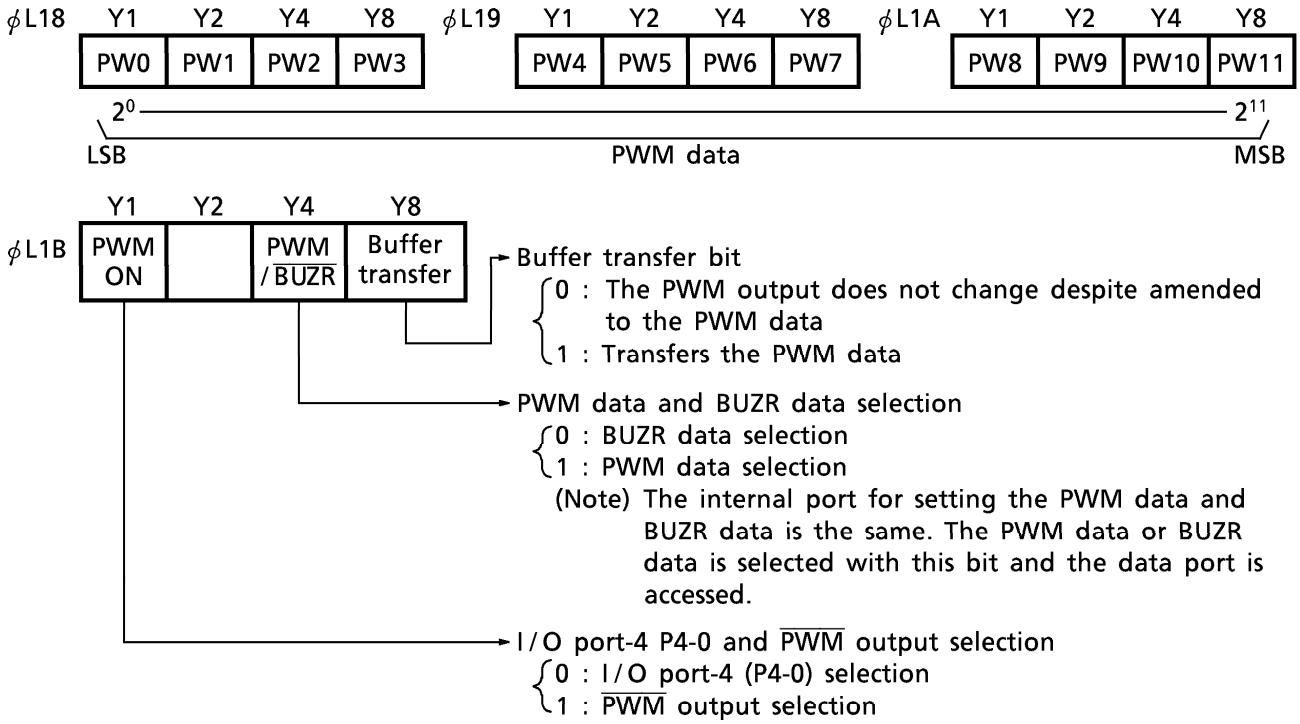


Example of serial interface timing

○ D / A conversion (pulse-width modulation: $\overline{PWM}$) output

The pulse-wide modulation output (PWM) can easily acquire D / A conversion output by the attachment of a low-pass filter. The $\overline{PWM}$ output is 12-bit resolution and is equipped with one-channel output.

1. PWM control port and data port



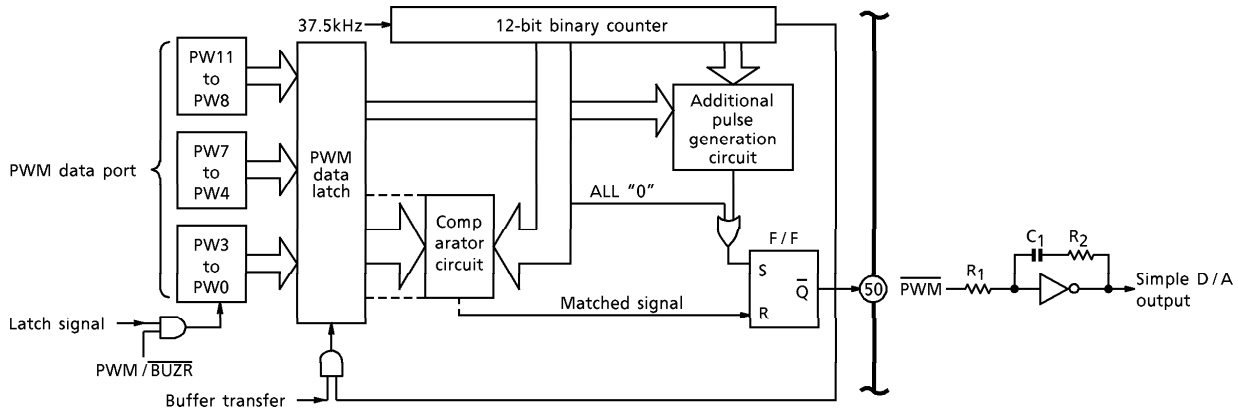
The $\overline{PWM}$ output is used together with the P4-0 I / O port. P4-0 switches across to the $\overline{PWM}$ output when '1' is set in the $\overline{PWM}$ ON bit.

PWM data setting is carried out after the PWM / $\overline{BUZR}$ bit is set at '1' and the buffer transfer bit is set at '0'. The PWM data is transferred to the PWM data latch when the buffer transfer bit is set at '1' after PWM data setting. A maximum of 109ms is required after the buffer transfer bit has been set at '1'. Owing to this, care must be taken as the $\overline{PWM}$ output will not be changed if this bit is set at '0' before the data can be sent to the PWM data latch.

PW0 is LSB and PW11 is MSB in the PWM data, and the eight high-order bits of data (PW4 to PW11) control the pulse output pulse width and the four low-order bits of data (PW0 to PW3) control the position to which the pulse added to one cycle of $\overline{PWM}$ output is to be output.

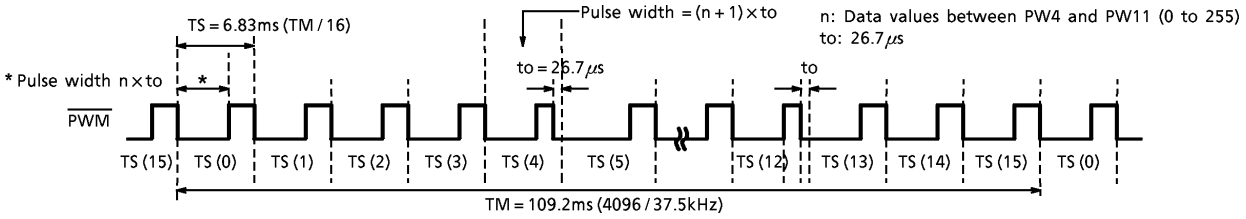
The setting for this data is performed with the OUT1 instruction for which [C_N = 8H-BH] has been specified in the operand.

2. $\overline{\text{PWM}}$ output circuit configuration



The $\overline{\text{PWM}}$ output circuit consists of a 12-bit binary counter, a PWM latch, comparator circuit and other elements.

3. $\overline{\text{PWM}}$ output waveform



Example of $\overline{\text{PWM}}$ output timing (Pulse added to TS (4) and TS (12): PW1 bit = '1')

PW DATA BITS	AREA IN WHICH THE ADDITIONAL PULSE IS OUTPUT (○ represents the position to which pulses have been added)															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PW0									○							
PW1					○								○			
PW2			○				○				○				○	
PW3		○		○		○		○		○		○		○		○

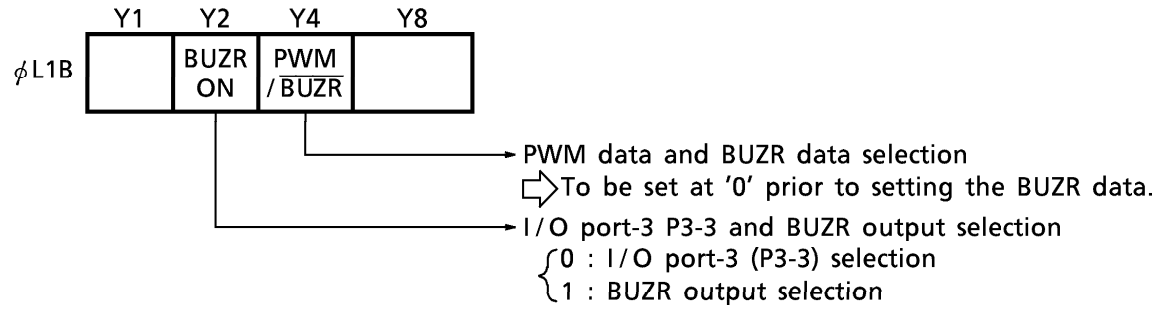
(Note) The above-mentioned numerals are the i values of TS (i)
Additional pulses are added to the positions marked above with circles when the PW data bit is set at '1'.

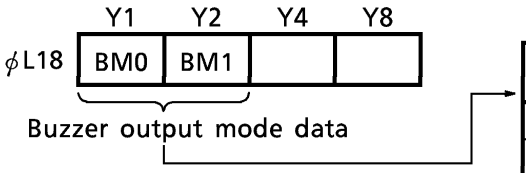
One cycle of the $\overline{\text{PWM}}$ output waveform is TM = 2^{12} / 37.5kHz = 109.2ms, and a pulse with a resolution of 12 bits is output. The eight high-order bits between PW4 and PW11 of the PWM data control the pulse width of the pulse output for the TS (TS = TM / 16 = 6.83ms) cycle. The low-level pulse width for the TS cycle becomes n × to (to = 1 / 37.5kHz) when the value of PW4 to PW11 is n (n = 0 to 255).
The four low-order bits between PW0 to PW3 control the position for the output of the to width's added pulse within the 16 TS (i) areas (i = 0 to 15) within the TM cycle. The low-level pulse width becomes (n + 1) × to in the areas to which the additional pulses are output. An additional pulse is output to the m location within the 16 TS (i) areas when the data for the low-order bit is m (m = 0 to 15). The area to which this additional pulse is added is shown in the above table. (However, the additional pulse will not be output to the TS (0) area.)

○ Buzzer output (BUZR)

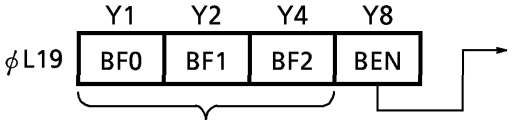
The buzzer output can be used to output tones and alarm tones to confirm key operations and the tuning scan mode. Buzzer types can be selected from a combination of four output modes and eight different frequencies.

1. Buzzer control port and data port





BM1	BM0	BUZZER OUTPUT MODE
0	0	Continual output (Mode A)
0	1	Staggered output (Mode B)
1	0	10Hz intermittent output (Mode C)
1	1	10Hz intermittent output with 1Hz intervals (Mode D)

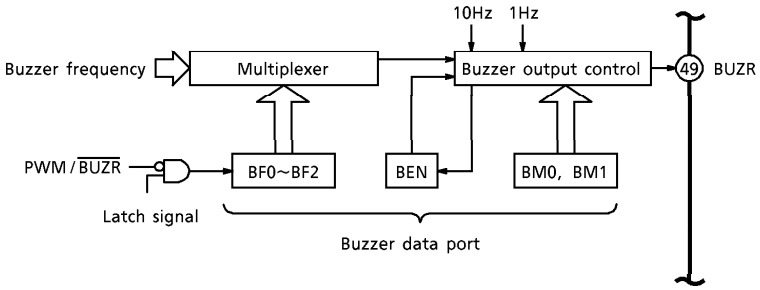


BF2	BF1	BF0	BUZZER FREQUENCY (kHz)	DUTY
0	0	0	0.625	1/2
0	0	1	0.75	1/2
0	1	0	1	2/3
0	1	1	1.25	1/2
1	0	0	1.5	1/2
1	0	1	2.08	2/3
1	1	0	2.5	1/2
1	1	1	3	2/3

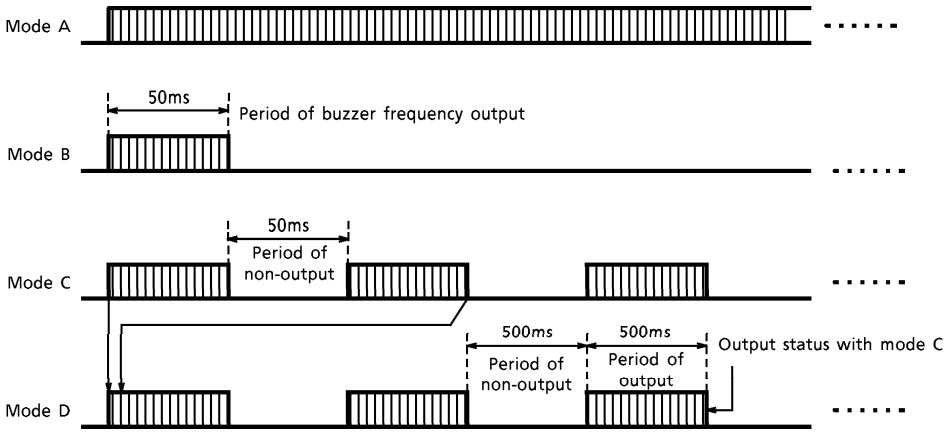
Buzzer output is used together with the P3-3 I/O port. '1' is set in the BUZR ON bit to set buzzer output. This switches P3-3 across to BUZR output.
Buzzer data setting (output mode, frequency selection and output enabling) is performed after the PWM/$\overline{\text{BUZR}}$ bit has been set at '0'.

(Note) The contents of the BM0, BM1, BF0 to BF2 and BEN bits are reset at '0' when the system is reset.

2. Buzzer circuit configuration



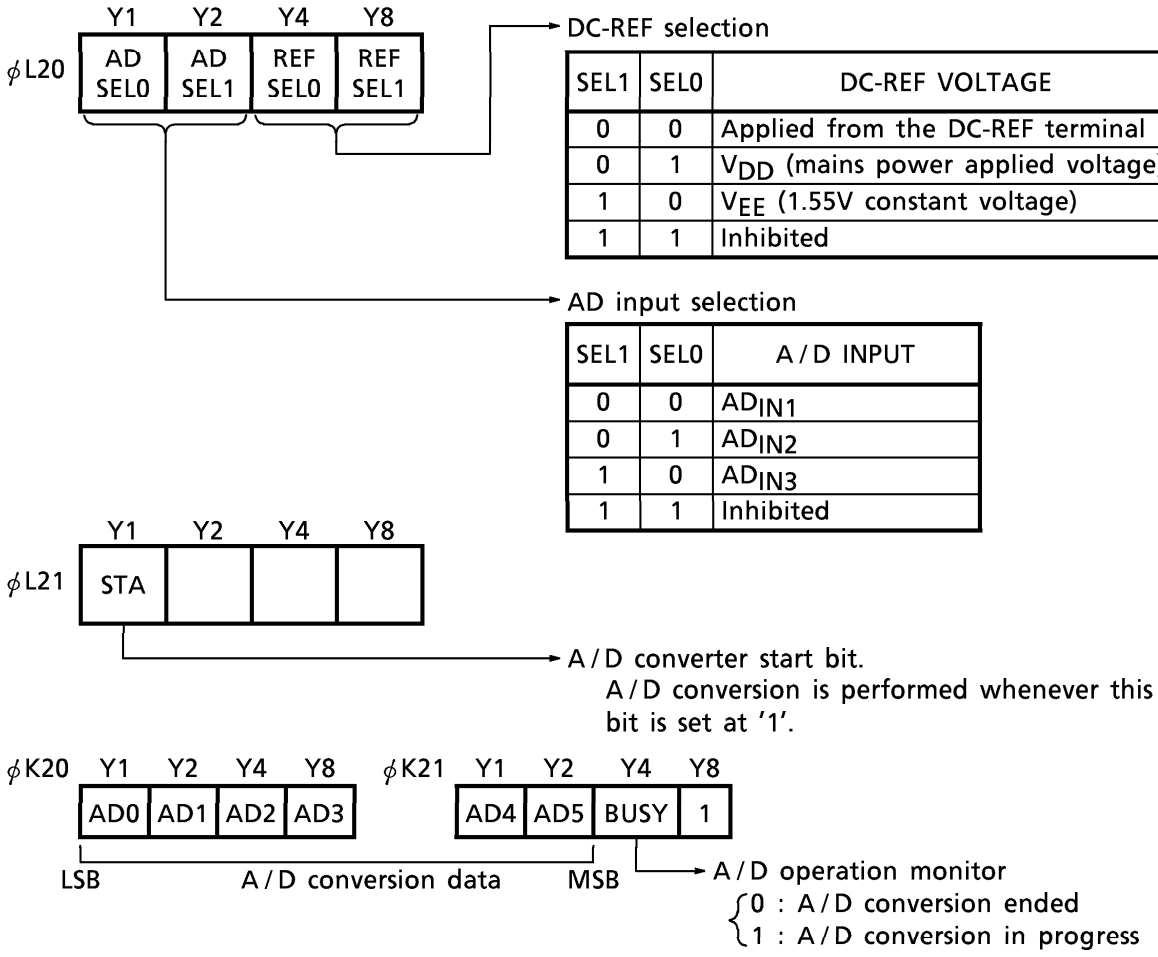
3. Buzzer output waveform



○ A / D converter

The A / D converter is used for measuring the strength of electric fields and the voltage of batteries with 3-channel 6-bit resolution.

1. A / D converter control port and data port

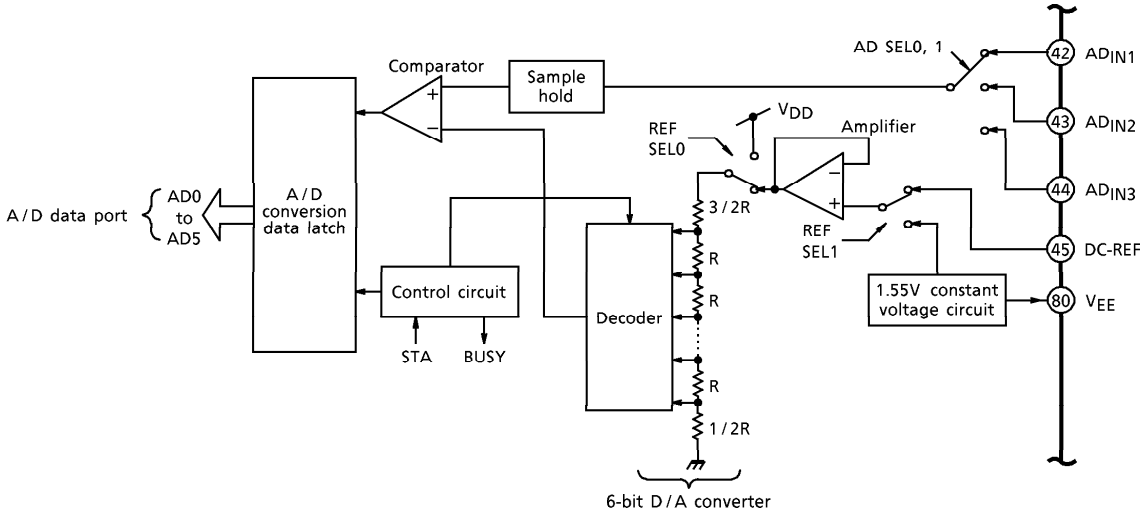


SEL1	SEL0	DC-REF VOLTAGE
0	0	Applied from the DC-REF terminal
0	1	V_{DD} (mains power applied voltage)
1	0	V_{EE} (1.55V constant voltage)
1	1	Inhibited

SEL1	SEL0	A / D INPUT
0	0	AD_{IN1}
0	1	AD_{IN2}
1	0	AD_{IN3}
1	1	Inhibited

The A / D converter has 6-bit resolution. It is possible to select between external voltage (DC-REF terminal), mains power voltage (V_{DD}) and 1.55V constant voltage (V_{EE}) for the standard voltage of A / D conversion. Also, the A / D conversion input follows the external input terminal 3-channel (terminals AD_{IN1} to AD_{IN3}) multiplex method.
Under normal circumstances, the standard voltage is set at the external voltage or mains power voltage, A / D conversion performed on the external input level, and the strength of the electrical field and volume level measured.
The A / D converter can also carry out measurements on batteries and mains power applied voltage. The battery signal is output when the battery or mains power applied voltage becomes low, and control moves across to the back-up mode.
The A / D converter performs A / D conversion whenever the STA bit is set at '1', and this is ended after seven machine cycles (280μs). A / D conversion completion is determined by referencing the BUSY bit, and the A / D conversion data is loaded into the data memory after conversion has finished.
The control for this is access by the OUT2 and IN2 instructions for which [C_N = 0H, 1H) has been specified in the operand.

2. A / D converter circuit configuration



The A / D converter consists of a 6-bit D / A converter, a comparator, an A / D conversion latch, a control circuit, an A / D data port, a 1.55V constant voltage circuit (mains power for the LCD driver) and other elements.
The A / D converter sequentially latches the data A / D converted with the 6-bit sequential comparison method onto the A / D conversion data latch.

(Note) The DC-REF terminal is built into the amplifier and is a high impedance input.

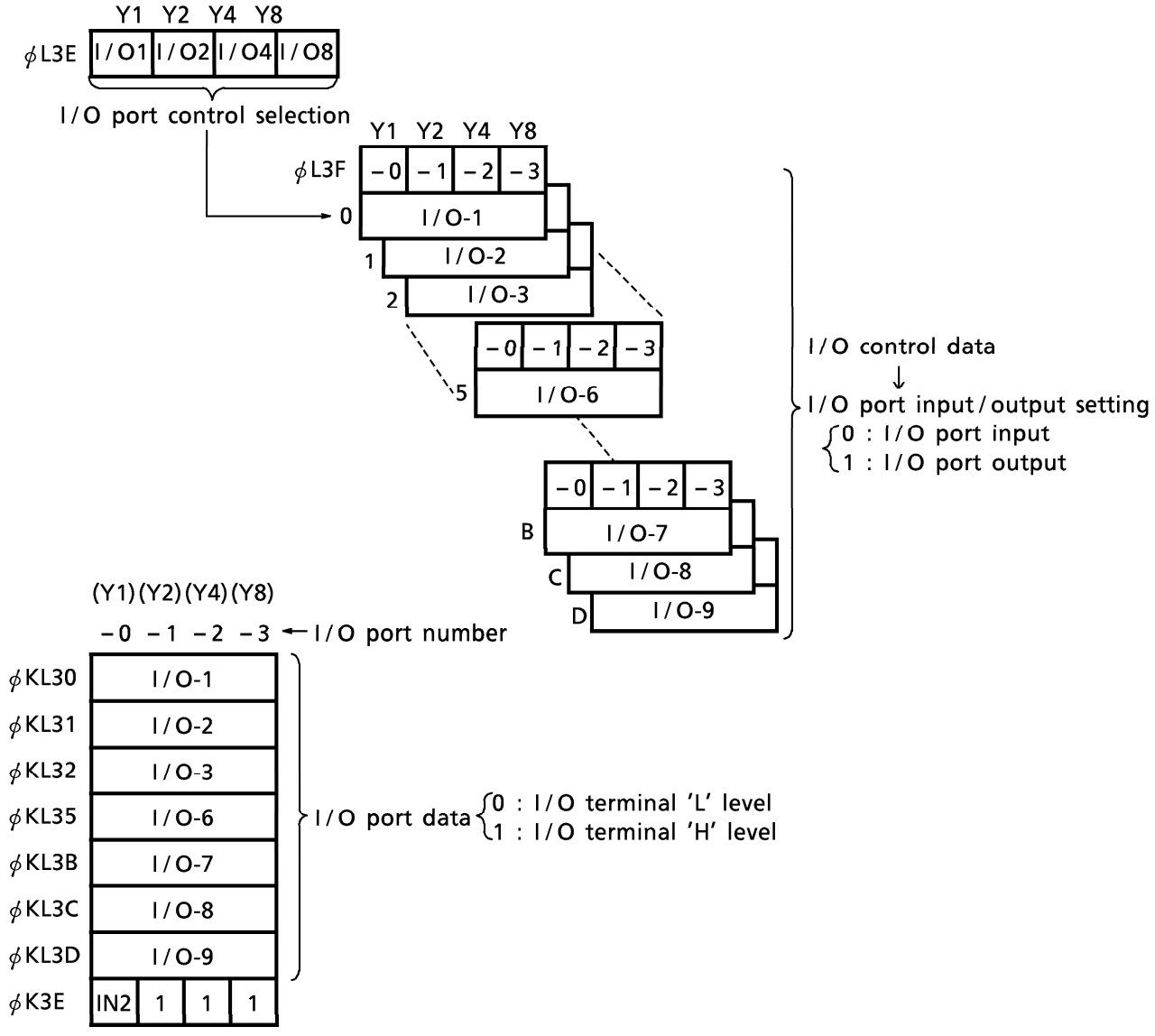
(Note) Correct data cannot be acquired even when the A / D conversion data is referenced during A / D conversion. Referencing must be performed after checking with the A / D operation monitor and confirming that conversion has finished.

(Note) '0' (input setting) must be set in the bit which corresponds with the I / O port-2 control port (ϕL3F1) for the terminals which use A / D input and DC-REF.

○ I/O ports

There are 36 I/O ports available between I/O port-1 and I/O port-9 which are used to input and output control signals. Of these 36 I/O ports, I/O port-2 is used together with the A/D converter input, I/O port-3 in used together with the serial interface and buzzer output, I/O port-4 is used together with the PWM output, I/O port-6 is used together with the counter input, and I/O ports 7, 8 and P9-0 are used together with the LCD driver output.
I/O ports 7, 8 and P9-0 are usually used as the LCD driver output.

1. I/O port control and I/O port data



(Note) The contents of the I/O control data between I/O-1 and IO-6 and the contents of P9-1 to 3 in I/O-9 are set at '0' (the input port) when the system is reset.

(Note) I/O-1, I/O-2 through to I/O-9 correspond to each of the P1-0 to 3, P2-0 to 3 through to P9-0 to 3 terminals.

The input/output for the I/O ports is set with the contents of the I/O control data port. '0' is set in the I/O control data port bit which corresponds to the relevant port when setting the input port, and '1' is set when setting the output port.
The I/O control data port is divided by the I/O control selection (ϕL3E). The data which corresponds with the port which is to be set in the I/O control selection is set and the I/O control data port is accessed. 1 is added to the I/O control selection data whenever the I/O control data port is accessed.
The output status of the I/O port is controlled by executing the OUT3 instruction which corresponds to each I/O port during output port setting. The contents of the data currently output can also be loaded into the data memory by executing the IN3 instruction.
The data input in the I/O port is loaded into the data memory by executing the IN3 instruction which corresponds to each I/O port during input port setting. The contents of the output latch will have absolutely no effect on the input data at this point.
Input for I/O ports 2 to 5 and 7 to 9 and terminals P6-0, P6-1 and IN2 use the NOR input structure. The NOR input gate signal ($\overline{\text{input instruction}}$) is set at on by executing the IN3 instruction which corresponds to each I/O port, and the input data is read into the memory. This enables abnormal mains current consumption to be constrained even when the input electrical potential reaches the intermediate potential. As the configuration prevents the generation of abnormal electrical current when these I/O ports are used with N-ch open drain output, low-potential pull-up is possible with the V_{DD} potential. I/O ports-1, P6-2 and P6-3 are always impedance input, so the previously-mentioned functions do not apply.
I/O ports 7, 8 and P9-0 are used together with the LCD driver output. As these terminals use the V_{LCD} terminal (step-up voltage) for output power, the 'H' level outputs V_{LCD} potential. Care must be taken here as the 'H' level has no load capabilities (a load resistance of 1MΩ or more is recommended.) Also, the input power uses the V_{DD} terminal power, so other I/O ports can be used in the same way during input setting.
I/O ports 2 to 4 and 6 are used together with the A/D converter and BUZR output. These ports are set in the I/O port when the system is reset. The I/O port is also set as an input port after the system has been reset, and the combined LCD driver and I/O port terminals are set in the LCD driver output.
The execution of the WAIT instruction and CKSTP instruction is cancelled and CPU operations are re-started when the status of the I/O port input specified in the input port changes with I/O port-1. Also, the MUTE port and MUTE bit are forcibly set to '1' during changes in the input status when the MUTE port's I/O bit is set at '1'.

(Note) I/O port input/output setting and the I/O port data will be set at 'don't care' during LCD driver setting with the combined LCD driver and I/O port terminals.

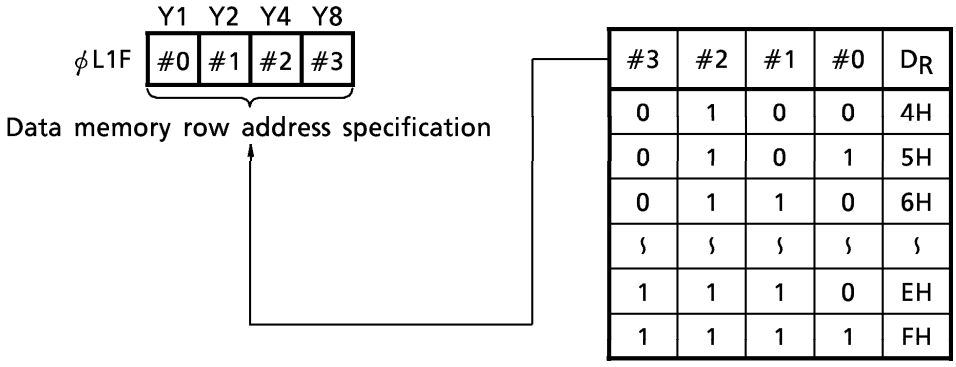
○ Register port

The G-register and data register outlined in the explanation on the CPU are also used as a single internal port.

1. G-register (ϕL1F)

This register addresses the data memory's row addresses (D_R = 4H to FH) during execution of the MVGD instruction and MVGS instruction. This register is accessed with the OUT1 instruction for which [C_N = FH] has been specified in the operand.

(Note) The contents of this register are only valid when the MVGD instruction and MVGS instruction are executed and are ineffective when any other instruction is executed.

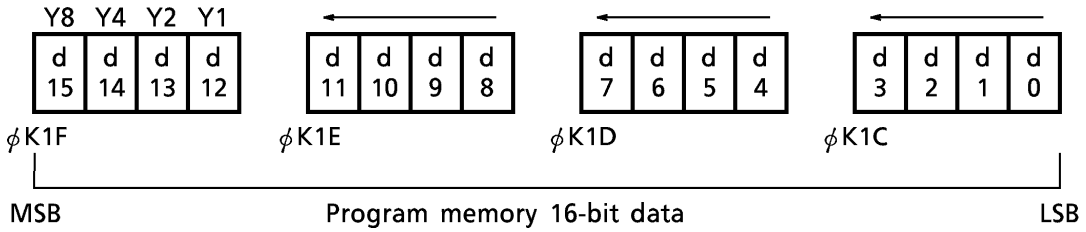


#3	#2	#1	#0	D_R
0	1	0	0	4H
0	1	0	1	5H
0	1	1	0	6H
≀	≀	≀	≀	≀
1	1	1	0	EH
1	1	1	1	FH

(Note) All of the data memory row addresses can be specified indirectly by setting data 0H to FH in the G-register. (D_R = 0H to FH)

2. Data registers (ϕK1C to ϕK1F)

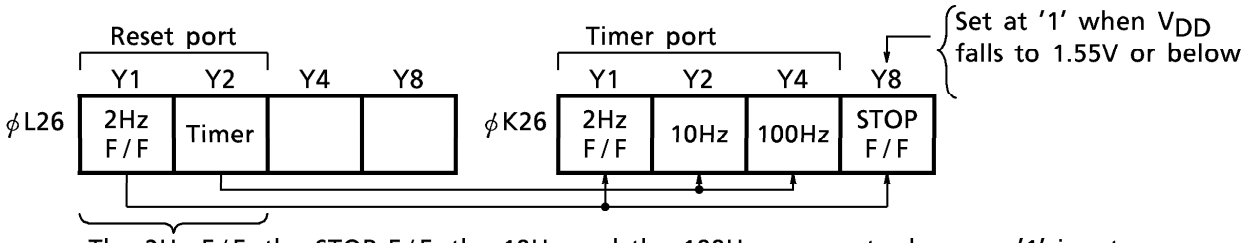
16-bit registers which load the program memory data when the DAL instruction is executed. The contents of this register are loaded into the data memory in 4-bit units with the execution of the IN1 instruction for which [C_N = CH to FH] has been specified in the operand.
This register can be used for loading LCD segment decoding operations, radio band edge data and the data related to binary to BCD conversion.



○ Timer and CPU stop functions

The timer is equipped with 100Hz, 10Hz and 2Hz F/F bits and is used for counting clock operations and the tuning scan mode, etc.
The CPU stop function suspends CPU operations with the voltage detection circuit when the applied V_{DD} voltage falls to 1.55V or below in order to prevent CPU malfunctions.

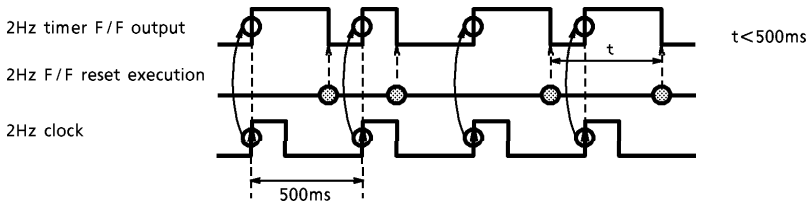
1. Timer port and STOP F/F bits



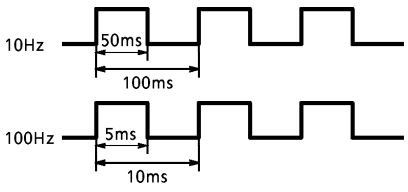
The timer port and STOP F/F bits are accessed with the OUT2 and IN2 instructions for which [C_N = 6H] has been specified in the operand.

2. Timer port timing

The 2Hz timer F/F is set with the 2Hz (500ms) signal and is reset by setting '1' in the reset port's 2Hz F/F. This bit is usually used as a clock counter.
The 2Hz timer F/F can only be reset with the reset port's 2Hz F/F, and incorrect counts will be output and correct times not acquired if not reset within a 500ms cycle.

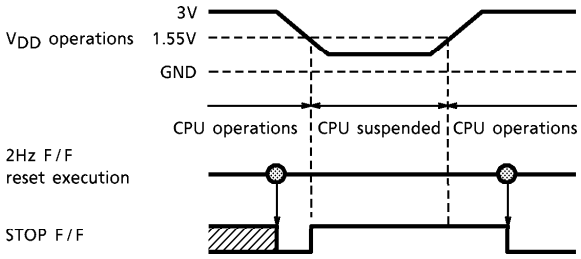


The 10Hz and 100Hz timers are output to 10Hz and 100Hz bits with respective cycles of 100ms and 10ms and a pulse of duty 50%. Counters at 1kHz or below will be reset whenever the reset port's timer bit is set at '1'.



3. CPU stop function and STOP F/F bit

The STOP F/F bit is set at '1' and CPU operations suspended if the applied V_{DD} voltage falls below 1.55V in order to prevent CPU malfunctions. The CPU program counter and the execution of instructions are suspended when a voltage of 1.55V or below is applied to the V_{DD} terminal. CPU operations are re-started when a voltage of 1.55V or higher is applied to the V_{DD} terminal. Abnormalities will occur with clocks during this period of non-operations. In this event, the situation will be determined by the contents of the STOP F/F, and initialization and clock correction will be performed if necessary.
The STOP F/F bit will be reset to '0' whenever the reset port's 2Hz F/F is set at '1'.

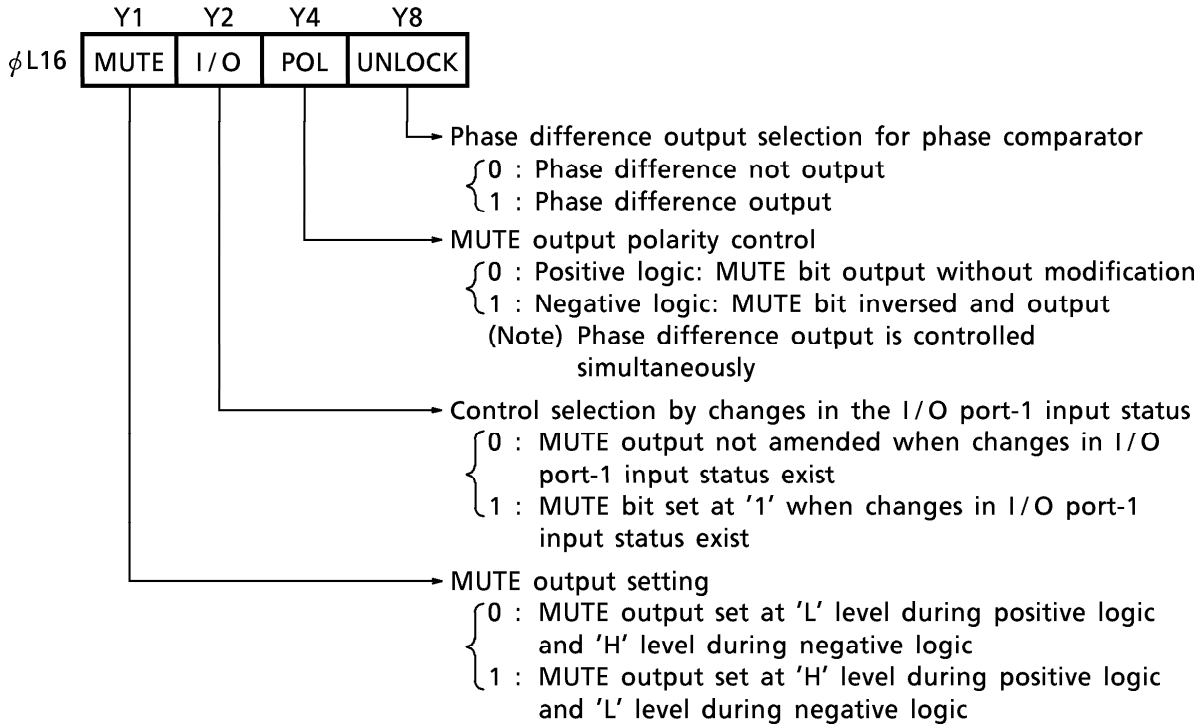


(Note) The contents of the timer port and STOP F/F will be reset at '0' when the system is reset and when the CKSTP instruction is executed.
(Note) The CKSTOP mode cannot be executed during clock stop mode setting if the voltage applied to the V_{DD} is 1.55V or below, so care must be taken over the mains power voltage timing when setting the radio off and similar operations.
(Note) The CPU stop function will be inhibited when all of the internal test port (ϕL1C) bits between #0 and #3 are set at '1'.

○ MUTE output

This is a dedicated 1-bit CMOS output port for muting control purposes.

1. MUTE port



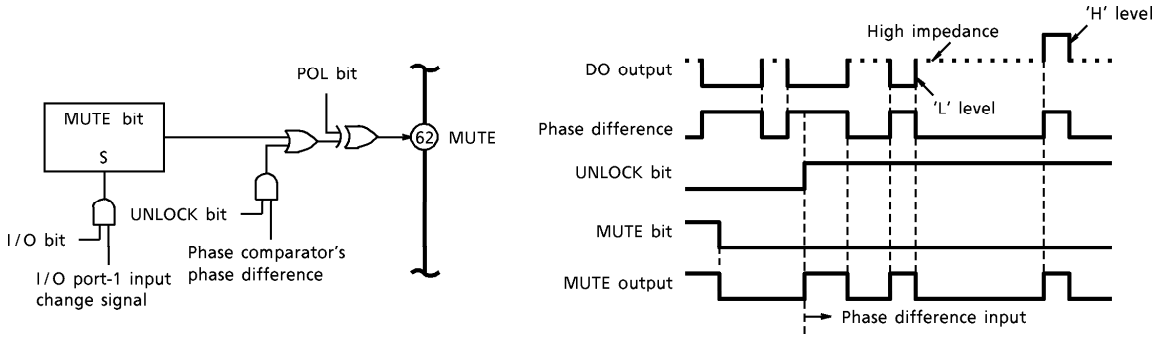
This port is accessed with the OUT1 instruction for which [C_N = 6H] has been specified in the operand. MUTE output is used for muting control. A function to set the MUTE bit at '1' during band switching with I/O port-1 input is also available.

This function prevents noise from being generated during linear circuit switching when band switching is performed with the I/O port-1 input for slide switches. Control for this function is performed with the contents of the I/O bit.

The POL bit sets the logic for MUTE output.

MUTE output can also control muting with the use of the phase difference output. The PLL element is output as a pulse when the lock status is not in effect (in the unlock status). A low-pass filter is attached to the MUTE output in this event, and the output is used for MUTE output. This can be selected with the UNLOCK bit.

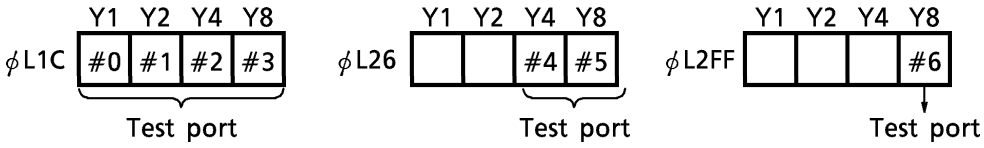
2. MUTE output configuration and timing



(Note) When the POL bit = '0'.
(Note) A low-pass filter must be attached to the MUTE output when the phase comparator's phase difference output is used.

○ Test port

An internal port for testing device functions. Access is performed with the OUT1 instruction for which [C_N = CH] has been specified in the operand, and the OUT2 instruction for which [C_N = 6H] has been specified in the operand. '0' is usually set with the program.



Bit #6 of the test port can suspend the LCD driver output internal frame signal. Suspension of the frame signal outputs all segment output as segment data inversed output. Segment output will usually enter the 'L' level when all segment data bits between COM1 and COM4 are set to '1', and usually enters the 'H' level when all bits are set to '0'. This can be used as a simple output port in systems which do not use LCD output. External mains power is to be set with the V_{LCD} OFF bit and a connection established between the V_{DD} terminal and V_{LCD} terminal in this case.
The CPU stop function is inhibited when all test port bits between #0 and #3 are set at '1' and enabled when set at '0'. The CPU stop function must be inhibited when external mains power voltage detection is to be performed.

(Note) The contents of bits #4 to #6 are reset to '0' and bits #0 to #3 are set to '1' when the system is reset.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~4.0	V
Input Voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power Dissipation	P_D	100	mW
Operating Temperature	T_{opr}	−10~60	°C
Storage Temperature	T_{stg}	−55~125	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, Ta = 25°C, V_{DD} = 3.0V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN	TYP.	MAX	UNIT
Range Of Operating Supply Voltage	V_{DD}	—	(*)		1.8	~	3.6	V
Range Of Memory Retention Voltage	V_{HD}	—	Crystal oscillation stopped (CKSTP instruction executed) (*)		1.0	~	3.6	
Operating Current	I_{DD1}	—	Under ordinary operation No output load FM_{IN} = 230MHz input	V_{DD} = 3.0V	—	7.0	12	mA
			Under ordinary operation No output load FM_{IN} = 130MHz input	V_{DD} = 3.0V	—	6.0	10	
	I_{DD2}	—	Under CPU operation only (PLL off, display turned on)	V_{DD} = 3.0V	—	50	100	μA
	I_{DD3}	—	Soft Wait mode (Crystal oscillator, display circuit operating, CPU stopped, PLL off)		—	30	60	
	I_{DD4}	—	Hard Wait mode (crystal oscillator operating only)		—	20	40	
Memory Retention Current	I_{HD}	—	Crystal oscillation stopped (CKSTP instruction executed)		—	0.1	10	
Crystal Oscillation Frequency	f_{XT}	—	(*)		—	75	—	kHz
Crystal oscillation Start-up Time	t_{ST}	—	Crystal oscillation f_{XT} = 75kHz		—	—	1.0	s

VOLTAGE DOUBLER CIRCUIT

Voltage Doubler Reference Voltage	V_{EE}	—	GND reference (V_{EE})	1.35	1.55	1.75	V
Constant Voltage Temperature Characteristics	D_V	—	GND reference (V_{EE})	—	−5	—	mV/°C
Voltage Doubler Boosting Voltage	V_{LCD}	—	GND reference (V_{LCD})	2.7	3.1	3.5	V

For conditions marked by an asterisk (*), guaranteed when V_{DD} = 1.8 to 3.6V, Ta = −10 to 60°C

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT

OPERATING FREQUENCY RANGES FOR PROGRAMMABLE COUNTER AND LF COUNTER

FM_{IN} (VHF Mode)	f_{VHF}	—	Sine wave input when V_{IN} = 0.3V_{p-p} (*) Sine wave input when V_{IN} = 0.2V_{p-p}, V_{DD} = 1.8~3.0V, Ta = −10~60°C	50	~	230	MHz
FM_{IN} (FM Mode)	f_{FM}	—	Sine wave input when V_{IN} = 0.2$_{p-p}$ (*)	40	~	130	
AM_{IN} (HF Mode)	f_{HF}	—	Sine wave input when V_{IN} = 0.2$_{p-p}$ (*)	1	~	45	
AM_{IN} (LF Mode)	f_{LF}	—	Sine wave input when V_{IN} = 0.2$_{p-p}$ (*)	0.5	~	12	
IF_{IN}	f_{IF}	—	Sine wave input when V_{IN} = 0.2$_{p-p}$ (*)	0.35	~	12	
Input Amplitude	V_{IN}	—	FM_{IN} input (VHF mode) (*)	0.3	~	V_{DD} − 0.8	V_{p-p}
			FM_{IN} input (VHF mode) V_{DD} = 1.8~3.0V, Ta = −10 to 60°C	0.2	~	V_{DD} − 0.8	
			FM_{IN} (FM mode), AM_{IN}, IF_{IN} input (*)	0.2	~	V_{DD} − 0.8	

LCD COMMON OUTPUT / SEGMENT OUTPUT, GENERAL-PURPOSE I / O PORTS
(COM 1 to COM4, S1 to S16, S17 / P7-0 to S25 / P9-0, P9-1 to 3, IN2)

Output Current	"H" Level	I_{OH1}	—	V_{LCD} = 3V, V_{OH} = 2.7V	−0.4	−0.8	—	mA
	"L" Level	I_{OL1}	—	V_{LCD} = 3V, V_{OL} = 0.3V	0.4	0.8	—	mA
Output Voltage 1 / 2 Level		V_{BS}	—	No load	1.35	1.55	1.75	V
Input Leak Current		I_{LI}	—	V_{IH} = V_{DD}, V_{IL} = 0V (when using I / O port, IN port)	—	—	±1.0	μA
Input Voltage	"H" Level	V_{IH1}	—	(when using I / O port, IN port)	V_{DD} × 0.6	~	V_{DD}	V
	"L" Level	V_{IL1}	—	(when using I / O port, IN port)	0	~	V_{DD} × 0.1	

I / O PORT (P1-0 to P1-3)

Output Current	"H" Level	I_{OH1}	—	V_{OH} = 2.7V	−0.4	−0.8	—	mA
	"L" Level	I_{OL1}	—	V_{OL} = 0.3V	0.4	0.8	—	mA
Input Leak Current		I_{LI}	—	V_{IH} = 3.0V, V_{IL} = 0V (when using I / O port)	—	—	±1.0	μA
Input Voltage	"H" Level	V_{IH2}	—	(When using I / O port)	2.4	~	3.0	V
	"L" Level	V_{IL2}	—	(When using I / O port)	0	~	0.6	
N-ch Load Resistance		R_{ON}	—	V_{OL} = 3.0V (When connected to load resistance)	50	100	200	kΩ

For conditions marked by an asterisk (*), guaranteed when V_{DD} = 1.8 to 3.6V, Ta = −10 to 60°C

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
$\overline{HOLD}$ INPUT PORT								
Input Leak Current		I_{LI}	—	V_{IH} = 3.0V, V_{IL} = 0V	—	—	± 1.0	μA
Input Voltage	"H" Level	V_{IH3}	—	—	2.4	~	3.0	V
	"L" Level	V_{IL3}	—	—	0	~	1.2	
A / D CONVERTER (AD_{IN1} to AD_{IN3}, DC-REF)								
Analog Input Voltage Range		V_{AD}	—	AD_{IN1}~AD_{IN3}	0	~	V_{DD}	V
Analog Reference Voltage Range		V_{REF}	—	DC-REF, V_{DD} = 2.0~3.6V	1.0	~	V_{DD} × 0.9	V
Resolution		V_{RES}	—	—	—	6	—	bit
Conversion Total Error		—	—	V_{DD} = 2.0~3.6V	—	± 1.0	± 4.0	LSB
Analog Input Leak		I_{LI}	—	V_{IH} = 3.0V, V_{IL} = 0V (AD_{IN1}~AD_{IN3}, DC-REF)	—	—	± 1.0	μA
KEY INPUT PORT (K0 to K3)								
Key Input Voltage Range		V_{KI}	—	—	0	~	V_{DD}	V
A / D Conversion Resolution		V_{RES}	—	—	—	3	—	bit
A / D Conversion Total Error		—	—	V_{DD} = 1.8~2.0V	—	—	± 1.5	LSB
				V_{DD} = 2.0~3.6V	—	—	± 0.5	
N-ch / P-ch Input Resistance		R_{IN1}	—	—	50	100	200	kΩ
Input Voltage	"H" Level	V_{IH4}	—	When releasing WAIT instruction	1.8	~	3.0	V
	"L" Level	V_{IL4}	—	When releasing WAIT instruction	0	~	0.3	V
Input Leak Current		I_{LI}	—	When input resistance is off, V_{IH} = 3.0V, V_{IL} = 0V	—	—	± 1.0	μA
DO1 / OT2, DO2 OUTPUT, MUTE, OT1 OUTPUT								
Output Current	"H" Level	I_{OH1}	—	V_{OH} = 2.7V	− 0.4	− 0.8	—	mA
	"L" Level	I_{OL1}	—	V_{OL} = 0.3V	0.4	0.8	—	
Output Off Leak Current		I_{TL}	—	V_{TLH} = 3.0V, V_{TLL} = 0V (DO1, DO2)	—	—	± 100	nA

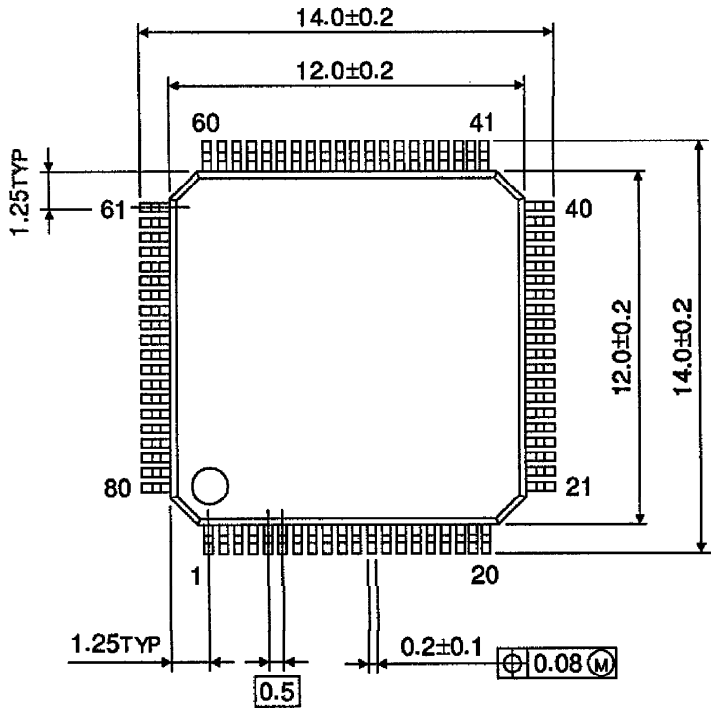
For conditions marked by an asterisk (*), guaranteed when V_{DD} = 1.8 to 3.6V, Ta = − 10 to 60°C

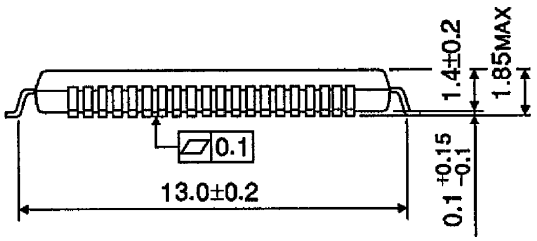
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
GENERAL-PURPOSE I/O PORT (P2-0 to P6-3)								
Output Current	"H" Level	I_{OH1}	—	V_{OH} = 2.7V	−0.4	−0.8	—	mA
	"L" Level	I_{OL1}	—	V_{OL} = 0.3V	0.4	0.8	—	
Input Leak Current		I_{LI}	—	V_{IH} = 3.0V, V_{IL} = 0V	—	—	±1.0	μA
Input Voltage	"H" Level	V_{IH2}	—	—	2.4	~	3.0	V
	"L" Level	V_{IL2}	—	—	0	~	0.6	
IN1/SC_{IN}, $\overline{RESET}$ INPUT PORT								
Input Leak Current		I_{LI}	—	V_{IH} = 3.0V, V_{IL} = 0V (excluding SC_{IN} input)	—	—	±1.0	μA
Input Voltage	"H" Level	V_{IH2}	—	—	2.4	~	3.0	V
	"L" Level	V_{IL2}	—	—	0	~	0.6	
OTHERS								
Input Pull-down Resistance		R_{IN2}	—	(TEST)	15	30	60	kΩ
X_{IN} Amp. Feedback Resistance		R_{fXT}	—	(X_{IN}-X_{OUT})	—	20	—	MΩ
X_{OUT} Output Resistance		R_{OUT}	—	(X_{OUT})	—	4	—	kΩ
Input Amp. Feedback Resistance		R_{fIN1}	—	(FM_{IN}, AM_{IN})	150	300	600	kΩ
		R_{fIN2}	—	(IF_{IN}/SC_{IN})	500	1000	2000	
Voltage Drop Detection Voltage		V_{STP}	—	(V_{DD})	1.35	1.55	1.75	V
Voltage Drop Detection Temperature Property		D_S	—	(V_{DD})	—	−3	—	mV/°C

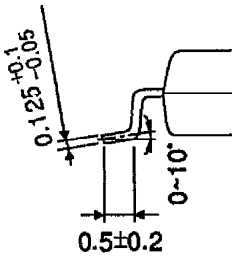
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OUTLINE DRAWING

LQFP80-P-1212-0.50A







Weight : 0.45g (Typ.)