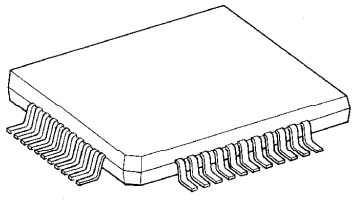
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9307AF

SINGLE CHIP DTS CONTROLLER WITH BUILT-IN PRESCALER·PLL·LCD DRIVER (DTS-12)

TC9307AF is a 4bit CMOS single chip microcontroller for digital tuning system with built-in prescaler, PLL and LCD driver.
It can compose a single chip type digital tuning system and is suitable for application to radio cassette equipment.
CPU has 4bit parallel addition and substruction (AI / SI instructions), logical operation (OR, AN instructions), plural bit judge, comparison instructions (TM, SL instructions) and time base function.
The package is of 44-pin mini-flat type, and it provides with abundant I / O ports and exclusive key-input ports controlled by the powerful input / output instructions (IO, KEY instructions), and besides has exclusive LCD terminal of 1 / 4 duty·1 / 3 bias driving with built-in 3V voltage regulation circuit. 2-modulus prescaler, PLL circuit, and 16bit general purpose IF counter for generating auto-stop signal through counting IF signal are incorporated.



QFP44-P-1414-0.80A

Weight : 0.8g (Typ.)

FEATURES

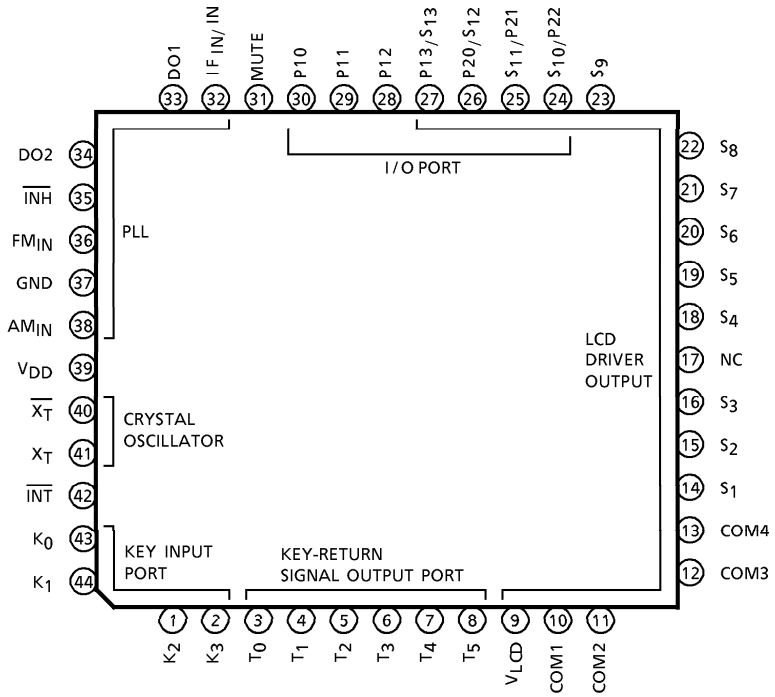
- 4bit microcontroller for digital tuning system.
- 5V ± 10% single power supply. CMOS structure with low power consumption.
  - At PLL operation : V_{DD} = 4.5~5.5V
  - At only CPU operation : V_{DD} = 3.0~5.5V
- Back up of data memory (RAM) and of various kinds of ports are easily made. (With $\overline{INH}$ terminal)
- Built-in LCD driver (1 / 4 duty, 1 / 3 bias, driving frequency : 125Hz, 52 segment max.) and 3V voltage regulation circuit for display.
- Program memory (ROM) : 16bit × 2048 steps.
- Data memory (RAM) : 4bit × 128 words.
- 65 kinds of powerful instruction sets. (All are single-word instructions)
- Crystal resonator of 150kHz or 75kHz can be selected with program.
- Instruction execution time : 150kHz crystal connection : 40μs
  : 75kHz crystal connection : 80μs
- Abundant instructions of addition and substruction. (12 kinds of addition instruction, 12 kinds of substruction instructions)
- Powerful compound judgment instructions. (TMTR, TMFR, TMT, TMF, TMTN, TMFN instructions)

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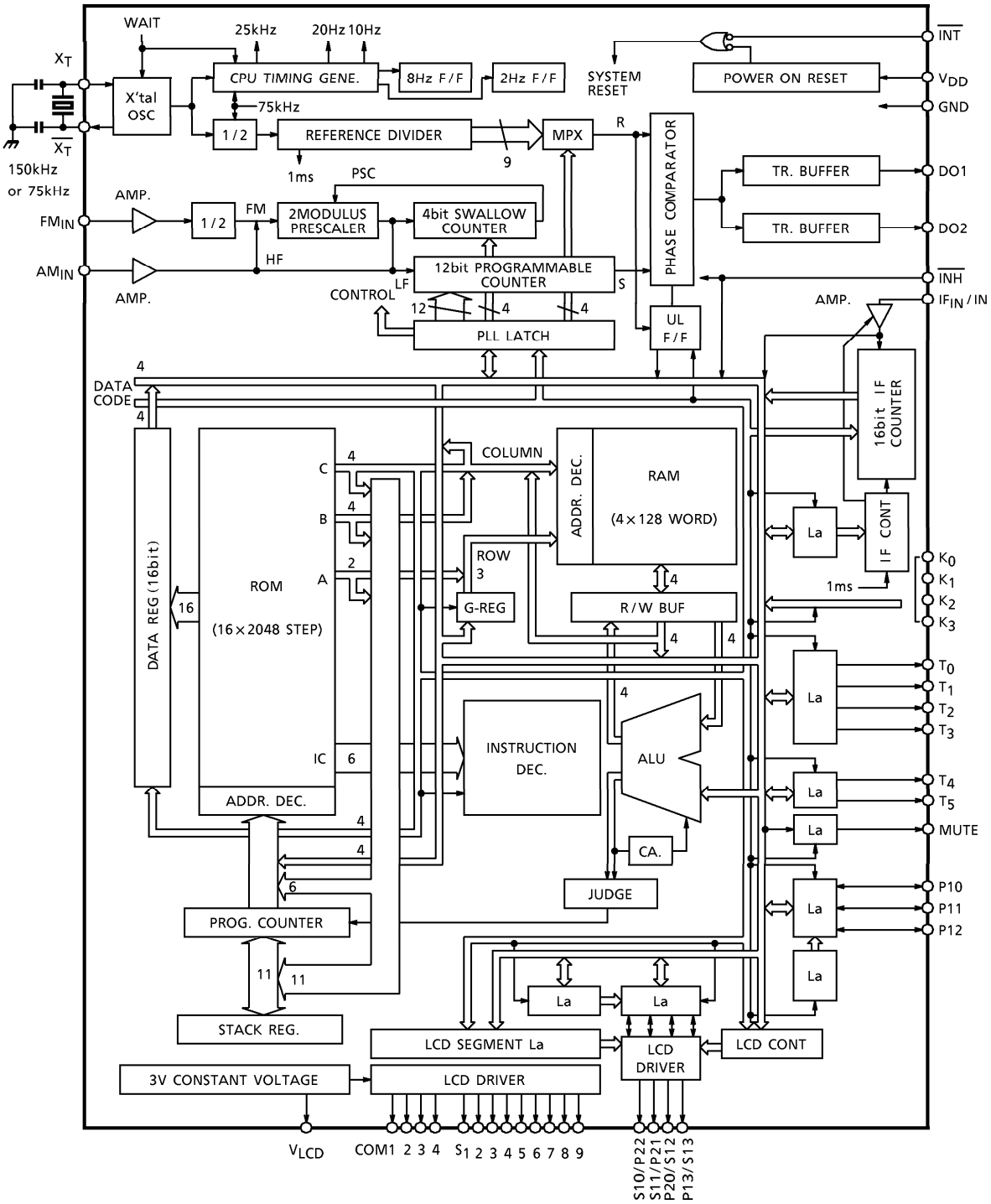
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- Data transfer in the same low address is possible.
- Indirect data transfer with registers is possible. (MVRD, MVRS, MVGD, MVGS instructions)
- Powerful 16 general registers. (arranged in RAM)
- Stack level : 1 level
- Program memory (ROM) has no conception of page, field, and JUMP and CAL instructions can be freely made among 2048 steps.
- It is possible to freely refer to the contents, 16 bits, of optional address within 1024 steps in program memory (ROM). (DAL instruction)
- Powerful input and output instruction (IO, KEY instructions)
- Exclusive input port (K0~K3) and output port (T0~T5) for key matrix.
- Abundant 19 I/O ports. (port which can be assigned to input or output for each bit : 7 (max.), exclusive input : 6 (max.), exclusive output port : 7)
- Port of segment outputs can be changed to I/O ports for each bit, and vice versa. (S10/P22, S11/P21, P20/S12, P13/S13)
- 3 kinds of back-up mode (only CPU operation, Crystal oscillation and Clock stop) can be selected by instructions. (CKSTP, WAIT instruction)
- 2Hz timer F/F, 8Hz timer F/F (4Hz at 75kHz crystal connection), 10Hz/20Hz interval pulse output are provided. (Internal port for time base use)
- Independent frequency input terminal at FM and AM (FM_{IN}, AM_{IN}) and two phase-comparator outputs (D01, D02)
- 9 kinds of reference frequency can be selected with program.
  (At 150kHz crystal connection : 1kHz, 3kHz, 3.125kHz, 5kHz, 6.25kHz, 10kHz, 12.5kHz, 25kHz, 50kHz)
  (At 75kHz crystal connection : 1kHz, 3kHz, 3.125kHz, 5kHz, 6.25kHz, 12.5kHz, 25kHz)
- Locked condition of PLL can be detected.
- 16bit universal-type IF counter is built in, and input terminal of IF counter can be changed to general purpose input port. (IF_{IN}/IN)

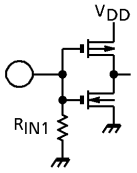
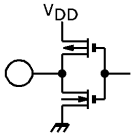
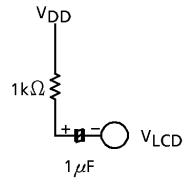
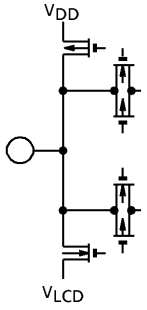
PIN CONNECTION

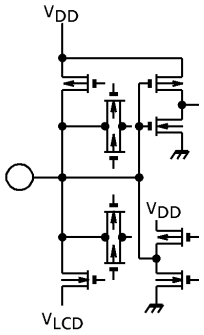
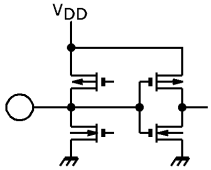
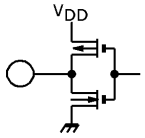
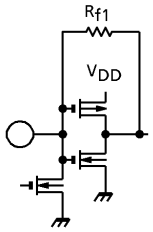


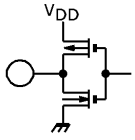
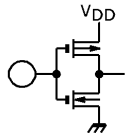
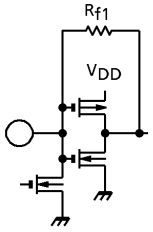
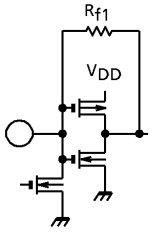
BLOCK DIAGRAM

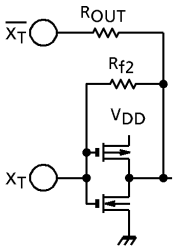
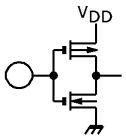


PIN FUNCTION

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
1, 2, 43, 44	K_0~K_3	Key Input Port	This is a 4bit input port for key matrix input. 24 (=4×6) key can be used with matrix made with T0~T5 key return Timing Output Port. All these terminals are built in pull-down resistance.	
3~8	T_0~T_5	Key Return Timing Output Port	This is a 4bit output port for key Return Timing Output. Usually, it's used for output of the timing signal for key matrix.	
9	V_{LCD}	3V Regulation Voltage Output Terminal	This is a 3V regulation voltage output terminal for driving LCD. Connect the resistance and capacitors in series between V_{DD} and V_{LCD} terminal. (Typ. R=1kΩ, C=1μF) As regulation voltage output has temperature characteristic of −15mV/°C, it can control the influence of temperature on LCD display. (Note)Output is fixed "H" level at executing system reset and CKSTP instruction.	
10~13	COM1 ~COM4	LCD Common Output	This is a LCD drive output terminal of 1/4 duty, 1/3 bias type. Display of maximum 52 segments are available with matrix made with COM1~COM4 and S1~S13. The frame frequency is 125kHz and it outputs four value of voltage V_{DD}, 1/3 level, 2/3 level, V_{LCD}. The data of segment terminal is output by the execution of SEG instruction and MARK instruction. (Note)Output is fixed "H" level at executing system reset and CKSTP instruction.	
14~23	S_1~S_9	LCD Segment Output		

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
24, 25	S_{10} / P22 S_{11} / P21	LCD Segment Output / I/O Port	This terminal can be used both as I/O port and segment output. It can be assigned to general I/O port or segment output for each bit by program. Assignment to I/O port on segment output is executed by contents of segment control port. At using as I/O port, it can set up the input/output port for each bit. (Note) At executing system reset, each terminal is set up segment output (S10, S11) and input port (P20, P13). At executing CKSTP instruction, segment output is fixed "H" level and Output port is "L" level automatically.	
26, 27	P20 / S_{12} P13 / S_{13}	I/O Port / LCD Segment Output		
28~30	P10~P12	I/O Port	These are 3bit general purpose I/O port. It can be assigned to input or output for each bit by program. (Note) At system reset, I/O port is set up input, port. At executing CKSTP instruction, output port is fixed at "L" level automatically.	
31	MUTE	Muting Output Port	This is a 1bit output port. This is usually used as muting control signal output.	
32	IF_{IN} / IN	IF Counter Input / Input Port	This is a IF signal input terminal of 16bit general purpose IF counter and can be input frequency of 0.3~12MHz ($0.4V_{p-p}$ min.). This terminal has built-in amplifiers, and operates with C-connection and small amplitude. This terminal can be used as input port by content of IN control port. (Note) At assignment of IF inputs, when $\overline{INH}$ terminal is "L" level, this terminal is set up pull-down.	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
33, 34	DO1, DO2	Phase Comparator Output	This is a Phase comparator output terminal of PLL. D01 and D02 are parallel outputs. Therefore, optimum filter constant can be designed for each band of FM / AM.	
35	$\overline{INH}$	Inhibit Input	This is a signal input terminal for selecting radio mode. "H" : radio ON, "L" : radio OFF In radio OFF mode, PLL and IF counter become reset condition. Further, if CKSTP instruction is used in the program and this CKSTP instruction is executed while $\overline{INH}$ is at "L" level, the internal clock generator and CPU stop their operations, and memory back up condition can be realized at low current consumption (less than 1μA). At this time, segment output terminal is fixed "H" level and other output is "L" level automatically.	
36	FM_{IN}	FM Programmable Counter Input	Prescaler input terminal at FM band. Local oscillator output signal (VCO output) of 50~130MHz is input. This terminal has built-in amplifier and operates with C-connection and small amplitude. (Note)In LF mode or HF mode and $\overline{INH}$ = "L" level, this terminal is set up pull-down.	
38	AM_{IN}	AM Programmable Counter Input	Programmable counter input terminal at AM band. Direct-dividing mode (LF mode) and Pulse-swallow mode (HF mode) can freely be changed over. In direct-dividing mode, local oscillator output signal (VCO output) of 0.5~10MHz ($0.4V_{p-p}$ min.) is input, and in pulse-swallow mode, local oscillator output signal of 5~60MHz ($0.4V_{p-p}$ min.) is input. This terminal has built-in amplifier and operates with C-connetion and small amplifier. (Note)In FM mode an $\overline{INH}$ = "L" level, the terminal is set up pull-down	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
40	$\overline{X_T}$	Crystal Oscillation Terminal	This is a crystal oscillation terminal. Connect 150kHz or 75kHz crystal resonator for reference. Selection of 150kHz / 75kHz is executed by contents of internal 75kHz port. (75kHz = "0" : 150kHz, 75kHz = "1" : 75kHz) At executing CKSTP instruction, crystal oscillation stops.	
41	X_T			
42	$\overline{INT}$	Initializing Input	This is a system reset signal input terminal of device. During $\overline{INT}$ is at "L" level, reset is applied, and when "H" level is reached, program starts from address 0. When voltage of 0V→3V is supplied to V_{DD} terminal, system reset is usually executed (power-on reset), so this terminal is fixed at "H" level to be used. (Note)If power supply voltage is applied to V_{DD} terminal at "L" level of $\overline{INT}$ terminal, device is set up test mode condition.	
39	V_{DD}	Power Supply Terminal	This is power supply terminal. At PLL operation, voltage of 4.5~5.5V is supplied. At CPU operation only, supply voltage can be reduced down to 3V and further, down to 1.7V at back up condition (at executing CKSTP instruction). When voltage of 0V→3V is supplied to this terminal, system reset is executed to device and program starts from address 0. (Power-on reset) (Note)For power-on reset operation, design the rising time of power supply voltage to device to be time of 10~100ms. (Note)As the content of each port (output port, internal port, etc.) is indefinite at the time of power supply, so initialization must be made by program according to your use.	—
37	GND			

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	−0.3~6.0	V
Input Voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power Dissipation	P_D	400	mW
Operating Temperature	T_{opr}	−20~60	°C
Storage Temperature	T_{stg}	−55~125	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V_{DD} = 5.0V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Power Supply Voltage Range	V_{DD1}	—	At CPU, PLL operation	*	4.5	5.0	5.5	V
	V_{DD2}	—	At only CPU operation	*	3.0	5.0	5.5	
Memory Holding Voltage Range	V_{HD}	—	Crystal oscillation stops (Excuting CKSTP instrucion)	*	1.7	~	5.5	
Operating Power Supply Current	I_{DD1}	—	At CPU, PLL operation, FM_{IN} = 130MHz		—	10	25	mA
	I_{DD2}	—	At only CPU operation, X_T = 150kHz V_{DD} = 5V		—	100	200	μA
	I_{DD3}	—	At only CPU operation, X_T = 75kHz V_{DD} = 5V		—	50	100	
	I_{DD4}	—	At only crystal oscillation, X_T = 150kHz V_{DD} = 5V		—	80	150	
	I_{DD5}	—	At only crystal oscillation, X_T = 75kHz V_{DD} = 5V		—	40	80	
Memory Holding Power Supply Current	I_{HD}	—	Crystal oscillation stop, V_{DD} = 5V		—	0.07	1.0	
Crystal Oscillation Frequency	f_{XT}	—		*	—	75 or 150	—	kHz

Programmable counter, IF counter

Operating Frequency Range	f_{FM}	—	FM_{IN} input, V_{IN} = 0.4V_{p-p}	*	50	~	130	MHz
	f_{HF}	—	AM_{IN} input (HF mode), V_{IN} = 0.4V_{p-p}	*	5	~	60	
	f_{LF}	—	AM_{IN} input (LF mode), V_{IN} = 0.4V_{p-p}	*	0.5	~	10	
	f_{IF}	—	IF_{IN} input, V_{IN} = 0.4V_{p-p}	*	0.3	~	12	
Operating Input Amplitude Range	f_{FM}	—	FM_{IN} input, F_{IN} = 50~130MH	*	0.4	~	V_{DD} − 0.5	V_{p-p}
	f_{HF}	—	AM_{IN} input (HF mode), F_{IN} = 5~60MHz	*	0.4	~	V_{DD} − 0.5	
	f_{LF}	—	AM_{IN} input (LF mode), F_{IN} = 0.5~10MHz	*	0.4	~	V_{DD} − 0.5	
	f_{IF}	—	IF_{IN} input, F_{IN} = 0.3~12MHz	*	0.4	~	V_{DD} − 0.5	
Amp. Feedback Resisitance	R_{f1}	—	FMI_N, AM_{IN}, IF_{IN} input		250	500	1500	kΩ

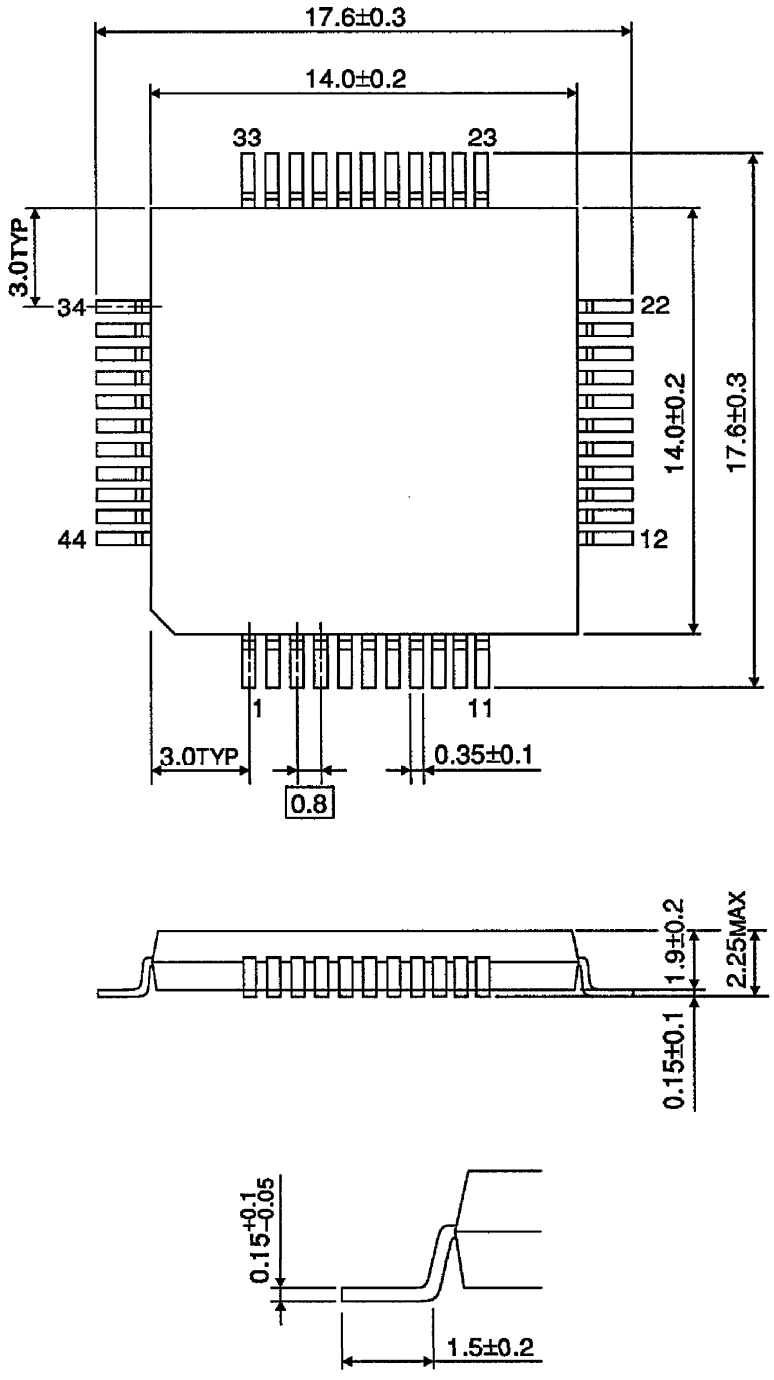
(Note) Items marked with * are guranteed within the range of V_{DD} = 4.5~5.5V, Ta = −20~60° C

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
3V voltage regulation circuit for LCD driving, LCD output							
Regulation Voltage Range	V_{LCD}	—	V_{DD} Reference	−3.25	−3.0	−2.75	V
Temperature Characteristic Of Regulation Voltage	D_V	—	—	—	−15	—	mV/°C
Output Voltage 1/3 Level	V_{O1}	—	V_{LCD} = 2V, V_{DD} = 5V, No-Load, GND Reference	2.8	3.0	3.2	V
Output Voltage 2/3 Level	V_{O2}	—	V_{LCD} = 2V, V_{DD} = 5V, No-Load, GND Reference	3.8	4.0	4.2	V
MUTE, T_0~T_5, P10~P22							
Output Current "H" Level	I_{OH1}	—	V_{OH} = 4.0V	−2.0	−7.0	—	mA
Output Current "L" Level	I_{OL1}	—	V_{OL} = 1.0V	2.0	5.0	—	mA
Input Voltage "H" Level	V_{IH1}	—	(P10~P22)	3.5	~	5.0	V
Input Voltage "L" Level	V_{IL1}	—	(P10~P22)	0	~	1.5	V
Input Leakage Current	I_{LI}	—	V_{IH} = 5.0V, V_{IL} = 0V (P10~P22)	—	—	±1.0	μA
D01, 2 output							
Output Current "H" Level	I_{OH1}	—	V_{OH} = 4.0V	−2.0	−7.0	—	mA
Output Current "L" Level	I_{OL1}	—	V_{OL} = 1.0V	2.0	5.0	—	mA
Output Off-Leakage Current	I_{TL}	—	V_{TLH} = 5.0V, V_{TLL} = 0V	—	—	±100	nA
$\overline{INT}$ input, input port (K_0~K_3, IN)							
Input Voltage "H" Level	V_{IH1}	—	—	3.5	~	5.0	V
Input Voltage "L" Level	V_{IL1}	—	—	0	~	1.5	V
Input Leakage Current	I_{LI}	—	($\overline{INT}$, IN Input) V_{IH} = 5.0V V_{IL} = 0V	—	—	±1.0	μA
Input Pull-Down Resistance	R_{IN1}	—	(K_0~K_3 Input)	50	150	300	kΩ
$\overline{INH}$ input port							
Input Voltage "H" Level	V_{IH2}	—	—	4.3	~	5.0	V
Input Voltage "L" Level	V_{IL2}	—	—	0	~	2.7	V
Input Leakage Current	I_{LI}	—	V_{IH} = 5.0V, V_{IL} = 0V	—	—	±1.0	μA
Crystal oscillation terminal							
Amp. Feedback Resistance	R_{f2}	—	(X_T Input)	1	5	15	MΩ
$\overline{X_T}$ Output Resistance	R_{OUT}	—	($\overline{X_T}$ Output)	50	150	300	kΩ

OUTLINE DRAWING

QFP44-P-1414-0.80A

Unit : mm



Weight : 0.8g (Typ.)