TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

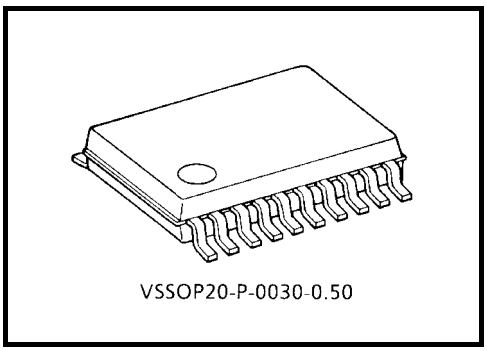
TC7MBL3245AFK

Octal Bus Switch

The TC7MBL3245AFK provides eight bits of low-voltage, high-speed bus switching in a standard '245 device pinout. The low ON-resistance of the switch allows connections to be made with minimal propagation delay and while maintaining CMOS low power dissipation.

The device comprises a single 8-bit switch. When output enable ($\overline{OE}$) is low, the switch is on and port A is connected to port B. When $\overline{OE}$ is high, the switch is open and a high-impedance state exists between the two ports.

All inputs are equipped with protection circuits to guard against static discharge.

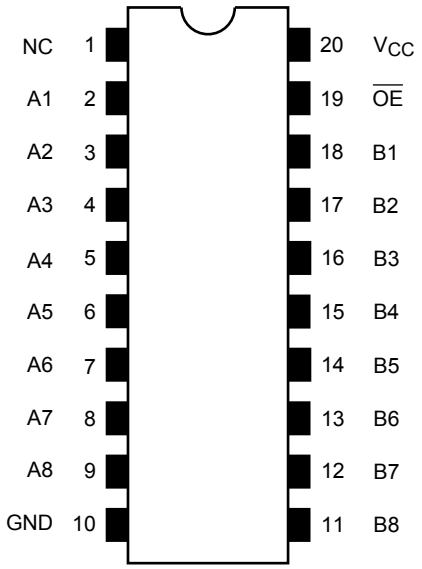


Weight: 0.03 g (typ.)

Features

- Operating voltage: V_{CC} = 2.0~3.6 V
- High speed: t_{pd} = 0.31 ns (max) @ V_{CC} = 3.0 V
- Low ON-resistance: R_{ON} = 5 Ω (typ.) @ V_{CC} = 3.0 V
- ESD performance: Machine model ≥ ±200 V
  Human body model ≥ ±2000 V
- Power-down protection for inputs ($\overline{OE}$ input only)
- Package: VSSOP (US20)
- Pin compatible with the 74xx245 type

Pin Assignment (top view)

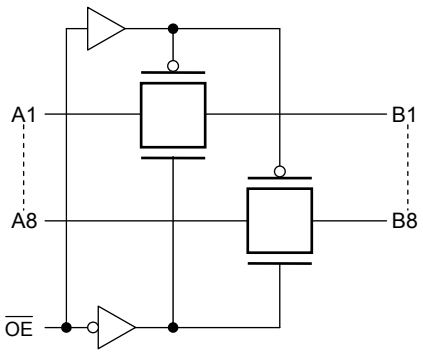


NC-No Internal Connection

Truth Table

Inputs $\overline{OE}$	Function
L	A port = B port
H	Disconnect

System Diagram



Absolute Maximum Ratings (Note)

Characteristic		Symbol	Rating	Unit
Power supply range		V_{CC}	−0.5~4.6	V
Control pin input voltage		V_{IN}	−0.5~4.6	V
Switch terminal I/O voltage		V_S	−0.5~Vcc+0.5	V
Clump diode current	Control input pin	I_{IK}	−50	mA
	Switch terminal		±50	
Switch I/O current		I_S	128	mA
Power dissipation		P_D	180	mW
DC V_{CC}/GND current		I_{CC}/I_{GND}	±100	mA
Storage temperature		T_{stg}	−65~150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristic	Symbol	Rating	Unit
Power supply voltage	V_{CC}	2.0~3.6	V
Control pin input voltage	V_{IN}	0~3.6	V
Switch I/O voltage	V_S	0~Vcc	V
Operating temperature	T_{opr}	−40~85	°C
Input rise and fall time	dt/dv	0~10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Electrical Characteristics

DC Characteristics (Ta = –40 to 85°C)

Characteristic	Symbol	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit
High-level control input voltage	V_{IH}	—	2.0 to 3.6	0.7 × V_{CC}	—	—	V
Low-level control input voltage	V_{IL}	—	2.0 to 3.6	—	—	0.3 × V_{CC}	V
Control input current	I_{IN}	V_{IN} = 0 to 3.6 V	2.0 to 3.6	—	—	±1.0	μA
Power off leakage current	I_{OFF}	$\overline{OE}$ = 0 to 3.6 V	0	—	—	±1.0	μA
Off-stage leakage current (switch off)	I_{SZ}	A, B = 0 to V_{CC}, $\overline{OE}$ = V_{CC}	2.0 to 3.6	—	—	±1.0	μA
Switch ON-resistance (Note 2)	R_{ON}	V_{IS} = 0 V, I_{IS} = 30 mA (Note 1)	3.0	—	2	7	Ω
		V_{IS} = 3.0 V, I_{IS} = 30 mA (Note 1)	3.0	—	3	9	
		V_{IS} = 2.4 V, I_{IS} = 15 mA (Note 1)	3.0	—	5	20	
		V_{IS} = 0 V, I_{IS} = 24 mA (Note 1)	2.3	—	3	10	
		V_{IS} = 2.3 V, I_{IS} = 24 mA (Note 1)	2.3	—	4	15	
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0	3.6	—	—	10	μA

Note 1: All typical values are at Ta = 25°C.

Note 2: Measured by voltage drop between A and B pins at indicated current through the switch. ON-resistance is determined by the lower of the voltages on the two pins (A or B).

AC Characteristics (Ta = –40 to 85°C)

Characteristic	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Propagation delay (bus to bus)	t_{pLH} t_{pHL}	Figure 1, Figure 2 (Note)	3.3 ± 0.3	—	0.31	ns
			2.5 ± 0.2	—	0.52	
Output enable time	t_{pZL} t_{pZH}	Figure 1, Figure 3	3.3 ± 0.3	—	6.5	ns
			2.5 ± 0.2	—	8	
Output disable time	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	3.3 ± 0.3	—	6.5	ns
			2.5 ± 0.2	—	8	

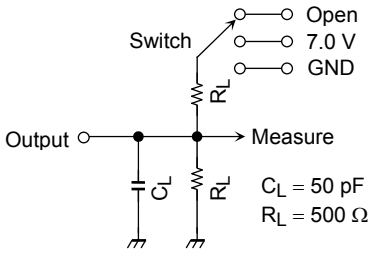
Note: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical ON-resistance of the switch and the 50 pF load capacitance when driven by an ideal voltage from the source (zero output impedance).

Capacitance (Ta = 25°C)

Characteristic	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Control input capacitance	C_{IN}		3.0	3	pF
Switch terminal capacitance	$C_{I/O}$	$\overline{OE}$ = V_{CC}	3.0	17	pF

Note : This parameter is guaranteed by design.

AC Test Circuit



Parameter	Switch
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	2 × V_{CC}
t_{pHZ}, t_{pZH}	GND

Figure 1

AC Waveforms

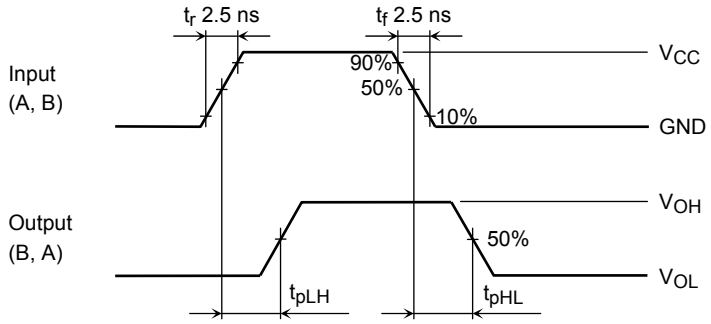


Figure 2 t_{pLH}, t_{pHL}

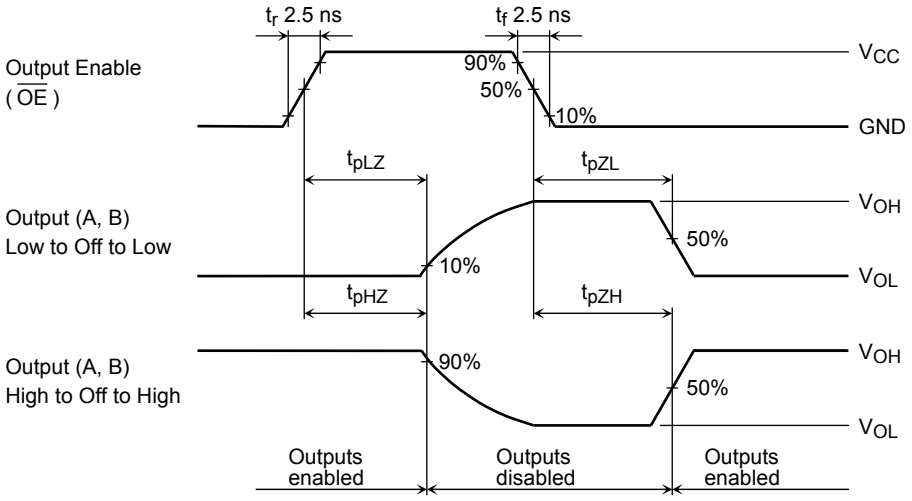
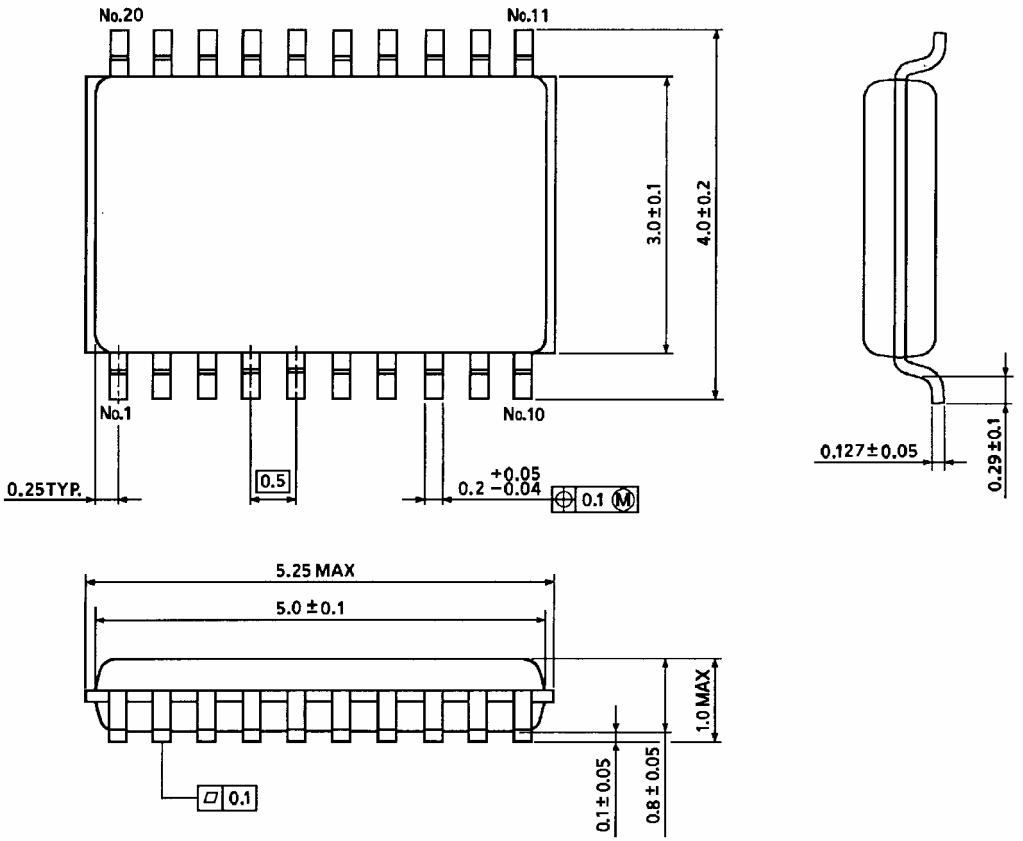


Figure 3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

Package Dimensions

VSSOP20-P-0030-0.50 Unit : mm



Weight: 0.03 g (typ.)

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20070701-EN GENERAL

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