

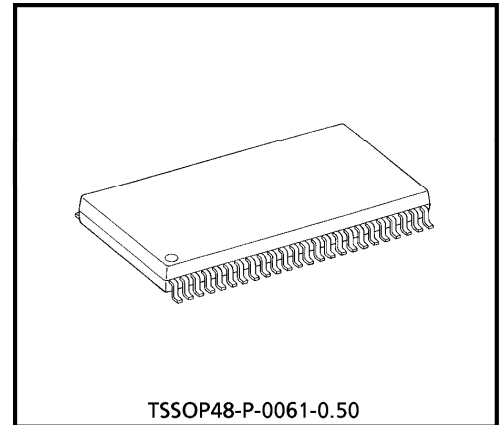
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VCX16244FT**LOW-VOLTAGE 16-BIT BUS BUFFER
WITH 3.6V TOLERANT INPUTS AND OUTPUTS**

The TC74VCX16244FT is a high performance CMOS 16-bit BUS BUFFER. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. It is also designed with over voltage tolerant inputs and outputs up to 3.6V.

This device is non-inverting 3-state buffer having four active-low output enables. It can be used as four 4-bit buffers two 8-bit buffers or one 16-bit buffer. When the $\overline{OE}$ input is high, the outputs are in a high impedance state. This device is designed to be used with 3-state memory address drivers, etc.

All inputs are equipped with protection circuits against static discharge.



Weight : 0.25g (Typ.)

FEATURES

- Low Voltage Operation : $V_{CC} = 1.8 \sim 3.6V$
- High Speed Operation : $t_{pd} = 2.5ns$ (max.) at $V_{CC} = 3.0 \sim 3.6V$
 $t_{pd} = 3.0ns$ (max.) at $V_{CC} = 2.3 \sim 2.7V$
 $t_{pd} = 5.0ns$ (max.) at $V_{CC} = 1.8V$
- 3.6V Tolerant inputs and outputs.
- Output Current : $I_{OH} / I_{OL} = \pm 24mA$ (min.) at $V_{CC} = 3.0V$
 $I_{OH} / I_{OL} = \pm 18mA$ (min.) at $V_{CC} = 2.3V$
 $I_{OH} / I_{OL} = \pm 6mA$ (min.) at $V_{CC} = 1.8V$
- Latch-up Performance : $\pm 300mA$
- ESD Performance : Human Body Model $> \pm 2000V$
Machine Model $> \pm 200V$
- Package : TSSOP
(Thin Shrink Small Outline Package)
- Power Down Protection is provided on all inputs and outputs.
- Supports live insertion / withdrawal (Note 1)

(Note 1) To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

PIN CONNECTION

1 $\overline{OE}$	1 $\circ$	48	2 $\overline{OE}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V_{CC}	7	42	V_{CC}
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V_{CC}	18	31	V_{CC}
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4 $\overline{OE}$	24	25	3 $\overline{OE}$

(TOP VIEW)

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TRUTH TABLE

INPUTS		OUTPUTS
1OE	1A1-1A4	1Y1-1Y4
L	L	L
L	H	H
H	X	Z

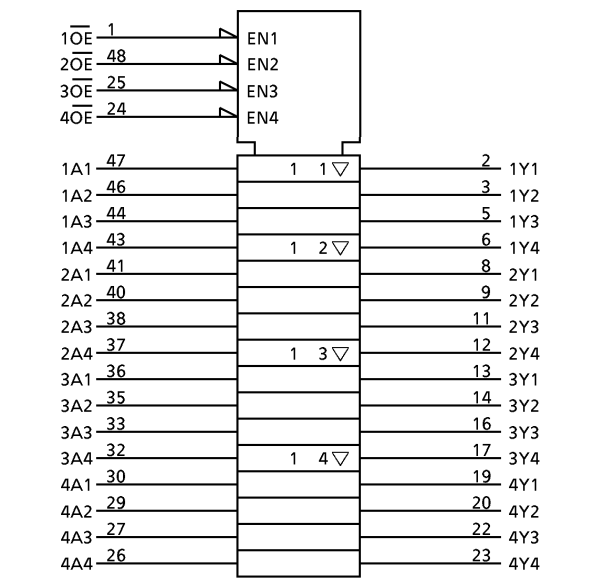
INPUTS		OUTPUTS
2OE	1A1-2A4	2Y1-2Y4
L	L	L
L	H	H
H	X	Z

INPUTS		OUTPUTS
3OE	3A1-3A4	3Y1-3Y4
L	L	L
L	H	H
H	X	Z

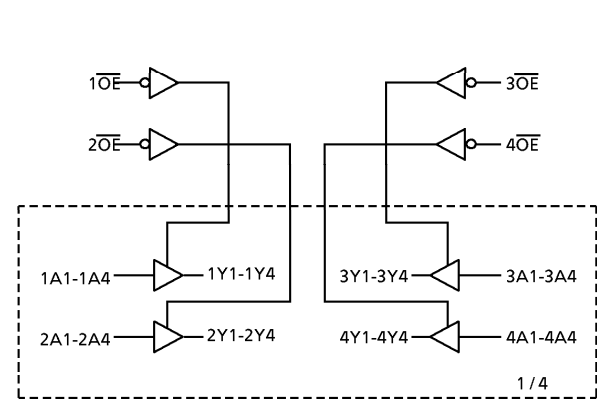
INPUTS		OUTPUTS
4OE	4A1-4A4	4Y1-4Y4
L	L	L
L	H	H
H	X	Z

X : Don't Care
Z : High impedance

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



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MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	- 0.5~4.6	V
DC Input Voltage	V_{IN}	- 0.5~4.6	V
DC Output Voltage	V_{OUT}	- 0.5~4.6 (Note 1)	V
		- 0.5~ V_{CC} + 0.5 (Note 2)	
Input Diode Current	I_{IK}	- 50	mA
Output Diode Current	I_{OK}	± 50 (Note 3)	mA
DC Output Current	I_{OUT}	± 50	mA
Power Dissipation	P_D	400	mW
DC V_{CC} / Ground Current Per Supply Pin	I_{CC} / I_{GND}	± 100	mA
Storage Temperature	T_{stg}	- 65~150	°C

(Note 1) Off-State

(Note 2) High or Low State. I_{OUT} absolute maximum rating must be observed.(Note 3) $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	1.8~3.6	V
		1.2~3.6 (Note 4)	
Input Voltage	V_{IN}	-0.3~3.6	V
Output Voltage	V_{OUT}	0~3.6 (Note 5)	V
		0~ V_{CC} (Note 6)	
Output Current	I_{OH} / I_{OL}	± 24 (Note 7)	mA
		± 18 (Note 8)	
		± 6 (Note 9)	
Operating Temperature	T_{opr}	- 40~85	°C
Input Rise And Fall Time	dt / dv	0~10 (Note 10)	ns / V

(Note 4) Data Retention Only

(Note 5) Off-State

(Note 6) High or Low State

(Note 7) $V_{CC} = 3.0 \sim 3.6V$ (Note 8) $V_{CC} = 2.3 \sim 2.7V$ (Note 9) $V_{CC} = 1.8V$ (Note 10) $V_{IN} = 0.8 \sim 2.0V$, $V_{CC} = 3.0V$

ELECTRICAL CHARACTERISTICS

DC characteristics ($T_a = -40 \sim 85^\circ\text{C}$, $2.7\text{V} < V_{CC} \leq 3.6\text{V}$)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN.	MAX.	UNIT
Input Voltage	"H" Level	V _{IH}			2.7~3.6	2.0	—	V
	"L" Level	V _{IL}			2.7~3.6	—	0.8	V
Output Voltage	"H" Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = - 100μA	2.7~3.6	V _{CC} - 0.2	—	V
				I _{OH} = - 12mA	2.7	2.2	—	
				I _{OH} = - 18mA	3.0	2.4	—	
				I _{OH} = - 24mA	3.0	2.2	—	
	"L" Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100μA	2.7~3.6	—	0.2	V
				I _{OL} = 12mA	2.7	—	0.4	
				I _{OL} = 18mA	3.0	—	0.4	
				I _{OL} = 24mA	3.0	—	0.55	
Input Leakage Current		I _{IN}	V _{IN} = 0~3.6V		2.7~3.6	—	± 5.0	μA
3-State Output Off-State Current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0~3.6V		2.7~3.6	—	± 10.0	μA
Power Off Leakage Current		I _{OFF}	V _{IN} , V _{OUT} = 0~3.6V		0	—	10.0	μA
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND		2.7~3.6	—	20.0	μA
			V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6V		2.7~3.6	—	± 20.0	
Increase In I _{CC} Per Input		ΔI _{CC}	V _{IH} = V _{CC} - 0.6V		2.7~3.6	—	750	μA

ELECTRICAL CHARACTERISTICS

DC characteristics ($T_a = -40 \sim 85^\circ\text{C}$, $2.3\text{V} \leq V_{CC} \leq 2.7\text{V}$)

PARAMETER		SYMBOL	TEST CONDITION			MIN.	MAX.	UNIT
			V _{CC} (V)					
Input Voltage	"H" Level	V _{IH}	2.3~2.7			1.6	—	V
	"L" Level	V _{IL}	2.3~2.7			—	0.7	V
Output Voltage	"H" Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = - 100μA	2.3~2.7	V _{CC} - 0.2	—	V
				I _{OH} = - 6mA	2.3	2.0	—	
				I _{OH} = - 12mA	2.3	1.8	—	
				I _{OH} = - 18mA	2.3	1.7	—	
	"L" Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100μA	2.3~2.7	—	0.2	V
				I _{OL} = 12mA	2.3	—	0.4	
				I _{OL} = 18mA	2.3	—	0.6	
Input Leakage Current		I _{IN}	V _{IN} = 0~3.6V		2.3~2.7	—	± 5.0	μA
3-State Output Off-State Current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0~3.6V		2.3~2.7	—	± 10.0	μA
Power Off Leakage Current		I _{OFF}	V _{IN} , V _{OUT} = 0~3.6V		0	—	10.0	μA
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND		2.3~2.7	—	20.0	μA
			V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6V _{CC}		2.3~2.7	—	± 20.0	

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = -40~85°C, 1.8V ≤ V_{CC} < 2.3V)

PARAMETER		SYMBOL	TEST CONDITION		V _{CC} (V)	MIN.	MAX.	UNIT
Input Voltage	“H” Level	V _{IH}			1.8~2.3	0.7 × V _{CC}	—	V
	“L” Level	V _{IL}			1.8~2.3	—	0.2 × V _{CC}	V
Output Voltage	“H” Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = - 100μA	1.8	V _{CC} - 0.2	—	V
				I _{OH} = - 6mA	1.8	1.4	—	
	“L” Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100μA	1.8	—	0.2	V
				I _{OL} = 6mA	1.8	—	0.3	
Input Leakage Current		I _{IN}	V _{IN} = 0~3.6V		1.8	—	± 5.0	μA
3-State Output Off-State Current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0~3.6V		1.8	—	± 10.0	μA
Power Off Leakage Current		I _{OFF}	V _{IN} , V _{OUT} = 0~3.6V		0	—	10.0	μA
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND		1.8	—	20.0	μA
			V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6V		1.8	—	± 20.0	

AC characteristics (Ta = -40~85°C, Input t_r = t_f = 2.0ns, C_L = 30pF, R_L = 500Ω)

PARAMETER		SYMBOL	TEST CONDITION		V _{CC} (V)	MIN.	MAX.	UNIT
Propagation Delay Time	t _{pLH} t _{pHL}	(Fig.1, 2)			1.8	1.5	5.0	ns
					2.5 ± 0.2	1.0	3.0	
					3.3 ± 0.3	0.8	2.5	
3-State Output Enable Time	t _{pZL} t _{pZH}	(Fig.1, 3)			1.8	1.5	6.5	ns
					2.5 ± 0.2	1.0	4.1	
					3.3 ± 0.3	0.8	3.5	
3-State Output Disable Time	t _{pLZ} t _{pHZ}	(Fig.1, 3)			1.8	1.5	5.0	ns
					2.5 ± 0.2	1.0	3.8	
					3.3 ± 0.3	0.8	3.5	
Output To Output Skew	t _{osLH} t _{osHL}	(Note 11)			1.8	—	0.5	ns
					2.5 ± 0.2	—	0.5	
					3.3 ± 0.3	—	0.5	

For C_L = 50pF, add approximately 300ps to the AC maximum specification.

(Note 11) Parameter guaranteed by design.

(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)

Dynamic switching characteristics (Ta = 25°C, Input $t_r = t_f = 2.0\text{ns}$, $C_L = 30\text{pF}$)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP.	UNIT
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	V _{IH} = 1.8V, V _{IL} = 0V (Note 12)	1.8	0.25	V
		V _{IH} = 2.5V, V _{IL} = 0V (Note 12)	2.5	0.6	
		V _{IH} = 3.3V, V _{IL} = 0V (Note 12)	3.3	0.8	
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	V _{IH} = 1.8V, V _{IL} = 0V (Note 12)	1.8	- 0.25	V
		V _{IH} = 2.5V, V _{IL} = 0V (Note 12)	2.5	- 0.6	
		V _{IH} = 3.3V, V _{IL} = 0V (Note 12)	3.3	- 0.8	
Quiet Output Minimum Dynamic V _{OH}	V _{OHV}	V _{IH} = 1.8V, V _{IL} = 0V (Note 12)	1.8	1.5	V
		V _{IH} = 2.5V, V _{IL} = 0V (Note 12)	2.5	1.9	
		V _{IH} = 3.3V, V _{IL} = 0V (Note 12)	3.3	2.2	

(Note 12) Parameter guaranteed by design.

Capacitive characteristics (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP.	UNIT
Input Capacitance	C _{IN}		1.8, 2.5, 3.3	6	pF
Output Capacitance	C _O		1.8, 2.5, 3.3	7	pF
Power Dissipation Capacitance	C _{PD}	f _{IN} = 10MHz (Note 13)	1.8, 2.5, 3.3	20	pF

(Note 13) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(\text{opr.})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 16 \text{ (per bit)}$$

6.0V or $V_{CC} \times 2$
 Open
 GND
 SWITCH
 R_L
 OUTPUT
 C_L
 R_L
 MEASURE
 $C_L = 30\text{pF}$
 $R_L = 500\Omega$

PARAMETER	SWITCH
t _{PLH} , t _{PHL}	Open
t _{PLZ} , t _{pZL}	6.0V @V _{CC} = 3.3 ± 0.3V V _{CCx2} @V _{CC} = 2.5 ± 0.2V @V _{CC} = 1.8V
t _{pHZ} , t _{pZH}	GND

Fig.2 t_{pLH} , t_{pHL}

The diagram illustrates the timing characteristics of a CMOS inverter. The input signal (A) is a square wave with a period of 2.0ns. The output signal (Y) is an inverted square wave. Key timing parameters are labeled: t_r (input rise time), t_f (input fall time), t_{pLH} (output propagation delay from low to high), t_{pHL} (output propagation delay from high to low), V_M (input and output voltage at 50% transition), V_{IH} (input high voltage), V_{OL} (output low voltage), V_{OH} (output high voltage), and V_{IL} (input low voltage). The input signal transitions are marked at 90% and 10% levels.

Timing diagram for the 74VHC125 3-state buffer. The diagram shows the relationship between the Output Enable (OE) control signal and the output signals (Y) for both Low to Off and High to Off transitions.

Output Enable (OE) Signal:

- High level: V_{IH}
- Low level: GND
- Rise time: t_r (2.0ns)
- Fall time: t_f (2.0ns)
- 90% V_M and 10% V_M levels are marked on the transitions.

Output (Y) Low to Off to Low:

- High level: $3.0V$ or V_{CC}
- Low level: V_{OL}
- Transition delay from OE high to output low: t_{pLZ}
- Transition delay from OE low to output high: t_{pZL}
- Output voltage levels: V_X (during transition), V_M (mid-level), V_{OL} (low level).

Output (Y) High to Off to High:

- High level: V_{OH}
- Low level: GND
- Transition delay from OE high to output high: t_{pHZ}
- Transition delay from OE low to output low: t_{pZH}
- Output voltage levels: V_Y (during transition), V_M (mid-level), V_{OH} (high level).

Output States:

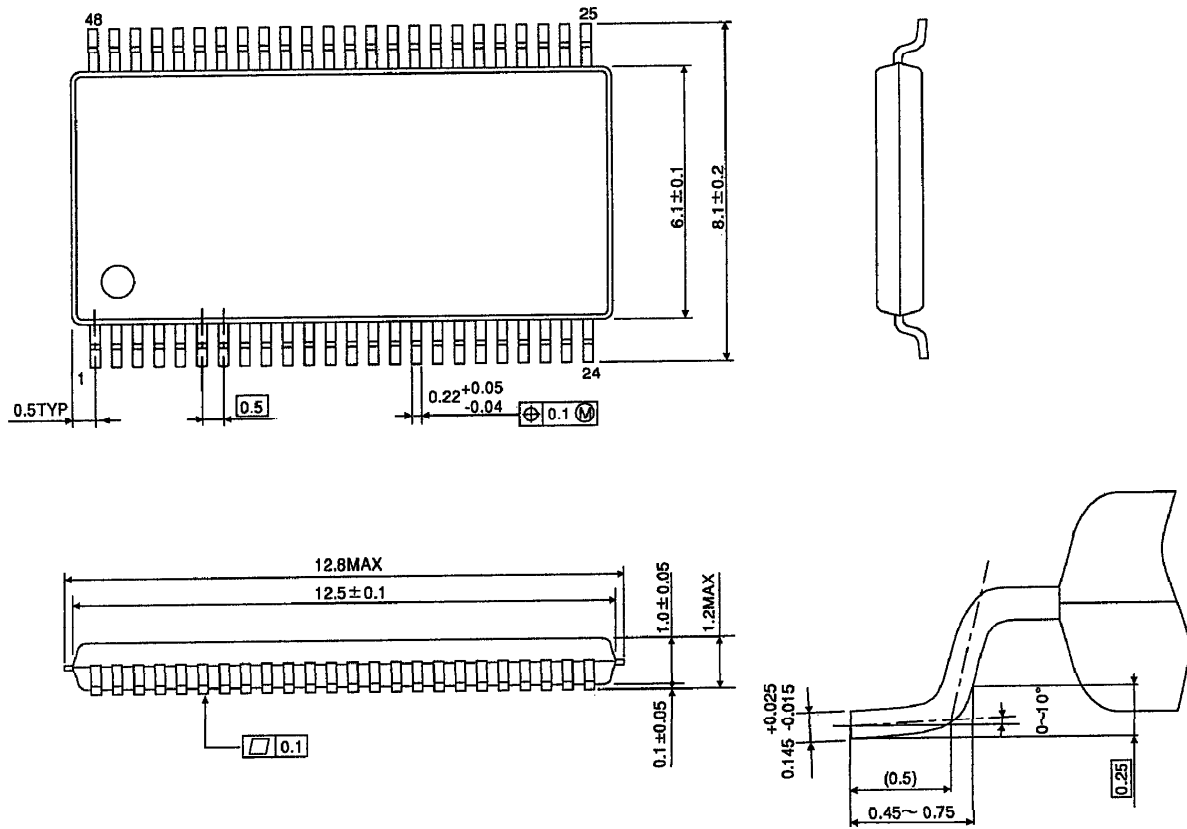
- OUTPUTS ENABLED:** When OE is low, the output is enabled and follows the input signal.
- OUTPUTS DISABLED:** When OE is high, the output is disabled and is in a high-impedance state.
- OUTPUTS ENABLED:** When OE is low, the output is enabled and follows the input signal.

SYMBOL	V _{CC}		
	3.3 ± 0.3V	2.5 ± 0.2V	1.8V
V _{IH}	2.7V	V _{CC}	V _{CC}
V _M	1.5V	V _{CC} / 2	V _{CC} / 2
V _X	V _{OL} + 0.3V	V _{OL} + 0.15V	V _{OL} + 0.15V
V _Y	V _{OH} - 0.3V	V _{OH} - 0.15V	V _{OH} - 0.15V

OUTLINE DRAWING

TSSOP48-P-0061-0.50

Unit : mm



Weight : 0.25g (Typ.)