TC6374AF (3in1 ATA)

PC Card ATA to SD Memory Card, MultiMediaCard and SmartMedia™ Controller

1. Outline

TC6374AF is an SD memory card / MultimediaCard / SmartMedia™ controller with PC Card ATA bus interface. 3 in 1 PC Card ATA adapter card can be easily realized with a firmware-installed NOR flash memory.

2. Features

- **PC Card ATA controller**
  - Conforms to PC Card ’97 Standard
  - Conforms to ATA/ATAPI-5 Standard T13 1321
  - Conforms to SD Card Association “SD Card PC Card Adopter - Media Card Pass Throug”
  - Supports 8/16 bit access
  - Power mode: 4 states (Sleep, Standby, Idle, Active)
  - Supports Auto power down
  - Supports Windows® standard ATA driver

- **SD Memory Card controller**
  - Conforms to SD Memory Card “Physical Layer Specification 1.0”
  - Supports 4 bit MultiMediaCard mode interface
  - Supports Write protect function
  - Supports Unique ID Read

- **MultiMediaCard controller**
  - Conforms to MultiMediaCard “System Specification 2.2”
  - Supports 1 bit MultiMediaCard mode interface
  - Supports Unique ID Read

- **SmartMedia™ Controller**
  - Conforms to SSFDC Forum “SmartMedia™ Physical Format”
  - Supports 3.3V 1M - 128M SmartMedia™
  - Supports 3.3V 4M - 128M MROM
  - SmartMedia™, MROM automatic recognition function

- Supports Wear Leveling function
- Supports Write protect function
- Supports ECCfunction (1 bit error correction / 2 bit error detect)
- Supports Unique ID Read

- **Controller firmware**
  - Installed on NORtype flash memory
  - Supports Firmware Update
  - Supply Firmware Object
  - Licence free

- **Operation Voltage**
  - Host Interface: 3.3V / 5V
  - Media Interface: 3.3V
  - Internal: 3.3V

- **Package**
  - Can be installed in PC Card Type II
  - 128-pin LQFP (Lead pitch: 0.4 mm)

3. Notes on Usage

#1, Take a note on the information listed in the solid line frame at the bottom of this page.

#2, Be sure to refer to the specification: “6-7. Notes on 3in1 PC Card ATA adapter”.

#3, In the system design, refer to the attached document: “Description on TC6374AF reference design (reference circuit diagram and information sheet)”. These reference documents are updated time by time, therefore be sure to check the latest information by inquiry.

#4, SmartMedia™ is a registered trademark of Toshiba.

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This data sheet is an interrim version arranging the target specification of products.
Note that the specificvation may be modified as necessary in the convenience of developmemt.
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If additional copies are required, contact with us so that we will prepare them by ourselves.
If the board design is based on this data sheet, contact with the Marketing staff in advance.

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[Notice]

#1. This product conforms to PC Card ’97 Standard.

#2. This product conforms to SmartMedia™ Physical format specification standardized and recommended by SSFDC Forum.

#3. This product conforms to ATA/ATAPI-5 standard.

#4. Voltage level indication differs per input/output signal.

#5. “Hi-Z” used in this document represents the High impedance state.

Voltage level	Input signal	Output signal
V_{DD}	“1”	“H”
V_{SS}	“0”	“L”

5. Pin assignment table

5-1. Pin assignment table 1

For marks in the table, refer to the footnotes below the table.

NO.	I/O	Symbol	Note	
			Input Buffer	Output Buffer
1	-	$V_{DD3.3}$	-	-
2	O	#NOR_CE	-	B4
3	O	#NOR_OE	-	B4
4	O	#NOR_WE	-	B4
5	O	NOR_A0	-	B4
6	O	NOR_A1	-	B4
7	-	V_{SS}	-	-
8	I	#NOR_BSY	LVTTL, S	-
9	O	#NOR_RP	-	B4
10	O	NOR_A2	-	B4
11	O	NOR_A3	-	B4
12		V_{SS}	-	-
13	O	NOR_A4	-	B4
14	O	NOR_A5	-	B4
15	I	SH/#FJ	LVTTL	-
16	-	V_{SS}	TEST IN	-
17	-	$V_{DD3.3}$	-	-
18	O	NOR_A6	-	B4
19	O	NOR_A7	-	B4
20	O	NOR_A8	-	B4
21	O	NOR_A9	-	B4
22	-	V_{SS}	-	-
23	O	NOR_A10	-	B4
24	O	NOR_A11	-	B4
25	I	FPSD	LVTTL	-
26	-	$V_{DD3.3}$	TEST IN	-
27	-	V_{SS}	-	-
28	O	NOR_A12	-	B4
29	O	NOR_A13	-	B4
30	I	SDWP	LVTTL	-

I: Input
O: Output **O (Tri): Tri-state**
B: Bidirection

Notice: Buffer Type

S: Schmidt LVTTL: 3V LVTTL level (same with 5V) PU: Pulled-up
PD: Pulled-down B4/B8IF: 3V= B4, 5V= B8IF
TEST IN: Should be tied to $V_{DD3.3}$ or V_{SS} specified in Symbol column.

5-2. Pin assignment table 2

NO.	I/O	Symbol	Note	
			Input Buffer	Output Buffer
31	-	V_{SS}	-	-
32	-	$V_{DD3.3}$	-	-
33	-	V_{DD}	-	-
34	I	#FCD	LVTTL	-
35	B	D10	LVTTL	B4/B8IF
36	B	D2	LVTTL	B4/B8IF
37	B	D9	LVTTL	B4/B8IF
38	B	D1	LVTTL	B4/B8IF
39	-	V_{SS}	-	-
40	I	#CD	LVTTL, S	-
41	I	A3	LVTTL	-
42	-	NC	-	-
43	I	A0	LVTTL	-
44		V_{SS}	-	-
45	O (Tri)	#IOIS16 (WP)	-	B4/B8IF
46	I	A1	LVTTL	-
47	I	#REG	LVTTL, PU	-
48	I	A2	LVTTL	-
49	-	V_{DD}	-	-
50	B	D8	LVTTL	B4/B8IF
51	B	D0	LVTTL	B4/B8IF
52	O (Tri)	#INPACK	-	B4/B8IF
53	I	A4	LVTTL	-
54	-	V_{SS}	-	-
55	I	RESET	LVTTL	-
56	I	A5	LVTTL	-
57	I	A6	LVTTL	-
58	-	$V_{DD3.3}$	-	-
59	-	V_{SS}	-	-
60	I	#WE	LVTTL, S, PU	-

I: **Input**
O: **Output** **O (Tri):** **Tri-state**
B: **Bidirection**

Notice: Buffer Type

S: Schmidt LVTTL: 3V LVTTL level (same with 5V) PU: Pulled-up

PD: Pulled-down B4/B8IF: 3V= B4, 5V= B8IF

TEST IN: Should be tied to $V_{DD3.3}$ or V_{SS} specified in Symbol column.

5-3. Pin assignment table 3

NO.	I/O	Symbol	Note	
			Input Buffer	Output Buffer
61	I	#IOWR	LVTTL, S, PU	-
62	I	A7	LVTTL	-
63	-	NC	-	-
64	-	V_{SS}	-	-
65	-	V_{DD}	-	-
66	I	A8	LVTTL	-
67	I	#IORD	LVTTL, S, PU	-
68	I	#OE	LVTTL, S, PU	-
69	I	#CE2	LVTTL, PU	-
70	-	V_{SS}	-	-
71	I	#CE1	LVTTL, PU	-
72	I	A9	LVTTL	-
73	B	D15	LVTTL	B4/B8IF
74	B	D7	LVTTL	B4/B8IF
75	B	D14	LVTTL	B4/B8IF
76	-	V_{SS}	-	-
77	B	D6	LVTTL	B4/B8IF
78	B	D13	LVTTL	B4/B8IF
79	B	D5	LVTTL	B4/B8IF
80	-	V_{DD}	-	-
81	-	$V_{DD3.3}$	-	-
82	I	A10	LVTTL	-
83	-	V_{SS}	TEST IN	-
84	-	V_{SS}	TEST IN	-
85	B	D12	LVTTL	B4/B8IF
86	-	V_{SS}	-	-
87	B	D4	LVTTL	B4/B8IF
88	B	D11	LVTTL	B4/B8IF
89	B	D3	LVTTL	B4/B8IF
90	I	SELBSY	LVTTL, PD	-

I: Input
O: Output **O (Tri): Tri-state**
B: Bidirection

Notice: Buffer Type

S: Schmidt LVTTL: 3V LVTTL level (same with 5V) PU: Pulled-up

PD: Pulled-down B4/B8IF: 3V= B4, 5V= B8IF

TEST IN: Should be tied to $V_{DD3.3}$ or V_{SS} specified in Symbol column.

5-4. Pin assignment table 4

NO.	I/O	Symbol	Note	
			Input Buffer	Output Buffer
91	-	V_{SS}	-	-
92	I	#PONRST	LVTTL, S	-
93	-	V_{SS}	TEST IN	-
94	O (Tri)	#IREQ (READY)	-	B4/B8IF
95	-	V_{SS}	TEST IN	-
96	-	V_{DD}	-	-
97	-	$V_{DD3.3}$	-	-
98	I	XI	CLOCK IN	-
99	O	XO	-	CLOCK OUT
100	-	V_{SS}	-	-
101	O	OSCOUT	-	B4
102	-	$V_{DD3.3}$	-	-
103	O	FCLE / MMCLK	-	B8
104	O	FALE	-	B4
105	I	#FBSY	LVTTL, S	-
106	O (Tri)	#FCE	-	B4
107	O (Tri)	#FRE	-	B4
108	-	V_{SS}	-	-
109	B	FD4	LVTTL	B4
110	B	FD5	LVTTL	B4
111	B	FD6	LVTTL	B4
112	B	FD7	LVTTL	B4
113	-	V_{DD}	-	-
114	-	$V_{DD3.3}$	-	-
115	-	V_{SS}	-	-
116	B	#FWE / MMCMD	LVTTL	B4
117	O	#FWP	-	B4
118	-	V_{SS}	-	-
119	I	RMCLK	LVTTL, S	-
120	O	OCTL	-	B4

I: **Input**
O: **Output** **O (Tri):** **Tri-state**
B: **Bidirection**

Notice: Buffer Type

S: Schmidt LVTTL: 3V LVTTL level (same with 5V) PU: Pulled-up

PD: Pulled-down B4/B8IF: 3V= B4, 5V= B8IF

TEST IN: Should be tied to $V_{DD3.3}$ or V_{SS} specified in Symbol column.

5-5. Pin assignment table 5

NO.	I/O	Symbol	Note	
			Input Buffer	Output Buffer
121	O	OUTCLK	-	B4
122	I	MCLK	LVTTL, S	-
123	-	VSS	-	-
124	B	FD0	LVTTL	B4
125	B	FD1	LVTTL	B4
126	B	FD2	LVTTL	B4
127	B	FD3	LVTTL	B4
128	-	VSS	-	-

I: Input
O: Output O (Tri): Tri-state
B: Bidirection

Notice: Buffer Type

S: Schmidt LVTTL: 3V LVTTL level (same with 5V) PU: Pulled-up
PD: Pulled-down B4/B8IF: 3V= B4, 5V= B8IF
TEST IN: Should be tied to $V_{DD3.3}$ or V_{SS} specified in Symbol column.

6. Pin description

6-1. Host interface 1

Pin name	Pin number	I/O	Pin function	Functional description
V_{DD}	33,49,65,80,96, 113	-	POWER SUPPLY	A power terminal for PC card interface circuit.
$V_{DD3.3}$	1,17,26,32,58,81, 97,102,114,	-	POWER SUPPLY	A power terminal other than PC card interface circuit.
V_{SS}	7,12,16,22,27,31, 39,44,54,59,64, 70,76,83,84,86, 91,93,95,100, 108,115,118,123, 128	-	GROUND	A ground terminal.
NC	42,63	-	NON CONNECTION	An open terminal. Keep it in the open state.
RESET	55	I	CARD RESET	A reset terminal. If set to ”1”, all the internal states including FCR are initialized. Set to the reset state if an edge moved to the assert state is detected, and reset is cleared if the negate state is detected. If, when SD Memory Card is used, this terminal is cleared from ”1” to ”0”, CMD0 for media reset is issued two times.
D15 - D0	73,75,78,85,88, 35,37,50,74,77, 79,87,89,36,38,51	B	DATA BUS	Data bus of 16-bit width (2 bytes). D15 is MSB and D0 is LSB. Normally, this bus is set to the input state and, only if read by the host, set to the output state.
A10 - A0	82,72,66,62,57, 56,53,41,48,46,43	I	ADDRESS BUS	Address bus. A10 is MSB and A0 is LSB. In TC6374AF, maximum number of address is 11. Number of decodes differ per mode. In word access, A0 is disabled.
#REG	47	I	ATTRIBUTE MEMORY SELECT	Set to “1”, Memory Mapped mode allows accessing I/O space with #OE and #WE. If #REG set to ”0”, CIS and FCR can be accessed by #OE and #WE, or by #IORD and #IOWR, I/O space in each mode of Independent I/O, Primary/Secondary can be accessed.(with pull-up resistor)
#CE1	71	I	CARD ENABLE 1	Set to “0” if accessed by host via D7 - D0 (with pull-up resistor)
#CE2	69	I	CARD ENABLE 2	Set to “0” if accessed by host via D15 - D8. Odd number addresses only can be accessed from D15 - D8 irrespective of A0 (with pull-up resistor)
#OE	68	I	OUTPUT ENABLE	Used to read I/O space in the CIS, FCR and Memory Mapped modes. In the write operation, this terminal shall be disabled (with pull-up resistor)
#WE	60	I	WRITE ENABLE	Used to write I/O space in the FCR and Memory Mapped mode (with pull-up resistor)

6-2. Host interface 2

Pin name	Pin number	I/O	Pin function	Functional description
#IORD	67	I	I/O READ	Used to read I/O space in Independent I/O, Primary and Secondary modes. In other modes than above, this terminal is disabled (with pull-up resistor)
#IOWR	61	I	I/O WRITE	Used to write to I/O space in Independent I/O, Primary and Secondary modes. In other modes than above, this terminal is disabled (with pull-up resistor)
#IOIS16 (WP)	45	O	I/O IS 16 bits PORT (WRITE PROTECT)	Fixed to “L” in the Independent I/O mode. In Primary or Secondary mode, “L” is outputted if data bus allows 16-bit access. With memory card interface, this terminal indicates the media write protect state for WP, i.e. ”H” for write protect state or ”L” for non- write protect state. Input values from FPSD terminal (i.e. SmartMedia™ write protect seal detect signal) and SDWP terminal (i.e. SD Memory Card write protect switch detect signal) are OR’ed and directly outputted from this terminal (This terminal is, if in the memory card interface, is set to H if FPSD=“1”, MMWP=“1” or MROM is inserted)
# IREQ (READY)	94	O	INTERRUPT REQUEST (READY)	Two types of output format are allowed for interrupt request in the I/O card interface. It can be changed by FCR Configuration Option register: LevIREQ”D6” bit. With this bit set to ”1”, the terminal is in the pulse mode (“L” pulse width of about 800ns) if it is in the level mode and set to “0”. Initial value immediately after reset is set to the value in the level mode. Output timing of the terminal is when ATA Status register: BSY”D7” bit changes ”H”->“L”. The terminal provides RDY/BSY function in the memory card interface. Or, if ATA Status register: BSY”D7”! bit is set to ”1”, or FCR Card Configuration and Status register:PWRDWN bit are in the setting mode, ”L” is outputted.
#INPACK	52	O	INPUT PORT ACKNOWLEDGE	Only if #CE1, #CE2 and #IORD are set to ”0” and the address on address bus matches with that in I/O space, the terminal outputs ”L”. In the memory card interface, the terminal outputs “Hi-Z”.

6-3. SD memory card/ MultiMediaCard/ SmartMedia™/ NOR flash memory interface 1

Pin name	Pin number	I/O	Pin function	Functional description
FD7 - FD4	112-109	B	MEDIA DATA BUS	The terminal is prepared to connect with media data bus. If clock is stabled after resetting and NOR flash memory is re-written, it takes the upper position of NOR flash memory data bus. In other modes, it takes the upper position of address/data common bus to SmartMedia™. Address and data (including command) are discriminated by FALE and FCLE. The terminal is set to Hi-Z when #CD="H"(media non-inserted).
FD3 - FD0	127-124	B	MEDIA DATA BUS	The terminal is prepared to connect with media data bus. If clock is stabled after resetting and NOR flash memory is re-written, it takes the lower position of NOR flash memory data bus. In other modes, it takes the lower position of address/data common bus to SmartMedia™. Address and data (including command) are discriminated by FALE and FCLE. When SD Memory Card is used, it is used as 4 bit data bus. If MultiMediaCard is used and SD Memory Card is in the 1 bit mode, FD0 only is used. It is set to Hi-Z when #CD= "H"(media non-inserted).
#FCE	106	O	SmartMedia™ CHIP ENABLE	The terminal indicates the chip enable output signal of SmartMedia™. If #CD="H"(media not-inserted), it indicates Hi-Z.
FCLE/MMCLK	103	O	SmartMedia™ COMMAND LATCH ENABLE/SD Memory Card & MultiMediaCard CLOCK	The terminal indicates, if SmartMedia™ is used, the command latch enable output signal to SmartMedia™. If command is outputted to FD bus, it outputs "H". If SD Memory Card and MultiMediaCard are used, it indicates 250KHz, 2MHz, 8MHz and16MHz clock output signal to SD Memory Card and MultiMediaCard. Clock output frequency is determined by the maximum operation frequency of media. It is set to "L" when #CD="H"(media not-inserted).
FALE	104	O	SmartMedia™ ADDRESS LATCH ENABLE	Indicates address latch enable output signal to SmartMedia™. Outputs "H" if address is outputted to FD bus. The terminal is set to "L" if #CD="H"(media not-inserted).
#FRE	107	O	SmartMedia™ READ ENABLE	Indicates read enable output signal to SmartMedia™. Outputs "L" if address is outputted to FD bus. The terminal is set to "Hi-Z" if #CD="H"(media not-inserted).
#FWE/MMCMD	116	B	SmartMedia™ WRITE ENABLE/SD Memory Card & MultiMediaCard COMMAND	Indicates the write enable output signal to SmartMedia™ if used. Outputs "L" if written to FD bus. If SD Memory Card and MultiMediaCard are used, it becomes command/response input/output signal from/to SD Memory Card and MultiMediaCard. The terminal is set to Hi-Z when #CD="H" (media not inserted).
#FBSY	105	I	SmartMedia™ BUSY	Indicates ready/busy input signal from SmartMedia™. Indicates the busy if "0" is inputted, or the ready if "1" is inputted. Connects with the terminal via pull-up resistor from SmartMedia™ ready/busy output.
#FWP	117	O	SmartMedia™ WRITE PROTECT	Indicates write protect output signal to SmartMedia™. Write protection is enabled except for the time when SmartMedia™ is accessed. The terminal is set to "L" if #CD= "H"(media not inserted).

6-4. SD memory card/ MultiMediaCard/ SmartMedia™/ NOR flash memory interface 2

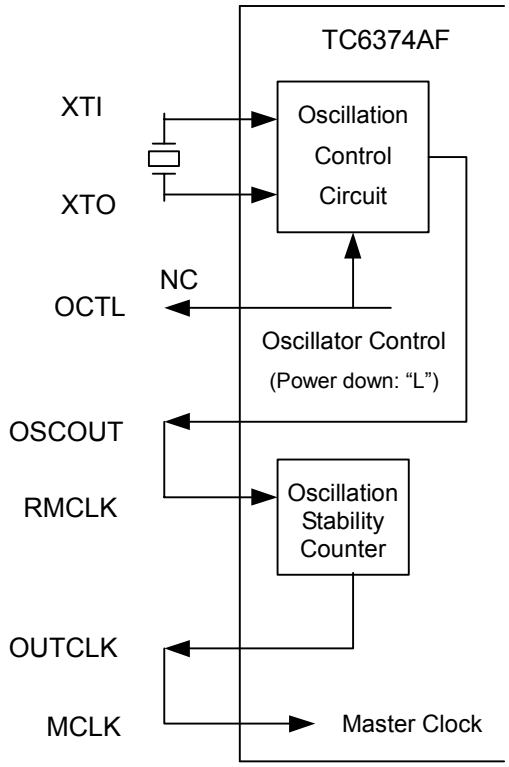
Pin name	Pin number	I/O	Pin function	Functional description
FPSD	25	I	SmartMedia™ WRITE PROTECT LABEL DETECT	Indicates the write protect input signal from SmartMedia™ write protect seal. If ”1” is inputted to the terminal, write related commands from host are aborted. The terminal input state is reflected to Pin Replacement Register: RWProt “D0” bit and ATA Error Register: WP”D6” bit on the to WP terminal and FCR, then the terminal input logic is directly outputted. The terminal will not change after the power is turned on, and must not be changed.
SDWP	30	I	SD Memory Card WRITE PROTECT DETECT	Indicates the write protect input signal from SD Memory Card write protect switch. If ”1” is inputted to the terminal, write related commands from host are aborted. The terminal input state is reflected to Pin Replacement Register: RWProt “D0” bit and ATA Error Register: WP”D6” bit on the to WP terminal and FCR, then the terminal input logic is directly outputted. The terminal will not change after the power is turned on, and must not be changed.
#FCD	34	I	SELECT MEDIA TYPE	Prepared to select the media type connected with TC6374AF. If the terminal input is set to ”0”, it is recognized as SmartMedia™, or if set to ”1”, it is recognized as SD Memory Card or MultiMediaCard.
#CD	40	I	MEDIA DETECT	Prepared to detect that TC6374AF is connected with media. If the terminal input is set to ”0”, it is recognized as media being connected, carrying out the normal operation. If the terminal input is set to ”1”, it is recognized that no media is connected, then TC6374AF enters the internal reset state and all removable media interface terminals turns to Hi-Z except for FCLE, FALE, and #FWP. In such event, OCTL=“L”, oscillation stops and ATA Status Register: BSY”D7” bit turns to ”H”. If the terminal state changes ”1”->“0”, the internal reset state is cleared, and the media is initialized 200ms after(with which contact between connector and media becomes stable). When SD Memory Card is used, the terminal is set to ”0”. If media insertion is detected, CMD0 is issued two times to initialize the media.
#NOR_CE	2	O	NOR CHIP ENABLE	Chip enable output signal used for the NOR flash memory in controller firmware.
#NOR_WE	4	O	NOR WRITE ENABLE	Write enable output signal used for the NOR flash memory in controller firmware.
#NOR_OE	3	O	NOR OUTPUT ENABLE	Output enable output signal used for the NOR flash memory in controller firmware.
#NOR_BSY	8	I	NOR BUSY	Busy signal used for the NOR flash memory in controller firmware.
NOR_A13 – 0	29,28,24,23 ,21-18,14,1 3,11,10,6,5	O	NOR ADDRESS BUD	Chip enable output signal used for the NOR flash memory in controller firmware.
SH/#FJ	15	I	SELECT NOR TYPE	Prepared to select the NOR flash memory type in controller firmware. If the input is set to ”0”, unit-1 3.3V NOR flash memory of Fujitsu (AMD) may be used. If the input is set to ”1”, unit-1 3.3V NOR flash memory of Sharp (Intel) may be used.
#NOR_RP	9	O	NOR RESET/DEEP POWER-DOWN	Prepared to control #RP terminal of flash memory if NOR flash of Sharp is used.

6-5. Others

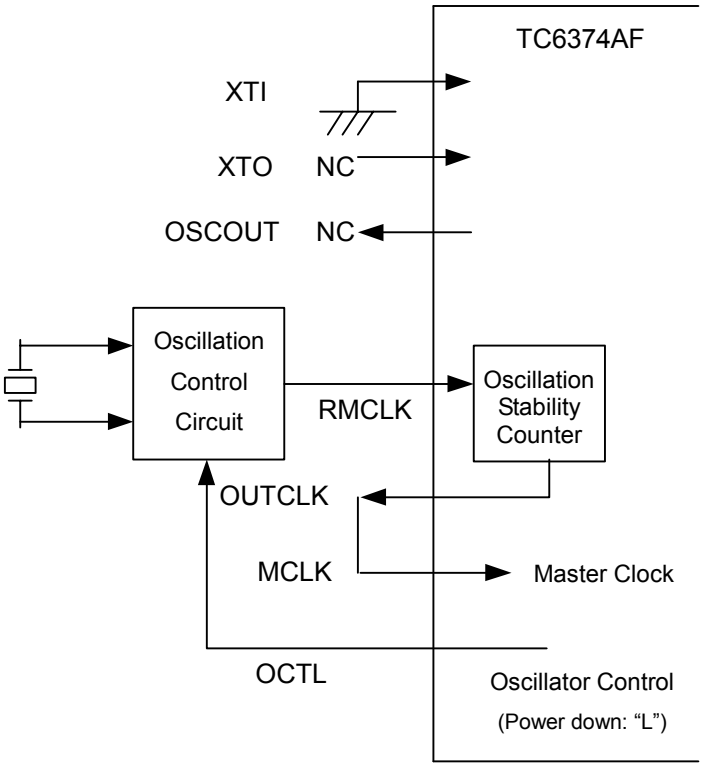
Pin name	Pin number	I/O	terminal function	functional description
#PONRST	92	I	POWER ON RESET	A terminal for performing the power-on reset to TC6374AF. Set to ”0” to move TC6374AF internally to the reset state, or if set to ”1”, the reset is cleared. When SD Memory Card is used, #CD is set to “0”(media insertion state). If the terminal is cleared from ”0” to ”1”, CMD0 is issued two times for media reset.
XI	98	I	CLOCK INPUT	Mask clock input to TC6374AF. Provides a terminal for duty ratio 45 - 55% 16 MHz oscillation module connection. Connect the terminal to the ground if an oscillator is connected with.
XO	99	O	CLOCK INPUT	Mask clock input to TC6374AF. Provides a terminal for duty ratio 45 - 55% 16 MHz oscillation module connection. Keep the terminal open if an oscillator is connected with.
OSCOUT	101	O	OSCILLATOR OUTPUT TO RMCLK	Connect directly to RMCLK if oscillation module is used. If the oscillator is used, keep the terminal open.
SELBSY	90	I	SELECT BUSY	A terminal to select busy time after ATA command is accepted. If set to ”0”, minimum busy time is about 150us immediately after ATA command is accepted. If set to ”1”, no busy time limit is imposed immediately after ATA command is accepted. Set ting to “0” as a default is recommended.
RMCLK	119	I	DEFERENCE MASTER CLOCK INPUT	Mask clock input to TC6374AF. Provides a terminal for duty ratio 45 – 55% 16 MHz oscillator connection. Directly connect with OSCOUT if an oscillation module is used.
OUTCLK	121	O	CLOCK OUT	Clock output after the oscillation becomes stable. Directly connect with MCLK.
MCLK	122	I	MASTER CLOCK INPUT TO OUTCLK	Master clock input to TC6374AF internal logic. Directly connect with OUTCLK.
OCTL	120	O	CLOCK CONTROL	Oscillator control signal. During the power-down and in the media not-connected state (#CD=“1”), ”L” is outputted and oscillation stop is requested. If the oscillator with oscillation control function is used, connect with the oscillator’s oscillation control terminal. If oscillation module is used, keep the terminal open.

6-6. Oscillation Circuit

The case which connected Oscillation Module



The case which connected Oscillator



6-7. Notes on 3in1 PC Card ATA adapter

Note: For the system design, refer to the attached document: "TC6374AF reference design description (reference circuit diagram and information sheet)". This document is updated as necessary, check the latest version by inquiry.

#1. RESET signal: For the compatibility with PC card interface, add a capacitor between a terminal and GND. Put pull-up resistorsto the terminal. (see reference circuit diagram)

#2. #CE1 signal: If, due to the crosstalk by simultaneous data bus switching by target system, add a capacitor between a terminal and GND. (see reference circuit design)

#3. #CE2 signal: If, due to the crosstalk by simultaneous data bus switching by target system, add a capacitor between a terminal and GND. (see reference circuit design)

#4. FPSD signal: Connect the terminal with the SmartMedia™ write protect output using a resistor of about 100kΩ pull-down.

#5. #PONRST signal: Apply a voltage detector of 2.9V in front stage of the terminal.

7. Operational descryption

7-1. Outline of Interface

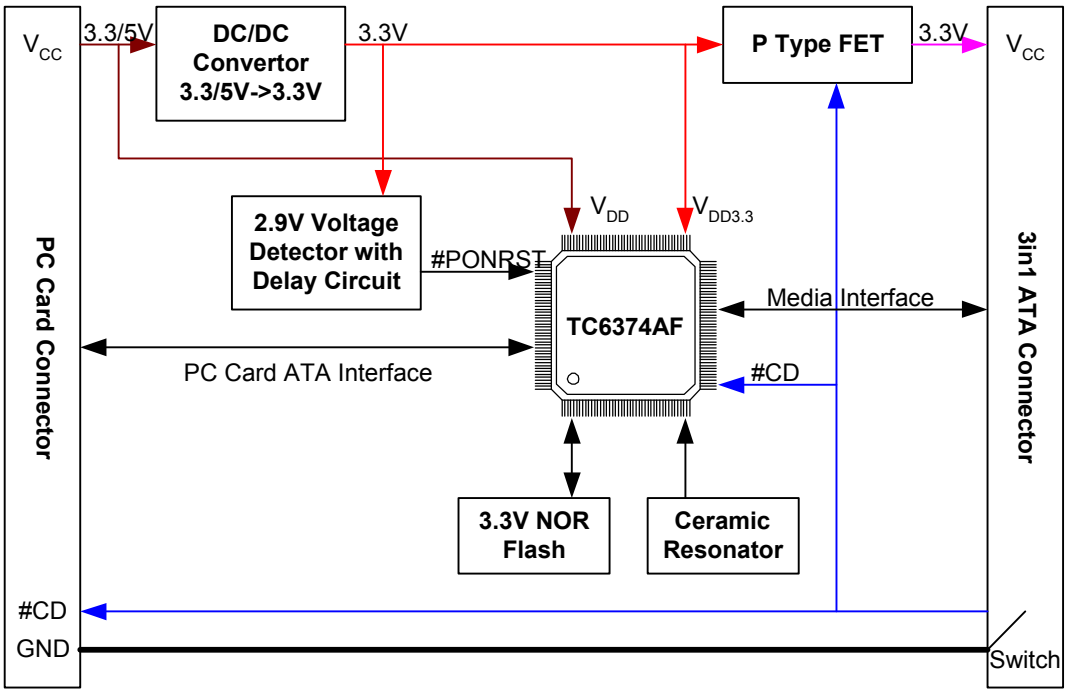
TC6374AF has four types of interfaces listed below.

- Host interface
- SD Memory Card / MultiMediaCard interface
- SmartMedia™ interface
- NOR flash memory interface

For examples of system configuration and interface, refer to 7-2 and 7-3 respectively.

7-2. Example of system configuration

[3in1 PC Card ATA Adaptor]



Note: The diagram above is a simplified one. For the detailed information, refer to the attached document: "TC6374AF reference design description (reference circuit diagram and information sheet)". As the information is updated as necessary, keep the latest one by inquiry.

7-3. Host interface

TC6374AF supports as a host interface the PC Card (Memory, ATA) interface. In PC Card ATA interface, it supports 4 types of I/O mode(Memory Mapped I/O, Independent I/O, Primary and Secondary). Furthermore, PC Card interface has a memory space called attribute memory allowing the software to configure TC6374AF("*" indicated in the table shown later means "Don't Care".).

7-4. PC Card interface

7-4-1. Attribute Memory space

Attribute memory consists of CIS(Card Information Structure) with which a host recognizes the function type connected with TC6374AF and FCR (Function Configuration Register) for configuration. Attribute memory can be accessed of course in the memory interface state, and additionally, even after set to the I/O interface. Access methods and addresses of register in the attribute memory are listed below.

7-4-1-1. Attribute Memory read operation

During the Attribute Memory Read Cycle, set #WE to inactive "1", and #REG and #OE to active "0". #CE2, #CE1 and A0 are controlled at odd/even addresses, though Attribute Memory access is enabled only at even address data.

Function Mode	#REG	#CE2	#CE1	A0	#OE	#WE	D15 - D8	D7 - D0
Standby Mode	*	1	1	*	*	*	Hi-Z	Hi-Z
Byte Access (8 Bits)	0	1	0	0	0	1	Hi-Z	Even byte
	0	1	0	1	0	1	Hi-Z	Invalid
Word Access (16 Bits)	0	0	0	*	0	1	Invalid	Even byte
Odd Byte Only Access	0	0	1	*	0	1	Invalid	Hi-Z

7-4-1-2. Attribute Memory write operation

During Attribute Memory Write Cycle, set #OE to inactive "1", and #REG and #WE to active "0".

Function Mode	#REG	#CE2	#CE1	A0	#OE	#WE	D15 - D8	D7 - D0
Standby Mode	*	1	1	*	*	*	*	*
Byte Access (8 Bits)	0	1	0	0	1	0	*	Even byte
	0	1	0	1	1	0	*	*
Word Access (16 Bits)	0	0	0	*	1	0	*	Even byte
Odd Byte Only Access	0	0	1	*	1	0	*	*

7-4-1-3. Attribute Memory address

Address	#CE	#REG	#WE	#OE	FCR	Read/Write
*	1	*	*	*	Standby	Invalid
*	0	1	1	0	Common Memory Read	R
*	0	1	0	1	Common Memory Write	W
*	0	0	1	0	Card Information Structure Read	R
*	0	0	*	*	Invalid Access	Invalid
200h	0	0	1	0	Configuration Option Register	R/W
	0	0	0	1		
202h	0	0	1	0	Card Configuration and Status Register	R/W
	0	0	0	1		
204h	0	0	1	0	Pin Replacement Register	R
	0	0	0	1		
206h	0	0	1	0	Socket and Copy Register	R/W
	0	0	0	1		
208h	0	0	1	0	Extended Status Register	R/W
	0	0	0	1		
20Ah	0	0	1	0	I/O Base 0	R/W
	0	0	0	1		
20Ch	0	0	1	0	I/O Base 1	R/W
	0	0	0	1		
20Eh	0	0	1	0	I/O Base 2	R/W
	0	0	0	1		
210h	0	0	1	0	I/O Base 3	R/W
	0	0	0	1		
212h	0	0	1	0	I/O Limit	R/W
	0	0	0	1		
214h	0	0	1	0	Power Management Register	R/W
	0	0	0	1		

7-4-2. Common Memory space

7-4-2-1. Common Memory read operation

During Common Memory Read Cycle, set #REG and #WE to inactive “1”, and #OE to active “0”.

Function Mode	#REG	#CE2	#CE1	A0	#OE	#WE	D15 - D8	D7 - D0
Standby Mode	*	1	1	*	*	*	Hi-Z	Hi-Z
Byte Access (8 Bits)	1	1	0	0	0	1	Hi-Z	Even byte
	1	1	0	1	0	1	Hi-Z	Odd byte
Word Access (16 Bits)	1	0	0	*	0	1	Odd byte	Even byte
Odd Byte Only Access	1	0	1	*	0	1	Odd byte	Hi-Z

7-4-2-2. Common Memory write operation

During Common Memory Write Cycle, set #REG and #OE to inactive “1”, and #WE to active “0”.

Function Mode	#REG	#CE2	#CE1	A0	#OE	#WE	D15 - D8	D7 - D0
Standby Mode	*	1	1	*	*	*	*	*
Byte Access (8 Bits)	1	1	0	0	1	0	*	Even byte
	1	1	0	1	1	0	*	Odd byte
Word Access (16 Bits)	1	0	0	*	1	0	Odd byte	Even byte
Odd Byte Only Access	1	0	1	*	1	0	Odd byte	*

7-4-3. I/O space

7-4-3-1. Read operation in I/O Addressing mode

Function Mode	#REG	#CE2	#CE1	A0	#IORD	#IOWR	D15 - D8	D7 - D0
Standby Mode	*	1	1	*	*	*	Hi-Z	Hi-Z
Byte Access (8 Bits)	0	1	0	0	0	1	Hi-Z	Even byte
	0	1	0	1	0	1	Hi-Z	Odd byte
Word Access (16 Bits)	0	0	0	*	0	1	Odd byte	Even byte
I/O Inhibit	1	*	*	*	0	1	Hi-Z	Hi-Z
Odd Byte Only Access	0	0	1	*	0	1	Odd byte	Hi-Z

7-4-3-2. Write operation in I/O Addressing mode

Function Mode	#REG	#CE2	#CE1	A0	#IORD	#IOWR	D15 - D8	D7 - D0
Standby Mode	*	1	1	*	*	*	*	*
Byte Access (8 Bits)	0	1	0	0	1	0	*	Even byte
	0	1	0	1	1	0	*	Odd byte
Word Access (16 Bits)	0	0	0	*	1	0	Odd byte	Even byte
I/O Inhibit	1	*	*	*	1	0	*	*
Odd Byte Only Access	0	0	1	*	1	0	Odd byte	*

7-4-4. Access method in ATA register

TC6374AF supports four types of I/O addressing modes for PC Card ATA in the host interface. I/O Addressing mode is determined by the configuration in the FCR Configuration Option Register: D5 - D0 bit, “Function Configuration Index”. Access method and addresses in each register are listed below for each I/O Addressing mode.

7-4-4-1. Memory Mapped mode

Each register address is shown in the Memory Mapped mode.

7-4-4-1-1. Lower byte access

#CE2	#CE1	#REG	Offset	A10	A9-A4	A3	A2	A1	A0	D15-D8	D7-D0	
											#OE = “0”	#WE = “0”
1	0	1	0h	0	*	0	0	0	0	Hi-Z	Read Data	Write Data
1	0	1	1h	0	*	0	0	0	1		Error	Features
1	0	1	2h	0	*	0	0	1	0		Sector Count	Sector Count
1	0	1	3h	0	*	0	0	1	1		Sector Number	Sector Number
1	0	1	4h	0	*	0	1	0	0		Cylinder Low	Cylinder Low
1	0	1	5h	0	*	0	1	0	1		Cylinder High	Cylinder High
1	0	1	6h	0	*	0	1	1	0		Device/Head	Device/Head
1	0	1	7h	0	*	0	1	1	1		Status	Command
1	0	1	8h	0	*	1	0	0	0		Duplicate Read Data	Duplicate Write Data
1	0	1	9h	0	*	1	0	0	1		Duplicate Odd Read Data	Duplicate Odd Write Data
1	0	1	Dh	0	*	1	1	0	1		Duplicate Error	Duplicate Features
1	0	1	Eh	0	*	1	1	1	0		Alternate Status	Device Control
1	0	1	Fh	0	*	1	1	1	1		Device Address	Reserved
1	0	1	-	1	*	*	*	*	0		Read Data	Write Data
1	0	1	-	1	*	*	*	*	1		Odd Read Data	Odd Write Data

7-4-4-1-2. Upper byte access

#CE2	#CE1	#REG	Offset	A10	A9-A4	A3	A2	A1	A0	D15-8		D7-D0
										#OE = “0”	#WE = “0”	
0	1	1	0h,1h	0	*	0	0	0	*	Error	Features	Hi-Z
0	1	1	2h,3h	0	*	0	0	1	*	Sector Number	Sector Number	
0	1	1	4h,5h	0	*	0	1	0	*	Cylinder High	Cylinder High	
0	1	1	6h,7h	0	*	0	1	1	*	Status	Command	
0	1	1	8h,9h	0	*	1	0	0	*	Duplicate Odd Read Data	Duplicate Odd Write Data	
0	1	1	Ch,Dh	0	*	1	1	0	*	Duplicate Error	Duplicate Features	
0	1	1	Eh,Fh	0	*	1	1	1	*	Device Address	Reserved	
0	1	1	-	1	*	*	*	*	*	Odd Read Data	Odd Write Data	

7-4-4-1-3. Word access

#CE2	#CE1	#REG	Offset	A10	A9-A4	A3	A2	A1	A0	#OE = "0"	#WE = "0"
										Upper Byte"D15-D8"	Upper Byte"D15-D8"
										Lower Byte"D7-D0"	Lower Byte"D7-D0"
0	0	1	0h,1h	0	*	0	0	0	*	Odd Read Data Even Read Data	Odd Write Data Even Write Data
0	0	1	2h,3h	0	*	0	0	1	*	Sector Number Sector Count	Sector Number Sector Count
0	0	1	4h,5h	0	*	0	1	0	*	Cylinder High Cylinder Low	Cylinder High Cylinder Low
0	0	1	6h,7h	0	*	0	1	1	*	Status Device / Head	Command Device / Head
0	0	1	8h,9h	0	*	1	0	0	*	Duplicate Odd Read Data Duplicate Even Read Data	Duplicate Odd Write Data Duplicate Even Write Data
0	0	1	Ch,Dh	0	*	1	1	0	*	Duplicate Error *	Duplicate Features
0	0	1	Eh,Fh	0	*	1	1	1	*	Device Address Alternate Status	Reserved Device Control
0	0	1	-	1	*	*	*	*	*	Odd Read Data Even Read Data	Odd Write Data Even Write Data

7-4-4-2. Independent I/O mode

Each register address is shown in the Independent I/O mode.

7-4-4-2-1. Lower byte access

#CE2	#CE1	#REG	Offset	A10-A4	A3	A2	A1	A0	D15-D8	D7-D0	
										#IORD = “0”	#IOWR = “0”
1	0	0	0h	*	0	0	0	0	Hi-Z	Read Data	Write Data
1	0	0	1h	*	0	0	0	1		Error	Features
1	0	0	2h	*	0	0	1	0		Sector Count	Sector Count
1	0	0	3h	*	0	0	1	1		Sector Number	Sector Number
1	0	0	4h	*	0	1	0	0		Cylinder Low	Cylinder Low
1	0	0	5h	*	0	1	0	1		Cylinder High	Cylinder High
1	0	0	6h	*	0	1	1	0		Device/Head	Device/Head
1	0	0	7h	*	0	1	1	1		Status	Command
1	0	0	8h	*	1	0	0	0		Duplicate Even Read Data	Duplicate Even Write Data
1	0	0	9h	*	1	0	0	1		Duplicate Odd Read Data	Duplicate Odd Write Data
1	0	0	Ch, Dh	*	1	1	0	*		Duplicate Error	Duplicate Features
1	0	0	Eh	*	1	1	1	0		Alternate Status	Device Control
1	0	0	Fh	*	1	1	1	1		Device Address	Reserved

7-4-4-2-2. Upper byte access

#CE2	#CE1	#REG	Offset	A10-A4	A3	A2	A1	A0	D15-8		D7-D0
									#IORD = “0”	#IOWR = “0”	
0	1	0	0h,1h	*	0	0	0	*	Error	Features	Hi-z
0	1	0	2h,3h	*	0	0	1	*	Sector Number	Sector Number	
0	1	0	4h,5h	*	0	1	0	*	Cylinder High	Cylinder High	
0	1	0	6h,7h	*	0	1	1	*	Status	Command	
0	1	0	8h,9h	*	1	0	0	*	Duplicate Odd Read Data	Duplicate Odd Write Data	
0	1	0	Ch,Dh	*	1	1	0	*	Duplicate Error	Duplicate Features	
0	1	0	Eh,Fh	*	1	1	1	*	Device Address	Reserved	

7-4-4-2-3. Word access

#CE2	#CE1	#REG	Offset	A10-A4	A3	A2	A1	A0	#IORD = "0" Upper Byte "D15-D8" Lower Byte "D7-D0"	#IOWR = "0" Upper Byte "D15-D8" Lower Byte "D7-D0"
0	0	0	0h,1h	*	0	0	0	*	Odd Read Data Even Read Data	Odd Write Data Even Write Data
0	0	0	2h,3h	*	0	0	1	*	Sector Number Sector Count	Sector Number Sector Count
0	0	0	4h,5h	*	0	1	0	*	Cylinder High Cylinder Low	Cylinder High Cylinder Low
0	0	0	6h,7h	*	0	1	1	*	Status Device/Head	Command Device/Head
0	0	0	8h,9h	*	1	0	0	*	Duplicate Odd Read Data Duplicate Even Read Data	Duplicate Odd Write Data Duplicate Even Write Data
0	0	0	Ch,Dh	*	1	1	0	*	Duplicate Error Hi-z	Duplicate Features *
0	0	0	Eh,Fh	*	1	1	1	*	Device Address Alternate Status	Reserved Device Control

7-4-4-3. Primary and Secondary I/O mode

Each register address is shown in the Primary, Secondary I/O mode.

7-4-4-3-1. Lower byte access

#CE2	#CE1	#REG	A10	A9-A4		A3	A2	A1	A0	D15-D8	D7-D0	
				Primary	Secondary						#IORD = “0”	#IOWR = “0”
1	0	0	*	1Fh	17h	0	0	0	0	Hi-z	Read Data	Write Data
1	0	0	*			0	0	0	1		Error	Features
1	0	0	*			0	0	1	0		Sector Count	Sector Count
1	0	0	*			0	0	1	1		Sector Number	Sector Number
1	0	0	*			0	1	0	0		Cylinder Low	Cylinder Low
1	0	0	*			0	1	0	1		Cylinder High	Cylinder High
1	0	0	*			0	1	1	0		Device/Head	Device/Head
1	0	0	*			0	1	1	1		Status	Command
1	0	0	*	3Fh	37h	0	1	1	0		Alternate Status	Device Control
1	0	0	*			0	1	1	1		Device Address	Reserved

7-4-4-3-2. Upper byte access

#CE2	#CE1	#REG	A10	A9-A4		A3	A2	A1	A0	D15-D8		D7-D0
				Primary	Secondary					#IORD = “0”	#IOWR = “0”	
0	1	0	*	1Fh	17h	0	0	0	*	Error	Features	Hi-z
0	1	0	*			0	0	1	*	Sector Number	Sector Number	
0	1	0	*			0	1	0	*	Cylinder High	Cylinder High	
0	1	0	*			0	1	1	*	Status	Command	
0	1	0	*	3Fh	37h	0	1	1	*	Device Address	Reserved	

7-4-4-3-3. Word access

#CE2	#CE1	#REG	A10	A9-A4		A3	A2	A1	A0	#IORD = "0"	#IOWR = "0"
				Primary	Secondary					Upper Byte "D15-D8" Lower Byte "D7-D0"	Upper Byte "D15-D8" Lower Byte "D7-D0"
0	0	0	*	1Fh	17h	0	0	0	*	Odd Read Data Even Read Data	Odd Write Data Even Write Data
0	0	0	*			0	0	1	*	Sector Number Sector Count	Sector Number Sector Count
0	0	0	*			0	1	0	*	Cylinder High Cylinder Low	Cylinder High Cylinder Low
0	0	0	*			0	1	1	*	Status Device/Head	Command Device/Head
0	0	0	*	3Fh	37h	0	1	1	*	Device Address Alternate Status	Reserved Device Control

7-5. Register description

Registers for attribute memory space and I/O space are described below.

7-5-1. CIS (Card Information Structure)

CIS is a read-only register used to indicate the attribute information about functions connected with TC6374AF. Its address is an even number in 000h - 1FFh for 256 bytes, and implemented with TC6374AF built-in RAM. At resetting, it is set by reading data from the firmware NOR flash memory, where TC6374AF sets RDY/BSY to ”L”, notifying the host interface of access-disabled. Default CIS is described below.

Note : CARD INFORMATION STRUCTURE is stored in TC6374AF firmware for NOR flash memory. Data shown below is a reference data (DEFAULT CARD INFORMATION STRUCTURE), and may be changed if so requested. Data modification is to be submitted within 256 byte. DEFAULT CARD INFORMATION STRUCTURE will not assure operations.

DEFAULT CARD INFORMATION STRUCTURE

Address	Data	Contens	Address	Data	Contens
000	01	Tuple ID (Device Information Tuple)	080	99	Functional Selection byte
002	03	Pointer for Next Tuple	082	07	Power: Parameter Selection byte (Vcc)
004	D9	Classification: I/O, Speed: 250ns	084	55	Power: Normal Voltage (5V)
006	01	Device Size 2Kbyte	086	4D	Power: Min Voltage (4.5V)
008	FF	End of Device Infromation Tuple	088	5D	Power: Max Voltage (5.5V)
00A	18	Tuple ID (JEDEC Device Information)	08A	64	I/O Space Description byte
00C	02	Pointer for Next Tuple	08C	F0	Interrupt Request: Interrupt Request Information
00E	DF	JEDEC Maker ID	08E	FF	Interrupt Request: IRQ0～7 Mask
010	01	JEDEC DeviceID (No VPP)	090	FF	Interrupt Request: IRQ8～15 Mask
012	20	Tuple ID (Manufacture Information)	092	20	Other Information (With CCSR Power-Down)
014	04	Pointer for Next Tuple	094	1B	Tuple ID (Configuration Entry) [Independent I/O]
016	00	Manufacture Code	096	05	Pointer for Next Tuple
018	00	“	098	01	Configuration Table Index byte
01A	00	Manufacture Information	09A	01	Interface Description Field
01C	00	“	09C	01	Functional Selection byte
01E	21	Tuple ID (Functional Information)	09E	B5	Power: Normal Voltage (3.3V)
020	02	Pointer for Next Tuple	0A0	1E	“ [Extension byte]
022	04	Card Function Code	0A2	1B	Tuple ID (Configuration Entry) [Primary I/O]
024	01	System Initialization Information	0A4	11	Pointer for Next Tuple
026	22	Tuple ID (Functional Extension)	0A6	C2	Configuration Table Index byte
028	02	Pointer for Next Tuple	0A8	41	Interface Description Field
02A	01	Disk-Functional Interface Tuple(TYPE1)	0AA	99	Functional Selection byte
02C	01	PC Card ATA Specification	0AC	07	Power: Parameter Selection byte (Vcc)
02E	22	Tuple ID(Functional Extension)	0AE	55	Power: Normal Voltage (5V)
030	03	Pointer for Next Tuple	0B0	4D	Power: Min Voltage (4.5V)
032	02	PC Card ATA Extension Tuple (TYPE2)	0B2	5D	Power: Max Voltage (5.5V)
034	04	ATA Functional byte1	0B4	EA	I/O Space Description byte
036	07	ATA Functional byte2	0B6	61	I/O Area Description byte
038	1C	Tuple ID (Additional Device Information Tuple)	0B8	F0	I/O Address Area
03A	04	Pointer for Next Tuple	0BA	01	01F0～01F7h
03C	03	3.3V Operation, WAIT Support	0BC	07	(8byte)
03E	D9	Classification: I/O, Speed: 250ns	0BE	F6	I/O Address Area
040	01	Device Size 2Kbyte	0C0	03	03F6～03F7h
042	FF	End of Device Information Tuple	0C2	01	(2byte)
044	1A	Tuple ID (Configuration Tuple)	0C4	EE	Interrupt Request Information (/IRQ14)
046	05	Pointer for Next Tuple	0C6	20	Othre Information (With CCSR Power-Down)
048	01	Field Size byte	0C8	1B	Tuple ID (Configuration Entry) [Primary I/O]
04A	03	Last Entry of Configuration Table	0CA	05	Pointer for Next Tuple
04C	00	CCR Base Address (L) 0200h	0CC	02	Configuration Table Index byte
04E	02	CCR Base Address (H) 0200h	0CE	01	Interface Description Field
050	0F	CCR Existence Mask 0h	0D0	01	Functional Selection byte
052	1B	Tuple ID (Configuration Entry) [Memory Mapped]	0D2	B5	Power: Normal Voltage (3.3V)
054	0A	Pointer for Next Tuple	0D4	1E	“ [Extension byte]
056	C0	Configuration Table Index byte	0D6	1B	Tuple ID [Secondary I/O]
058	C0	Interface Description Field	0D8	11	Pointer for Next Tuple
05A	A1	Functional Selection byte	0DA	C3	Configuration Table Index byte
05C	07	Power: Parameter Selectioin byte (Vcc)	0DC	41	Interface Description Field
05E	55	Power: Normal Voltage (5V)	0DE	99	Functional Selection byte
060	4D	Power: Min Voltage (4.5V)	0E0	07	Power: Parameter Selection byte (Vcc)
062	5D	Power: Max Voltage (5.5V)	0E2	55	Power: Normal Voltage (5V)
064	08	Memory address Book (LSB)	0E4	4D	Power: Min Voltage (4.5V)
066	00	Memory address Book (MSB)	0E6	5D	Power: Max Voltage (5.5V)
068	20	Other Information (With CCSR Power-Down)	0E8	EA	I/O Space Description byte
06A	1B	Tuple ID (Configuration Entry) [Memory Mapped]	0EA	61	I/O Area Description byte
06C	05	Pointer for Next Tuple	0EC	70	I/O Address Area
06E	00	Configuration Table Index byte	0EE	01	0170～0177h
070	01	Interface Description Field	0F0	07	(8byte)
072	01	Functional Selection byte	0F2	76	I/O Address Area
074	B5	Power: Normal Voltage (3.3V)	0F4	03	0376～0377h
076	1E	“ [Extension byte]	0F6	01	(2byte)
078	1B	Tuple ID (Configuration Entry) [Independent I/O]	0F8	EE	Interrupt Request Information (/IRQ14)
07A	0C	Pointer for Next Tuple	0FA	20	Other Information (With CCSR Power-Down)
07C	C1	Configuration Table Index byte	0FC	1B	Tuple ID [Secondary I/O]
07E	41	Interface Description Field	0FE	05	Pointer for Next Tuple

100	03	Configuration Table Index byte	120	00	End of Product Maker Information
102	01	Interface Description Field	122	20	Product Name Information
104	01	Functional Selection byte	124	20	“
106	B5	Power: Normal Voltage (3.3V)	126	20	“
108	1E	“ [Extension byte]	128	20	“
10A	15	Tuple ID (Product Informatioin Tuple)	12A	00	End of Product Name
10c	14	Pointer for Next Taple	12c	30	Product Version Informagion “0”
10E	05	Specification Version High[Ver.5]	12E	2E	“ “.”
110	00	Specification Version Low[.0]	130	30	“ “0”
112	20	Product Maker Information	132	00	End of Product Version Information
114	20	“	134	FF	End of Product Information Tuple
116	20	“	136	14	No-Link Tuple ID
118	20	“	138	00	Pointer for Next Tuple
11A	20	“	13A	FF	End of Progression Tuple
11c	20	“	13c	00	Null-tuple
11E	20	“	13E	00	Null-tuple
11E	20		13E	00	Null-tuple

7-5-2. FCRs (Function Configuration Registers)
The host to set TC6374AF uses these registers.

7-5-2-1. Configuration Option Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
200h	SRESET	LevIREQ	Function Configuration Index					
			Conf5	Conf4	Conf3	Conf2	Conf1	Conf0
Initial Value	0	1	0	0	0	0	0	0
Read/Write	R/W							

SRESET:

Used for PC Card Software Reset. Except that this bit is not reset, the same operation as in Power On Reset and Hardware Reset is applicable. If, when SD Memory Card is used, this bit is cleared from ”1” to ”0”, CMD0 is issued two times to initialize the media.
“1”: reset state “0”: reset cleared

LevIREQ:

A signal used to select the mod of interrupt signal to #IREQ terminal.
“1”: level mode (default) “0”: pulse mode

Function Configuration Index:

Used as an I/O mode select signal.

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Mode
0	0	0	0	0	0	Memory Mapped I/O
0	0	0	0	0	1	Independent I/O
0	0	0	0	1	0	Primary I/O 1F0~1F7/3F0~3F7
0	0	0	0	1	1	Secondary I/O 170~177/370~377

7-5-2-2. Card Configuration and Status Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
202h	Changed	SigChg	IOIs8	RFU	Audio	PwrDwn	Intr	IntrAck
Initial Value	0	0	0	0	0	0	0	0
Read/Write	0 Fixed		R/W	0 Fixed		R/W	R	0 Fixed

Changed:

Fixed to “0” since TC6374Af has no changes as specified in PC Card standard as shown below.

If Pin Replacement Register: D7-D4 bit is changed to ”1”, the above bit is set to 0 in TC6374AF.

If Extended Status Register bit is changed to”1”, for the purpose of modem card function, no changes occur in 3in1 PC Card ATA that uses TC6374AF.

SigChg:

Fixed to 0 in TC6374AF as no changes occur, which is to be treated in “Changed”.

IOIs8:

Indicates the data bus width on host interface.

“1” : 8 bit width “0” : 16 bit width (default)

This bit may be changed by executing ATA’s Set Feature command. Or, this bit is independent of #IOIS16 terminal operation.

PwrDwn:

Indicates the Power-down mode.

”1”: Power-down “0”: Operation state

If the bit is set to ”0”, the state stays in the ATA command state. If set to “1”, it is compatible with ATA stand-by mode. Even if, in the power-down mode clearing (transition), ATA command is disabled to accept, ATA Status Register:D6 bit “DRDY” will not move to ”L” (Not Ready). The host may enter the power-down state in the TC6374AF BSY mode. With the bit set to “1”, the oscillation stops.

Intr:

Operates with #IREQ terminal in parallel, though, if in the pulse mode, the bit operates as in the level mode.

“H” : #IREQ = “ L” “L” : #IREQ = “H”

IntrAck:

Intr bit read/write enable bit, fixed to **”0”.**

“0” : Intr = read-only “1” : Intr = read/write enabled

7-5-2-3. Pin Replacement Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
204h	CBVD1	CBVD2	CREDY	CWProt	RBVD1	RBVD2	RREDY	RWProt
Initial Value	0	0	0	0	1	1	1	-
Read/Write	0 Fixed				1 Fixed			R

D7 - D4:

Fixed to 0 since, in TC6374AF, no relevant changes occur in the PC Card standard under operation.

RWProt:

Outputs the input logic value of FPSD or SDWP terminal. The terminal will not change after the media insertion. No change allowed.

This bit goes to “1” when

- Using MROM or Read-only card
- “Permanent write protection” and “Temporary write protection” of the CSD is activated while Using SD memory card / MultiMediaCard

“0” : Non-write protect “1” : Write protect

7-5-2-4. Socket and Copy Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
206h	RFU	Copy Number			Socket Number			
Initial Value	0	0	0	0	0	0	0	0
Read/Write	R/W							

Copy Number:

Indicates the device number. If a card with same function is inserted to the host, the position of the card is written from the host. This value is compared with ATA Device/Head Register:D4 bit “DEV”. If not matched, TC6374AF will not respond with the access from host.

device 0: 000B=(D6,D5,D4)B

device 1: 001B=(D6,D5,D4)B

Socket Number:

Indicates the order of socket inserted, which is written by host. It does not affect **TC6374AF’s operation.**

7-5-2-5. Extended Status Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
208h	Event 3	Event 2	Event 1	ReqAttn	Enable 3	Enable 2	Enable 1	ReqAttn Enable
Initial Value	0	0	0	0	0	0	0	0
Read/Write	R/W							

This register is a read/write enabled for maintaining the compatibility, not affecting the **TC6374AF's operation.**

7-5-2-6. I/O Base 0 Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
20Ah	I/O Base 0							
Initial Value	0	0	0	0	0	0	0	0
Read/Write	R/W							

This register is a read/write enabled for maintaining the compatibility, not affecting the **TC6374AF's operation.**

7-5-2-7. I/O Base 1 Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
20Ch	I/O Base 1							
Initial Value	0	0	0	0	0	0	0	0
Read/Write	R/W							

This register is a read/write enabled for maintaining the compatibility, not affecting the **TC6374AF's operation.**

7-5-2-8. I/O Base 2 Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
20Eh	I/O Base 2							
Initial Value	0	0	0	0	0	0	0	0
Read/Write	R/W							

This register is a read/write enabled for maintaining the compatibility, not affecting the **TC6374AF's operation.**

7-5-2-9. I/O Base 3 Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
210h	I/O Base 3							
Initial Value	0	0	0	0	0	0	0	0
Read/Write	R/W							

This register is a read/write enabled for maintaining the compatibility, not affecting the **TC6374AF's operation.**

7-5-2-10. I/O Limit Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
212h	I/O Limit							
Initial Value	0	0	0	0	0	0	0	0
Read/Write	R/W							

This register is a read/write enabled for maintaining the compatibility, not affecting the **TC6374AF's operation.**

7-5-2-11. Power Management Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
214h	RFU (0)	RFU (0)	RFU (0)	RFU (0)	State Restored	Begin/ Done State Operation	Save/ Restore State	Stored State Exists
Initial Value	0	0	0	0	0	0	0	0
Read/Write	0 Fixed				R/W			0 Fixed

This register will not affect the **TC6374AF's operation.**

State Restored:

If, when Save/Restore State bit is set, Begin/Done State Operation bit is additionally set, this bit is set to "1". Cleared to "0" if this register is read.

Begin/Done State Operation:

Fixed to "0" when reading. If this bit is set to "1", State Restored bit is set to "1".

Save/Restore State:

A read/write enabled register.

7-5-3. ATA Registers

7-5-3-1. Data Register

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Data Word															
									Data byte							
Initial Value	Unidentified															
Read/Write	R/W															

A 16-bit register, used to transfer the data block between ATA data buffer in TC6374AF and host, allowing word access or byte access. Operation depends on data bus width, i.e. 8 bits or 16 bits, where, in 8 bit width, even and odd number data are outputted alternately. **For the detailed register's operation, refer to the outline description about ATA commands as well as ATA/ATAPI-5 standard.**

7-5-3-2. Error Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
	BBK	UNC(WP)	MC	IDNF	MCR	ABRT	NM	AMNF
Initial Value	0	0	0	0	0	0	0	1
Read/Write	R							

This register includes additional information about the sources of error generated when destination code is processed. Host must check this register if ATA Status Register: D0 bit "ERR" is set to "H". After Power On Reset or ATA Execute Device Diagnostic command is executed, this register is set to the diagnosis code. BBK, TKNOF and AMNF are present not for reporting the original error in detail, but for indicating the error code of ATA Execute Device Diagnostic command (for details, refer to the table below). **For the detailed operation of bits listed below, refer to the outline description about ATA commands as well as ATA/ATAPI-5 standard.**

BBK (Bad Block Detected):

Indicates that, in the sector's ID section, a mark of defective block is detected. TC6374AF is fixed to **"L".**

UNC (Uncorrectable Data Error) or WP (Write Protected Media):

Set to "H" if an unrecoverable error occurs, or if attempted to write to the write protect media.

MC (Media Changed):

Indicates that the state changes in the remove/insert type media. Fixed to 0 in TC6374AF, since no relevant changes defined in ATA/ATAPI-5 standard occur in operation.

IDNF (ID Not Found):

Set to “H” if no ID section is found for the sector requested.

MCR (Media Change Requested):

Indicates that, in the remove/insert type media, the release latch is pressed. Fixed to L in TC6374AF, since no relevant changes defined in ATA/ATAPI-5 standard occurs in operation.

ABRT (Aborted Command):

Indicates that a requested command is aborted.

NM (No Media):

Set to H if no media is inserted. Fixed to L in TC6374AF, since no relevant changes defined in ATA/ATAPI-5 standard occurs in operation.

AMNF (Address Mark Not Found):

Indicates no data address mask is found after ID section is normally detected.

Diagnostic Codes (Please refer to the EXECUTE DEVICE DIAGNOSTIC command for details.)

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error

7-5-3-3. Features Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
	Features byte							
Read/Write	W							

This register allows ATA command to have a special purpose, and is used to enable/disable the host interface function. **For the detailed operation of this register, refer to the SETFEATURES command in the outline description of ATA command, as well as ATA/ATAPI-5 standard.**

7-5-3-4. Sector Count Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
	Sector Count							
Initial Value	0	0	0	0	0	0	0	1
Read/Write	R/W							

A register used to write the sector count of data transfer-requested regarding ATA read/write operations between the host and TC6374AF. If this register is set to 0h (All “0”), sector count specifies 256. If, at the end of ATA command, this register is set to 0h, ATA command is normally completed. If normally completed, this register is set to the sector count, which must be transferred to complete the host request (specifying the count of remaining sectors to be transferred). Immediately after Power-on Reset, this register is set to “00h”. It is set to “01h” after TC6374AF’s initialization is completed. **For the detailed operation of this register, refer to the outline description of ATA command as well as ATA/ATAPI-5 standard.**

7-5-3-5. Sector Number Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
	Sector Number (CHS Addressing)							
	Logical Block Number bits A07~A00 (LBA Addressing)							
Initial Value	0	0	0	0	0	0	0	1
Read/Write	R/W							

This register is used to write the start sector number used by the host in the CHS mode. At the end of ATA command, the host can read from this register the last sector number. If LBA mode is selected, the host specifies Logical Block Number bits A07 - A00. At the end of ATA command, the host can read from this register the Logical Block Number. After Power-on Reset, this register is set to “00h”. It is set to “01h” after TC6374AF’s initialization is completed. **For the detailed operation of this register, refer to the outline description of ATA command as well as ATA/ATAPI-5 standard.**

7-5-3-6. Cylinder Low Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
	Cylinder Number Low byte (CHS Addressing)							
	Logical Block Number bits A15~A08 (LBA Addressing)							
Initial Value	0	0	0	0	0	0	0	0
Read/Write	R/W							

This register is used to write the lower bytes of start cylinder number used by the host in the CHS mode. At the end of ATA command, the host can read from this register the lower bytes of last cylinder number. If LBA mode is selected, the host specifies Logical Block Number bits A15 - A08. After ATA command completed, the host can read from this register the Logical Block Number. **For detailed operation of this register, refer to the outline description of ATA commands as well as ATA/ATAPI-5 standard.**

7-5-3-7. Cylinder High Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
	Cylinder Number High byte (CHS Addressing)							
	Logical Block Number bits A23~A16 (LBA Addressing)							
Initial Value	0	0	0	0	0	0	0	0
Read/Write	R/W							

This register is used to write the upper bytes of start cylinder number used by the host in the CHS mode. After ATA command is completed, the host can read from this register the upper bytes of last cylinder number. If LBA mode is selected, the host specifies Logical Block Number bits A23 - A16. If ATA command is completed, the host can read from this register the Logical Block Number. **For detailed operations of this register, refer to the outline description of ATA commands as well as ATA/ATAPI-5 standard.**

7-5-3-8. Device/Head Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
	1	LBA (0)	1	DEV	HS3	HS2	HS1	HS0
		LBA (1)			LBA27	LBA26	LBA25	LBA24
Initial Value	1	0	1	0	0	0	0	0
Read/Write	R/W							

This register is used to specify a drive out of a pair of drives that shares a set of registers. **For detailed operation of each bit, refer to the outline description of ATA commands as well as ATA/ATAPI-5 standard.**

LBA (Logical Block Address):

This bit is used to select either CHS mode or LBA mode.

"0" : CHS Addressing mode "1" : LBA Addressing mode

DEV (Device Address):

This bit is used to write the drive number selected by host.

"0" : drive 0 (card 0) "1" : drive 1 (card 1)

This bit affects ATA Device Address Register: nDS1 and nDS0.

HS3 - HS0:

Indicates, in the CHS Addressing mode, the head number: bits 3~0.

LBA27 - LBA24:

Indicates, in the LBA Addressing mode, Logical Block Number: bits 27~24.

(Reference Information)

LBA <-> CHSConversion Formula

CHS -> LBAConversion Formula LBA = (C x HpC + H) x SpH + S + 1

LBA -> CHSConversion Formula C = LBA / (HpC x SpH)

H = (LBA / SpH) mod HpC

S = (LBA mod SpH) + 1

C: Cylinder number

HpC: Head count per cylinder

H: Head count

SpH: Sector number per track

S: Sector number

7-5-3-9. Alternate Status Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
Initial Value	0	0	0	0	0	0	0	0
Read/Write	R							

A register used to report, according to the read instruction by the host, TC6374AF state. Reading out this register will not clear the interrupt (#IREQ). **For detailed operation of each bit, refer to the outline description ATA commands as well as ATA/ATAPI-5 standard.**

BSY (Busy) :

Indicates the TC6374AF busy state. Set always to H if ATA Command Registers accessed.

DRDY (Device Ready) :

Indicates that, when the bit is set to “H”, TC6374AF can responds to ATA command. If an error is present, this bit is latched and not changed until the host reads this register. If read again, this bit indicates the current TC6374AF state. At the power-on, this bit is cleared to “L”, and keeps it until being ready for the reception of ATA command.

DF (Device Fault):

Indicates the current device fault state. Fixed to **”L”.**

DSC (Device Seek Complete):

Indicates that the head is positioned on the track. TC6374AF, though, has no heads, then it is normally set to **”H”.** Set to “L” in the initial setup mode.

DRQ (Data Request):

Indicates that data transfer is ready in a unit of word or byte between the host and TC6374AF.

CORR (Corrected Data):

Fixed to **”L”. In ATA/ATAPI-5 standard, this bit is defined as no longer used.**

IDX (Index):

Fixed to **”L”. In ATA/ATAPI-5 standard, this bit is defined as no longer used.**

ERR (Error):

Indicates, while the previous ATA command is executed, an error occurs. ATA Error Register specifies the information related with error cause.

7-5-3-10. Status Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
Initial Value	0	0	0	0	0	0	0	0
Read/Write	R							

A register used to report, according to the read instruction from the host, the TC6374AF state. If this register is read, the interrupt (#IREQ) is cleared. For detailed information, refer to ATA Alternate Status Register. **For detailed operation of this register, refer to the outline description of ATA command as well as ATA/ATAPI-5 standard.**

7-5-3-11. Device Control Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	-	-	1	SRST	nIEN	0
Read/Write	W							

This register is used to control TC6374AF interrupt request and instruct to TC6374AF the ATA Software Reset. **For detailed operation of each bit, refer to the outline description of ATA commands as well as ATA/ATAPI-5 standard.**

SRST (Software Reset):

ATA Software Reset bit. With this bit set to “1”, reset state is stored. If this bit is cleared to “0”, reset is cleared. If SD Memory Card is used, the bit is changed from ”1” to ”0”, CMD0 is issued two times to initialize the media.

nIEN (Interrupt Enable):

This bit can be ignored while TC6374AF is set with Memory Mapped I/O. Whenever this bit is set to “1”, TC6374AF’s interrupt is prohibited.

7-5-3-12. Device Address Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
	—	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0
Initial Value	—	1	1	1	1	1	1	0
Read/Write	R							

This register is used to keep the compatibility with ATA disk drive interface. **For detailed operation of each bit, refer to the outline description of ATA command as well as ATA/ATAPI-5 standard.**

nWTG (Write Gate):

Cleared to L whenever write operation is in progress, or set to H when not. If the bit is cleared to “L”, the host must not change the voltage applied to TC6374AF.

nHS3~nHS0:

A head select bit, which is an inverted signal of ATA Device/Head Register: D3 - D0 bits “HS3 - HS0”.

nDS1:

Drive ”1” select bit. Set to 0 if Device/Head Register: DEV bit is set to ”1”.

nDS0:

Drive ”0” select bit. Set to 0 if Device/Head Register: DEV bit is set to ”0”.

7-5-3-13. Command Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
	Command							
Read/Write	W							

If a command is written to this register, the drive number in Socket and Copy Register and DRV bit in Device/Head Register are compared: only if matched, the command starts to run. **For detailed operation of this register, refer to the outline description of ATA commands as well as ATA/ATAPI-5 standard.**

7-5-3-14. Duplicate Even Data Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
	Duplicate Even Data							
Initial Value	Unidentified							
Read/Write	R/W							

This register is the same as the ATA Data Register.

7-5-3-15. Duplicate Odd Data Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
	Duplicate Odd Data							
Initial Value	Unidentified							
Read/Write	R/W							

Accessing from low ranks (D7~D0) or high ranks (D15~D8), this register can be accessed only data of odd addresses.

7-5-3-16. Duplicate Features Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
	Duplicate Features byte							
Read/Write	W							

This register is the same as the ATA Feature Register.

7-5-3-17. Duplicate Error Register

Address	D7	D6	D5	D4	D3	D2	D1	D0
	BBK	UNC	MC	IDNF	MCR	ABRT	TKNOF	AMNF
Initial Value	0	0	0	0	0	0	0	1
Read/Write	R							

This register is the same as the ATA Error Register.

8. ATA COMMAND

8-1. ATA COMMAND BLOCK

ATA Command Block is a generic name of seven registers used to transmit command using the ATA Command protocol. By interpreting the register value, address specify mode is determined which is used to specify the address of media connected with TC6374AF. CHS Addressing mode and LBA Addressing mode are supported.

Bit	7	6	5	4	3	2	1	0
Features	Features Register							
Sector Count	Sector Count Register							
Sector Number	Sector Number Register							
Cylinder Low	Cylinder Low Register							
Cylinder High	Cylinder High Register							
Device/Head	Device Register				Head Register			
Command	Command Register							

8-2. Operation of ATA COMMAND BLOCK REGISTER

A command is issued to TC6374AF, after necessary parameters are written to the relevant registered within Command Block, then the command code is written to the Command register. Reception of command has three classes (ND = Non Data Command, PI = PIO Data-In Command, PO = PIO Data-out Command). To receive all commands, BSY = ”0 “(“L” : negate) must be applicable in principle.

If commands for ND and PI are accepted, TC6374AF sets BSY to H within 400 ns.

By accepting PO command, TC6374AF sets BSY to H within 400 ns, sets up the sector buffer for the write operation, sets DRQ to H within 700 μs (For WRITE MULTIPLE command, sets DRQ to H within 20 ms), then clears BSY to L within 400ns after DRQ is set to “H”.

Note: If set to the power-down mode(If oscillation module or oscillator with oscillation control function are used, the state automatically moves to the self-powerdown mode, i.e. a powerdown mode, when no access occurs from host within 5ms. For detailed operation of the power-down mode, refer to the description below), oscillation module or oscillator with oscillation control function connected with TC6374AF stops its operation, then DRQ can not be set to “H” within700 μs.

Note: For PO, DRQ is so fast set to “H”, then BSY signal transition to BSY may take too short time for the host to recognize BSY = ”H”.

Note: If, when TC6374AF is still processing a command (Old Command), another command is issued, the TC6374AF will not respond to the new command.

8-3. ATA COMMAND CODE and PARAMETERS

8-3-1. STANDARD ATA COMMAND

proto	Command	typ	Command Code	Parameters Used				
				FR	SC	SN	CY	DH
ND	CHECK POWER MODE	M	98h, E5h		y			D
DD	EXECUTE DEVICE DIAGNOSTIC	M	90h		y	y	y	y
ND	FLUSH CASHE	M	E7h					D
ND	GET MEDIA STATUS	O	Dah					D
PI	IDENTIFY DEVICE	M	Ech					D
ND	IDLE	M	97h, E3h		y			D
ND	IDLE IMMEDIATE	M	95h, E1h					D
ND	INITIALIZE DEVICE PARAMETERS	M	91h		y			y
PI	READ BUFFER	O	E4h					D
PI	READ MULTIPLE	M	C4h		y	y	y	y
PI	READ SECTOR (S)	M	20h, 21h		y	y	y	y
ND	READ VERIFY SECTOR (S)	M	40h, 41h		y	y	y	y
ND	RECALIBRATE	O	1xh		y	y	y	y
ND	SEEK	M	70h			y	y	y
ND	SET FEATURE	M	EFh	y	y	y	y	y
ND	SET MULTIPLE MODE	M	C6h		y			D
ND	SLEEP	M	99h, E6h					D
ND	STANDBY	M	96h, E2h		y			D
ND	STANDBY IMMEDIATE	M	94h, E0h					D
PO	WRITE BUFFER	O	E8h					D
PO	WRITE MULTIPLE	M	C5h		y	y	y	y
PO	WRITE SECTOR (S)	M	30h, 31h		y	y	y	y

Note: The command codes, marked with a waved underline, are defined as “retired” or “obsolete” in ATA/ATAPI-5 standard, though, to maintain the compatibility with the past technologies, TC6374AF will support these. TC6374AF supports no DMA mode, i.e. not supporting READ DMA command and WRITE DMA command.

8-3-2. VENDOR UNIQUE COMMAND

proto	Command	typ	Command Code	Parameters Used				
				FR	SC	SN	CY	DH
ND	CHECK SD EXTENSION	V	D1h		y	y	y	y
ND	SD HEADER	V	D2h	y	y	y	y	y
ND PI PO	SD EXECUTE	V	D3h	y	y	y	y	y
PI	RETRIEVE RESPONSE	V	D4h		y			y
ND	SD DATA OUT	V	D5h					D
PI	READ MEDIA UNIQUE ID	V	F7h					D
PO	UPDATE FIRMWARE	V	Feh					D
PI	READ FIRMWARE	V	F6h					D
ND	VENDOR TEST ENABLE	V	F1h		y	y	y	
ND	SmartMedia™ BLOCK ERASE	V	F8h		y		y	
PI	SmartMedia™ READ	V	F9h		y	y	y	
PO	SmartMedia™ WRITE	V	F0h		y	y	y	

proto = command protocol, ND = Non-data command, DD = EXECUTE DEVICE DIAGNOSTIC, PO = PIO data-out command,

PI = PIO data-in command, typ = Command type, O = Optional, M = Mandatory, V = Vendor specific Implementation,

FR = Feature register(see command descriptions for use), SC = Sector Count register, SN = Sector Number register,

CY = Cylinder register, DH = Device/Head register,

y = the register contains a valid parameter for this command. For the Device/Head register, y means both the device and head parameters are used.

D = only the device parameter is valid and not the head parameter.

d = the device parameter is valid. The usage of the head parameter vendor specific.

8-4. Error indication report of ATA COMMAND

Command Name	Error Register					Status Register
	UNC(WP)	IDNF	ABRT	TKON	AMNF	ERR
CHECK POWER MODE			V			V
EXECUTE DEVICE DIAGNOSTIC				V	V *2	
FLUSH CASHE			V			V
GET MEDIA STATUS			V			V
IDENTIFY DEVICE			V			V
IDLE			V			V
IDLE IMMEDIATE			V			V
INITIALIZE DEVICE PARAMETERS			V			V
READ BUFFER			V			V
READ MULTIPLE	V	V	V			V
READ SECTOR (S)	V	V	V			V
READ VERIFY SECTOR (S)	V	V	V			V
RECALIBRATE			V			V
SEEK		V	V			V
SET FEATURE			V			V
SET MULTIPLE MODE			V			V
SLEEP			V			V
STANDBY			V			V
STANDBY IMMEDIATE			V			V
WRITE BUFFER			V			V
WRITE MULTIPLE	V	V	V			V
WRITE SECTOR (S)	V	V	V			V
CHECK SD EXTENSION			V			V
SD HEADER			V			V
SD EXECUTE	V		V			V
RETRIEVE RESPONSE			V			V
SD DATA OUT	V		V			V
READ MEDIA UNIQUE ID		V	V			V
UPDATE FIRMWARE			V			V
READ FIRMWARE			V			V
VENDOR TEST ENABLE			V			V
SmartMedia™ BLOCK ERASE		V	V			V
SmartMedia™ READ		V	V			V
SmartMedia™ WRITE		V	V			V

V = Varies with Executing this Command. *1 = Please refer to the command explanation. *2 = Only “0” is effective.(Negative logic)

8-5. General description of ATA COMMAND

8-5-1. STANDARD ATA COMMAND

8-5-1-1. CHECK POWER MODE - 98h, E5h

This command is used to check the current power mode in TC6374AF. If, when this command is issued, the oscillation module is operating, TC6374AF sets BSY and Sector Count Register to ”FFh”. Then, BSY is cleared and generates an interrupt. If the oscillation modules is in the oscillation stop state or the oscillation stop timer is set, TC6374AF sets BSY and sets Sector Count Register to”00h”. Then, it clears BSY and generates an interrupt.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Command	98h or E5h							

Note: Command code ”98h” is defined in ATA/ATAPI-5 standard as “Retired”, though, to maintain the compatibility with previous specifications, TC6374AF will still support it.

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	Result Value(00h or FFh)							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Sector Count Register = ”00h”

(if oscillation module is in the oscillation stop mode or ioscillation stop timer is set)

Sector Count Register = ”FFh”

(if oscillation module is under operation)

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	(0)	(0)	(0)	(0)	ABRT(1)	(0)	(0)
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

Error Register: ABRT = ”1” (Aborted Command)

8-5-1-2. EXECUTE DEVICE DAIGNOSTIC - 90h

In TC6374AF, this command only judges whether reset processing was performed normally.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device / Head	(1)	N/A	(1)	DEV	N/A			
Command	90h							

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	Diagnostic Code (01h)							
Sector Count	Signature (01h)							
Sector Number	Signature (01h)							
Cylinder Low	Signature (00h)							
Cylinder High	Signature (00h)							
Device / Head	Signature (00h)							
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Error Register = ”01h”(Reset processing normal end)

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	Diagnostic Code (02h)							
Sector Count	Signature (01h)							
Sector Number	Signature (01h)							
Cylinder Low	Signature (00h)							
Cylinder High	Signature (00h)							
Device / Head	Signature (00h)							
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Error Register = ”02h”(Reset processing abnormal end, un-initializing of media, or initialization is impossible.)

8-5-1-3. FLUSH CASHE - E7h

This command is used to write the write cache data internal the TC6374AF to the media. It, however, operates the register only because TC6374AF has no built-in write cache.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Command	E7h							

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Error Outputs

If, the data in the write cache is written to the media, an uncorrectable error occurs, the first sector address, in which the error occurs, is notified from Sector Number, Cylinder Low, Cylinder High register. **TC6374AF has no such errors based on the specification.**

Bit	7	6	5	4	3	2	1	0
Error	(0)	(0)	(0)	(0)	(0)	ABRT(1)	(0)	(0)
Sector Count	N/A							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

Error Register : ABRT = ”1” (Aborted Command)

8-5-1-4. GET MEDIA STATUS - DAh

This command is prepared in order to check the state of media.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Command	DAh							

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	WP	(0)	(0)	(0)	ABRT	(0)	(0)
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

Error Register: WP = “1” (Write Protected Media)

Reports status of Write protect switch and Write protect seal.

“Permanent write protection” and ”Temporary write protection” will also be reported when SD memory card or MultiMediaCard is inserted.

ABRT = ”1” (Aborted Command)

8-5-1-5. IDENTIFY DEVICE - ECh

This command allows the host to receive from TC6374AF the parameter information (IDENTIFY DEVICE INFORMATION) as shown in the next page. By issuing this command, TC6374AF sets BSY and enters the parameter information requested to the sector buffer to set DRQ, then generates an interrupt. Thus, the host can parameter information from the sector buffer.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Command	ECh							

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	(0)	(0)	(0)	(0)	ABRT(1)	(0)	(0)
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

Error Register : ABRT = ”1” (Aborted Command)

IDENTIFY DEVICE INFORMATION

This is default data while using SD card of 32MB. Note: Marked * of Word Address means to depend on Media Capacity.

Word Address	Default Value of Data	Number of Bytes	Information of Data
0	848Ah	2	Bit Information of General Configration
* 1	01DBh	2	Number of Cylinders
2	0000h	2	Reserve
* 3	0004h	2	Head Numbers
4	4000h	2	Unformatted byte numbers per track
5	0200h	2	Unformatted byte numbers per sector
* 6	0020h	2	Sector Numbers per track
7	0000h	2	Vender Unique
8	0000h	2	Vender Unique
9	0000h	2	Vender Unique
10- 19	0000h	20	Serial Number
20	0001h	2	Buffer Type
21	0001h	2	Buffer Size of 512Byte unit
22	0004h	2	ECC byte numbers pass through Read/Write Long Command (Default Value)
23- 26	aaa--aa	8	Firmware numbers (Ver.1.1) [5665,722E,312E,3120 h]
27- 46	aaa--aa	8	Model Number (Products Version Information of Attribute memory) [2020,2020,2020,2020,2020,2020,2020,2020,2020,2020, 2020,2020,2020,2020,2020,2020,2020,2020,2020,2020 h]
47	0001h	40	Maximum transferred Sector Numbers per Read/Write Multiple command interruption=1
48	0000h	2	No Double Word (32bit) Support
49	0200h	2	LBA Support, No DMA Transfer capacity
50	0000h	2	Reserve
51	0200h	2	PIO Data Transfer Timing
52	0000h	2	DMA Data Transfer Timing
53	0001h	2	Validity of registered area by Conversion Mode
* 54	01DBh	2	Current Cylinder Numbers (*1)
* 55	0004h	2	Current Head Numbers (*2)
* 56	0020h	2	Current Sector Numbers (*3) per track
* 57- 58	0000ED80h	4	Current Sector Capacity = (*1) x (*2) x (*3)
59	0000h	2	No Option Set about Multiple Sector Transfer
* 60- 61	0000ED80h	4	Sector Capacity in LBA Mode
62	0000h	2	No Single Word DMA Data Transfer Support
63	0000h	2	No Multiple DMA Data Transfer Support
64-127	0000h	128	Reserve
128-159	0000h	64	Vender Unique
160-175	0000h	16	Reserve
176	000Dh	2	SDA Command Mode Bit3:D5h Support Bit2:512 byte Fixed Transfer Bit0:Secure Command Support Others: Reserve
177	0009h	2	For D3h, Transfer byte numbers (2^9=512) in Current Multiple Transfer
178	0009h	2	For D3h, Transfer byte numbers (2^9=512) in Minimum Multiple Transfer
179	0009h	2	For D3h, Transfer byte numbers (2^9=512) in Maximum Multiple Transfer
180	0009h	2	For D3h, Transfer byte numbers (2^9=512) in Maximum Single Transfer
160-255	0000h	192	Reserve

Note: IDENTIFY DEVICE INFORMATION is stored in the NOR flash memory used for TC6374AF firmware. As the aforementioned data is used for the reference data (DEFAULT IDENTIFY DEVICE INFORMATION), it may be modified if so requested. Modification data must be submitted on a 256 word basis. DEFAULT IDENTIFY DEVICE INFORMATION will not assure the precise operation.

8-5-1-6. IDLE - 97h, E3h

If this command is issued, TC6374AF sets BSY and moves to the Idle mode. Then, it clears BSY and generates an interrupt, which is generated even if TC6374AF is not completely moved to the Idle mode. With Sector Count Register set to any values other than “00h”, the auto-power-down sequence is permitted and a countdown immediately starts. After the time set in the Sector Count Register elapses, the oscillation stops. During the power-down, the state allows for accepting commands. If Sector Count Register is set to “00h”, the auto-power-down sequence is prohibited.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	Timer period value (5 ms × Timer period value)							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Command	97h or E3h							

Sector Count Register = setting of auto-power-down sequence
“00h”: auto-power-down sequence prohibited
“Other than 00h”: auto-power-down permitted

Note: Command code ”97h” is defined in ATA/ATAPI-5 standard as “Retired”, though, to maintain the compatibility with the previous specification, TC6374AF still supports it.

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	(0)	(0)	(0)	(0)	ABRT(1)	(0)	(0)
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

Error Register: ABRT = ”1” (Aborted Command)

8-5-1-7. IDLE IMMEDIATE - 95h, E1h

This command performs a NOP operation in TC6374AF. Even during the power-down in this state, command can be accepted.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Command	95h or E1h							

Note: Command code ”95h” is defined in ATA/ATAPI-5 standard as “Retired”, though, to maintain the compatibility with the previous specification, TC6374AF still supports it.

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	(0)	(0)	(0)	(0)	ABRT(1)	(0)	(0)
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

Error Register: ABRT = ”1” (Aborted Command)

8-5-1-8. INITIALIZE DEVICE PARAMETERS - 91h

The host allows the host to specify the number of sectors per track and the number of heads per cylinder. If this command is issued, TC6374AF sets BSY then parameters. Then, BSY is cleared and an interrupt is generated. The validity in sector and head values is not verified in this command. When, if they were disabled, other command may generate an invalid access to notify the error.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	Logical sector per logical track							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	Max head			
Command	91h							

Sector Count Register = The number of sectors per track

Head Register = The number of heads per cylinder -1

Note: TC6374AF automatically caluculates and sets the Number of Cylinders from the Number of Heads and Sectors per Track set by this command. Number of Cylinders comes from Maximum sector number devided by Number of heads and Sectors per track. Since the Number of Cylinder is an integer value, the residue will be truncated. TC6374AF CAN'T ACCESS (READ/ WRITE) THESE TRUNCATED AREA WITH CTHE CHS ADDRESSING MODE.

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	(0)	(0)	(0)	(0)	ABRT(1)	(0)	(0)
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

Error Register : ABRT = ”1” (Aborted Command)

8-5-1-9. READ BUFFER - E4h

The host uses this command to read the current value in TC6374AF sector buffer. With this command issued, TC6374AF sets BSY and sets up the sector buffer for the read operation. Then, it sets DRQ, clears BSY, and generates an interrupt. The host then reads from the sector buffer the latest 512 byte data stored immediately before.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Command	E4h							

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	(0)	(0)	(0)	(0)	ABRT(1)	(0)	(0)
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

Error Register : ABRT = ”1” (Aborted Command)

8-5-1-10. READ MULTIPLE - C4h

Since this command is the same operation as "READ SECTOR (S)", refer to "READ SECTOR (S)" for it.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	Sector count							
Sector Number	Sector number (LBA7 - LBA0)							
Cylinder Low	Cylinder low (LBA15 - LBA8)							
Cylinder High	Cylinder high (LBA23 - LBA16)							
Device/Head	(1)	LBA	(1)	DEV	Head number (LBA27 - LBA24)			
Command	C4h							

Sector Count Register = Read sector number

Sector Number, Cylinder, Head Register = start sector address

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	“00h”							
Sector Number	Sector number (LBA7 - LBA0)							
Cylinder Low	Cylinder low (LBA15 - LBA8)							
Cylinder High	Cylinder high (LBA23 - LBA16)							
Device/Head	(1)	N/A	(1)	DEV	Head number (LBA27 - LBA24)			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Sector Count Register = ”00h”

Sector Number, Cylinder, Head Register = last read sector address

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	UNC	(0)	IDNF	(0)	ABRT	(0)	(0)
Sector Count	NA							
Sector Number	Sector number (LBA7 - LBA0)							
Cylinder Low	Cylinder low (LBA15 - LBA8)							
Cylinder High	Cylinder high (LBA23 - LBA16)							
Device/Head	(1)	N/A	(1)	DEV	Head number (LBA27 - LBA24)			
Status	BSY(0)	DRDY	DF(0)	DSC(1)	DRQ	CORR(0)	IDX(0)	ERR(1)

DRDY =" 0"

Status Register = "11h"

Error Register = "04h" (Aborted Command)

Multiple prohibition

Status Register = "51h"

Error Register = "04h" (Aborted Command)

Address over

Status Register = "59h" ("51h" after an end 512 byte data transfer)

Error Register = "10h" (ID Not Found)

Sector Count Register = The rest of transfer sector number

Sector Number, Cylinder, Head Register = Sector address of address over

Uncorrectable data

Status Register = "59h" ("51h" after an end 512 byte data transfer)

Error Register = "40h" (Uncorrectable Data Error)

Sector Count Register =The rest of transfer sector number

Sector Number, Cylinder, Head Register =Sector address of uncorrectable data

8-5-1-11. READ SECTOR (S) - 20h, 21h

This command allows the host to read 1-256 sectors specified in the TC6374AF Sector Count Register. Sector count 0 indicates the transfer request of 256 sectors. The transfer starts from the sector specified by Sector Number. Whether or not an error is present, before the data transfer, DRQ is always set. After this command is completed, task file is set to cylinder, head and sector numbers, which are lastly read. If an error occurs, the read operation stops at the sector where the error is generated. The task file is set to cylinder, head and sector numbers, where the error occurs. Data, in which an error occurs, remains in the sector buffer.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	Sector count							
Sector Number	Sector number (LBA7 - LBA0)							
Cylinder Low	Cylinder low (LBA15 - LBA8)							
Cylinder High	Cylinder high (LBA23 - LBA16)							
Device/Head	(1)	LBA	(1)	DEV	Head number (LBA27 - LBA24)			
Command	20h or 21h							

Sector Count Register = number of sectors to be read (“00h”: 256 sectors)

Sector Number, Cylinder, Head Register = start sector address

Note : Command code ”21h” is defined in ATA/ATAPI-5 standard as “Obsolete”, however, to maintain the compatibility with the previous specifications, TC6374AF supports it.

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	“00h”							
Sector Number	Sector number (LBA7 - LBA0)							
Cylinder Low	Cylinder low (LBA15 - LBA8)							
Cylinder High	Cylinder high (LBA23 - LBA16)							
Device/Head	(1)	N/A	(1)	DEV	Head number (LBA27 - LBA24)			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Sector Count Register = ”00h”

Sector Number, Cylinder, Head Register = last read sector address

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	UNC	(0)	IDNF	(0)	ABRT	(0)	(0)
Sector Count	NA							
Sector Number	Sector number (LBA7 - LBA0)							
Cylinder Low	Cylinder low (LBA15 - LBA8)							
Cylinder High	Cylinder high (LBA23 - LBA16)							
Device/Head	(1)	N/A	(1)	DEV	Head number (LBA27 - LBA24)			
Status	BSY(0)	DRDY	DF(0)	DSC(1)	DRQ	CORR(0)	IDX(0)	ERR(1)

DRDY = 0

Status Register = ”11h”

Error Register = ”04h” (Aborted Command)

Address over

Status Register = ”59h” (”51h” after an end 512 byte data transfer)

Error Register = ”10h” (ID Not Found)

Sector Count Register = The rest of transfer sector number

Sector Number, Cylinder, Head Register =Secter address of address over

Uncorrectable data

Status Register = ”59h” (”51h” after an end 512 byte data transfer)

Error Register = ”40h” (Uncorrectable Data Error)

Sector Count Register =The rest of transfer sector number

Sector Number, Cylinder, Head Register = Sector address of uncorrectable data

8-5-1-12. READ VERIFY SECTOER (S) - 40h, 41h

This command operates likely with READ SECTOR(S) command except that DRQ is not set and data is not transferred to the host. If the sector requested is verified, TC6374AF sets BSY and generates an interrupt. With this command completed, task file is set to the cylinder and sector numbers lastly verified. If an error occurs, the verify stops at the sector where the error occurs. The task file is set to the cylinder and sector numbers where the error occurs. Sector Count Register is set to the number of sectors that remains still unverified.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7 - LBA0)							
Cylinder Low	Cylinder Low (LBA15 - LBA8)							
Cylinder High	Cylinder High (LBA23 - LBA16)							
Device/Head	(1)	LBA	(1)	DEV	Head Number (LBA27 - LBA24)			
Command	40h or 41h							

Sector Count Register = Number of sectors to be verified (“00h”: 256 sectors)

Sector Number, Cylinder, Head Register = start sector address

Note : Command code ”41h” is defined in ATA/ATAPI-5 standard as “Obsolete”, though, to maintain the compatibility with previous specifications, TC6374AF still supports it.

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	“00h”							
Sector Number	Sector number (LBA7 - LBA0)							
Cylinder Low	Cylinder low (LBA15 - LBA8)							
Cylinder High	Cylinder high (LBA23 - LBA16)							
Device/Head	(1)	N/A	(1)	DEV	Head number (LBA27 - LBA24)			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Sector Count Register = ”00h”

Sector Number, Cylinder, Head Register = last verify sector address

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	UNC	(0)	IDNF	(0)	ABRT	(0)	(0)
Sector Count	NA							
Sector Number	Sector number (LBA7 - LBA0)							
Cylinder Low	Cylinder low (LBA15 - LBA8)							
Cylinder High	Cylinder high (LBA23 - LBA16)							
Device/Head	(1)	N/A	(1)	DEV	Head number (LBA27 - LBA24)			
Status	BSY(0)	DRDY	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

DRDY = " 0"

Status Register = "11h"

Error Register = "04h" (Aborted Command)

Address over

Status Register = "51h"

Error Register = "10h" (ID Not Found)

Sector Count Register =No verify sector number

Sector Number, Cylinder, Head Register =Sector address of address over

Uncorrectable data

Status Register = "51h"

Error Register = "40h" (Uncorrectable Data Error)

Sector Count Register =No verify sector number

Sector Number, Cylinder, Head Register =Sector address of uncorrectable data

8-5-1-13. RECALIBRATE - 1xh

This command is used originally to move the head to the cylinder ”00h”, though, in TC6374AF, only the interface timing operation is performed. If this command is issued, TC6374AF sets BSY, then, after waiting for the appropriate time, updates the status, clears BSY and generates an interrupt. TC6374AF, after this command is normally completed, initializes the Command Block register.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	LBA	(1)	DEV	N/A			
Command	1xh							

Note: Command code ”1xh” is defined in ATA/ATAPI-5 standard as “Retired” or “Obsolete”, though, to maintain the compatibility with previous specifications, TC6374AF still supports it.

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	“01h”							
Sector Number	“00h” or “01h”							
Cylinder Low	“00h”							
Cylinder High	“00h”							
Device/Head	(1)	N/A	(1)	DEV	“0h”			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

CHS Addressing Mode

Sector Count Register = “01h”
Sector Number Register = “01h”
Cylinder Register = “0000h”
Head Register = “0h”

LBA Addressing Mode

Sector Count Register = “01h”
Sector Number Register = “00h”
Cylinder Register = “0000h”
Head Register = “0h”

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	(0)	(0)	(0)	(0)	ABRT(1)	(0)	(0)
Sector Count	NA							
Sector Number	NA							
Cylinder Low	NA							
Cylinder High	NA							
Device/Head	(1)	N/A	(1)	DEV	NA			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

Error Register = ”04h” (Aborted Command)

8-5-1-14. SEEK - 70h

This command is used to seek the track and select the head, both or which are specified by the task file. TC6374AF actually operates the interface timing and register. To issue this command, the media connected with TC6374AF are not required to format. TC6374AF sets DSC.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	Sector number (LBA7 - LBA0)							
Cylinder Low	Cylinder low (LBA15 - LBA8)							
Cylinder High	Cylinder high (LBA23 - LBA16)							
Device/Head	(1)	LBA	(1)	DEV	Head number (LBA27 - LBA24)			
Command	70h							

Sector Number, Cylinder, Head Register = Seek sector address

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	(0)	(0)	IDNF	(0)	ABRT	(0)	(0)
Sector Count	NA							
Sector Number	NA							
Cylinder Low	NA							
Cylinder High	NA							
Device/Head	(1)	N/A	(1)	DEV	NA			
Status	BSY(0)	DRDY	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

DRDY = ”0”

Status Register = ”11h”

Error Register = ”04h” (Aborted Command)

Address over

Status Register = ”51h”

Error Register = ”10h” (ID Not Found)

Sector Number, Cylinder, Head Register =Sector address of address over

8-5-1-15. SET FEATURES - EFh

This command allows the host originally to modify the operation of function owned by TC6374AF, though, in TC6374AF, NOP is performed even if parameters shown below other than Subcommand codes ”95h” and ”ECh” are set.

Inputs

The case of Subcommand Code is other than ”ECh”

Bit	7	6	5	4	3	2	1	0
Features	Subcommand code							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Command	EFh							

The case of Subcommand Code is ”ECh”

Bit	7	6	5	4	3	2	1	0
Features	Subcommand code (“ECh”)							
Sector Count	Subcommand specific (“FFh”)							
Sector Number	Subcommand specific (“FFh”)							
Cylinder Low	Subcommand specific (“FFh”)							
Cylinder High	Subcommand specific (“FFh”)							
Device/Head	(1)	N/A	(1)	DEV	“Fh”			
Command	EFh							

SET FEATURES register definitions

Subcommand code Value	Operation	TC6374AF internal operation
01h	Enable 8-bit PIO transfer mode	D5”IOis8”bit of FCR Card Configuration & Status Register is affected. IOis8 = “1”
55h	Disable read look-ahead feature	NOP
66h	Disable reverting to power on default	NOP
81h	Disable 8-bit PIO transfer mode	D5”IOis8”bit of FCR Card Configuration & Status Register is affected. IOis8 = “0”
95h	Enable media status notification	Please refer the Normal Outputs description.
9Ah	Obsolete.	NOP
BBh	Obsolete	NOP
CCh	Enable reverting to power on default	NOP
ECh	Get media information	Please refer the Normal Outputs description.

In power injection or after hardware reset, it’s set as “81h”.

Normal Outputs

The case of Subcommand Code is ”95h”, other than ”ECh”

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

The case of Subcommand Code is ”95h”

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	VER(“00h”)							
Cylinder High	(0)	(0)	(0)	(0)	(0)	PEJ(0)	LOCK(0)	PENA
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

PENA = “1” (When this command is already received)

PENA = “0” (When this command is received for the first time)

The case of Subcommand Code is ”ECh”

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	“5Dh”							
Sector Number	“53h”							
Cylinder Low	“43h”							
Cylinder High	“50h”							
Device/Head	“xBh”							
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

If register’s return value takes the above state, TC6374AF stores in the read write buffer 10 byte information (Media Information). With READ BUFFER command, the following information can be read out.

Media Information

Byte	Media Information
Byte 0	A type of media (0 : SmartMedia™, 1 : SD Memory Card, 2 : MultiMediaCard
Byte 1	SD Memory Card, MultiMediaCard : Write block length & Read block length, SmartMedia™ : Sector counts/block
Byte 2	SD Memory Card, MultiMediaCard : C_SIZE (7 - 0), SmartMedia™ : Dummy data
Byte 3	SD Memory Card, MultiMediaCard : C_SIZE (11 - 8), SmartMedia™ : Dummy data
Byte 4	SD Memory Card, MultiMediaCard : C_SIZE_MULTI, SmartMedia™ : Dummy data
Byte 5	SD Memory Card, MultiMediaCard : ERASE_BLOCK_LEN & SECTOR_SIZE, SmartMedia™ : Dummy data
Byte 6	SD Memory Card : SIZE_OF_PROTECTED_AREA (7 - 0), MultiMediaCard, SmartMedia™ : Dummy data
Byte 7	SD Memory Card : SIZE_OF_PROTECTED_AREA (15 - 8), MultiMediaCard, SmartMedia™ : Dummy data
Byte 8	SD Memory Card : SIZE_OF_PROTECTED_AREA (23 - 16), MultiMediaCard, SmartMedia™ : Dummy data
Byte 9	SD Memory Card : SIZE_OF_PROTECTED_AREA (31 - 24), MultiMediaCard, SmartMedia™ : Dummy data

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	(0)	(0)	(0)	(0)	ABRT(1)	(0)	(0)
Sector Count	NA							
Sector Number	NA							
Cylinder Low	NA							
Cylinder High	NA							
Device/Head	(1)	N/A	(1)	DEV	NA			
Status	BSY(0)	DRDY	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

DRDY = “0”

Status Register = ”11h”

Error Register = ”04h” (Aborted Command)

Not supporting parameter

Status Register = ”51h”

Error Register = ”04h” (Aborted Command)

8-5-1-16. SET MULTIPLE MODE - C6h

This command is used originally to allow TC6374AF to execute READ MULTIPLE and WRITE MULTIPLE operations. Sector Count Register is allowed to set “00h” and “01h”. In TC6374AF, this command is also issued to execute READ MULTIPLE and WRITE MULTIPLE commands.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	Sectors per block (“00h” or “01h”)							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Command	C6h							

Sector Count Register = The number of sector per block

“00h” = Multiple command prohibited

“01h” = Multiple command permitted

Other than “00h”, “01h” = Multiple command prohibited

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	(0)	(0)	(0)	(0)	ABRT(1)	(0)	(0)
Sector Count	NA							
Sector Number	NA							
Cylinder Low	NA							
Cylinder High	NA							
Device/Head	(1)	N/A	(1)	DEV	NA			
Status	BSY(0)	DRDY	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

DRDY =" 0"

Status Register = "11h"

Error Register = "04h" (Aborted Command)

Not supporting block size (Sector Count Register = Other than "00h", "01h")

Status Register = "51h"

Error Register = "04h" (Aborted Command)

8-5-1-17. SLEEP - 99h, E6h

This command is used to move TC6374AF to the Sleep mode. By executing a hardware reset or software reset or accepting ATA command, TC6374AF returns from the Sleep mode. In Sleep mode, ATA Status Register: D6 bit “DRDY” is set to ”H”(Ready). If, in Sleep mode, ATA command is issued, it recovers and processes the command. If this command is issued, TC6374AF moves immediately to the power-down mode. Oscillation module then stops.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Command	99h or E6h							

Note: Command code ”99h” is defined in ATA/ATAPI-5 standard as “Retired”, though, to maintain the compatibility with previous specifications, TC6374AF will still support it.

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	(0)	(0)	(0)	(0)	ABRT(1)	(0)	(0)
Sector Count	NA							
Sector Number	NA							
Cylinder Low	NA							
Cylinder High	NA							
Device/Head	(1)	N/A	(1)	DEV	NA			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

Error Register : ABRT = ”1” (Aborted Command)

8-5-1-18. STANDBY - 96h, E2h

This command allows TC6374AF to set BSY and move the state to the Standby mode. Then, it clears BSY and generates an interrupt. Interrupt is generated even if TC6374AF is not completely moved to the Standby mode. Whichever value the Sector Count Register is set to, TC6374AF immediately moves to the power-down mode and the oscillation module stops. If, when Sector Count Register is set to “00h”, it accepts a command after it is once turned off, then it will no more move to the power-down mode. If, when Sector Count Register is set to other than “00h”, it accepts a command after it is once turned off, then the countdown starts soon after the command is completed with auto-power-down sequence being permitted. When the time specified in Sector Count Register elapses, the oscillation stops. During the power-down, the state can accepts ATA command.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	Time period value (5 ms × Timer Count)							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Command	96h or E2h							

Sector Count Register = setting of auto-power-down sequence

“00h” : auto-power-down sequence prohibited

Other than “00h” : auto-power-down permitted

Note: Command code ”96h” is defined in ATA/ATAPI-5 standard as “Retired”, though, to maintain the compatibility with previous specifications, TC6374AF supports it.

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	(0)	(0)	(0)	(0)	ABRT(1)	(0)	(0)
Sector Count	NA							
Sector Number	NA							
Cylinder Low	NA							
Cylinder High	NA							
Device/Head	(1)	N/A	(1)	DEV	NA			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

Error Register : ABRT = ”1” (Aborted Command)

8-5-1-19. STANDBY IMMEDIATE - 94h, E0h

This command is used to cause TC6374AF to set BSY and enter the Standby mode. Then, it clears BSY and generates an interrupt. The interrupt is generated even if TC6374AF is not completely enter the Standby mode. TC6374AF moves, immediately after this command is issued, to the power-down mode. The oscillation will stop. If, once the power-down is performed, the command is accepted, then auto-powerdown sequence starts based on the value of Sector Count Register set by STANDBY and IDLE commands. Even during the power-down operation, the state can accept ATA command.

Input

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Command	94h or E0h							

Note: Command code ”96h” is defined in ATA/ATAPI-5 standard as “Retired”, though, to maintain the compatibility with previous specifications, TC6374AF supports it.

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	(0)	(0)	(0)	(0)	ABRT(1)	(0)	(0)
Sector Count	NA							
Sector Number	NA							
Cylinder Low	NA							
Cylinder High	NA							
Device/Head	(1)	N/A	(1)	DEV	NA			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

Error Register : ABRT = ”1” (Aborted Command)

8-5-1-20. WRITE BUFFER - E8h

This command allows the host to replace TC6374AF data buffer value with data pattern you want. Buffer area allows 512 byte address access, which is same with the read buffer area.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Command	E8h							

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	(0)	(0)	(0)	(0)	ABRT(1)	(0)	(0)
Sector Count	NA							
Sector Number	NA							
Cylinder Low	NA							
Cylinder High	NA							
Device/Head	(1)	N/A	(1)	DEV	NA			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

Error Register : ABRT = ”1” (Aborted Command)

8-5-1-21. WRITE MULTIPLE - C5h

Since this command is the same operation as "WRITE SECTOR (S)", refer to "WRITE SECTOR (S)" for it.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	Sector count							
Sector Number	Sector number (LBA7 - LBA0)							
Cylinder Low	Cylinder low (LBA15 - LBA8)							
Cylinder High	Cylinder high (LBA23 - LBA16)							
Device/Head	(1)	LBA	(1)	DEV	Head number (LBA27 - LBA24)			
Command	C5h							

Sector Count Register = written sector number

Sector Number, Cylinder, Head Register = sector address

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	“00h”							
Sector Number	Sector number (LBA7 - LBA0)							
Cylinder Low	Cylinder low (LBA15 - LBA8)							
Cylinder High	Cylinder high (LBA23 - LBA16)							
Device/Head	(1)	N/A	(1)	DEV	Head number (LBA27 - LBA24)			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Sector Count Register = ”00h”

Sector Number, Cylinder, Head Register = last write sector address

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	WP	(0)	IDNF	(0)	ABRT	(0)	(0)
Sector Count	Sector count							
Sector Number	Sector number (LBA7 - LBA0)							
Cylinder Low	Cylinder low (LBA15 - LBA8)							
Cylinder High	Cylinder high (LBA23 - LBA16)							
Device/Head	(1)	N/A	(1)	DEV	Head number (LBA27 - LBA24)			
Status	BSY(0)	DRDY	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

DRDY =" 0"

Status Register = "11h"
Error Register = "04h" (Aborted Command)

Multiple prohibition

Status Register = "51h"
Error Register = "04h" (Aborted Command)

Address over

Status Register = "51h"
Error Register = "10h" (ID Not Found)
Sector Count Register = The rest of transfer sector number
Sector Number, Cylinder, Head Register =Sector address of address over

No empty block

Status Register = "51h"
Error Register = "04h" (Aborted Command)
Sector Count Register =The rest of transfer sector number
Sector Number, Cylinder, Head Register = Miswritten sector address

Write Protected Media (SD Memory Card/MultiMediaCardCSD is generated to Permanent write Protection, Temporary Write Protection by Media write protect switch and seal.)

Status Register = "51h"
Error Register = "40h" (Write Protected Media)
Sector Count Register = The rest of transfer sector number
Sector Number, Cylinder, Head Register =Miswritten sector address

8-5-1-22. WRITE SECTOR (S) - 30h or 31h

This command allows host to write data to the media. Set sector count (”00h” stands for 256 sector.) to sector count register and begin writing head sector address set to register. After completing this command, the last sector address remains in the register. If error has been occurred when writing multiple sectors, the writing operation will be stopped and the sector address remains in the register.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	Sector count							
Sector Number	Sector number (LBA7 – LBA0)							
Cylinder Low	Cylinder low (LBA15 - LBA8)							
Cylinder High	Cylinder high (LBA23 - LBA16)							
Device / Head	(1)	LBA	(1)	DEV	Head number (LBA27 - LBA24)			
Command	30h or 31h							

Sector Count Register = Sector numbers to be written (“00h”= 256 sectors)

Sector Number, Cylinder, Head Register = Sector address

Note: Command code ”31h” is defined in ATA/ATAPI-5 standard as “Obsolete”, though, to maintain the compatibility with previous specifications, TC6374AF still supports it.

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	“00h”							
Sector Number	Sector number (LBA7 - LBA0)							
Cylinder Low	Cylinder low (LBA15 - LBA8)							
Cylinder High	Cylinder high (LBA23 - LBA16)							
Device / Head	(1)	N/A	(1)	DEV	Head number (LBA27 - LBA24)			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Sector Count Register =” 00h”

Sector Number, Cylinder, Head Register = Most recent write sector address

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	WP	(0)	IDNF	(0)	ABRT	(0)	(0)
Sector Count	Sector count							
Sector Number	Sector number (LBA7 - LBA0)							
Cylinder Low	Cylinder low (LBA15 - LBA8)							
Cylinder High	Cylinder high (LBA23 - LBA16)							
Device / Head	(1)	N/A	(1)	DEV	Head number (LBA27 - LBA24)			
Status	BSY(0)	DRDY	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

DRDY = 0

Status Register = ”11h”
Error Register = ”04h” (Aborted Command)

Address over

Status Register = ”51h”
Error Register = ”10h” (ID Not Found)
Sector Count Register = The rest of transfer sector number
Sector Number, Cylinder, Head Register = Sector address of address over

No empty block

Status Register = ”51h”
Error Register = ”04h” (Aborted Command)
Sector Count Register = The rest of transfer sector number
Sector Number, Cylinder, Head Register = Miswritten sector address

Write Protected Media (SD Memory Card/MultiMediaCardCSD is generated to Permanent write Protection, Temporary Write Protection by Media write protect switch and seal.)

Status Register = ”51h”
Error Register = ”40h” (Write Protected Media)
Sector Count Register = The rest of transfer sector number
Sector Number, Cylinder, Head Register =Miswritten sector address

8-5-2. VENDOR UNIQUE ATA COMMAND

8-5-2-1. CHECK SD EXTENSION – D1h

This command is used to check if ATA command for SD memory card (ATA SD extension set) is supported or not.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	N/A							ENB
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device / Head	(1)	N/A	(1)	DEV	N/A			
Command	D1h							

ENB = Provided to check Media Card Pass Through Command is supported or not. And, allow / prohibit the Media Card Pass Through Command after this command is issued.
"1" = Allow Media Card Pass Through Command. (D2h-D4h command)
"0" = Prohibit Media Card Pass Through Command. (D2h-D4h command)

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	55h							
Sector Number	AAh							
Cylinder Low	RCA Bit 7 - 0							
Cylinder High	RCA Bit 15 - 8							
Device / Head	(1)	N/A	(1)	DEV	WP	Media type		
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Sector Count Register = Signature (“55h”)

Sector Number Register = Signature (“AAh”)

Cylinder Low Register = RCA: Reports RCA lower byte (Bit7 - 0) which is to be uset for SD command argument.

Cylinder High Register = RCA: Reports RCA upper byte (Bit15 - 8) which is to be used for SD command argument.

Head Register = WP: Reports write protect status set by media’s write protect switch. When using SD Memory Card / MultiMediaCard, reports Permanent Write Protection status and Temporary Write Protection status by CSD.

“1” = Write Protected Media

“0” = No Write Protected Media

Media Type: Reports kind of media.

“001b” = SD Memory Card

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	(0)	(0)	(0)	(0)	ABRT(1)	(0)	(0)
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device / Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

When SmartMedia™ or MultiMediaCard is inserted

Status Register = “51h”

Error Register = ”04h” (Aborted Command)

Notes:

#1. After this command is issued, SD Memory Card goes to transfer mode/ 4-bit bus width/ optimizedclock (MAX.16MHz) state.

#2. Be sure to check Standard ATA Command is completed before issuing this command.

#3. Be sure to issue this command and check “Dxh” Vendor Unique Command is available or not before issuing “Dxh” Vendor Unique Command.

#4. “Dxh” Vendor Unique Command can’t be issued if SD IO Card or locked SD Memory Card is inserted because ATA Status Register’s DRDY ”D6” bit does not turn ”H”. Standard ATA Command can’t be issued either.

8-5-2-2. SD HEADER – D2h

This command transfers Header portion of SD command to TC6374AF. After this command is issued, the host must issue SD EXECUTE command.

Inputs

Bit	7	6	5	4	3	2	1	0
Features	SD Command Argument 4 (Bit 15 - 8)							
Sector Count	SD Command Argument 3 (Bit 23 - 16)							
Sector Number	SD Command Argument 2 (Bit 31 - 24)							
Cylinder Low	SD Command Argument 1 (Bit 39 - 32)							
Cylinder High	(0)	ACMD	SD Command Index (Bit 45 - 40)					
Device / Head	(1)	N/A	(1)	DEV	Response Type			
Command	D2h							

Features, Sector Count, Sector Number, Cylinder Low Register, Cylinder High Register
= Set SD command's Bit 8 – 45.

Cylinder High Register = ACMD: Specify the command in the SD Command Index is CMD or ACMD.
0: CMD (The controller issuees command in the SD Command Index.)
1: ACMD (The controller issues CMD55 before issuing the command in the SD Command Index.)

Head Register = Set Response Type as followings.
"0011b" : No Response
"0100b": R1, R6 (,R4, R5)
"0101b" : R1b
"0110b" : R2
"0111b" : R3
"0000b" - "0010b", "1000b" - "1111b" : Reserved
(Above Reserved codes are not supported by TC6374AF.)

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	NA							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device / Head	(1)	N/A	(1)	DEV	Response Type			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Head Register = Report input value as the Response Type.

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	(0)	(0)	(0)	(0)	ABRT(1)	(0)	(0)
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device / Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

When Reserved code is issued

Status Register = “51h”

Error Register = ”04h” (Aborted Command)

When D1h command ENB bit = ”0”

Status Register = “51h”

Error Register = ”04h” (Aborted Command)

Note:

#1. This command can be issued to any media because the command does not make an access to media. Therefore, before issuing this command, issue ”D1h” command and check SD Memory Card is sure to be inserted.

#2. Don’t change the SD Memory Card frequency when issuing ”Dxh” command. Don’t issue ”Dxh” commands which needs low frequency. (Only CMD0 on the protocol.)

#3. This controller sets the connected SD Memory Card bus width to as broad as possible. Don’t issue Change bus width command in ”Dxh” command.

#4. Don’t issue Change RCA commands in “Dxh” command.

#5. Don’t set CMD0, CMD2, ACMD6, ACMD41 to the SD Command Index.

#6. After issuing Standard ATA Command, SD Memory Card goes to Transfer mode. Therefore, Be careful when issuing ”Dxh” Vendor Unique Command after issuing Standard ATA Command.

#7. Don’t activate Permanent Write Protection and Temporary Write Protection on CSD by “Dxh” command.

8-5-2-3. SD EXECUTE – D3h

Input

Bit	7	6	5	4	3	2	1	0
Features	Subcommand Code (N/A)							
Sector Count	Data Transfer Length (LSB)							
Sector Number	Data Transfer Length (Middle Byte)							
Cylinder Low	Data Transfer Length (MSB)							
Cylinder High	CRC (N/A)							(0)
Device / Head	(1)	N/A	(1)	DEV	DATA	BLKH	(0)	DIR
Command	D3h							

Features Register = Set Subcommand code.

(See the table below. **TC6374AF does not recognize these codes.**)

Sector Count, Sector Number, Cylinder Low Register = Set Data transfer Length.

(**Since the maximum block number of multiple block is 256 blocks, Cylinder Low Register's Bit7 – 2 are invalid.**

Since the maximum length of the Single block is 512 bytes, Sector Number Register's Bit7 – 2 and Cylinder Low's all bits are invalid.

Available value of the Data Transfer Length is power of 2 (2^n; $1 \leq n \leq 9$; n=integer). i.e. 2, 4, 8, 16, 32, 64, 128, 256, 512 bytes.

Data transfer is done by word length, so, Sector Count Register's Bit0 is invalid.)

Cylinder High Register = Set CRC.

(**TC6374AF does not recognize this code.**)

Head Register = Specify with/ no data to DATA.

"0": No data transfer

"1": With data transfer

Specify single/ multiple sector to BLKH.

"0": Single sector transfer

"1": Multiple sector transfer

Specify data direction to DIR.

"0": Read from SD Memory Card

"1": Write to SD Memory Card

Subcommand Code

Subcommand	Protocol	Data	Direction
D0h	Non-data command	0	0 or 1
D1h	PIO data-in command	1	0
D2h	PIO data-out command	1	1
00h – CFh, D3h - FFh	Reserved	-	-

TC6374AF does not use above Subcommand Codes. TC6374AF will neglect above codes.

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	Response bit 15 – 8							
Sector Number	Response bit 23 – 16							
Cylinder Low	Response bit 31 – 24							
Cylinder High	Response bit 39 – 32							
Device / Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(0)

Sector Count, Sector number, Cylinder Register = Report Response bit 8 – 39 (Response data for SD command).

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	UNC	(0)	(0)	(0)	ABRT	(0)	(0)
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device / Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

When SmartMedia™ or MultiMediaCard is inserted

Status Register = “51h”

Error Register = ”04h” (Aborted Command)

Time out error

(250ms write timeout error)

Status Register = ”51h”

Error Register = ”04h” (Aborted Command)

CRC error

(response CRC error, 128 clock no response error, 250ms read timeout error, data CRC error, write CRC error)

Status Register = ”51h”

Error Register = ”40h” (Uncorrectable Data Error)

When D1h command’s ENB bit = ”0”

Status Register = “51h”

Error Register = ”04h” (Aborted Command)

Note: Both 250ms write timeout error and 250ms read timeout error doesn’t have any relation with SD Memory Card/ MultiMediaCard clock frequency. Timeout time is fixed to 250ms.

Note:

#1. Aborted Command error will be occurred when SD Memory Card is not inserted. DRQ bit will not goes to "H" even if it is during read request.

#2. After this command has been issued, Standard ATA Command will initialize the media state (will not issue CMD0) and goes to transfer mode/ 4-bit bus width/ optimized clock frequency (Max.16MHz).

#3. When you want to continue to issue "Dxh" command during/ after "Dxh" Vendor Unique Command, Don't execute ATA Soft Reset. TC6374AF automatically issues CMD00 when executing ATA Soft Reset.

#4. Though this command is a READ command, DRQ bit will not be set when response CRC error or no response error. This command is a special command.

#5. This command doesn't retry issuing CMD0 or ACMD0 when error has been occurred in SD Memory Card CMD or ACMD. Therefore, the host must retry issuing CMD or ACMD. The only exeption is a "D2h" command (ACMD-bit = "1") CMD13. TC6374AF automatically processes the routine in this command.

#6. When ACMD is issued in "D2h" command (ACMD-bit = "1"), TC6374AF automatically issue CMD55 before issuing ACMD. On CMD55 has automatically issued, error process is as followings. For all errors, the return value of the ATA error register is "40h" when "D3h" command has been finished. (Host can't recognize whether the error has been occurred in CMD55 or in ACMD). When the host retries issuing ACMD by "D2h" command (ACMD-bit = "1") TC6374AF restart command routine from issuing CMD55.

#6-1. When Card Status Error (any of ILLEGAL_COMMAND = "1", CC_ERROR = "1", ERROR = "1", APP_CMD = "0") occurred in CMD55:

The command will immediately abort without executing CMD55 or ACMD.

#6-2. When Response CRC error or No response error occurred in CMD55:

Continuously issue CMD13 and wait until it goes back to Transfer mode. If it recognizes the first command as ACMD13, thus it will go back to the state before CMD55. And furthermore, the error occurs in CMD13 is as follows.

#6-2-1. When the Card status error occurred in CMD13:

Immediately abort.

#6-2-2. When Response CRC error or No response error has been occurred in CMD13:

Retries 10 times and abort if in vain.

#6-2-3. When TC6374AF will not go back to transfer mode even if it issues CMD13:

Abort if it won't go back to tranfer mode even if it retries more than 400msec.

8-5-2-4. RETRIEVE RESPONSE – D4h

This command get SD command response data which issued in advance. Response data will reported by data register as following Retrieve Response Data Format.

Input

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	Response Length							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device / Head	(1)	N/A	(1)	DEV	N/A			
Command	D4h							

Sector Count Register = Set response data length (unit: byte) of the last issued SD command in Response Length.

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	Response Data transferred in bytes							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device / Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY (0)	DRDY (1)	DF (0)	DSC (1)	DRQ (0)	CORR (0)	IDX (0)	ERR (0)

Sector Count Register = Transferred data size (unit: byte) will be reported in “Response Data transferred in bytes”.

Retrieve Response Data Format

Word	48-bit Response	136-bit Response	
0	Response bit 0-15	Response bit 0-15	
1	Response bit 16-31	Response bit 16-31	
2	Response bit 32-47	Response bit 32-47	
3	Reserved (00)	Response bit 48-63	
4	Reserved (00)	Response bit 64-79	
5	Reserved (00)	Response bit 80-95	
6	Reserved (00)	Response bit 96-111	
7	Reserved (00)	Response bit 112-127	
8	Reserved (00)	00000000	Response bit 128-135
9-255	Reserved (00)	Reserved (00)	

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	(0)	(0)	(0)	(0)	ABRT(1)	(0)	(0)
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device / Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

When SmartMedia™ or MultiMediaCard is inserted

Status Register = ”51h”

Error Register = ”04h” (Aborted Command)

When the ENB bit of the D1h command = “0”

Status Register = “51h”

Error Register = ”04h” (Aborted Command)

Note: TC6384 never reports “Aborted Command Error” when SD Memory Card is inserted and ENB bit of D1h command=”1”. TC6384AF always transfers register content to buffer in this condition.

8-5-2-5. SD DATA OUT – D5h

Note: This command is deleted from Firmware Revision 2.19.

This command transfers TC6374AF read write buffer data to SD Memory Card. Used for data transfer less than or equal to 512-bytes

Input

Bit	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device / Head	(1)	N/A	(1)	DEV	N/A			
Command	D5h							

Normal Outputs

Bit	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device / Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY (0)	DRDY (1)	DF (0)	DSC (1)	DRQ (0)	CORR (0)	IDX (0)	ERR (0)

Error Outputs

Bit	7	6	5	4	3	2	1	0
Error	(0)	UNC	(0)	(0)	(0)	ABRT	(0)	(0)
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device / Head	(1)	N/A	(1)	DEV	N/A			
Status	BSY(0)	DRDY(1)	DF(0)	DSC(1)	DRQ(0)	CORR(0)	IDX(0)	ERR(1)

When SmartMedia™ or MultiMediaCard inserted

Status Register = ”51h”
Error Register = ”04h” (Aborted Command)

Time out error (50ms write time out error)

Status Register = ”51h”
Error Register = ”04h” (Aborted Command)

CRC error

Status Register = ”51h”
Error Register = ”40h” (Uncorrectable Data Error)

8-5-2-6. READ MEDIA UNIQUE ID – F7h

This command is used to read the unique ID in the removable media connected with TC6374AF. For detailed operation, refer to the attached document (TC6374AF VENDOR UNIQUE COMMAND MANUAL). SmartMedia™ ID requires the prior Nondisclosure Agreement with SmartMedia™ maker.

8-5-2-7. UPDATE FIRMWARE - FEh

This command is used to update TC6374AF firmware. For detailed operation, refer to the attached document (TC6374AF VENDOR UNIQUE COMMAND MANUAL).

8-5-2-8. READ FIRMWARE – F6h

This command is used to read TC6374AF firmware. For detailed operation, refer to the attached document (TC6374AF VENDOR UNIQUE COMMAND MANUAL).

8-5-2-9. VENDOR TEST ENABLE – F1h

This command is used to enable Vendor Unique Test command. For detailed operation, refer to the attached document (TC6374AF VENDOR UNIQUE COMMAND MANUAL).

8-5-2-10. SmartMedia™ BLOCK ERASE – F0h

This command is used to delete the data specified with SmartMedia™ physical block address. For detailed operation, refer to the attached document (TC6374AF VENDOR UNIQUE COMMAND MANUAL).

8-5-2-11. SmartMedia™ READ – F8h

This command is used to read the data specified with SmartMedia™ physical address. For detailed operation, refer to the attached document (TC6374AF VENDOR UNIQUE COMMAND MANUAL).

8-5-2-12. SmartMedia™ WRITE – F9h

This command is used to write the data specified with SmartMedia™ physical address. For detailed operation, refer to the attached document (TC6374AF VENDOR UNIQUE COMMAND MANUAL).

9. Reset operation

TC6374AF prepares four types of resets as described below.

9-1. Hardware rest by #PONRST terminal

- TC6374AF performs a series of initialization processes to set initial values in ATA Command Block Register.
- After reset being cleared, the host interface returns to Memory Mapped mode.
- Default values in ATA Command Block Register are listed below:
  - Error Register: “01h”, Cylinder Low Register: “00h”, Features Register: “81h”, Cylinder High Register: “00h”, Sector Count Register: “01h”, Device/Head Register: “A0h”, Sector Number Register: “01h”, FCR Configuration Option Register SRESET”D7” bit : “0”

9-2. Hardware reset by RESET terminal

- TC6374AF performs a series of initialization processes to set ATA Command Block Register to the initial values.
- After reset being cleared, the host interface returns to Memory Mapped mode.
- Default values in ATA Command Block Register are same with those for the hardware rest by #PONRST terminal.

9-3. Software reset by FCR Configuration Option Register:SRESET “D7” bit

- TC6374AF performs a series of initialization processes to set ATA Command Block Register to the initial values.
- After reset being cleared, the host interface returns to Memory Mapped mode.
- Default values in ATA Command Block Register are same with those for the hardware rest by #PONRST terminal.
- This reset will not affect SRESET bit, thus set SRESET = ”0” to clear the reset.

9-4. Software reset by ATA Device Control Register:SRST “D2” bit

- TC6374AF resets the host interface circuit.
- This reset will not affect SRESET bit, thus set SRST= ”0” to clear the reset.
- Whatever the Set Features command state is, all parameters before reset are saved. ATA Command Block Register except for Features Register, though, is initialized.
- ATA software reset function only is provided, but PC Card interface is not reset. Even if the reset process is performed at the completion of every command run, no parameters are cleared. Then, access may be performed without additional operations.

Note: When SD Memory Card is used, CMD0 is issued two times to initialize the media for all reset operations described above.

10. Control of low power consumption

TC6374AF prepares two modes of power supply: i.e. normal mode (oscillation state) and power-down mode (oscillation stop state). In addition, two modes of power-down operation are prepared: i.e. self-powerdown mode automatically performed by TC6374AF, and auto-powerdown mode performed by the power control using ATA commands(e.g. IDLE command). Both power-down modes assume the use of either oscillation module or oscillator with oscillation control function. In the self-powerdown mode, if no access from host for longer than about 5ms will automatically stop the oscillation by TC6374AF, entering the power-down mode. In the auto-power-down mode, the state moves to the powerdown mode depending on the then register value when ATA commands related with power control are issued. In the power-down mode, auto-power-down mode has a priority. For the auto-power-down operation, refer to the outline description of ATA commands.

11. NOR flash memory

TC6374AF connects with NOR flash memory, which contains:

- TC6374AF firmware
- 256 byte Card Information Structure
- 256 word Identify Device Information

For NOR flash memory allowed to connect with TC6374AF, refer to ”TC6374AF reference design description (reference circuit diagram and information sheet)”. As the information is updated as necessary, keep the latest one by inquiry. For the AC/DC characteristics, refer the description that follows.

Rewriting and confirming data in NOR flash memory connected with TC6374AF are supported by Vendor Unique Commands. For detailed information, refer to TC6374AF VENDOR UNIQUE COMMAND MANUAL.

12. Removable media memory capacity

12-1. SmartMedia™

TC6374AF can be set as capacity as shown in the following table then used to SmartMedia™.

Drive Capacity	SmartMedia™ Capacity	Number of Cylinders	Number of Heads	Sectors per Track	Number of Sectors
1 Mbytes	8 Mbits	125	4	4	2,000
2 Mbytes	16 Mbits	125	4	8	4,000
4 Mbytes	32 Mbits	250	4	8	8,000
8 Mbytes	64 Mbits	250	4	16	16,000
16 Mbytes	128 Mbits	500	4	16	32,000
32 Mbytes	256 Mbits	500	8	16	64,000
64 Mbytes	512 Mbits	500	8	32	128,000
128 Mbytes	1 Gbit	500	16	32	256,000

Moreover, refer to the SmartMedia™ logical format specification.

12-2. SD Memory Card/ MultiMediaCard

TC6374AF can be set as capacity as shown in the following table then used to SD Memory Card/ MultiMediaCard.

Drive Capacity	Memory Capacity (Max. LBA)	Number of Cylinders (Max.)	Number of Heads	Sectors per Track	Number of Sectors (Max.)
～ 8Mbytes	～ 4000h = ～16,384	512	4	8	16,384
～ 16 Mbytes	～ 8000h = ～32,768	512	2	32	32,768
～ 32Mbytes	～ 10000h = ～ 65,536	512	4	32	65,536
～ 128 Mbytes	～ 40000h = ～ 262,144	1,024	8	32	262,144
～ 4Gbytes	～ 800000h = ～ 8,388,608	16,384	16	32	8,388,608

"Number of Heads" and "Sectors per Track" are fixed value. "Number of Cylinders" and "Number of Sectors" are reference data (not a fixed value). "Number of Cylinders" is a value which "memory capacity" (caluculated from media CSD) divided by "Number of Heads" and "Sectors per Track". Residue will be truncated. "Number of Sectors" never goes over "memory capacity". If the residue is not zero, the truncated sectors cannot be accessed (read/ write) by CHS addressing mode.

Refer also to the specification of media logic format.

13. Recognizing the removable media

13-1. SmartMedia™

TC6374AF recognizes the capacity of SmartMedia™ connected using SmartMedia™ Device ID. To check that physical format is performed after the normal Device ID is read from SmartMedia™, the heading 10 bytes of "CIS/Identify Device Information Area", a valid heading block of SmartMedia™, is compared. If Device ID not supported or illegal data from heading 10 bytes are found, they are prohibited to use(BSY state). In such case where the use prohibited (BSY state) occurs, format physically the SmartMedia™ using Vendor Unique ATA Command.

SmartMedia™ recognizeable Device ID is following.

SmartMedia™	Device ID
1 Mbytes	"6Eh" "E8h" "ECh"
2 Mbytes	"EAh"
4 Mbytes	"E3h" "E5h"
8 Mbytes	"E6h"
16 Mbytes	"73h"
32 Mbytes	"75h"
64 Mbytes	"76h"
128 Mbytes	"79h"

Mask ROM type SmartMedia™	Device ID
4 Mbytes	"D5h"
8 Mbytes	"D6h"
16 Mbytes	"57h"
32 Mbytes	"58h"
64 Mbytes	"D9h"
128 Mbytes	"DAh"

Note: TC6374AF first accesses SmartMedia™ at the timing 1024μs after #PONRST terminal and RESET terminal clears the reset, and #CD terminal detects the media. Thus, during this interval, perform the SmartMedia™ powering and stabilizing the terminal contact.

Note that TC6374AF only supports 3.3V SmartMedia™. 5V SmartMedia™ is not supported. For SmartMedia™ allowed to connect with TC6374AF, refer to "TC6374AF reference design description (reference circuit diagram and information sheet)". As the information is updated as necessary, keep the latest one by inquiry.

13-2. SD Memory Card/MultiMediaCard

- Media capacity

Memory capacity is recognized by calculating the media CSD value with the formula shown below:

Memory Capacity =((C_SIZE+1)*2^(C_SISE_MULT+2))*2^WRITE_BL_LEN

Refer to the specification of each media.

- CMD issued to media

TC6374AF issues following commands to the media by itself or from STANDARD ATA COMMAND.

CMD0
CMD2
CMD3
CMD7
CMD9
CMD10
CMD12
CMD13
CMD16
CMD17
CMD18
CMD24
CMD25
CMD55
ACMD6
ACMD 13
ACMD41
ACMD42
ACMD51

- Setting media bus width

When using SD Memory Card, if error occurs setting the media bus width to 4-bit by ACMD6, TC6374AF treat the media as non-useable card.

- Media block length

TC6374AF can handle following length of READ_BL_LEN, WRITE_BL_LEN.

Less than 512-bytes

: Can’t be used

512-bytes

: Can be used

More than 512-bytes

: Can be used only when Pertial read/ write is allowed. On SD Memory Card, can be used when [{WRITE_BL_LEN = 10 (1024Bytes) or 11 (2048Bytes)} and {WRITE_BL_PARTIAL = 0}]. MultiMediaCard can’t be used in above condition.

14. Others

TC6374AF is used to install the removal disk with the following characteristics. Note that values listed below are only for reference based on theoretical values or actual measurement.

14-1. System Performance

14-1-1. Toshiba 128MB SmartMedia™

- Media Transfer Rate
  - Read (Total Time to Read 4MB Data) 5s
  - Write (Total Time to Write 4MB Data) 7s
- Interface Transfer Rate
  - Read/Write (Max) 8.0 Mbytes/s (2byte/250ns)

14-1-2. Matsushita 64MB SD Memory Card

- Media Transfer Rate
  - Read (Total Time to Read 4MB Data) 4s
  - Write (Total Time to Write 4MB Data) 5s
- Interface Transfer Rate
  - Read/Write (Max) 8.0 Mbytes/s (2byte/250ns)

14-1-3. SanDisk 16MB MultiMediaCard

- Media Transfer Rate
  - Read (Total Time to Read 4MB Data) 7s
  - Write (Total Time to Write 4MB Data) 27s
- Interface Transfer Rate
  - Read/Write (Max) 8.0 Mbytes/s (2byte/250ns)

Note: Media Transfer Rate listed above are actual measurement results. Note that values may depend on individual media and environment (PC). If customers describe such kind of data on their catalogue, use those based on their own measurements.

14-2. The Calculation of Read and Write Performance

14-2-1. SmartMedia™

- Assumptions
  - SmartMedia™
    - Toshiba 64Mbyte
  - Read time per sector
    - Approx. 0.1ms
  - Write time per sector
    - Approx.0.3ms (for details, refer to “NAND type flash memory data sheet”)
  - Delete time per block (32 sectors)
    - Approx.3ms (for details, refer to “NAND type flash memory data sheet”)
  - Controller process time required for newly writing 1-32 sectors at the address hit
    - Approx. 2.1ms
  - Controller process time required for newly writing 1-32 sectors at the address mishit
    - Approx. 14.8ms
  - Controller process time required for overwriting 1-32 sectors at the address hit
    - Approx. 4.7ms
  - Controller process time required for overwriting 1-32 sectors at the address mishit
    - Approx. 17.4ms
  - Controller process time required for reading 1-32 sectors at the address hit
    - Approx. 0.2ms
  - Controller process time required for reading 1-32 sectors at the address mishit
    - Approx. 12.9ms

Note) This controller only one zone of flash memory for address conversion table used to convert from host’s logical address to the flash memory’s physical address. If host’s logical address is within the address conversion table (i.e. address hit), high-speed operation is available. If not found in the address conversion table (i.e. address mishit), address conversion table is reproduced followed by the subsequent processes, decreasing the performance.

- Read operation
  - Read speed is calculated by:

  read time per sector (0.1ms) x sector count + controller process time for reading one sector at address hit or address mishit x sector count + main unit’s transfer time

- Write operation
  - Write speed depends on the sector count, sector number (write start address), write method, then the speed can not be generally identified. Actual examples are described below.

- Example1)
  - Conditions
    - sector count : 32
    - write start address : block heading
    - write method: overwrite, at address hit
      - write speed

- delete time per block = 3ms
- write time per 32 sectors = 9.6ms (0.3ms x 32)
- controller's process time for writing 32 sectors = 4.7ms
- As a result, 3 + 9.6 + 4.7 = approx. 17.3ms + main unit's transfer time

- Example2)
  - Conditions
    - sector count : 32
    - write start address : block heading
    - write method: overwrite, at address mishit
      - write speed
        - delete time per block = 3ms
        - write time per 32 sectors = 9.6ms (0.3ms x 32)
        - controller's process time for writing 32 sectors = 17.4ms
        - As a result, 3 + 9.6 + 17.4 = approx. 30ms + main unit's transfer time

- Example3)
  - Conditions
    - sector count : 32
    - write start address : 2nd sector in block
    - write method : overwrite, at address hit
      - write speed
        - delete time per 2 blocks= 6ms (3ms x 2)
        - write time per 64 sectors= 19.2ms (0.3ms x 64)
        - controller's process time for writing 64 sectors= 9.4 ms (4.7ms x 2)
        - As a result, 6 + 19.2 + 9.4 = approx. 34.6ms + main unit's transfer time

- Example4)
  - Conditions
    - sector count : 32
    - write start address : 2nd sector in block
    - write method : overwrite, at address mishit
      - write speed
        - delete time per 2 blocks= 6ms (3ms x 2)
        - write time per 64 sectors= 19.2ms (0.3ms x 64)
        - controller's process time for writing 64 sectors= 34.8ms (17.4ms x 2)
        - As a result, 6 + 19.2 + 34.8 = approx. 60ms + main unit's transfer time

- Example5)
  - Conditions
    - sector count : 32
    - write start address : block heading
    - write method : new, at address hit
      - write speed

- write time per 32 sectors = 9.6ms (0.3ms x 32)
- controller's process time for writing 32 sectors = 2.1ms
- As a result, 9.6+2.1 = approx. 11.7ms + main unit's transfer time

- Example6)
  - Conditions
    - sector count : 32
    - write start address : block heading
    - write method : new, at address mishit
      - write speed
        - write time per 32 sectors = 9.6ms (0.3ms x 32)
        - controller's process time for writing 32 sectors = 14.8ms
        - As a result, 9.6+14.8 = approx. 24.4ms + main unit's transfer time

- Example7)
  - Conditions
    - sector count : 32
    - write start address : 2nd sector in block
    - write method : new, at address hit
      - write speed
        - write per 64 sectors = 19.2ms (0.3ms x 64)
        - controller's process time for writing 64 sectors = 4.2 ms (2.1ms x 2)
        - As a result, 19.2 + 4.2 = approx. 23.4ms + main unit's transfer time

- Example8)
  - Conditions
    - sector count : 32
    - write start address : 2nd sector in block
    - write method : new, at address mishit
      - write speed
        - write time per 64 sectors = 19.2ms (0.3ms x 64)
        - controller's process time for writing 64 sectors = 29.6ms (14.8ms x 2)
        - As a result, 19.2 + 29.6 = approx. 48.8ms + main unit's transfer time

- Example9)
  - Conditions
    - sector count : 1
    - write start address : block heading (same result, at the middle sector in a block)
    - write method : overwrite, at address hit
      - write speed
        - delete time per block = 3ms
          - write time per 32 sectors = 9.6ms (0.3ms x 32)
          - controller's process time for writing 32 sectors = 4.7ms
          - As a result, 3 + 9.6 + 4.7 = approx. 17.3ms + main unit's transfer time

- Example10)
  - Conditions
    - sector count : 1
    - write start address : block heading (same result, at the middle sector in a block)
    - write method : overwrite, at address mishit
      - write speed
        - delete time per block = 3ms
        - write time per 32 sectors = 9.6ms (0.3ms x 32)
        - controller's process time for writing 32 sectors = 17.4ms
        - As a result, 3 + 9.6 + 17.4 = approx. 30ms + main unit's transfer time

- Example11)
  - Conditions
    - sector count : 1
    - write start address : block heading(same result, at the middle sector in a block)
    - write method : new, at address hit
      - write speed
        - write time per 32 sectors = 9.6ms (0.3ms x 32)
        - controller's process time for writing 32 sectors = 2.1ms
        - As a result, 9.6+2.1 = approx. 11.7ms + main unit's transfer time

- Example12)
  - Conditions
    - sector count : 32
    - write start address : block heading (same result, at the middle sector in a block)
    - write method : new, at address mishit
      - write speed
        - write time per 32 sectors = 9.6ms (0.3ms x 32)
        - controller's process time for writing 32 sectors = 14.8ms
        - As a result, 9.6+14.8 = approx. 24.4ms + main unit's transfer time

The above values are derived using Toshiba SmartMedia™ with typical write/delete times. Use the maximum write/delete times of SmartMedia™ to derive actual values.

14-2-2. SD Memory Card

For the specification, refer to the specification of respective media.

14-2-3. MultiMediaCard

For the specification, refer to the specification of respective media.

14-3. Setup Time

14-3-1. Toshiba 128MB SmartMedia™

Power Down to Active (Typ.)	700μs
Power on to Ready (Typ.)	260ms
Change zone to zone (Typ.)	50 ms

14-3-2. Matsushita 64MB SD Memory Card

Power Down to Active (Typ.)	700μs
Power on to Ready (Typ.)	340ms

14-3-3. SanDisk 16MB MultiMediaCard

Power Down to Active (Typ.)	700μs
Power on to Ready (Typ.)	250ms

Note: Media Transfer Rate listed above are actual measurement results. Note that values may depend on individual media and environment (PC). If customers describe such kind of data on their catalogue, use those based on their own measurements.

14-4. PC Card ATA Power Consumption of TC6374AF

Reference value will be described in the “Information sheet”.

Note: The reference value of the power consumption varies by media, hardware or PC settings. Be sure to measure power consumption data by yourself.

14-5. MTBF

14-5-1. SmartMedia™

MTBF is calculated viewing not the physical aspect but logical aspect of the rewrite count limitation. thus using the formula below.

$$\text{MTBF} = \frac{\text{block count} \times \text{rewrite count} \times \text{rate of rewrite portion to the total capacity}}{\text{average sector count written per hour (1 sector} = \text{512 bytes)}}$$

Note: Rewrite portion to the total capacity is defined as the area, which is derived by excluding the portion of unrewritable area from the total area since program area has less possibility of rewriting if once written. In case, for example, where card capacity is 4 Mbytes and write accesses of 32 kbytes(64 sectors) per 5 minutes occur, and 30% of the total capacity is rewritten, MTBF is derived as follows:

MTBF = (512 x 1,000,000 x 0.3)/(64 x 12)
= 200,000 times

Even if write access increases up to five times, the device life time reaches 40,000 hours. If such MTBF is insufficient, the device lifetime may be prolonged by rewriting regularly the area, such as program area, in which rewriting occurs less frequently. With this way, “rate of rewrite portion to the total capacity” comes close to 100% in the above formula.

14-5-2. SD Memory Card/MultiMediaCard

For this specification, refer to the specification on respective media.

14-6. ECC

14-6-1. SmartMedia™

44 bits/Sector (error correction of 1 bit and error detection of 2 bits are available)

14-6-2. SD Memory Card/MultiMediaCard

ECC processes are performed by SD Memory Card/MultiMediaCard controller. For this specification, refer to the specification on respective media.

14-7. Reliability

14-7-1. SmartMedia™

$1/10^{15}$ bits Read

14-7-2. SD Memory Card/MultiMediaCard

For this specification, refer to the specification on respective media.

15. Absolute maximum ratings (V_{SS} = 0V)

Item	Symbol	Specification		Unit
		Min.	Max.	
Power supply voltage	V_{DD}	-0.3	+6.0	V
	$V_{DD3.3}$	-0.3	+4.5	
Input voltage	VIN_{VDD}	-0.3	V_{DD}+0.3	V
	$VIN_{VDD3.3}$	-0.3	$V_{DD3.3}$+0.3	
Output voltage	$VOUT_{VDD}$	-0.3	V_{DD}+0.3	V
	$VOUT_{VDD3.3}$	-0.3	$V_{DD3.3}$+0.3	
Input current	IIN	-10	+10	mA
Storage temperature	Tstg	-40	+125	°C

16. Standard operation condition (V_{SS} = 0V)

Item	Symbol	Specification		Unit
		Min.	Max.	
Power supply voltage	V_{DD}	4.5	5.5	V
	$V_{DD3.3}$	3.0	3.6	
Ambient tempareture	Ta	-25	+70	°C

17. DC electrical characteristic

Symbol	Item		Condition	Specification			Unit
				Min.	Typ.	Max.	
VIH	Level high input voltage						V
		LVTTL		2.0			
		LVTTL Schmitt trigger		2.0			
VIL	Level low input voltage						V
		LVTTL				0.8	
		LVTTL Schmitt trigger				0.8	
IIH	Level high input current (5V interface)		VINA = V_{DD}	-10		10	μA
		With pull-down resistor		10		200	
	Level high input current (3V interface)		VINB = $V_{DD3.3}$	-10		10	
		With pull-down resistor		10		200	
IIL	Level low input current (5V interface)		VINA = V_{SS}	-10		10	μA
		With pull-up resistor		-200		-10	
	Level low input current (3V interface)		VINB = V_{SS}	-10		10	
		With pull-up resistor		-200		-10	
VOH	Level high output voltage			2.4			V
	VOHB	B4	IOH=-4mA				
	VOHB	B8	IOH=-8mA				
	VOHA	B8IF	IOH=-8mA				
	VOHA/ VOHB		IOH = -1μA	V_{DD}-0.05			
VOL	Level low output voltage					0.4	V
	VOLB	B4	IOL=4mA				
	VOLB	B8	IOL=8mA				
	VOLA	B8IF	IOL=8mA				
	VOLA/ VOLB		IOL = 1μA	V_{SS}+0.05			
IOZ	Output leak current		VOUTA=V_{DD} or V_{SS}, VOUTB= $V_{DD3.3}$ or V_{SS}	-10		10	μA
VH	Hysteresis voltage						V
	LVTTL				0.4		
IDDS	Static current consumption		VINA=V_{DD} or V_{SS} , VINB= $V_{DD3.3}$ or V_{SS}			142	μA

18. AC characteristics

18-1. PC Card interface

18-1-1. Attribute memory and common memory write/read timing

Item	Symbol	Specification		Unit
		Min.	Max.	
Write Cycle Time	tcW	250		ns
Write Puls Width	tw(WE)	150		
Address Setup Time	tsu(A)	30		
Address Setup Time for #WE	tsu(A-WEH)	180		
Card Enable Setup Time for #WE	tsu(CE-WEH)	180		
Data Setup Time for #WE	tsu(D-WEH)	80		
Data Hold Time	th(D)	30		
Writre Recover Time	trec(WE)	30		
Output Disable Time from #WE	tdis(WE)		100	
Output Disable Time from #OE	tdis(OE)		100	
Output Enable Time from #WE	ten(WE)	5		
Output Enable Time from #OE	ten(OE)	5		
Output Enable Setup from #WE	tsu(OE-WE)	10		
Output Enable Setup from #OE	th(OE-WE)	10		
Card Enable Setup Time	tsu(CE)	0		
Card Enable Hold Time	th(CE)	20		
Read Cycle Time	tcR	300		ns
Address Access Time	ta(A)		300	
Card Enable Access Time	ta(CE)		300	
Output Enable Access Time	ta(OE)		150	
Output Disable Time from #OE	tdis(OE)		100	
Output Enable Time from #OE	ten(OE)	5		
Data Valid from Address Change	tv(A)	0		
Address Setup Time	tsu(A)	30		
Address Hold Time	th(A)	20		
Card Enable Setup Time ゜	tsu(CE)	0		
Card Enable Hold Time	th(CE)	20		

Note: For timing diagram, refer to PC CARD ELECTRICAL SPECIFICATION.

18-1-2. I/O write/ read timing

Item	Symbol	Specification		Unit
		Min.	Max.	
Data Setup before #IOWR	tsu(IOWR)	60		ns
Data Hold following #IOWR	th(IOWR)	30		
#IOWR Witdh Time	twIOWR	165		
Address Setup before #IOWR	tsuA(IOWR)	70		
Address Hold following #IOWR	thA(IOWR)	20		
#CE Setup before #IOWR	tsuCE(IOWR)	5		
#CE Hold following #IOWR	thCE(IOWR)	20		
#REG Setup before #IOWR	tsuREG(IOWR)	5		
#REG Hold following #IOWR	thREG(IOWR)	0		
#IOIS16 Delay Falling from Address	tdfIOIS16(ADR)		35	
#IOIS16 Delay Rising from Address	tdrIOIS16(ADR)		35	
Data Delay after #IORD	td(IORD)		100	ns
Data Hold following #IORD	th(IORD)	0		
#IORD Witdh Time	twIORD	165		
Address Setup before #IORD	tsuA(IORD)	70		
Address Hold following #IORD	thA(IORD)	20		
#CE Setup before #IORD	tsuCE(IORD)	5		
#CE Hold following #IORD	thCE(IORD)	20		
#REG Setup before #IORD	tsuREG(IORD)	5		
#REG Hold following #IORD	thREG(IORD)	0		
#INPACK Delay Falling from #IORD	tdfINPACK(IORD)	0	45	
#INPACK Delay Rising from #IORD	tdrINPACK(IORD)		45	
#IOIS16 Delay Falling from Address	tdfIOIS16(ADR)		35	
#IOIS16 Delay Rising from Address	tdrIOIS16(ADR)		35	

Note: For timing diagram, refer to PC CARD ELECTRICAL SPECIFICATION.

18-2. SmartMedia™ interface

18-2-1. SmartMedia™ write timing

Item	Symbol	Specification		Unit
		Min.	Max.	
FCLE Setup Time	tCLS	50		ns
FCLE Hold Time	tCLH	50		
#FCE Setup Time	tCS	50		
#FCE Hold Time	tCH	50		
#FWE Pulse Width	tWP	50		
FALE Setup Time	tALS	50		
FALE Hold Time	tALH	50		
Data Setup Time	tDS	50		
Data Hold Time	tDH	50		
Write Cycle Time	tWC	100		
#FWE High Hold Time	tWH	50		
#FWE High to #FBSY	tWB		205	

Note: For the timing diagram, refer to the SmartMedia™ Electric Specification.

18-2-2. SmartMedia™ read timing

Item	Symbol	Specification		Unit
		Min.	Max.	
Ready to #FRE Low	tRR	150		ns
Read Pulse Time	tRP	60		
Read Cycle Time	tRC	100		
#FRE Access Time (Serial Data Access)	tREA	50		
#FRE Access Time (Status Read)	tRSTO	50		
#FRE Access Time (ID Read)	tREAID	120		
#FRE High Hold Time	tREH	25		
#FWE High to #FRE Low	tWHR	70		
Last #FRE High to #FBSY	tRB		205	

Note: For the timing diagram, refer to the SmartMedia™ Electric Specification..
SmartMedia™ has no timing restriction on tR, tCRY, tBERASE, tPROG, tBERS.

18-3. SD Memory Card/ MultiMediaCard interface

Item	Symbol	Specification		Unit
		Min.	Max.	
Clock Frequency Data Transfer Mode	fPP		16	MHz
Clock Frequency Identification Mode	fOD		250	kHz
Clock Low Time	tWL	24		ns
Clock High Time	tWH	24		
Clock Rise Time	tTLH		10	
Clock Fall Time	tTHL		10	
Input Setup Time	tISU	10		
Input Hold Time	tIH	20		
Output Delay Time	tODLY		14	

Note: For timing diagram, refer to the specification of each media.

18-4. NOR flash memory interface

18-4-1. Fujitsu (AMD) NOR flash memory interface

Item	Symbol	Spec.		Unit
		Min.	Max.	
Write Cycle Time	TWC	120		ns
Address Setup Time	TAS	0		
Address Hold Time	TAH	50		
Data Setup Time	TDS	50		
Data Hold Time	TDH	0		
Output Enable Setup Time	TOES	0		
Output Enable Hold Time	TOEH	10		
Read Recovery Time	TGHW(E)L	0		
#NOR_CE Setup Time	TCS	0		
#NOR_WE Setup Time	TWS	0		
#NOR_CE Hold Time	TCH	0		
#NOR_WE Hold Time	TWH	0		
#NOR_WE Pulse Witdh	TWP	50		
#NOR_CE Pulse Witdh	TCP	50		
#NOR_WE Pulse Witdh High	TWPH	30		
#NOR_CE Pulse Witdh High	TCPH	30		
Read Cycle Time	TRC	120		ns
Address Access Time	TACC		120	
Data Output from #NOR_CE	TCE		120	
Data Output from #NOR_OE	TOE		50	
Data Output Flowting from #NOR_CE	TDF		30	
DATA Output Flowting from #NOR_OE	TDF		30	
Output Hold Time	TOH	0		

Note: For timing diagram, refer to the specification of each media.

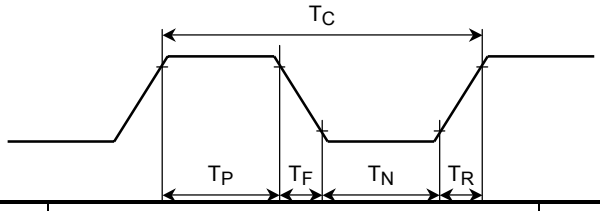
18-4-2. Sharp (Intel) NOR flash memory interface

Item	Symbol	Spec.		Unit
		Min.	Max.	
Write Cycle Time	tAVAV	150		ns
#NOR_RP High Recovery to #NOR_WE Going Low	tPHWL	1		us
#NOR_CE Setup to #NOR_WE Going Low	tELWL	10		ns
#NOR_WE Pulse Witdh	tWLWH	50		
Address Setup to #NOR_WE Going High	tAVWH	50		
Data Setup to #NOR_WE Going High	tDVWH	50		
Data Hold from #NOR_WE High	tWHDX	5		
Address Hold from #NOR_WE High	tWHAX	5		
#NOR_CE Hold from #NOR_WE High	tWHEH	10		
#NOR_WE Pulse Witdh	tWHWL	30		
#NOR_WE High to #NOR_BSY Going Low	tWHRL		100	
Write Recovery before Read	tWHGL	0		
Read Cycle Time	tAVAV	150		ns
Address to Output Delay	tAVQV		150	
#NOR_CE to Output Delay	tELQV		150	
#NOR_RP high to Output Delay	tPHQV		600	
#NOR_OE to Output Delay	tGLQV		55	
#NOR_CE to Output in Low Z	tELQX	0		
#NOR_CE High to Output in High Z	tEHQZ		55	
#NOR_OE to Output in Low Z	tGLQX	0		
#NOR_OE High to Output in High Z	tGHQZ		25	
Output Hold	tOH	0		

Note: For timing diagram, refer to the specification of each media.

18-5. Clock input condition

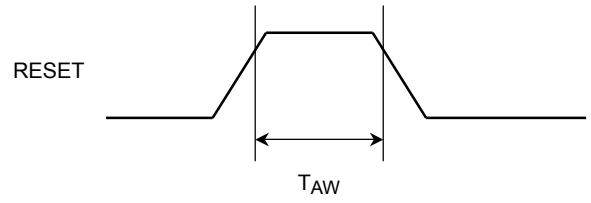
Clock input condition for TC6374AF is following.



Symbol	Item	Specification		Unit
		Min	Max	
T_P	“1” Pulse Witdh	28		ns
T_N	“0” Pulse Witdh	28		
T_R	Rising Time		5	
T_F	Falling Time		5	
T_C	Cycle Time	62.5		

18-6. Reset input condition

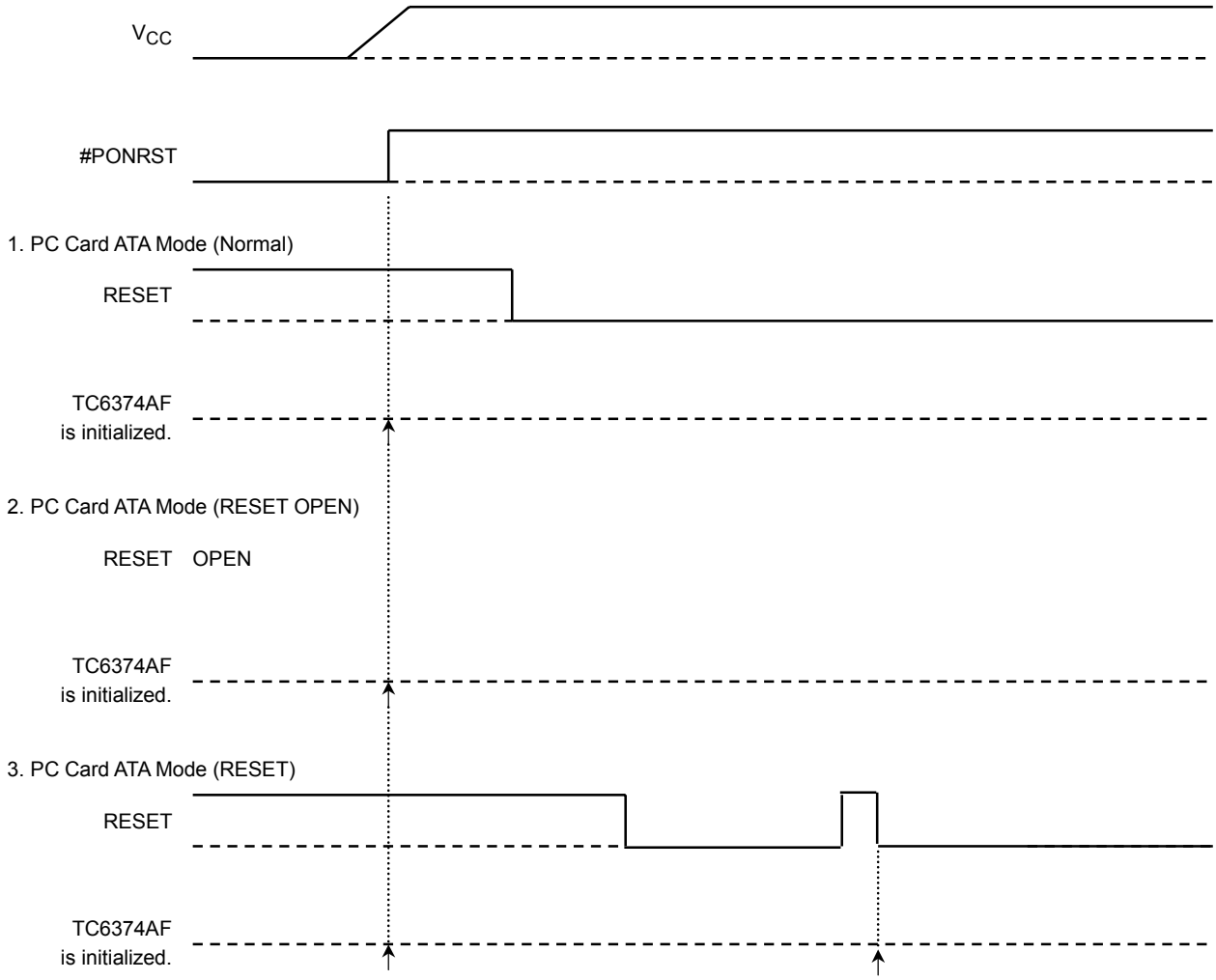
Reset input condition for TC6374AF is following.



Item	Symbol	Specification		Unit
		Min.	Max.	
Reset Pulse Width	T_{AW}	30		ns

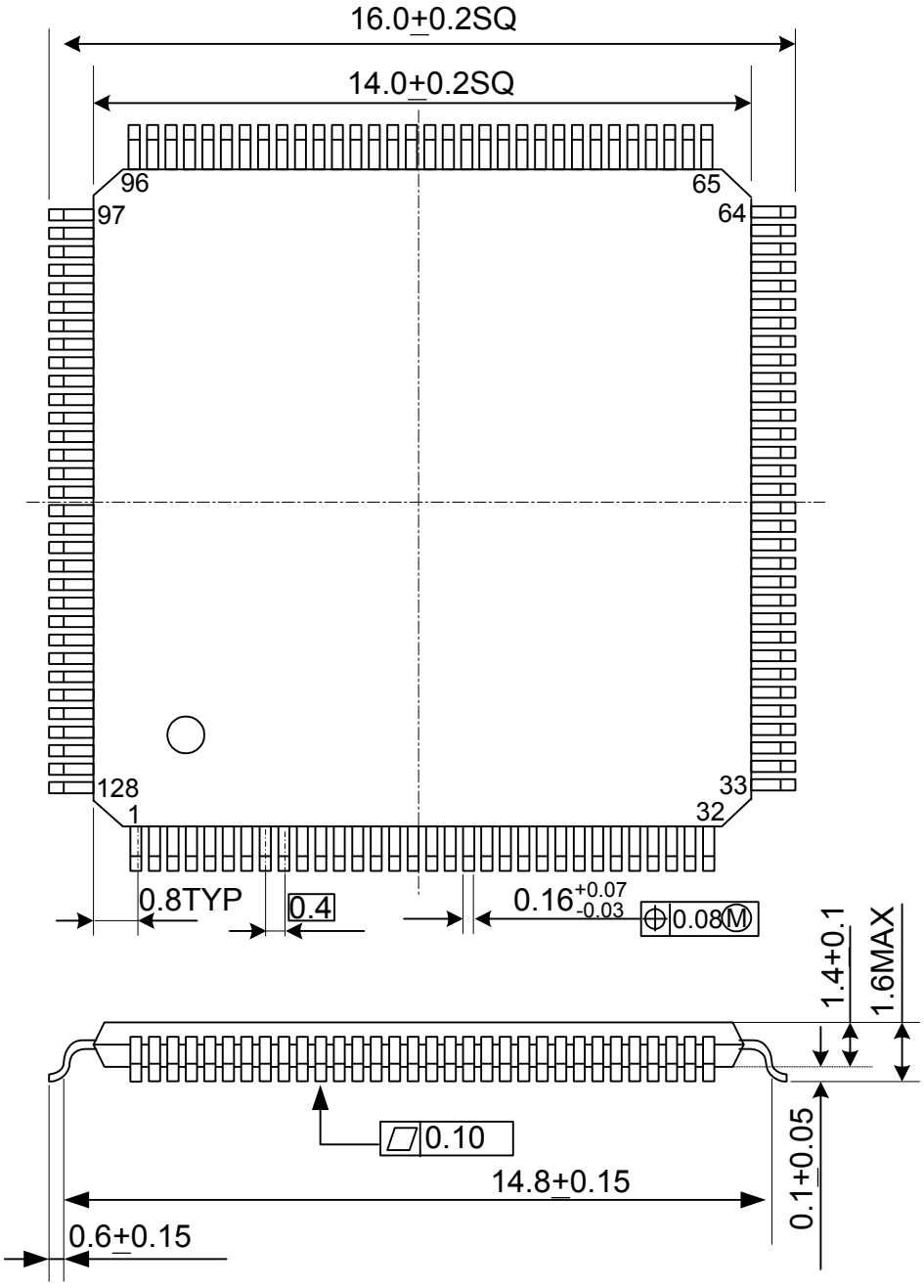
Moreover, refer to “19. Reset sequence”

19. Reset sequence



Note: RESET state is canceled on above " ↑ " timing.

20. Package outline



This datasheet describes the TC6374AF operation with use of Version 2.50 or upper version of firmware.

- We are intent on improving quality and reliability, but generally Semiconductor products can be at malfunction and fault. If you are using our Semiconductor products, you are reqested to draw a safety design of the equipmen at buyer's risk not to infringe on other people's lives, boky and property because of Semiconductore products malfunction and problems.

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TC6374AF hardware datasheet revision history

Revi-sion	Approval	Author	Date	Note
0.94	T. Takada	K. Naito	2001/ 03/07	Issued
1.00	T. Takada	S. Kawasaki	2001/ 05/18	5. Pin assignment table: Revised 6-7. Notes on 3in1 PC Card ATA adapter: Revised 13-1. SmartMedia™: Recognizeable Device ID table Revised 14-4. PC Card ATA Power Consumption of TC6374AF: Revised 15. Absolute maximum ratings: Added 16. Standard operation conditions: Added 17. DC electrical characteristics: Added 20. Package outline: Revised
1.01	T. Takada	S. Kawasaki	2001/ 11/30	Added commands below: 8-5-1-22. WRITE SECTOR (S) - 30h or 31h 8-5-2-1. CHECK SD EXTENSION - D1h 8-5-2-2. SD HEADER - D2h 8-5-2-3. SD EXECUTE - D3h 8-5-2-4. RETRIEVE RESPONSE - D4h 8-5-2-5. SD DATA OUT - D5h
1.21	T. Takada	K. Naito	2002/ 1/31	4. Contents: Page number revised 6-2. Host interface 2: Revised 7-4-4-2-1. Lower byte access: Revised 7-5-2-2. Card Configuration and Status Register: Revised 7-5-2-3. Pin Replacement Register: Revised 8-2. Operation of ATA COMMAND BLOCK REGISTER: Added 8-5-1-4. GET MEDIA STATUS – Dah: Added 8-5-1-8. INITIALIZE DEVICE PARAMETERS – 91h: Added/ Revised 8-5-1-15. SET FEATURES – Efh, Normal Outputs – The case of Subcommand Code is “Ech”: Revised value 8-5-2-1. CHECK SD EXTENSION – D1h: Added/ Revised 8-5-2-2. SD HEADER – D2h: Added 12-2. SD Memory Card / MultiMediaCard: Added/ Revised 18-4-2. Sharp (Intel) NOR flash memory interface: Revised Added firmware revision information
1.22	T. Takada	K. Naito	2002/ 2/15	7-4-4-1-3. Word Access: Corrected 7-5-3-12. Device Address Register D7 bit: Deleted 12-2. SD Memory Card/ Multimedia Card: Revised