TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

16-MBIT (2M × 8 BITS / 1M × 16 BITS) CMOS FLASH MEMORY

DESCRIPTION

The TC58FVT160/B160A is a 16,777,216-bit, 3.0-V read-only electrically erasable and programmable flash memory organized as 2,097,152 words × 8 bits or as 1,048,576 words × 16 bits. The TC58FVT160/B160A features commands for Read, Program and Erase operations to allow easy interfacing with microprocessors. The commands are based on the JEDEC standard. The Program and Erase operations are automatically executed in the chip.

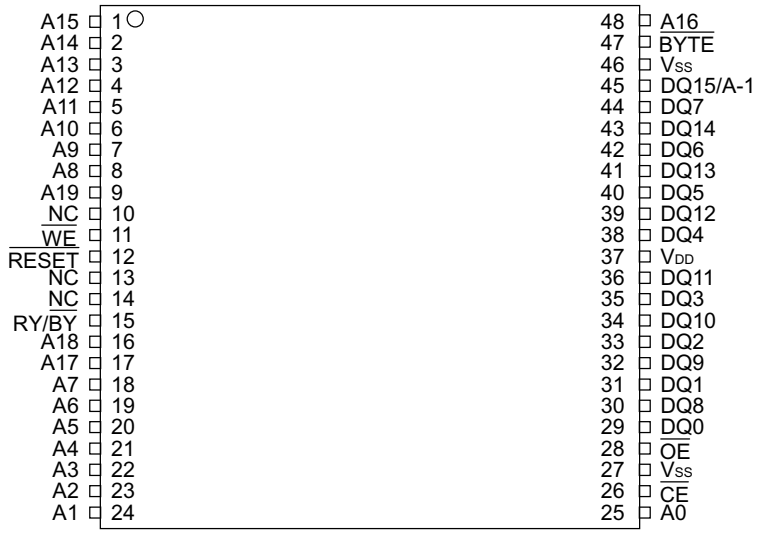
FEATURES

- Power supply voltage
  V_{DD} = 2.7 V~3.6 V
- Operating temperature
  Ta = –40°C~85°C
- Organization
  2M × 8 bits / 1M × 16 bits
- Functions
  Auto Program, Auto Erase
  Fast Program Mode
  Program Suspend/Resume
  Erase Suspend/Resume
  data polling / Toggle bit
  block protection
  Automatic Sleep, support for hidden ROM area
  common flash memory interface (CFI)
  Byte/Word Modes
- Block erase architecture
  1 × 16 Kbytes / 2 × 8 Kbytes
  1 × 32 Kbytes / 31 × 64 Kbytes
- Boot block architecture
  TC58FVT160AFT/AXB: top boot block
  TC58FVB160AFT/AXB: bottom boot block
- Mode control
  Compatible with JEDEC standard commands
- Erase/Program cycles
  10^5 cycles typ.
- Access time
  70 ns (C_L: 30 pF)
  100 ns (C_L: 100 pF)
- Power consumption
  5 μA (Standby)
  30 mA (Read operation)
  15 mA (Program/Erase operations)
- Package
  TC58FVT160/B160AFT:
  TSOPI48-P-1220-0.50 (weight: 0.51 g)
  TC58FVT160/B160AXB:
  P-TFBGA48-0608-0.80AZ (weight: 0.090 g)

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PIN ASSIGNMENT (TOP VIEW) ···TC58FVT160/B160AFT



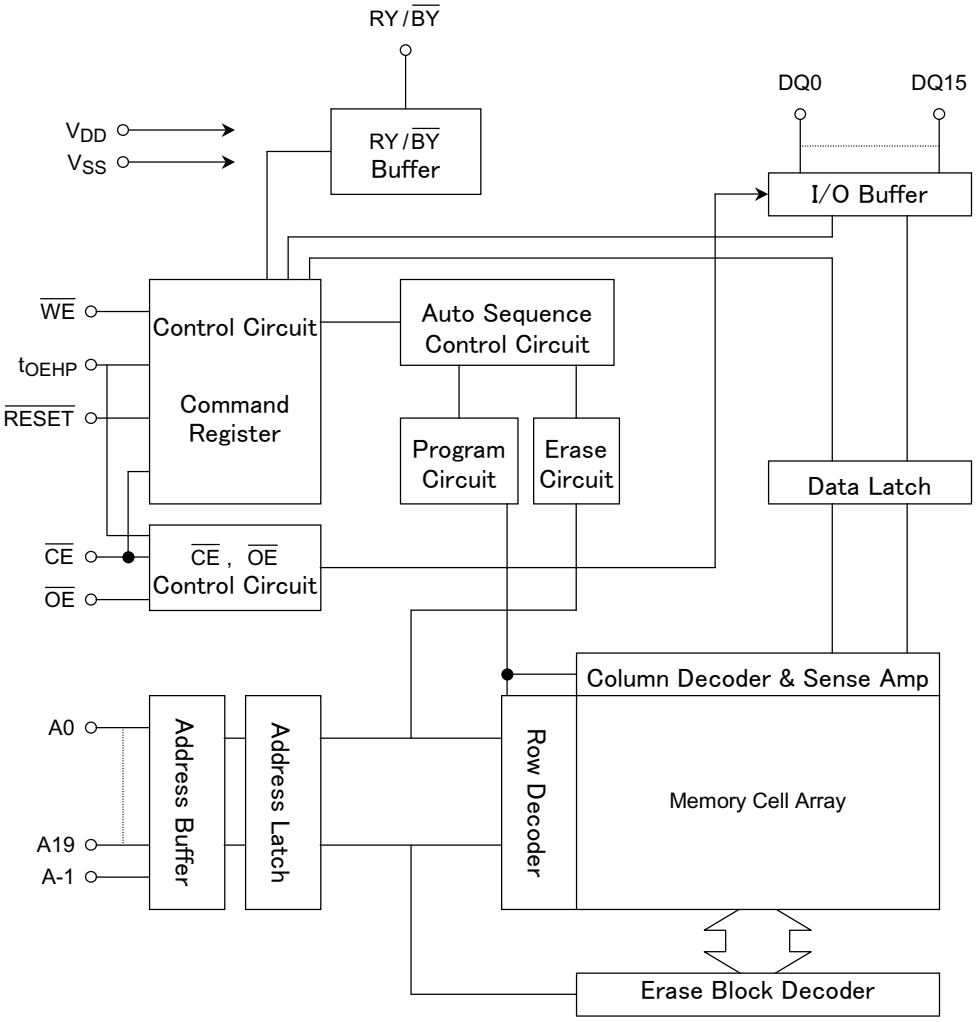
PIN NAMES

A-1, A0~A19	Address Input
DQ0~DQ15	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{BYTE}$	Word/Byte Select Input
$\overline{WE}$	Write Enable Input
RY/$\overline{BY}$	Ready/Busy Output
$\overline{RESET}$	Hardware Reset Input
NC	Not Connected
V_{DD}	Power Supply
V_{SS}	Ground

PIN ASSIGNMENT (TOP VIEW)···TC58FVT160/B160AXB

	1	2	3	4	5	6
A	A3	A7	RY/$\overline{BY}$	$\overline{WE}$	A9	A13
B	A4	A17	NC	$\overline{RESET}$	A8	A12
C	A2	A6	A18	NC	A10	A14
D	A1	A5	NC	A19	A11	A15
E	A0	DQ0	DQ2	DQ5	DQ7	A16
F	$\overline{CE}$	DQ8	DQ10	DQ12	DQ14	$\overline{BYTE}$
G	$\overline{OE}$	DQ9	DQ11	V_{DD}	DQ13	DQ15
H	V_{SS}	DQ1	DQ3	DQ4	DQ6	V_{SS}

BLOCK DIAGRAM



MODE SELECTION

									BYTE MODE	WORD MODE
MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A9	A6	A1	A0	$\overline{RESET}$	DQ0~DQ7(1)	DQ0~DQ15
Read	L	L	H	A9	A6	A1	A0	H	D_{OUT}	D_{OUT}
ID Read (Manufacturer Code)	L	L	H	V_{ID}	L	L	L	H	Code	Code
ID Read (Device Code)	L	L	H	V_{ID}	L	L	H	H	Code	Code
Standby	H	*	*	*	*	*	*	H	High-Z	High-Z
Output Disable	*	H	H	*	*	*	*	*	High-Z	High-Z
Write	L	H	(2)	A9	A6	A1	A0	H	D_{IN}	D_{IN}
Block Protect 1	L	V_{ID}	(2)	V_{ID}	L	H	L	H	*	*
Verify Block Protect	L	L	H	V_{ID}	L	H	L	H	Code	Code
Temporary Block Unprotect	*	*	*	*	*	*	*	V_{ID}	*	*
Hardware Reset / Standby	*	*	*	*	*	*	*	L	High-Z	High-Z

Notes: * = V_{IH} or V_{IL}, L = V_{IL}, H = V_{IH}

(1) DQ8~DQ14 are High-Z and DQ15/A-1 is Address Input in Byte Mode.
Addresses are A19~A0 in Word Mode ($\overline{BYTE}$ = V_{IH}), A19~A-1 in Byte Mode ($\overline{BYTE}$ = V_{IL}).

(2) Pulse input

ID CODE TABLE

CODE TYPE		A19~A12	A6	A1	A0	CODE (HEX)(1)
Manufacturer Code		*	L	L	L	0098H
Device Code	TC58FVT160A	*	L	L	H	00C2H
	TC58FVB160A	*	L	L	H	0043H
Verify Block Protect		BA(2)	L	H	L	Data(3)

Notes: * = V_{IH} or V_{IL}, L = V_{IL}, H = V_{IH}

(1) DQ8~DQ14 are High-Z and DQ15/A-1 is Address Input in Byte Mode.

(2) BA: Block Address

(3) 0001H - Protected Block
0000H - Unprotected Block

COMMAND SEQUENCES

COMMAND SEQUENCE		BUS WRITE CYCLES REQ'D	FIRST BUS WRITE CYCLE		SECOND BUS WRITE CYCLE		THIRD BUS WRITE CYCLE		FOURTH BUS WRITE CYCLE		FIFTH BUS WRITE CYCLE		SIXTH BUS WRITE CYCLE	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset		1	XXXH	F0H										
Read/Reset	Word	3	555H	AAH	2AAH	55H	555H	F0H	RA(1)	RD(2)				
	Byte		AAAH		555H		AAAH							
ID Read	Word	3	555H	AAH	2AAH	55H	555H	90H	IA(3)	ID(4)				
	Byte		AAAH		555H		AAAH							
Auto-Program	Word	4	555H	AAH	2AAH	55H	555H	A0H	PA(5)	PD(6)				
	Byte		AAAH		555H		AAAH							
Program Suspend		1	V_{IH} or V_{IL}	B0H										
Program Resume		1	V_{IH} or V_{IL}	30H										
Auto Chip Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
	Byte		AAAH		555H		AAAH		AAAH		555H		AAAH	
Auto Block Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	BA(7)	30H
	Byte		AAAH		555H		AAAH		AAAH		555H			
Block Erase Suspend		1	V_{IH} or V_{IL}	B0H										
Block Erase Resume		1	V_{IH} or V_{IL}	30H										
Block Protect 2		4	XXXH	60H	BPA(8)	60H	XXXH	40H	BPA(8)	BPD(9)				
Verify Block Protect	Word	3	555H	AAH	2AAH	55H	555H	90H	BPA(8)	BPD(9)				
	Byte		AAAH		555H		AAAH							
Fast Program Set	Word	3	555H	AAH	2AAH	55H	555H	20H						
	Byte		AAAH		555H		AAAH							
Fast Program		2	XXXH	A0H	PA(5)	PD(6)								
Fast Program Reset		2	XXXH	90H	XXXH	F0H(12)								
Hidden ROM Mode Entry	Word	3	555H	AAH	2AAH	55H	555H	88H						
	Byte		AAAH		555H		AAAH							
Hidden ROM Program	Word	4	555H	AAH	2AAH	55H	555H	A0H	PA(5)	PD(6)				
	Byte		AAAH		555H		AAAH							
Hidden ROM Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	BA(7)	30H
	Byte		AAAH		555H		AAAH		AAAH		555H			
Hidden ROM Mode Exit	Word	4	555H	AAH	2AAH	55H	555H	90H	XXXH	00H				
	Byte		AAAH		555H		AAAH							
Query Command	Word	2	55H	98H	CA(10)	CD(11)								
	Byte		AAH											

Notes: The system should generate the following address patterns:
Word Mode: 555H or 2AAH on address pins A10~A0
Byte Mode: AAAH or 555H on address pins A10~A-1
DQ8~DQ15 are ignored in Word Mode.

(1) RA: Read Address
(2) RD: Read Data
(3) IA: ID Read Address (A6, A1, A0)
Manufacturer Code = (0, 0, 0)
Device Code = (0, 0, 1)
(4) ID: ID Data
(5) PA: Program Address
(6) PD: Program Data
(7) BA: Block Address = A19~A12
(8) BPA: Block Address and ID Read Address (A6, A1, A0)
Block Address = A19~A12
ID Read Address = (0, 1, 0)
(9) BPD: Verify Data
(10) CA: CFI Address
(11) CD: CFI Data
(12) F0H: 00H is valid too

OPERATION MODES

In addition to the Read, Write and Erase Modes, the TC58FVT160/B160A features many functions including block protection and data polling. When incorporating the device into a deign, please refer to the timing charts and flowcharts in combination with the description below.

READ MODE

To read data from the memory cell array, set the device to Read Mode. In Read Mode the device can perform high-speed random access as asynchronous ROM.

The device is automatically set to Read Mode immediately after power-on or on completion of automatic operation. A software reset releases ID Read Mode and the lock state which the device enters if automatic operation ends abnormally, and sets the device to Read Mode. A hardware reset terminates operation of the device and resets it to Read Mode. When reading data without changing the address immediately after power-on, either input a hardware Reset or change $\overline{CE}$ from H to L.

ID Read Mode

ID Read Mode is used to read the device maker code and device code. The mode is useful in that it allows EPROM programmers to identify the device type automatically.

ID read can be executed in two ways, as follows:

(1) Applying V_{ID} to A9

This method is used mainly by EPROM programmers. Applying V_{ID} to A9 sets the device to ID Read Mode, outputting the maker code from address 00H and the device code from address 01H. Releasing V_{ID} from A9 returns the device to Read Mode.

(2) Input command sequence

Inputting an ID Read command sets to ID Read Mode. The maker code is output from address 00; the device code is output from address 01. Inputting a Reset command releases ID Read Mode and returns the device to Read Mode.

Access time in ID Read Mode is the same as that in Read Mode. For a list of the codes, please refer to the ID Code Table.

Standby Mode

There are two ways to put the device into Standby Mode.

(1) Control using $\overline{CE}$ and $\overline{RESET}$

With the device in Read Mode, input $V_{DD} \pm 0.3$ V to $\overline{CE}$ and $\overline{RESET}$. The device will enter Standby Mode and the current will be reduced to the standby current (I_{DDS1}).

(2) Control using $\overline{RESET}$ only

With the device in Read Mode, input $V_{SS} \pm 0.3$ V to $\overline{RESET}$. The device will enter Standby Mode and the current will be reduced to the standby current (I_{DDS1}).

In Standby Mode DQ is put in High-Impedance state.

Auto-Sleep Mode

This function suppresses power dissipation during reading. If the address input does not change for 150 ns, the device will automatically enter Sleep Mode and the current will be reduced to the standby current (I_{DDS2}). Because the output data is latched, data is output in Sleep Mode. When the address is changed, Sleep Mode is automatically released, and data from the new address is output.

Output Disable Mode

Inputting V_{IH} to $\overline{OE}$ disables output from the device and sets DQ to High-Impedance.

Command Write

The TC58FVT160/B160A uses the standard JEDEC control commands for a single-power supply E^2PROM. A Command Write is executed by inputting the address and data into the Command Register. The command is written by inputting a pulse to $\overline{WE}$ with $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IH} ($\overline{WE}$ control). The command can also be written by inputting a pulse to $\overline{CE}$ with $\overline{WE}$ = V_{IL} ($\overline{CE}$ control). The address is latched on the falling edge of either $\overline{WE}$ or $\overline{CE}$. The data is latched on the rising edge of either $\overline{WE}$ or $\overline{CE}$. DQ0~DQ7 are valid for data input and DQ8~DQ15 are ignored.

To abort input of the command sequence use the Reset command. The device will reset the Command Register and enter Read Mode. If an undefined command is input, the Command Register will be reset and the device will enter Read Mode.

Software Reset

Apply a software reset by inputting a Read/Reset command. A software reset returns the device from ID Read Mode or CFI Mode to Read Mode, releases the lock state if automatic operation has ended abnormally, and clears the Command Register.

Hardware Reset

A hardware reset initializes the device and sets it to Read Mode. When a pulse is input to $\overline{RESET}$ for t_{RP}, the device abandons the operation which is in progress and enters Read Mode after t_{READY}. Note that if a hardware reset is applied during data overwriting, such as a Write or Erase operation, data at the address or block being written to at the time of the reset will become undefined.

After a hardware reset the device enters Read Mode if $\overline{RESET}$ = V_{IH} or Standby Mode if $\overline{RESET}$ = V_{IL}. The DQ pins are High-Impedance when $\overline{RESET}$ = V_{IL}. After the device has entered Read Mode, Read operations and input of any command are allowed.

Comparison between Software Reset and Hardware Reset

ACTION	SOFTWARE RESET	HARDWARE RESET
Releases ID Read Mode or CFI Mode.	True	True
Clears the Command Register.	True	True
Releases the lock state if automatic operation has ended abnormally.	True	True
Stops any automatic operation which is in progress.	False	True
Stops any operation other than the above and returns the device to Read Mode.	False	True

$\overline{BYTE}$/Word Mode

$\overline{BYTE}$ is used select Word Mode (16 bits) or Byte Mode (8 bits) for the TC58FVT160/B160A. If V_{IH} is input to $\overline{BYTE}$, the device will operate in Word Mode. Read data or write commands using DQ0~DQ15. When V_{IL} is input to $\overline{BYTE}$, read data or write commands using DQ0~DQ7. DQ15/A-1 is used as the lowest address. DQ8~DQ14 will become High-Impedance.

Auto-Program Mode

The TC58FVT160/B160A can be programmed in either byte or word units. Auto-Program Mode is set using the Program command. The program address is latched on the falling edge of the $\overline{WE}$ signal and data is latched on the rising edge of the fourth Bus Write cycle (with $\overline{WE}$ control). Auto programming starts on the rising edge of the $\overline{WE}$ signal in the fourth Bus Write cycle. The Program and Program Verify commands are automatically executed by the chip. The device status during programming is indicated by the Hardware Sequence flag. To read the Hardware Sequence flag, specify the address to which the Write is being performed.

During Auto-Program execution, a command sequence cannot be accepted. To terminate execution, use a hardware reset. Note that if the Auto-Program operation is terminated in this manner, the data written so far is invalid.

Any attempt to program a protected block is ignored. In this case the device enters Read Mode 3 μs after the rising edge of the $\overline{WE}$ signal in the fourth Bus Write cycle.

If an Auto-Program operation fails, the device remains in the programming state and does not automatically return to Read Mode. The device status is indicated by the Hardware Sequence flag. Either a Reset command or a hardware reset is required to return the device to Read Mode after a failure. If a programming operation fails, the block which contains the address to which data could not be programmed should not be used.

The device allows 0s to be programmed into memory cells which contain a 1. 1s cannot be programmed into cells which contain 0s. If this is attempted, execution of Auto Program will fail. This is a user error, not a device error. A cell containing 0 must be erased in order to set it to 1.

Fast Program Mode

Fast Program is a function which enables execution of the command sequence for the Auto Program to be completed in two cycles. In this mode the first two cycles of the command sequence, which normally requires four cycles, are omitted. Writing is performed in the remaining two cycles. To execute Fast Program, input the Fast Program command. Write in this mode uses the Fast Program command but operation is the same at that for ordinary Auto-Program. The status of the device is indicated by the Hardware Sequence flag and read operations can be performed as usual. To exit this mode, the Fast Program Reset command must be input. When the command is input, the device will return to Read Mode.

Program Suspend/Resume Mode

Program Suspend is used to enable Data Read by suspending the Write operation. The device accepts a Program Suspend command in Write Mode (including Write operations performed during Erase Suspend) but ignores the command in other modes. After input of the command, the device will enter Program Suspend Read Mode after t_{SUSP}.

During Program Suspend, Cell Data Read, ID Read and CFI Data Read can be performed. When Data Write is suspended, the address to which Write was being performed becomes undefined. ID Read and CFI Data Read are the same as usual.

After completion of Program Suspend input a Program Resume command to return to Write Mode. On receiving the Resume command, the device returns to Write Mode and resumes outputting the Hardware Sequence flag for the bank to which data is being written.

Program Suspend can be run in Fast Program Mode.

Auto Chip Erase Mode

The Auto Chip Erase Mode is set using the Chip Erase command. An Auto Chip Erase operation starts on the rising edge of $\overline{WE}$ in the sixth bus cycle. All memory cells are automatically preprogrammed to 0, erased and verified as erased by the chip. The device status is indicated by the Hardware Sequence flag.

Command input is ignored during an Auto Chip Erase. A hardware reset can interrupt an Auto Chip Erase operation. If an Auto Chip Erase operation is interrupted, it cannot be completed correctly. Hence an additional Erase operation must be performed.

Any attempt to erase a protected block is ignored. If all blocks are protected, the Auto Erase operation will not be executed and the device will enter Read mode 100 μs after the rising edge of the $\overline{WE}$ signal in the sixth bus cycle.

If an Auto Chip Erase operation fails, the device will remain in the erasing state and will not return to Read Mode. The device status is indicated by the Hardware Sequence flag. Either a Reset command or a hardware reset is required to return the device to Read Mode after a failure.

In this case it cannot be ascertained which block the failure occurred in. Either abandon use of the device altogether, or perform a Block Erase on each block, identify the failed block, and stop using it. The host processor must take measures to prevent subsequent use of the failed block.

Auto Block Erase / Auto Multi-Block Erase Modes

The Auto Block Erase Mode and Auto Multi-Block Erase Mode are set using the Block Erase command. The block address is latched on the falling edge of the $\overline{WE}$ signal in the sixth bus cycle. The block erase starts as soon as the Erase Hold Time (t_{BEH}) has elapsed after the rising edge of the $\overline{WE}$ signal. When multiple blocks are erased, the sixth Bus Write cycle is repeated with each block address and Auto Block Erase command being input within the Erase Hold Time (this constitutes an Auto Multi-Block Erase operation). If a command other than an Auto Block Erase command or Erase Suspend command is input during the Erase Hold Time, the device will reset the Command Register and enter Read Mode. The Erase Hold Time restarts on each successive rising edge of $\overline{WE}$. Once operation starts, all memory cells in the selected block are automatically preprogrammed to 0, erased and verified as erased by the chip. The device status is indicated by the setting of the Hardware Sequence flag. When the Hardware Sequence flag is read, the addresses of the blocks on which auto-erase operation is being performed must be specified.

All commands (except Erase Suspend) are ignored during an Auto Block Erase or Auto Multi-Block Erase operation. Either operation can be aborted using a Hardware Reset. If an auto-erase operation is interrupted, it cannot be completed correctly; therefore, a further erase operation is necessary to complete the erasing.

Any attempt to erase a protected block is ignored. If all the selected blocks are protected, the auto-erase operation is not executed and the device returns to Read Mode 100 μs after the rising edge of the $\overline{WE}$ signal in the last bus cycle.

If an auto-erase operation fails, the device remains in Erasing state and does not return to Read Mode. The device status is indicated by the Hardware Sequence flag. After a failure either a Reset command or a Hardware Reset is required to return the device to Read Mode. If multiple blocks are selected, it will not be possible to ascertain the block in which the failure occurred. In this case either abandon use of the device altogether, or perform a Block Erase on each block, identify the failed block, and stop using it. The host processor must take measures to prevent subsequent use of the failed block.

Erase Suspend / Erase Resume Modes

Erase Suspend Mode suspends Auto Block Erase and reads data from or writes data to an unselected block. The Erase Suspend command is allowed during an auto block erase operation but is ignored in all other oreration modes .

In Erase Suspend Mode only a Read, Program or Resume command can be accepted. If an Erase Suspend command is input during an Auto Block Erase, the device will enter Erase Suspend Read Mode after t_{SUSE}. The device status (Erase Suspend Read Mode) can be verified by checking the Hardware Sequence flag. If data is read consecutively from the block selected for Auto Block Erase, the DQ2 output will toggle and the DQ6 output will stop toggling and RY/$\overline{BY}$ will be set to High-Impedance.

Inputting a Write command during an Erase Suspend enables a Write to be performed to a block which has not been selected for the Auto Block Erase. Data is written in the usual manner.

To resume the Auto Block Erase, input an Erase Resume command. On receiving an Erase Resume command, the device returns to the state it was in when the Erase Suspend command was input. If an Erase Suspend command is input during the Erase Hold Time, the device will return to the state it was in at the start of the Erase Hold Time. At this time more blocks can be specified for erasing. If an Erase Resume command is input during an Auto Block Erase, Erase resumes. At this time toggle output of DQ6 resumes and 0 is output on RY/$\overline{BY}$.

Block Protection

Block Protection is a function for disabling writing and erasing specific blocks. Block protection can be carried out in two ways: by supplying a high voltage (V_{ID}) to the device (see Block protection 1) or by supplying a high voltage and a command sequence (see Block protection 2).

(1) Block protection 1

Specify a device block address and make the following signal settings A9 = $\overline{OE}$ = V_{ID}, A1 = V_{IH} and $\overline{CE}$ = A0 = A6 = V_{IL}. Now when a pulse is input to $\overline{WE}$ for t_{PPLH}, the device will start to write to the block protection circuit. Block protection can be verified using the Verify Block Protect command. Inputting V_{IL} on $\overline{OE}$ sets the device to Verify Mode. 01H is output if the block is protected and 00H is output if the block is unprotected. If block protection was unsuccessful, the operation must be repeated. Releasing V_{ID} from A9 and $\overline{OE}$ terminates this mode.

(2) Block protection 2

Applying V_{ID} to $\overline{RESET}$ and inputting the Block Protect 2 command also performs block protection. The first cycle of the command sequence is the Set-up command. In the second cycle, the Block Protect command is input, in which a block address and A1 = V_{IH} and A0 = A6 = V_{IL} are input. Now the device writes to the block protection circuit. There is a wait of t_{PPLH} until this write is completed; however, no intervention is necessary during this time. In the third cycle the Verify Block Protect command is input. This command verifies the write to the block protection circuit. Read is performed in the fourth cycle. If the protection operation is complete, 01H is output. If a value other than 01H is output, block protection is not complete and the Block Protect command must be input again. Removing the V_{ID} input from $\overline{RESET}$ exits this mode.

Temporary Block Unprotection

The TC58FVT160/B160A has a temporary block unprotection feature which disables block protection for all protected blocks. Unprotection is enabled by applying V_{ID} to the $\overline{RESET}$ pin. Now Write and Erase operations can be performed on all blocks. The device returns to its previous state when V_{ID} is removed from the $\overline{RESET}$ pin. That is, previously protected blocks will be protected again.

Verify Block Protect

The Verify Block Protect command is used to ascertain whether a block is protected or unprotected. Verification is performed either by inputting the Verify Block Protect command or by applying V_{ID} to the A9 pin, as for ID Read Mode, and setting the block address = A0 = A6 = V_{IL} and A1 = V_{IH}. If the block is protected, 01H is output. If the block is unprotected, 00H is output.

Hidden ROM Area

The TC58FVT160/B160A features a 64-Kbyte hidden ROM area which is separate from the memory cells. The area consists of one block. Data Read, Write and Protect can be performed on this block. Because Protect cannot be released, once the block is protected, data in the block cannot be overwritten.

The hidden ROM area is located in the address space indicated in the HIDDEN ROM AREA ADDRESS TABLE. To access the Hidden ROM area, input a Hidden ROM Mode Entry command. The device now enters Hidden ROM Mode, allowing Read, Write, Erase and Block Protect to be executed. Write and Erase operations are the same as auto operations except that the device is in Hidden ROM Mode. To protect the hidden ROM area, use the block protection function. The operation of Block Protect here is the same as a normal Block Protect except that V_{IH} rather than V_{ID} is input to $\overline{RESET}$. Once the block has been protected, protection cannot be released, even using the temporary block unprotection function. Use Block Protect carefully.

To exit Hidden ROM Mode, use the Hidden ROM Mode Exit command. This will return the device to Read Mode.

HIDDEN ROM AREA ADDRESS TABLE

TYPE	BOOT BLOCK ARCHITECTURE	BYTE MODE		WORD MODE	
		ADDRESS RANGE	SIZE	ADDRESS RANGE	SIZE
TC58FVT160A	TOP BOOT BLOCK	1F0000H~1FFFFFH	64 Kbytes	F8000H~FFFFFH	32 Kwords
TC58FVB160A	BOTTOM BOOT BLOCK	000000H~00FFFFH	64 Kbytes	000000H~007FFFH	32 Kwords

COMMON FLASH MEMORY INTERFACE (CFI)

The TC58FVT160/B160A conforms to the CFI specifications. To read information from the device, input the Query command followed by the address. In Word Mode DQ8~DQ15 all output 0s. To exit this mode, input the Reset command.

CFI CODE TABLE

ADDRESS A6~A0	DATA DQ15~DQ0	DESCRIPTION
10H 11H 12H	0051H 0052H 0059H	ASCII string "QRY"
13H 14H	0002H 0000H	Primary OEM command set 2: AMD/FJ standard type
15H 16H	0040H 0000H	Address for primary extended table
17H 18H	0000H 0000H	Alternate OEM command set 0: none exists
19H 1AH	0000H 0000H	Address for alternate OEM extended table
1BH	0027H	V_{DD} (min) (Write/Erase) DQ7~DQ4: 1 V DQ3~DQ0: 100 mV
1CH	0036H	V_{DD} (max) (Write/Erase) DQ7~DQ4: 1 V DQ3~DQ0: 100 mV
1DH	0000H	V_{PP} (min) voltage
1EH	0000H	V_{PP} (max) voltage
1FH	0004H	Typical time-out per single byte/word write (2^N μs)
20H	0000H	Typical time-out for minimum size buffer write (2^N μs)
21H	000AH	Typical time-out per individual block erase (2^N ms)
22H	0000H	Typical time-out for full chip erase (2^N ms)
23H	0005H	Maximum time-out for byte/word write (2^N times typical)
24H	0000H	Maximum time-out for buffer write (2^N times typical)
25H	0004H	Maximum time-out per individual block erase (2^N times typical)
26H	0000H	Maximum time-out for full chip erase (2^N times typical)
27H	0015H	Device Size (2^N byte)
28H 29H	0002H 0000H	Flash device interface description 2: ×8/×16
2AH 2BH	0000H 0000H	Maximum number of bytes in multi-byte write (2^N)

ADDRESS A6~A0	DATA DQ15~DQ0	DESCRIPTION
2CH	0004H	Number of erase block regions within device
2DH 2EH 2FH 30H	0000H 0000H 0040H 0000H	Erase Block Region 1 information Bits 0~15: y = block number Bits 16~31: z = block size (z × 256 bytes)
31H 32H 33H 34H	0001H 0000H 0020H 0000H	Erase Block Region 2 information
35H 36H 37H 38H	0000H 0000H 0080H 0000H	Erase Block Region 3 information
39H 3AH 3BH 3CH	001EH 0000H 0000H 0001H	Erase Block Region 4 information
40H 41H 42H	0050H 0052H 0049H	ASCII string “PRI”
43H	0031H	Major version number, ASCII
44H	0031H	Minor version number, ASCII
45H	0000H	Address-Sensitive Unlock 0: Required 1: Not required
46H	0002H	Erase Suspend 0: Not supported 1: For Read-only 2: For Read & Write
47H	0001H	Block Protect 0: Not supported X: Number of blocks per group
48H	0001H	Block Temporary Unprotect 0: Not supported 1: Supported
49H	0004H	Block Protect/Unprotect scheme
4AH	0000H	Simultaneous operation 0: Not supported 1: Supported
4BH	0000H	Burst Mode 0: Not supported
4CH	0000H	Page Mode 0: Not supported
4FH	000XH	Top/Bottom Boot Block Flag 2: TC58FVB160 3: TC58FVT160
50H	0001H	Program suspend 0: Not supported 1: Supported

HARDWARE SEQUENCE FLAGS

The TC58FVT160A/B160A has a Hardware Sequence flag which allows the device status to be determined during an auto mode operation. The output data is read out using the same timing as that used when $\overline{CE}$ = $\overline{OE}$ = V_{IL} in Read Mode. The RY/$\overline{BY}$ output can be either High or Low.

The device re-enters Read Mode automatically after an auto mode operation has been completed successfully. The Hardware Sequence flag is read to determine the device status and the result of the operation is verified by comparing the read-out data with the original data.

STATUS				DQ7	DQ6	DQ5	DQ3	DQ2	RY/$\overline{BY}$
In Progress	Auto Programming			$\overline{DQ7}$	Toggle	0	0	1	0
	Read in Program Suspend(1)			Data	Data	Data	Data	Data	High-Z
	In Auto Erase	Erase Hold Time	Selected(2)	0	Toggle	0	0	Toggle	0
			Not-selected(3)	0	Toggle	0	0	1	0
		Auto Erase	Selected	0	Toggle	0	1	Toggle	0
			Not-selected	0	Toggle	0	1	1	0
	In Erase Suspend	Read	Selected	1	1	0	0	Toggle	High-Z
			Not-selected	Data	Data	Data	Data	Data	High-Z
		Programming	Selected	$\overline{DQ7}$	Toggle	0	0	Toggle	0
			Not-selected	$\overline{DQ7}$	Toggle	0	0	1	0
Time Limit Exceeded	Auto Programming			$\overline{DQ7}$	Toggle	1	0	1	0
	Auto Erase			0	Toggle	1	1	NA	0
	Programming in Erase Suspend			$\overline{DQ7}$	Toggle	1	0	NA	0

Notes: DQ outputs cell data and RY/$\overline{BY}$ goes High-Impedence when the operation has been completed.
DQ0 and DQ1 pins are reserved for future use.
0 is output on DQ0, DQ1 and DQ4.
(1) Data output from an address to which Write is being performed is undefined.
(2) Output when the block address selected for Auto Block Erase is specified and data is read from there. During Auto Chip Erase, all blocks are selected.
(3) Output when a block address not selected for Auto Block Erase and data is read from there.

DQ7 ($\overline{DATA}$ polling)

During an Auto-Program or auto-erase operation, the device status can be determined using the data polling function. $\overline{DATA}$ polling begins on the rising edge of $\overline{WE}$ in the last bus cycle. In an Auto-Program operation, DQ7 outputs inverted data during the programming operation and outputs actual data after programming has finished. In an auto-erase operation, DQ7 outputs 0 during the Erase operation and outputs 1 when the Erase operation has finished. If an Auto-Program or auto-erase operation fails, DQ7 simply outputs the data.

When the operation has finished, the address latch is reset. Data polling is asynchronous with the $\overline{OE}$ signal.

DQ6 (Toggle bit 1)

The device status can be determined by the Toggle Bit function during an Auto-Program or auto-erase operation. The Toggle bit begins toggling on the rising edge of $\overline{WE}$ in the last bus cycle. DQ6 alternately outputs a 0 or a 1 for each $\overline{OE}$ access while $\overline{CE}$ = V_{IL} while the device is busy. When the internal operation has been completed, toggling stops and valid memory cell data can be read by subsequent reading. If the operation fails, the DQ6 output toggles.

If an attempt is made to execute an Auto Program operation on a protected block, DQ6 will toggle for around 3 μs. It will then stop toggling. If an attempt is made to execute an auto erase operation on a protected block, DQ6 will toggle for around 100 μs. It will then stop toggling. After toggling has stopped the device will return to Read Mode.

DQ5 (internal time-out)

If the internal timer times out during a Program or Erase operation, DQ5 outputs a 1. This indicates that the operation has not been completed within the allotted time.

Any attempt to program a 1 into a cell containing a 0 will fail (see Auto-Program Mode). In this case DQ5 outputs a 1. Either a hardware reset or a software Reset command is required to return the device to Read Mode.

DQ3 (Block Erase timer)

The Block Erase operation starts 50 μs (the Erase Hold Time) after the rising edge of $\overline{WE}$ in the last command cycle. DQ3 outputs a 0 for the duration of the Block Erase Hold Time and a 1 when the Block Erase operation starts. Additional Block Erase commands can only be accepted during the Block Erase Hold Time. Each Block Erase command input within the hold time resets the timer, allowing additional blocks to be marked for erasing. DQ3 outputs a 1 if the Program or Erase operation fails.

DQ2 (Toggle bit 2)

DQ2 is used to indicate which blocks have been selected for Auto Block Erase or to indicate whether the device is in Erase Suspend Mode.

If data is read continuously from the selected block during an Auto Block Erase, the DQ2 output will toggle. Now 1 will be output from non-selected blocks; thus, the selected block can be ascertained. If data is read continuously from the block selected for Auto Block Erase while the device is in Erase Suspend Mode, the DQ2 output will toggle. Because the DQ6 output is not toggling, it can be determined that the device is in Erase Suspend Mode. If data is read from the address to which data is being written during Erase Suspend in Programming Mode, DQ2 will output a 1.

RY/$\overline{BY}$ (READY/$\overline{BUSY}$)

The TC58FVT160A/B160A has a RY/$\overline{BY}$ signal to indicate the device status to the host processor. A 0 (Busy state) indicates that an Auto-Program or auto-erase operation is in progress. A 1 (Ready state) indicates that the operation has finished and that the device can now accept a new command. RY/$\overline{BY}$ outputs a 0 when an operation has failed.

RY/$\overline{BY}$ outputs a 0 after the rising edge of $\overline{WE}$ in the last command cycle.

During an Auto Block Erase operation, commands other than Erase Suspend are ignored. RY/$\overline{BY}$ outputs a 1 during an Erase Suspend operation. The output buffer for the RY/$\overline{BY}$ pin is an open-drain type circuit, allowing a wired-OR connection. A pull-up resistor must be inserted between V_{DD} and the RY/$\overline{BY}$ pin.

DATA PROTECTION

The TC58FVT160/B160A includes a function which guards against malfunction or data corruption.

Protection against Program/Erase Caused by Low Supply Voltage

To prevent malfunction at power-on or power-down, the device will not accept commands while V_{DD} is below V_{LKO}. In this state, command input is ignored.

If V_{DD} drops below V_{LKO} during an Auto Operation, the device will terminate Auto-Program execution. In this case, Auto operation is not executed again when V_{DD} return to recommended V_{DD} voltage Therefore, command need to be input to execute Auto operation again.

When $V_{DD} > V_{LKO}$, make up countermeasure to be input accurately command in system side please.

Protection against Malfunction Caused by Glitches

To prevent malfunction during operation caused by noise from the system, the device will not accept pulses shorter than 3 ns (Typ.) input on $\overline{WE}$, $\overline{CE}$ or $\overline{OE}$. However, if a glitch exceeding 3 ns (Typ.) occurs and the glitch is input to the device malfunction may occur.

The device uses standard JEDEC commands. It is conceivable that, in extreme cases, system noise may be misinterpreted as part of a command sequence input and that the device will acknowledge it. Then, even if a proper command is input, the device may not operate. To avoid this possibility, clear the Command Register before command input. In an environment prone to system noise, Toshiba recommend input of a software or hardware reset before command input.

Protection against Malfunction at Power-on

To prevent damage to data caused by sudden noise at power-on, when power is turned on with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IL}$, the device does not latch the command on the first rising edge of $\overline{WE}$ or $\overline{CE}$. Instead, the device automatically Resets the Command Register and enters Read Mode.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RANGE	UNIT
V_{DD}	V_{DD} Supply Voltage	−0.6~4.6	V
V_{IN}	Input Voltage	−0.6~V_{DD} + 0.5 (≤ 4.6)	V
V_{DQ}	Input/Output Voltage	−0.6~V_{DD} + 0.5 (≤ 4.6)	V
V_{IDH}	Maximum Input Voltage for A9, $\overline{OE}$ and $\overline{RESET}$	13.0	V
P_D	Power Dissipation	126	mW
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	−40~85	°C
I_{OSHORT}	Output Short-Circuit Current(1)	100	mA

(1) Outputs should be shorted for no more than one second.
No more than one output should be shorted at a time.

CAPACITANCE (Ta = 25°C, f = 1 MHz)

TSOPI

SYMBOL	PARAMETER	CONDITION	MAX	UNIT
C_{IN}	Input Pin Capacitance	V_{IN} = 0 V	4	pF
C_{OUT}	Output Pin Capacitance	V_{OUT} = 0 V	8	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0 V	7	pF

This parameter is periodically sampled and is not tested for every device.

TFBGA

SYMBOL	PARAMETER	CONDITION	MAX	UNIT
C_{IN}	Input Pin Capacitance	V_{IN} = 0 V	4	pF
C_{OUT}	Output Pin Capacitance	V_{OUT} = 0 V	8	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0 V	7	pF

This parameter is periodically sampled and is not tested for every device.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DD}	V_{DD} Supply Voltage	2.7	3.6	V
V_{IH}	Input High-Level Voltage	0.7 × V_{DD}	V_{DD} + 0.3(2)	
V_{IL}	Input Low-Level Voltage	−0.3(1)	0.2 × V_{DD}	
V_{ID}	High-Level Voltage for A9, $\overline{OE}$ and $\overline{RESET}$ (3)	11.4	12.6	
Ta	Operating Temperature	−40	85	°C

(1) −2 V (pulse width of 20 ns max)

(2) +2 V (pulse width of 20 ns max)

(3) Do not apply V_{ID} when the supply voltage is not within the device's recommended operating voltage range.

DC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	$0 V \le V_{IN} \le V_{DD}$	—	±1	μA
I_{LO}	Output Leakage Current	$0 V \le V_{OUT} \le V_{DD}$	—	±1	
V_{OH}	Output High Voltage	$I_{OH} = -0.1$ mA	$V_{DD} - 0.4$	—	V
		$I_{OH} = -2.5$ mA	$0.85 \times V_{DD}$	—	
V_{OL}	Output Low Voltage	$I_{OL} = 4.0$ mA	—	0.4	
I_{DDO1}	V_{DD} Average Read Current	$V_{IN} = V_{IH}/V_{IL}$, $I_{OUT} = 0$ mA $t_{CYCLE} = t_{RC} = 100$ ns	—	30	mA
I_{DDO2}	V_{DD} Average Program Current	$V_{IN} = V_{IH}/V_{IL}$, $I_{OUT} = 0$ mA	—	15	
I_{DDO3}	V_{DD} Average Erase Current	$V_{IN} = V_{IH}/V_{IL}$, $I_{OUT} = 0$ mA	—	15	
I_{DDO4}	V_{DD} Average Program-while-Erase-Suspend Current	$V_{IN} = V_{IH}/V_{IL}$, $I_{OUT} = 0$ mA	—	15	
I_{DDS1}	V_{DD} Standby Current	$\overline{CE} = \overline{RESET} = V_{DD}$ or $\overline{RESET} = V_{SS}V$	—	5	μA
I_{DDS2}	V_{DD} Standby Current (Automatic Sleep Mode(1))	$V_{IH} = V_{DD}$ $V_{IL} = V_{SS}$	—	5	
I_{ID}	High-Voltage Input Current for A9, $\overline{OE}$ and $\overline{RESET}$	$11.4 V \le V_{ID} \le 12.6 V$	—	35	
V_{LKO}	Low-V_{DD} Lock-out Voltage	—	2.3	2.5	V

(1) The device enters Automatic Sleep Mode in which the address remains fixed for during 150 ns.

AC TEST CONDITIONS

PARAMETER	CONDITION
Input Pulse Level	V_{DD}, 0.0 V
Input Pulse Rise and Fall Time (10%~90%)	5 ns
Timing Measurement Reference Level (input)	1.5 V, 1.5 V
Timing Measurement Reference Level (output)	1.5 V, 1.5 V
Output Load	C_L (100 pF) + 1 TTL Gate / C_L (30 pF) + 1 TTL Gate

AC CHARACTERISTICS AND OPERATING CONDITIONS

READ CYCLE

		PRODUCT NAME	−70				−10		
		OUTPUT CAPACITANCE LOAD (C_L)	30 pF		100 pF				
SYMBOL	PARAMETER		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t_{RC}	Read Cycle Time		70	—	80	—	100	—	ns
t_{ACC}	Address Access Time		—	70	—	80	—	100	ns
t_{CE}	$\overline{CE}$ Access Time		—	70	—	80	—	100	ns
t_{OE}	$\overline{OE}$ Access Time		—	30	—	35	—	40	ns
t_{CEE}	$\overline{CE}$ to Output Low-Z		0	—	0	—	0	—	ns
t_{OEE}	$\overline{OE}$ to Output Low-Z		0	—	0	—	0	—	ns
t_{OH}	Output Data Hold Time		0	—	0	—	0	—	ns
t_{DF1}	$\overline{CE}$ to Output High-Z		—	20	—	25	—	30	ns
t_{DF2}	$\overline{OE}$ to Output High-Z		—	20	—	25	—	30	ns

BLOCK PROTECT

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{VPT}	V_{ID} Transition Time	4	—	µs
t_{VPS}	V_{ID} Set-up Time	4	—	µs
t_{CESP}	$\overline{CE}$ Set-up Time	4	—	µs
t_{VPH}	$\overline{OE}$ Hold Time	4	—	µs
t_{PPLH}	$\overline{WE}$ Low-Level Hold Time	100	—	µs

PROGRAM AND ERASE CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
t_{PPW}	Auto-Program Time (Byte Mode)	—	8	300	µs
	Auto-Program Time (Word Mode)	—	11	300	µs
t_{PCEW}	Auto Chip Erase Time	—	25	350	s
t_{PBEW}	Auto Block Erase Time	—	0.7	10	s
t_{EW}	Erase/Program Cycle	10^5	—	—	Cycles

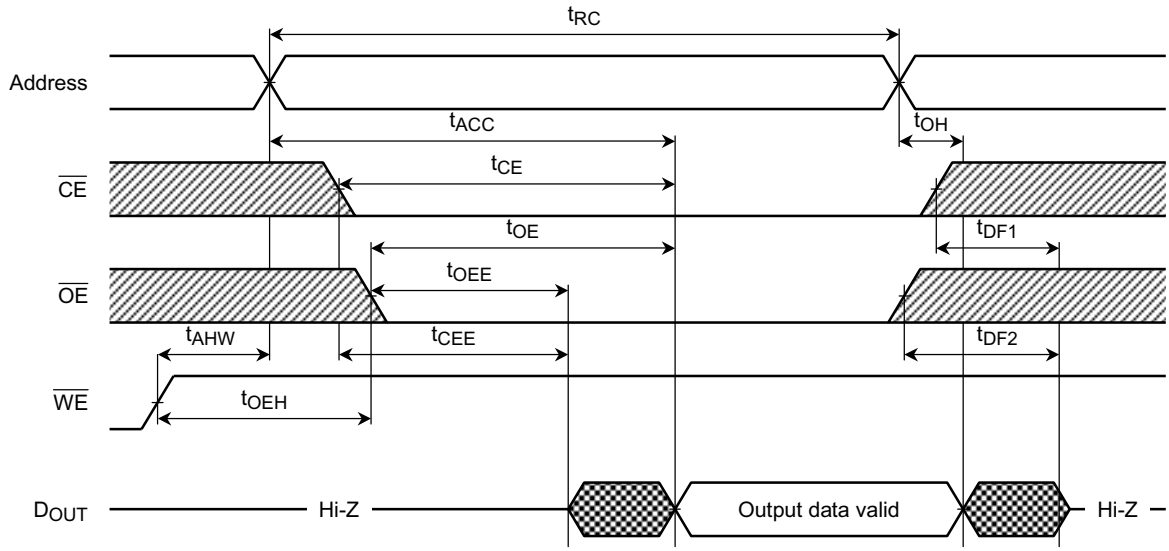
COMMAND WRITE/PROGRAM/ERASE CYCLE

SYMBOL	PARAMETER	−70		−10		UNIT
		MIN	MAX	MIN	MAX	
t_{CMD}	Command Write Cycle Time	70	—	100	—	ns
t_{AS}	Address Set-up Time / $\overline{BYTE}$ Set-up Time	0	—	0	—	ns
t_{AH}	Address Hold Time / $\overline{BYTE}$ Hold Time	35	—	50	—	ns
t_{AHW}	Address Hold Time from $\overline{WE}$ High level	20	—	20	—	ns
t_{DS}	Data Set-up Time	35	—	50	—	ns
t_{DH}	Data Hold Time	0	—	0	—	ns
t_{WELH}	$\overline{WE}$ Low-Level Hold Time ($\overline{WE}$ Control)	35	—	50	—	ns
t_{WEHH}	$\overline{WE}$ High-Level Hold Time ($\overline{WE}$ Control)	20	—	20	—	ns
t_{CES}	$\overline{CE}$ Set-up Time to $\overline{WE}$ Active ($\overline{WE}$ Control)	0	—	0	—	ns
t_{CEH}	$\overline{CE}$ Hold Time from $\overline{WE}$ High Level ($\overline{WE}$ Control)	0	—	0	—	ns
t_{CELH}	$\overline{CE}$ Low-Level Hold Time ($\overline{CE}$ Control)	35	—	50	—	ns
t_{CEHH}	$\overline{CE}$ High-Level Hold Time ($\overline{CE}$ Control)	20	—	20	—	ns
t_{CHW}	$\overline{CE}$ Hold Time from $\overline{WE}$ High Level	20	—	20	—	ns
t_{WES}	$\overline{WE}$ Set-up time to $\overline{CE}$ Active ($\overline{CE}$ Control)	0	—	0	—	ns
t_{WEH}	$\overline{WE}$ Hold Time from $\overline{CE}$ High Level ($\overline{CE}$ Control)	0	—	0	—	ns
t_{OES}	$\overline{OE}$ Set-up Time	0	—	0	—	ns
t_{OEHP}	$\overline{OE}$ Hold Time (Toggle, Data Polling)	90	—	90	—	ns
t_{OEHT}	$\overline{OE}$ High-Level Hold Time (Toggle)	20	—	20	—	ns
t_{BEH}	Erase Hold Time	50	—	50	—	µs
t_{VDS}	V_{DD} Set-up Time	500	—	500	—	µs
t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay	—	90	—	90	ns
	Program/Erase Valid to RY/$\overline{BY}$ Delay during Suspend Mode	—	300	—	300	ns
t_{RP}	$\overline{RESET}$ Low-Level Hold Time	500	—	500	—	ns
t_{READY}	$\overline{RESET}$ Low-Level to Read Mode	—	20	—	20	µs
t_{RB}	RY/$\overline{BY}$ Recovery Time	0	—	0	—	ns
t_{RH}	$\overline{RESET}$ Recovery Time	50	—	50	—	ns
t_{CEBTS}	$\overline{CE}$ Set-up time $\overline{BYTE}$ Transition	5	—	5	—	ns
t_{BTD}	$\overline{BYTE}$ to Output High-Z	—	30	—	30	ns
t_{SUSP}	Program Suspend Command to Suspend Mode	—	1.5	—	1.5	µs
t_{RESP}	Program Resume Command to Program Mode	—	1	—	1	µs
t_{SUSE}	Erase Suspend Command to Suspend Mode	—	15	—	15	µs
t_{RESE}	Erase Resume Command to Erase Mode	—	1	—	1	µs

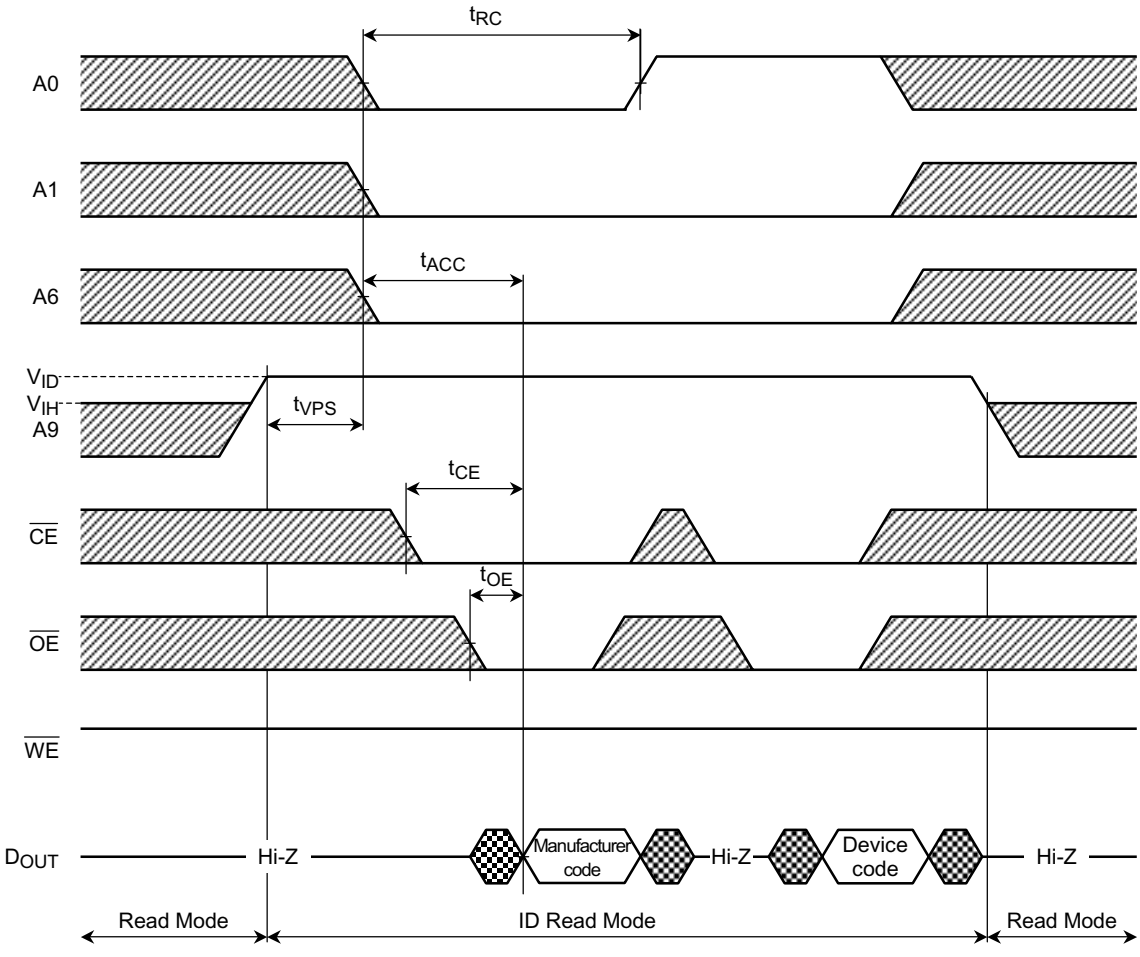
TIMING DIAGRAMS

V_{IH} or V_{IL} Data invalid

Read / ID Read Operation



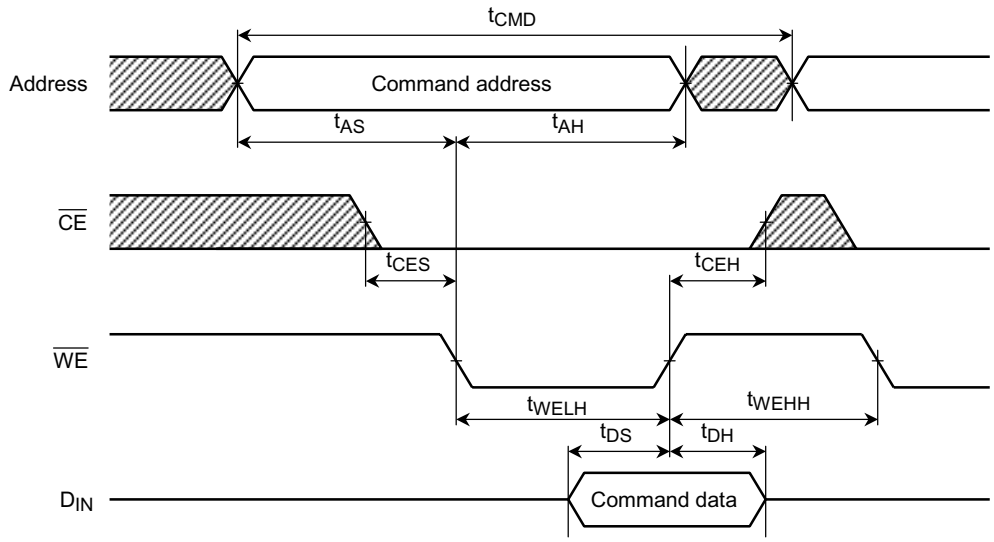
ID Read Operation (apply V_{ID} to A9)



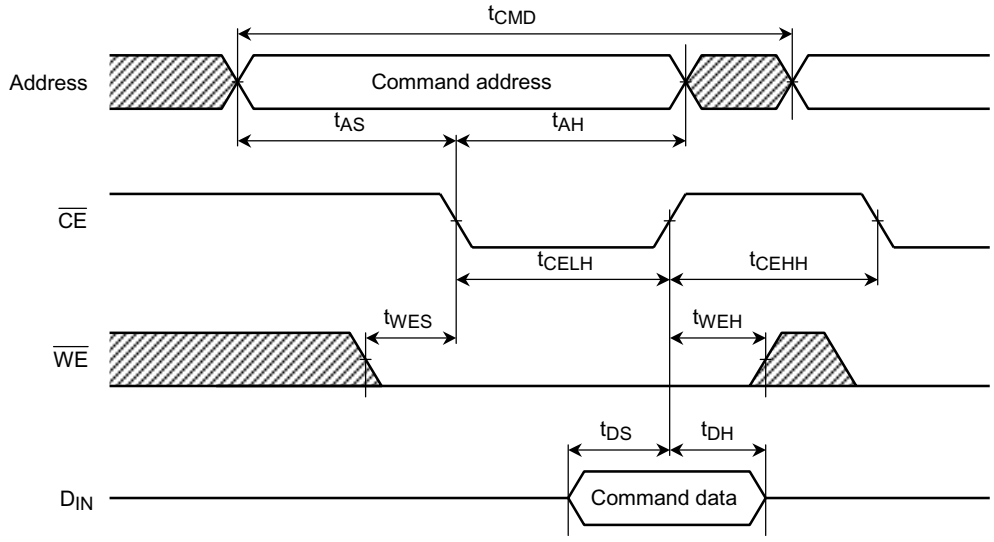
Command Write Operation

This is the timing of the Command Write Operation. The timing which is described in the following pages is essentially the same as the timing shown on this page.

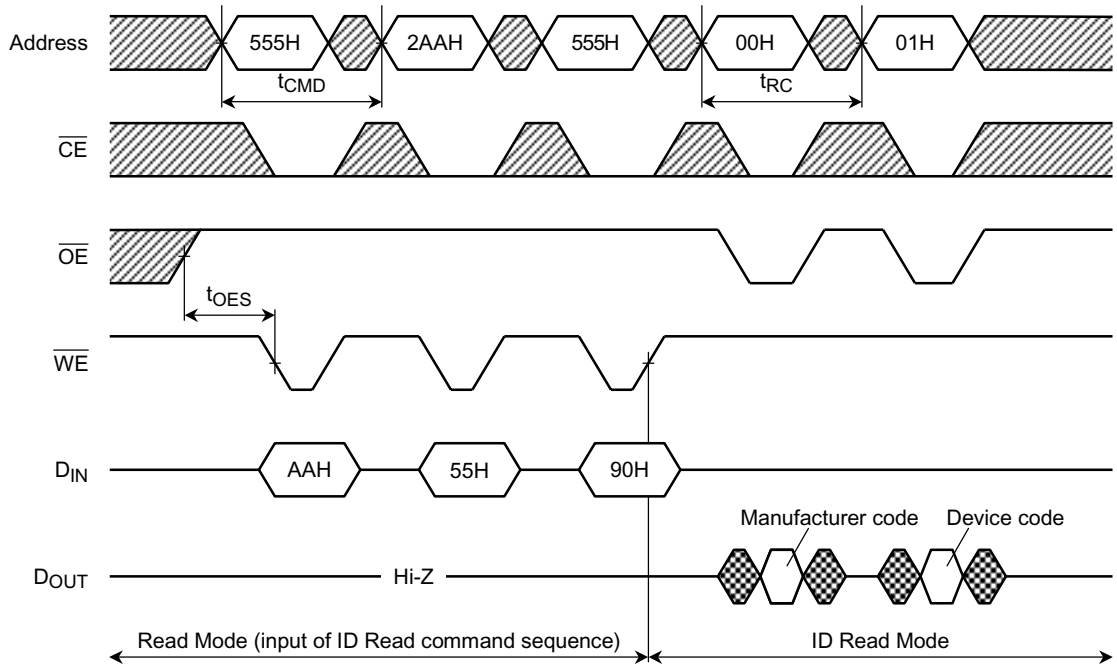
- $\overline{WE}$ Control



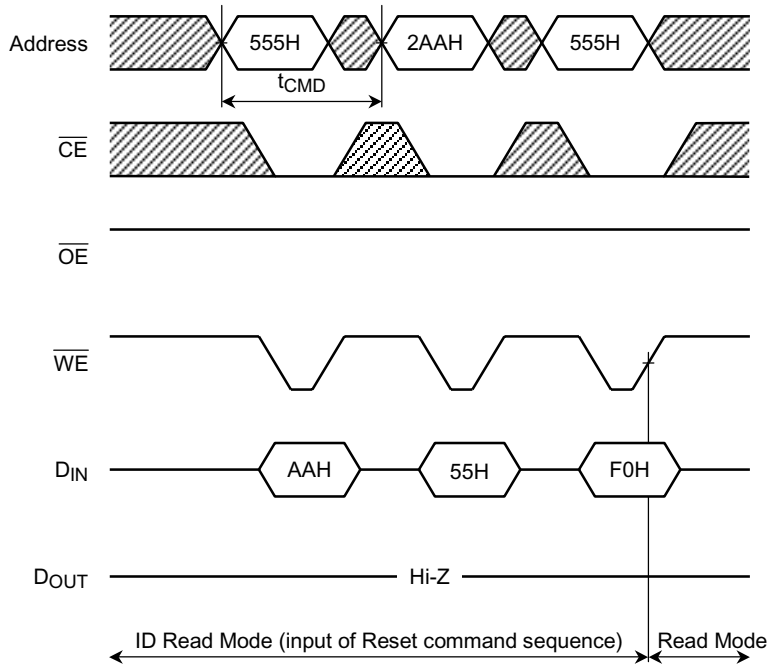
- $\overline{CE}$ Control



ID Read Operation (input command sequence)

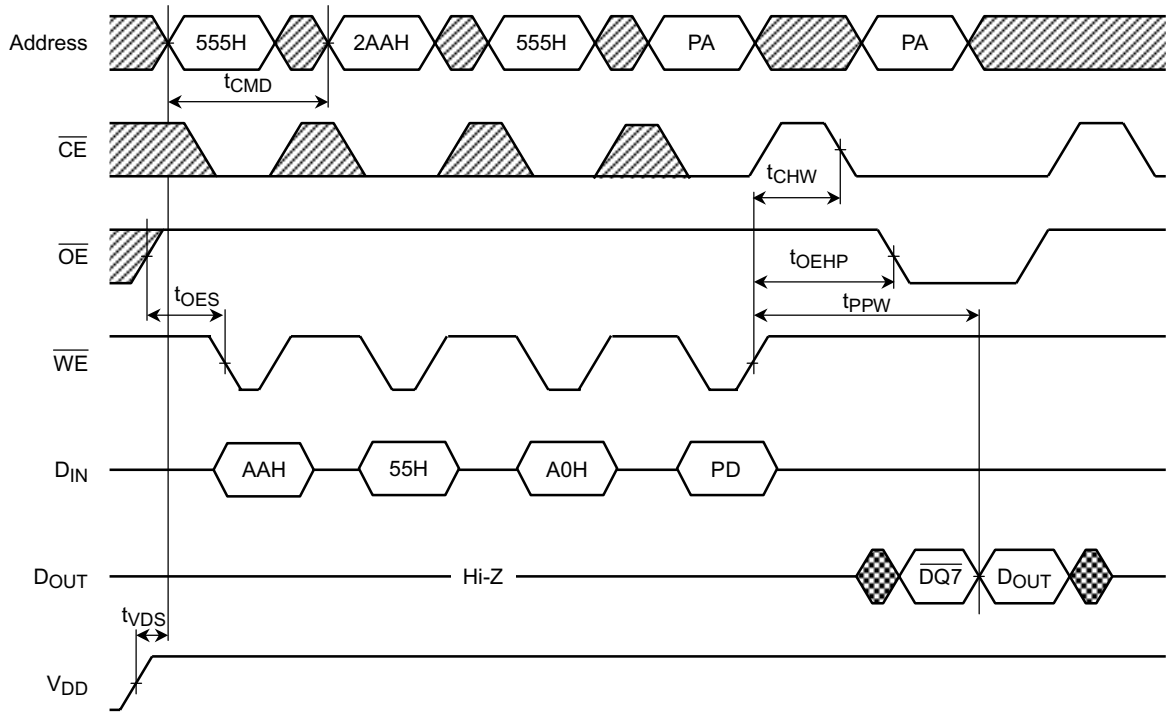


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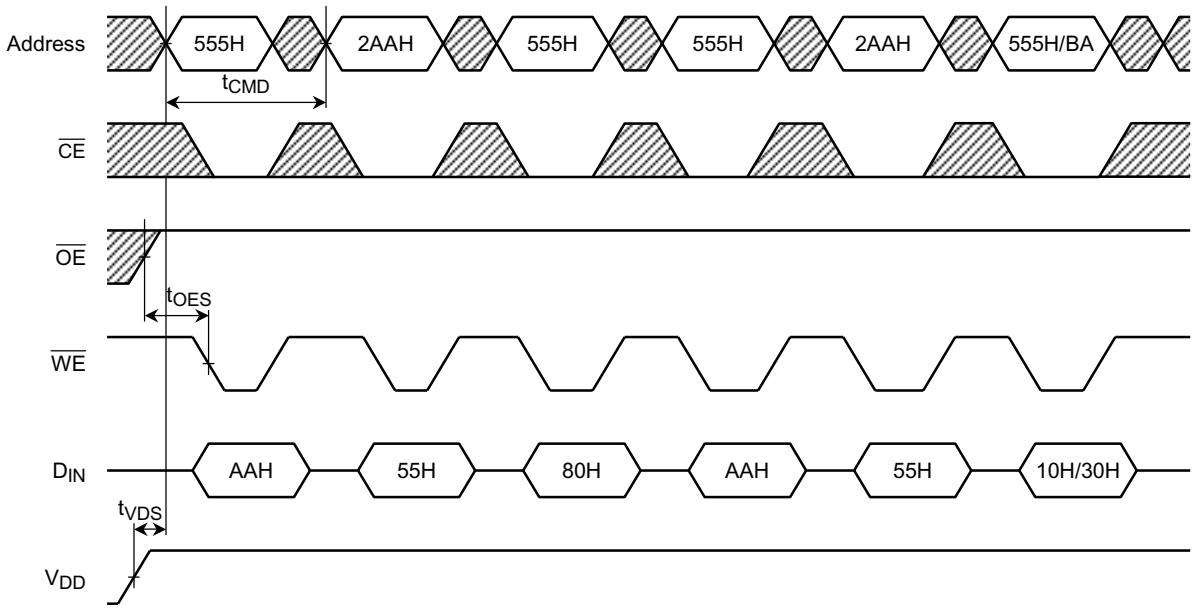
Note: Word Mode address shown.

Auto-Program Operation ($\overline{WE}$ Control)



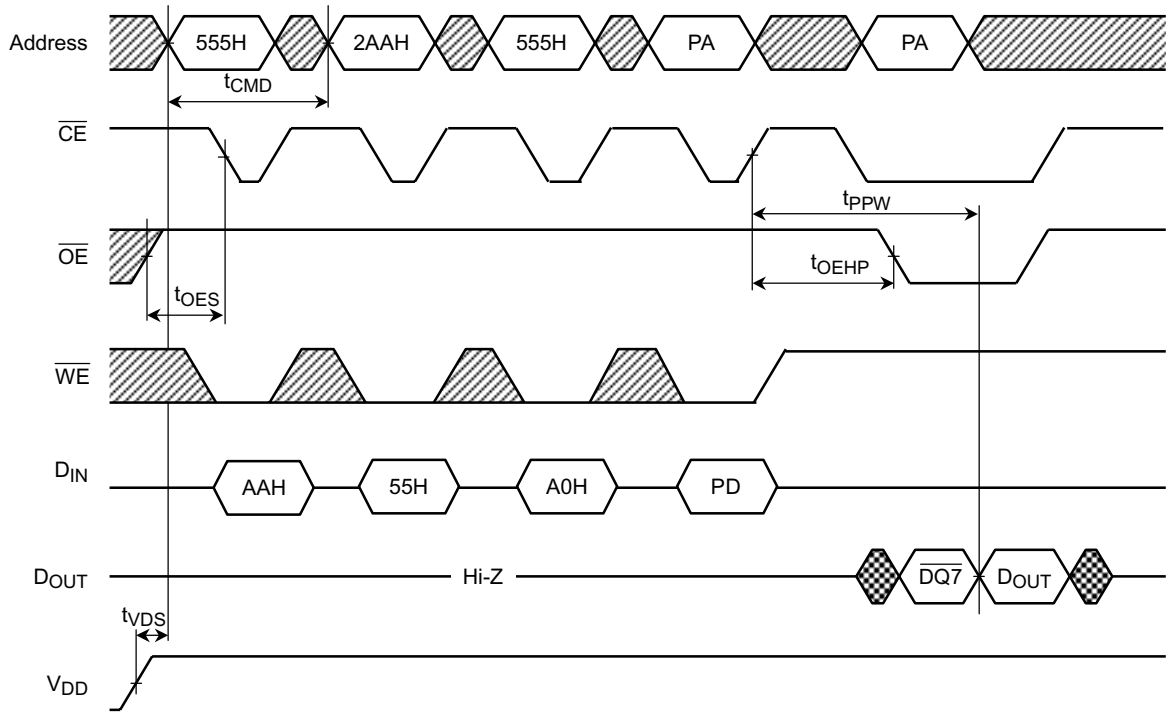
Note: Word Mode address shown.
PA: Program address
PD: Program data

Auto Chip Erase / Auto Block Erase Operation ($\overline{WE}$ Control)



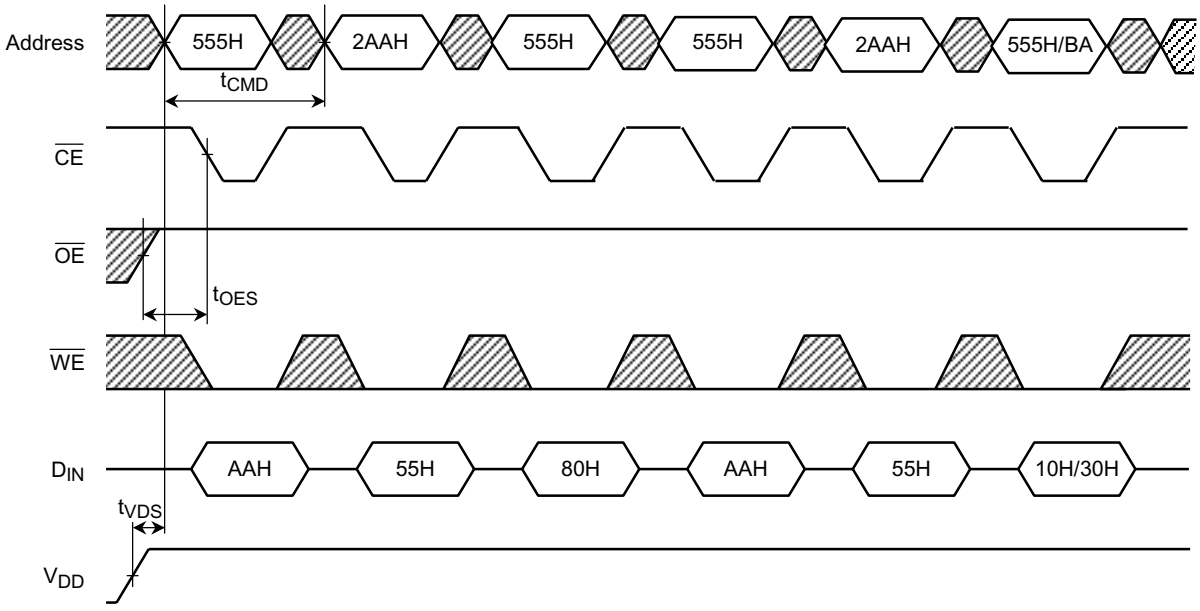
Note: Word Mode address shown.
BA: Block address for Auto Block Erase operation

Auto-Program Operation ($\overline{CE}$ Control)



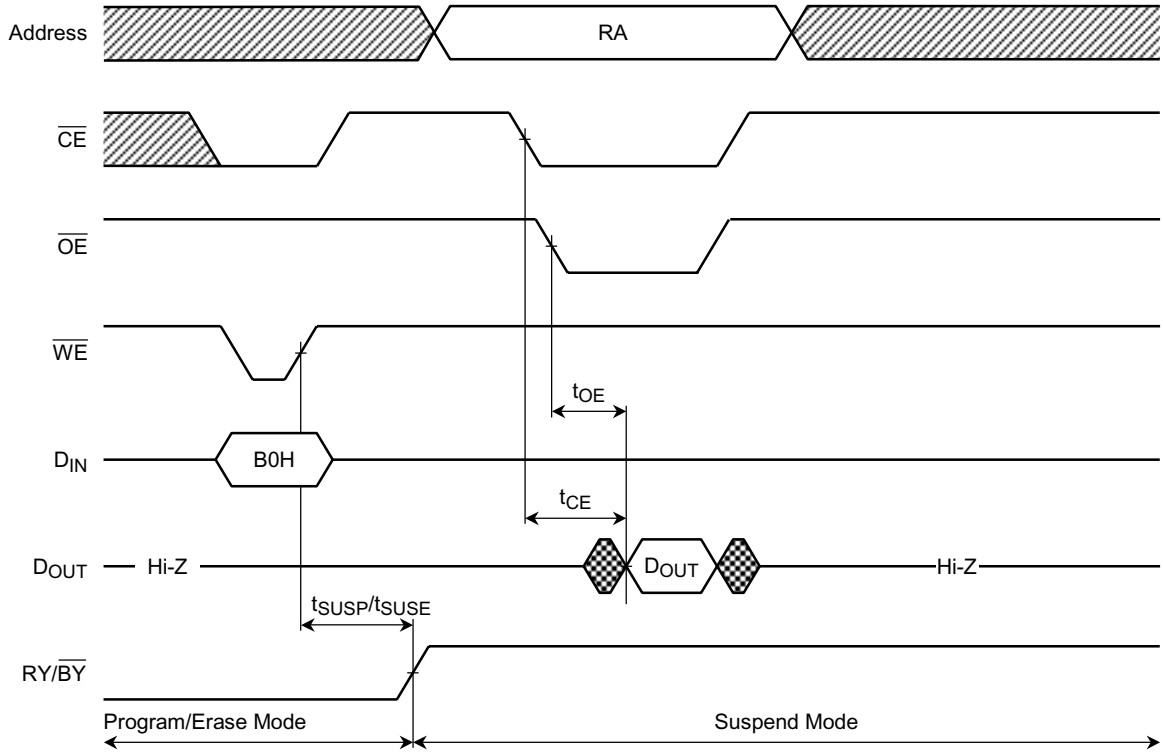
Note: Word Mode address shown.
PA: Program address
PD: Program data

Auto Chip Erase / Auto Block Erase Operation ($\overline{CE}$ Control)



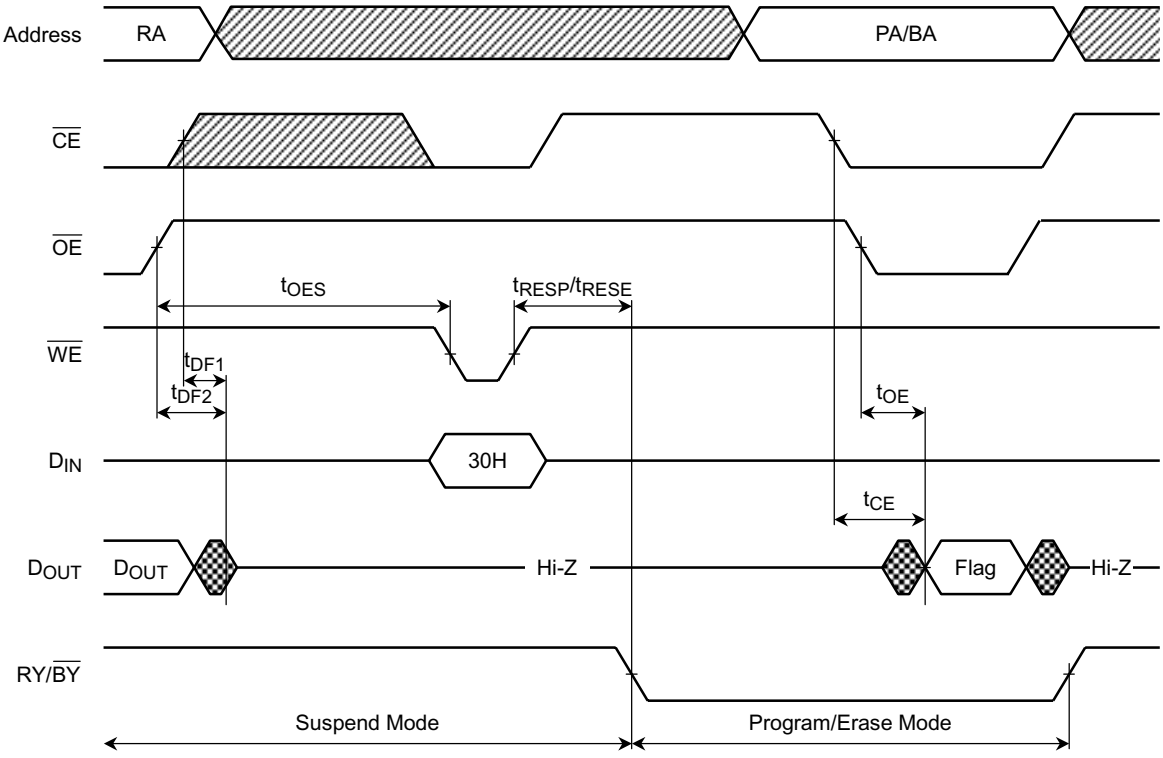
Note: Word Mode address shown.
BA: Block address for Auto Block Erase operation

Program/Erase Suspend Operation



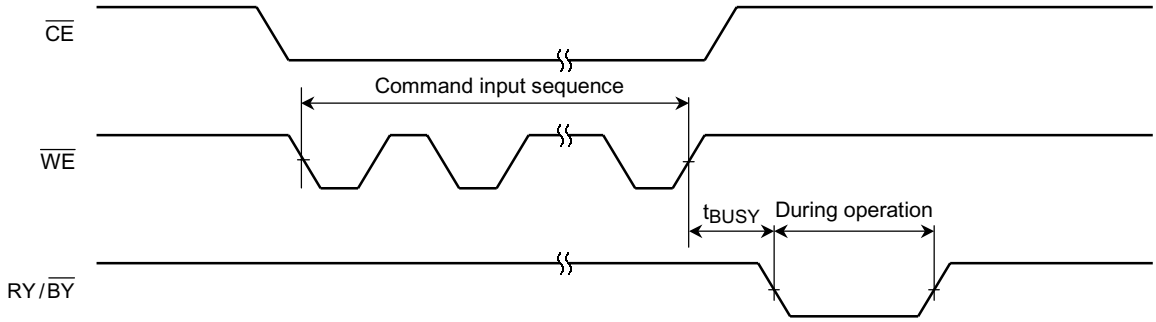
RA: Read address

Program/Erase Resume Operation

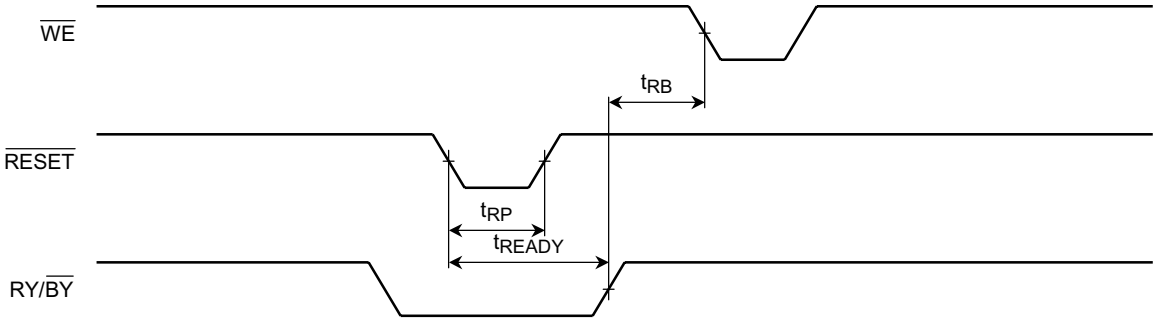


PA: Program address
BA: Block address
RA: Read address
Flag: Hardware Sequence flag

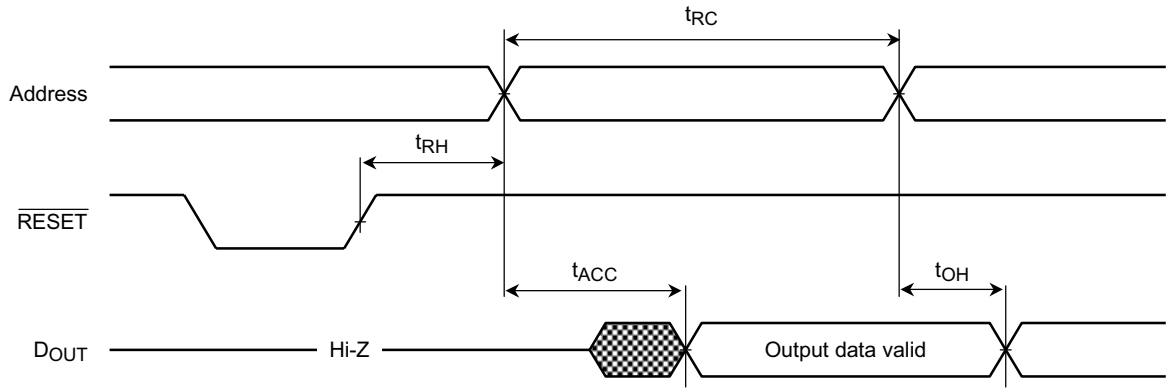
RY/$\overline{BY}$ during Auto Program/Erase Operation



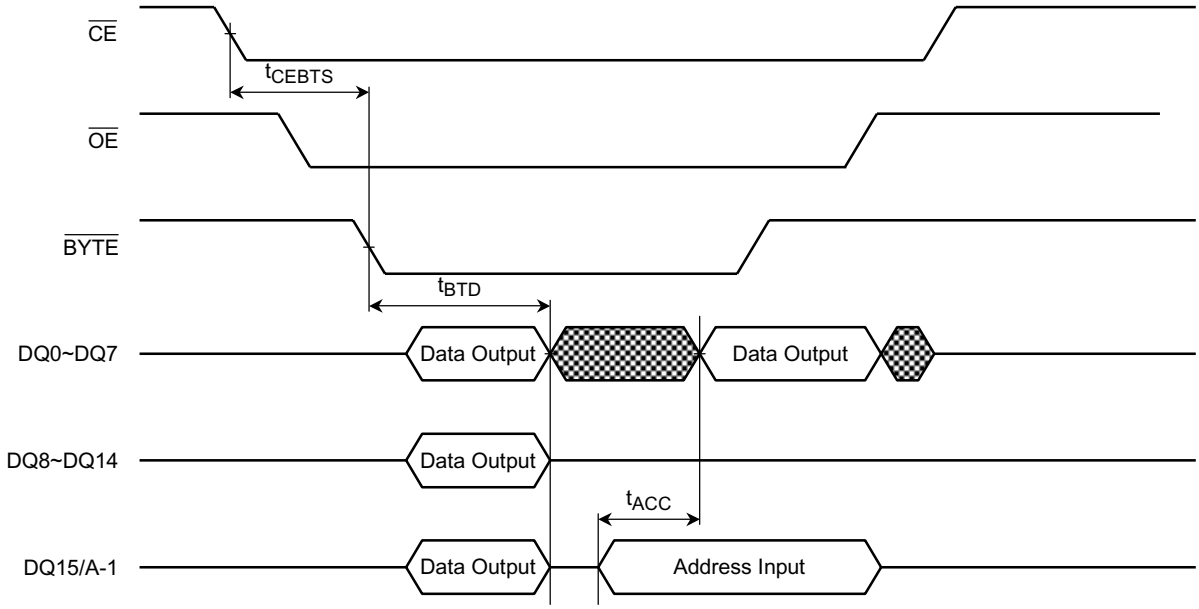
Hardware Reset Operation



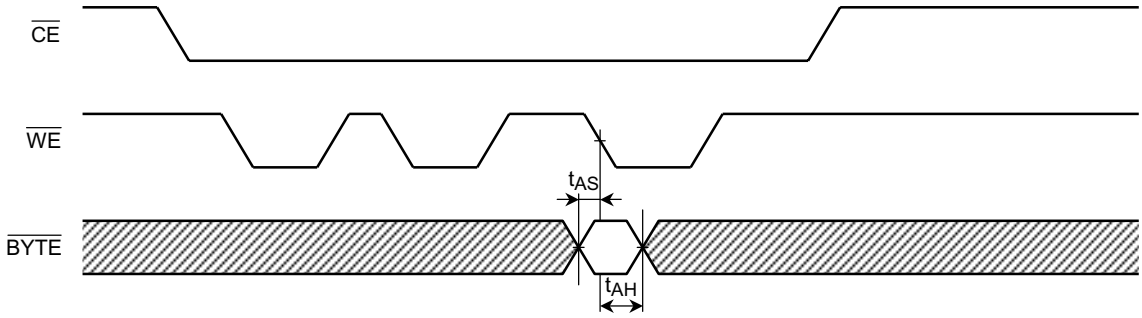
Read after $\overline{RESET}$



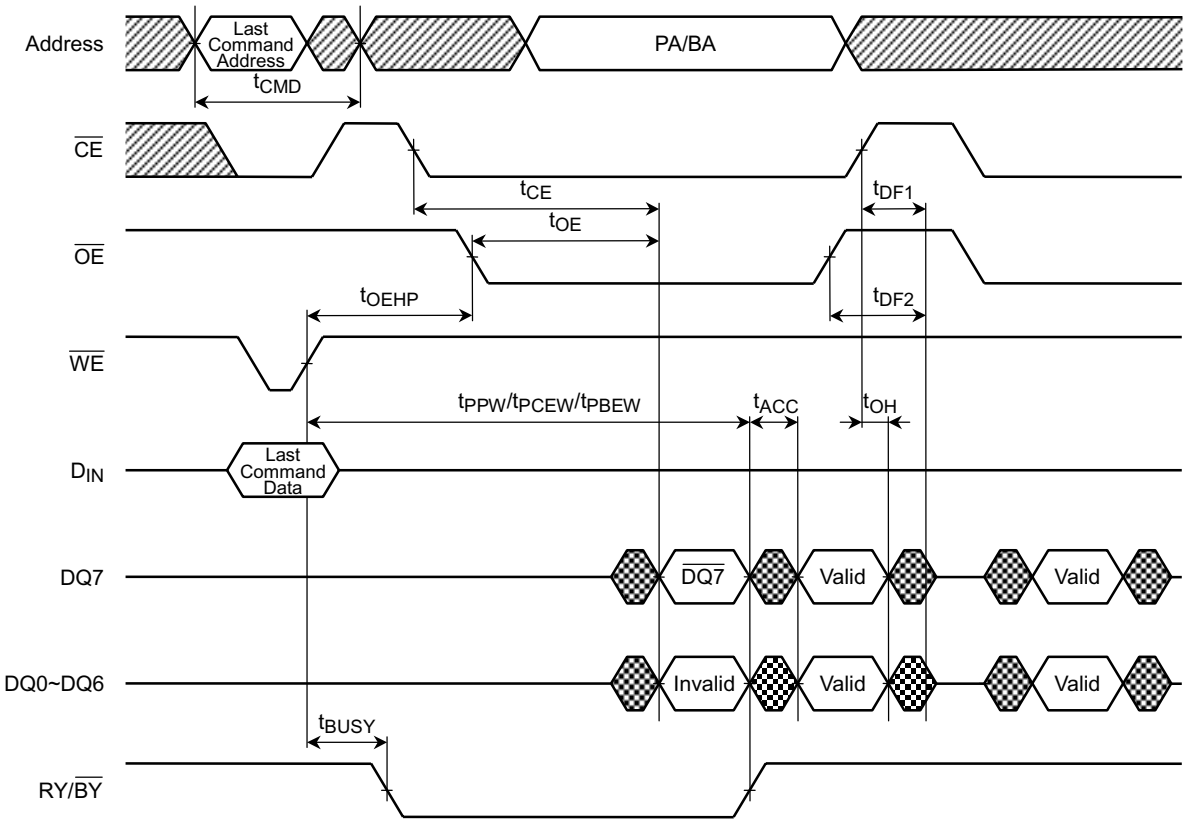
$\overline{\text{BYTE}}$ during Read Operation



$\overline{\text{BYTE}}$ during Write Operation

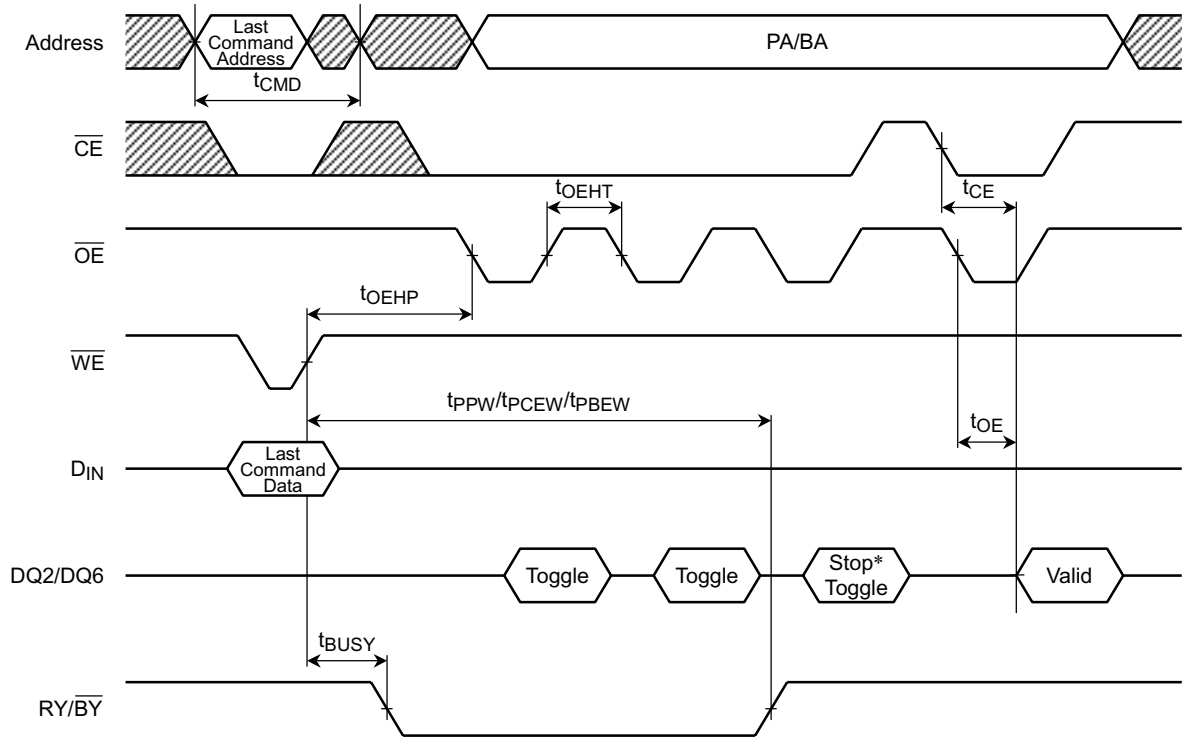


Hardware Sequence Flag ($\overline{\text{DATA}}$ Polling)



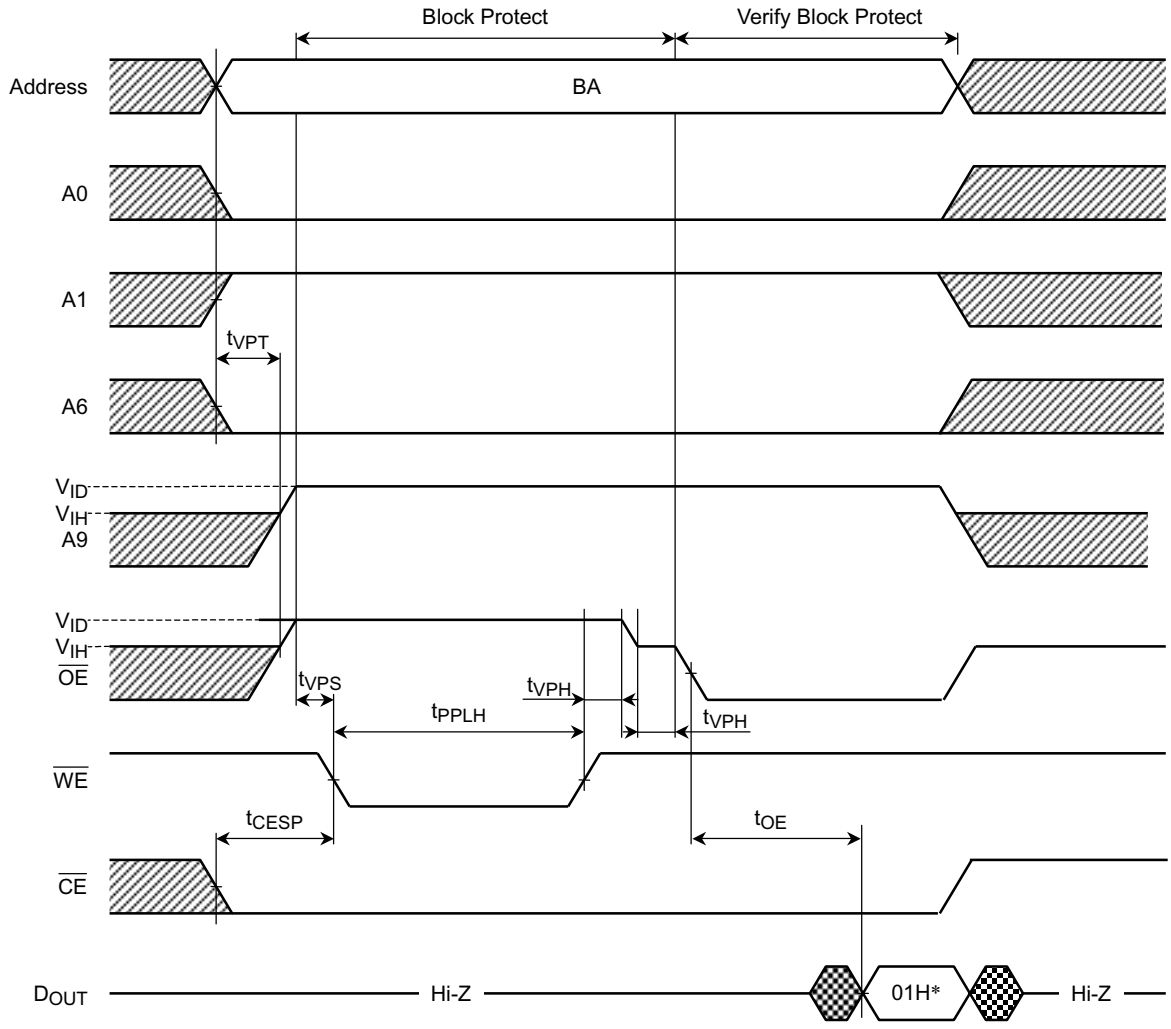
PA: Program address
BA: Block address

Hardware Sequence Flag (Toggle bit)



PA: Program address
BA: Block address
*DQ2/DQ6 stops toggling when auto operation has been completed.

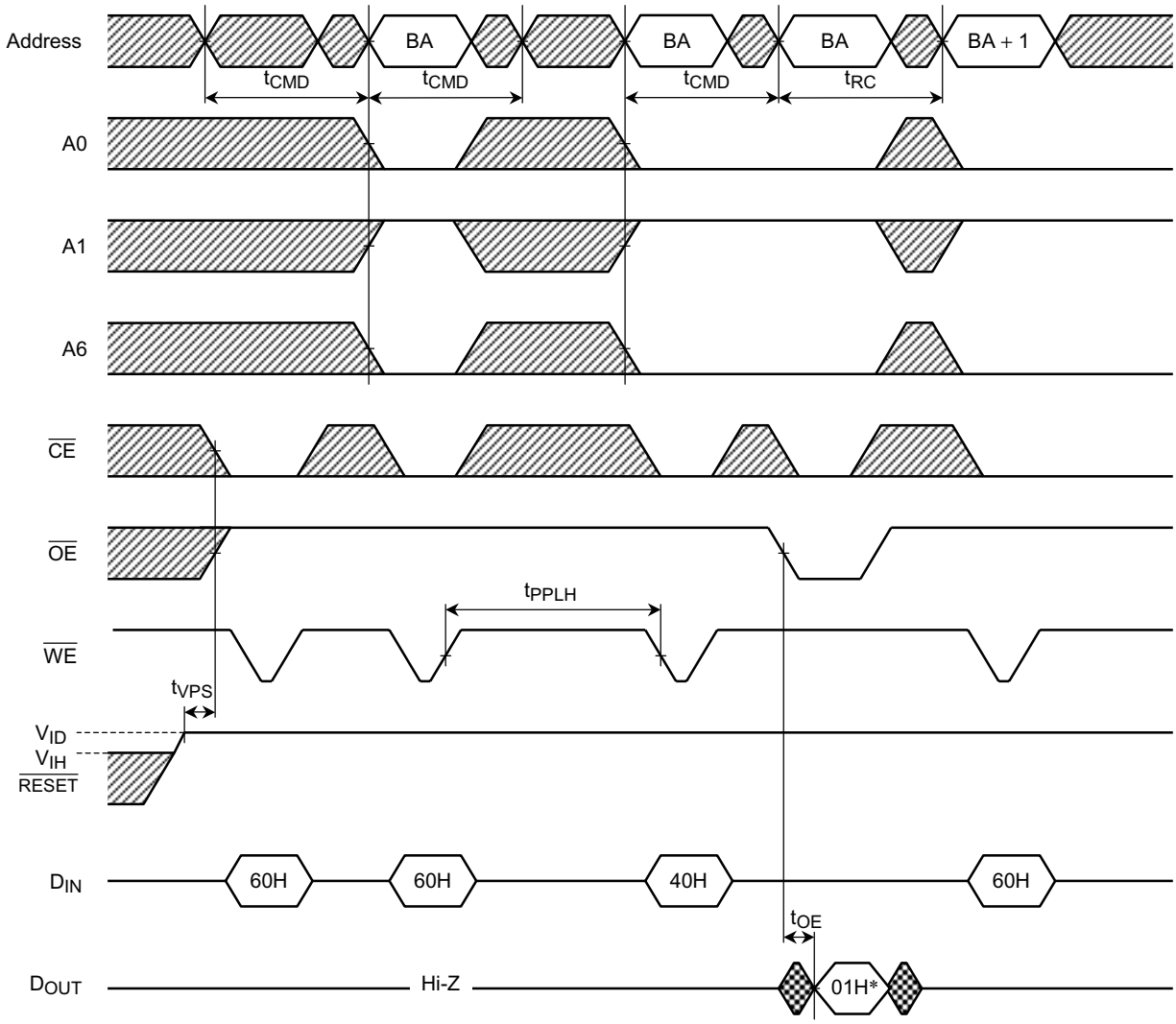
Block Protect 1 Operation



BA: Block address

*: 01H indicates that block is protected.

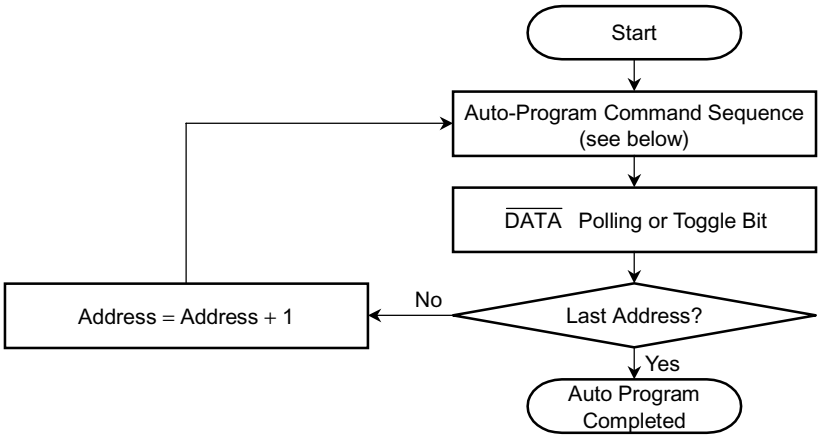
Block Protect 2 Operation



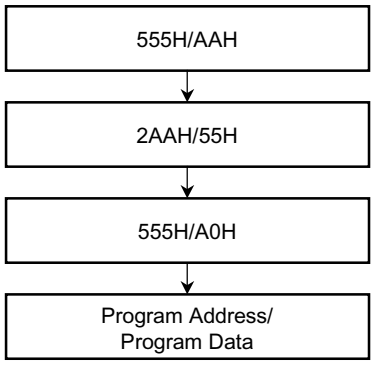
BA: Block address
BA + 1: Address of next block
*: 01H indicates that block is protected.

FLOWCHARTS

Auto Program

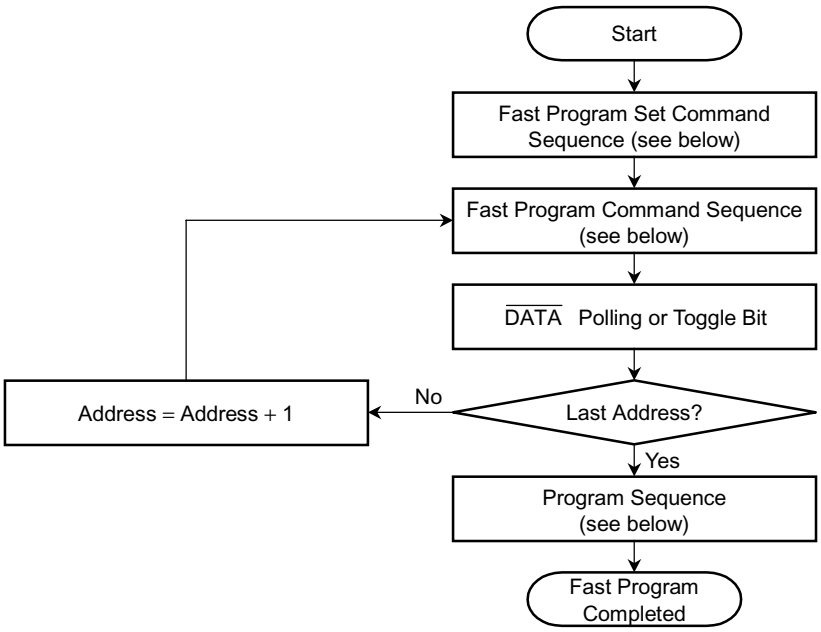


Auto-Program Command Sequence (address/data)

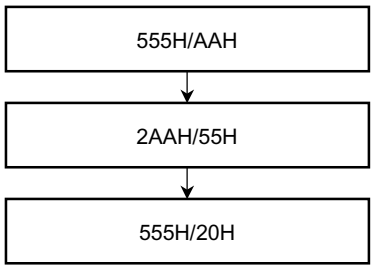


Note: The above command sequence takes place in Word Mode.

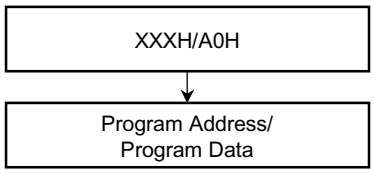
Fast Program



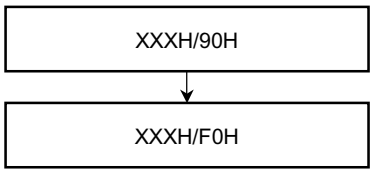
Fast Program Set Command Sequence (Address/Data)



Fast Program Command Sequence (Address/Data)

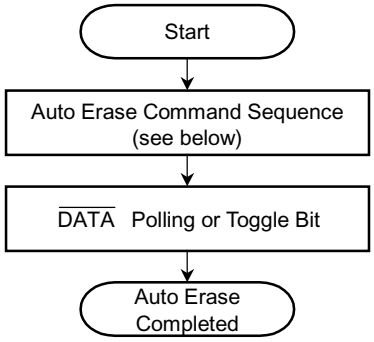


Fast Program Reset Command Sequence (Address/Data)

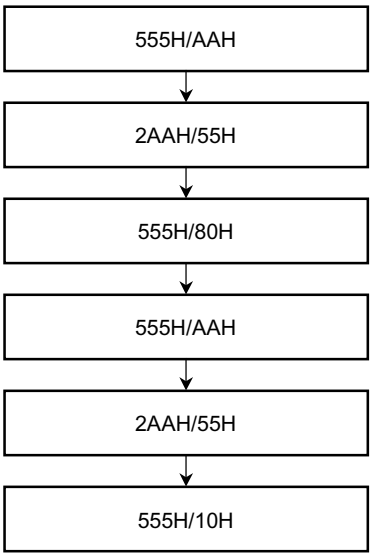


Note: The above command sequence takes place in word mode.

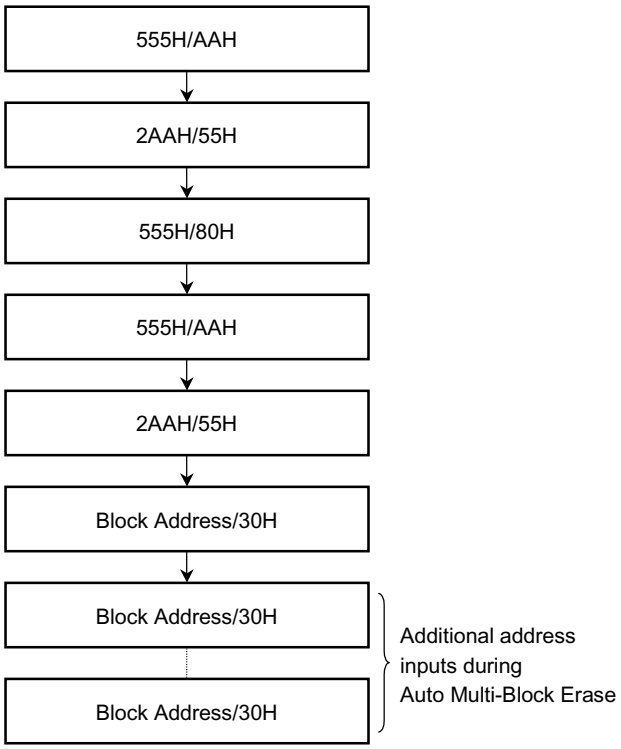
Auto Erase



Auto Chip Erase Command Sequence
(address/data)

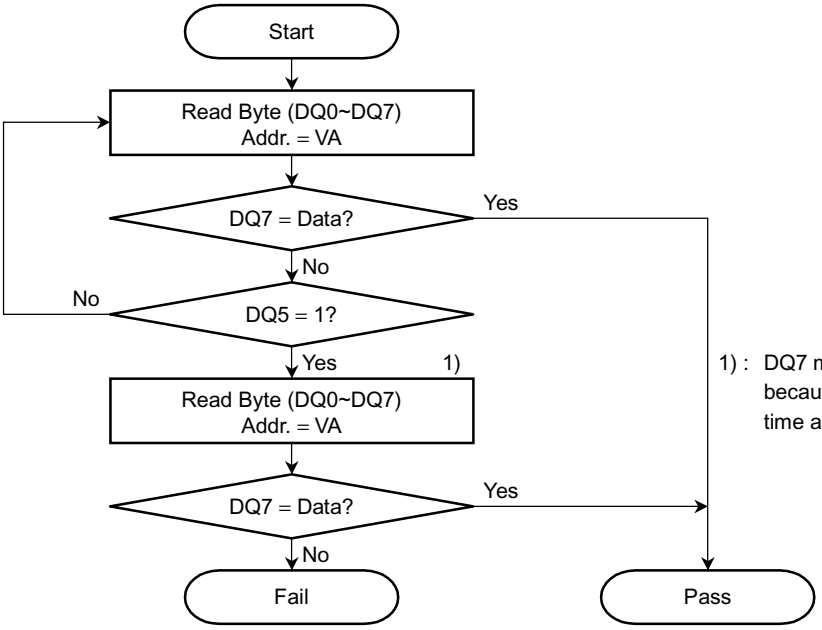


Auto Block / Auto-Multi Block Erase Command Sequence
(address/data)



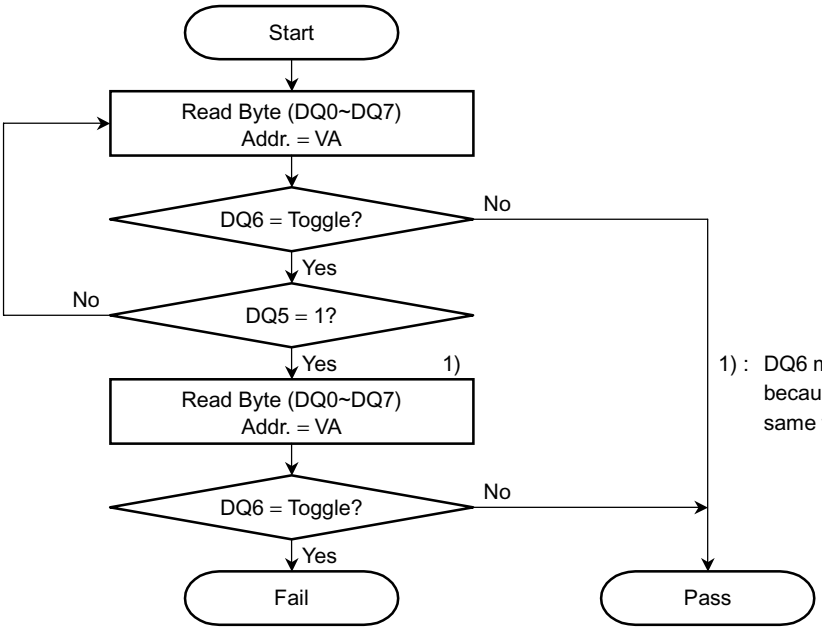
Note: The above command sequence takes place in Word Mode.

DQ7 $\overline{\text{DATA}}$ Polling



1) : DQ7 must be rechecked even if DQ5 = 1 because DQ7 may change at the same time as DQ5.

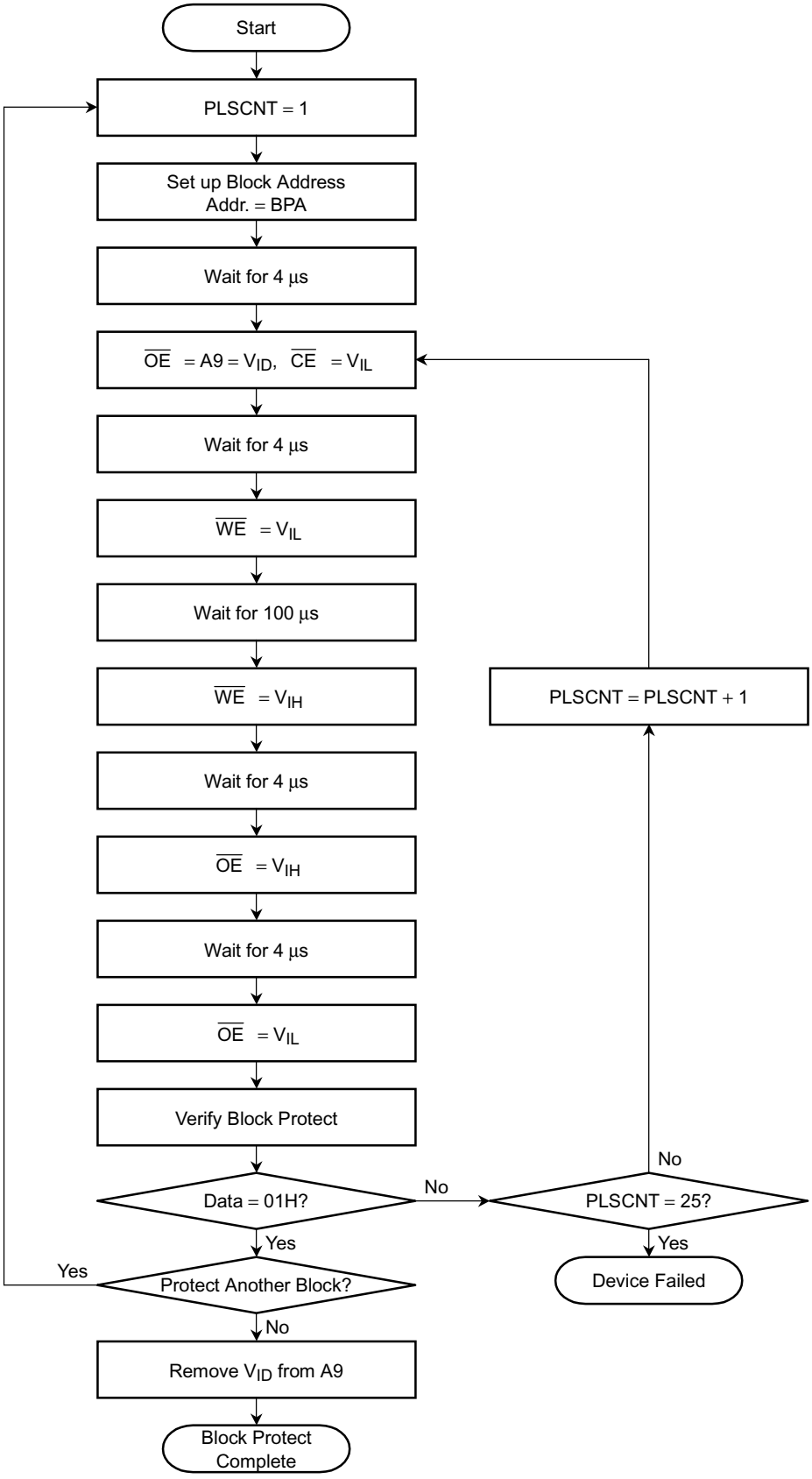
DQ6 Toggle Bit



1) : DQ6 must be rechecked even if DQ5 = 1 because DQ6 may stop toggling at the same time that DQ5 changes to 1.

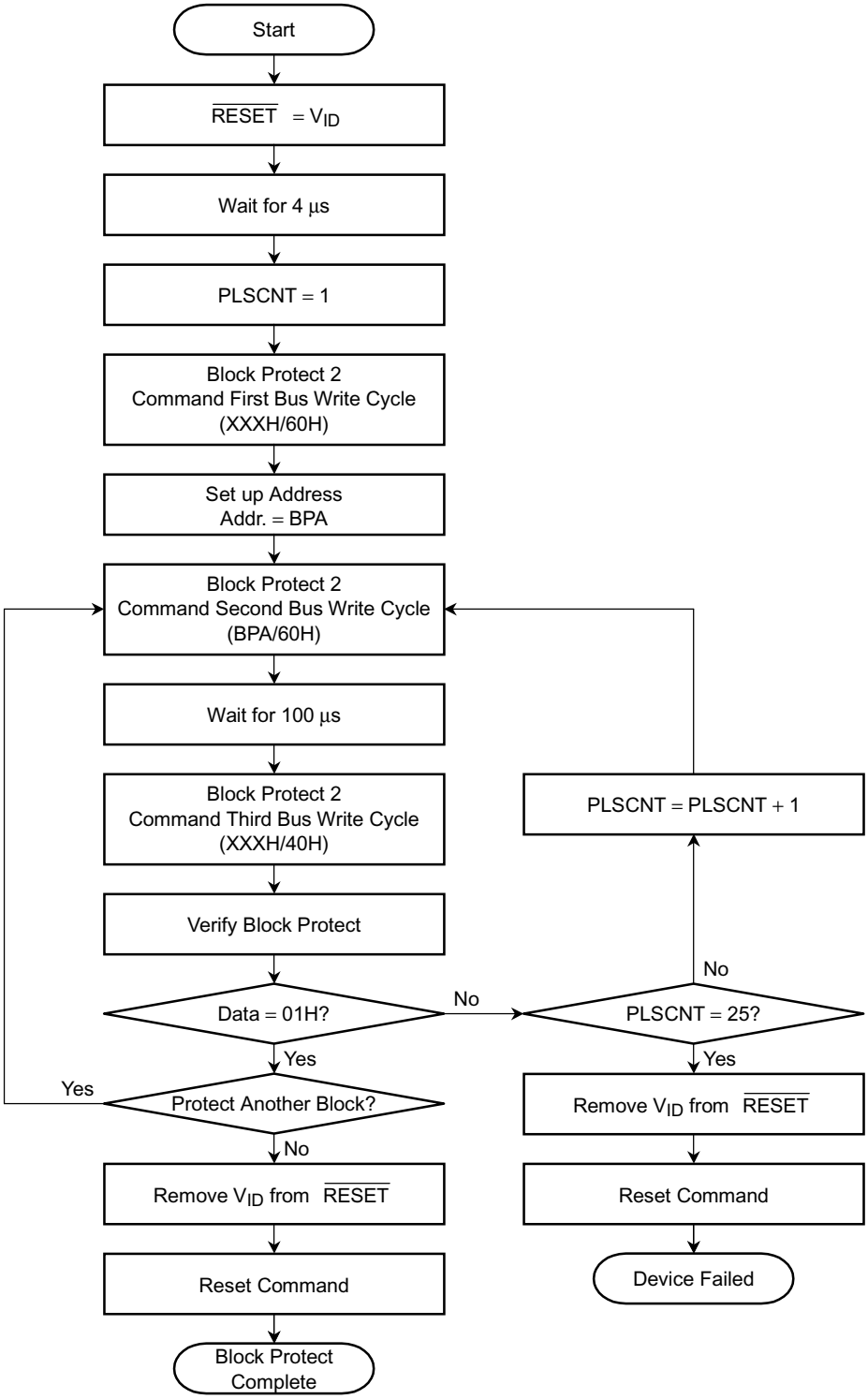
VA: Byte address for programming
Any of the addresses within the block being erased during a Block Erase operation
"Don't care" during a Chip Erase operation
Any address not within the current block during an Erase Suspend operation

Block Protect 1



BPA: Block Address and ID Read Address (A6, A1, A0)
ID Read Address = (0, 1, 0)

Block Protect 2



BPA: Block Address and ID Read Address (A6, A1, A0)
ID Read Address = (0, 1, 0)

BLOCK ERASE ADDRESS TABLES

(1) TC58FVT160A (top boot block)

BLOCK #	BLOCK ADDRESS								BLOCK SIZE (Kbytes/Kwords)	ADDRESS RANGE	
	A19	A18	A17	A16	A15	A14	A13	A12		BYTE MODE	WORD MODE
BA0	0	0	0	0	0	×	×	×	64/32	00000h~0FFFFh	00000h~07FFFh
BA1	0	0	0	0	1	×	×	×	64/32	10000h~1FFFFh	08000h~0FFFFh
BA2	0	0	0	1	0	×	×	×	64/32	20000h~2FFFFh	10000h~17FFFh
BA3	0	0	0	1	1	×	×	×	64/32	30000h~3FFFFh	18000h~1FFFFh
BA4	0	0	1	0	0	×	×	×	64/32	40000h~4FFFFh	20000h~7FFFFh
BA5	0	0	1	0	1	×	×	×	64/32	50000h~5FFFFh	28000h~2FFFFh
BA6	0	0	1	1	0	×	×	×	64/32	60000h~6FFFFh	30000h~37FFFh
BA7	0	0	1	1	1	×	×	×	64/32	70000h~7FFFFh	38000h~3FFFFh
BA8	0	1	0	0	0	×	×	×	64/32	80000h~8FFFFh	40000h~47FFFh
BA9	0	1	0	0	1	×	×	×	64/32	90000h~9FFFFh	48000h~4FFFFh
BA10	0	1	0	1	0	×	×	×	64/32	A0000h~AFFFFh	50000h~57FFFh
BA11	0	1	0	1	1	×	×	×	64/32	B0000h~BFFFFh	58000h~5FFFFh
BA12	0	1	1	0	0	×	×	×	64/32	C0000h~CFFFFh	60000h~67FFFh
BA13	0	1	1	0	1	×	×	×	64/32	D0000h~DFFFFh	68000h~6FFFFh
BA14	0	1	1	1	0	×	×	×	64/32	E0000h~EFFFFh	70000h~77FFFh
BA15	0	1	1	1	1	×	×	×	64/32	F0000h~FFFFFh	78000h~7FFFFh
BA16	1	0	0	0	0	×	×	×	64/32	100000h~10FFFFh	80000h~87FFFh
BA17	1	0	0	0	1	×	×	×	64/32	110000h~11FFFFh	88000h~8FFFFh
BA18	1	0	0	1	0	×	×	×	64/32	120000h~12FFFFh	90000h~97FFFh
BA19	1	0	0	1	1	×	×	×	64/32	130000h~13FFFFh	98000h~9FFFFh
BA20	1	0	1	0	0	×	×	×	64/32	140000h~14FFFFh	A0000h~A7FFFh
BA21	1	0	1	0	1	×	×	×	64/32	150000h~15FFFFh	A8000h~AFFFFh
BA22	1	0	1	1	0	×	×	×	64/32	160000h~16FFFFh	B0000h~B7FFFh
BA23	1	0	1	1	1	×	×	×	64/32	170000h~17FFFFh	B8000h~BFFFFh
BA24	1	1	0	0	0	×	×	×	64/32	180000h~18FFFFh	C0000h~C7FFFh
BA25	1	1	0	0	1	×	×	×	64/32	190000h~19FFFFh	C8000h~CFFFFh
BA26	1	1	0	1	0	×	×	×	64/32	1A0000h~1AFFFFh	D0000h~D7FFFh
BA27	1	1	0	1	1	×	×	×	64/32	1B0000h~1BFFFFh	D8000h~DFFFFh
BA28	1	1	1	0	0	×	×	×	64/32	1C0000h~1CFFFFh	E0000h~E7FFFh
BA29	1	1	1	0	1	×	×	×	64/32	1D0000h~1DFFFFh	E8000h~EFFFFh
BA30	1	1	1	1	0	×	×	×	64/32	1E0000h~1EFFFFh	F0000h~F7FFFh
BA31	1	1	1	1	1	0	×	×	32/16	1F0000h~1F7FFFh	F8000h~FBFFFh
BA32	1	1	1	1	1	1	0	0	8/4	1F8000h~1F9FFFh	FC000h~FCFFFh
BA33	1	1	1	1	1	1	0	1	8/4	1FA000h~1FBFFFh	FD000h~FDFFFh
BA34	1	1	1	1	1	1	1	×	16/8	1FC000h~1FFFFFh	FE000h~FFFFFh

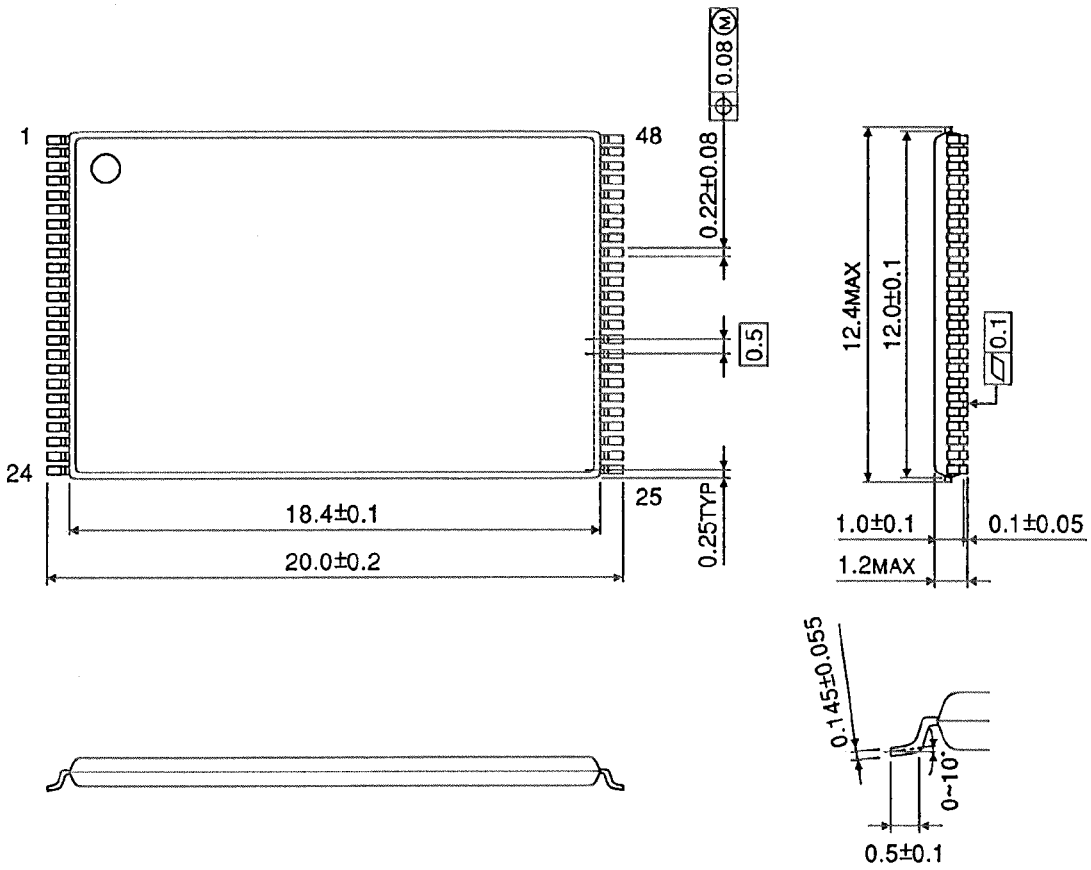
(2) TC58FVB160A (bottom boot block)

BLOCK #	BLOCK ADDRESS								BLOCK SIZE (Kbytes/Kwords)	ADDRESS RANGE	
	A19	A18	A17	A16	A15	A14	A13	A12		BYTE MODE	WORD MODE
BA0	0	0	0	0	0	0	0	×	16/8	0000h~3FFFh	0000h~1FFFh
BA1	0	0	0	0	0	0	1	0	8/4	4000h~5FFFh	2000h~2FFFh
BA2	0	0	0	0	0	0	1	1	8/4	6000h~7FFFh	3000h~3FFFh
BA3	0	0	0	0	0	1	×	×	32/16	8000h~FFFFh	4000h~7FFFh
BA4	0	0	0	0	1	×	×	×	64/32	10000h~1FFFFh	8000h~FFFFh
BA5	0	0	0	1	0	×	×	×	64/32	20000h~2FFFFh	10000h~17FFFh
BA6	0	0	0	1	1	×	×	×	64/32	30000h~3FFFFh	18000h~1FFFFh
BA7	0	0	1	0	0	×	×	×	64/32	40000h~4FFFFh	20000h~27FFFh
BA8	0	0	1	0	1	×	×	×	64/32	50000h~5FFFFh	28000h~2FFFFh
BA9	0	0	1	1	0	×	×	×	64/32	60000h~6FFFFh	30000h~37FFFh
BA10	0	0	1	1	1	×	×	×	64/32	70000h~7FFFFh	38000h~3FFFFh
BA11	0	1	0	0	0	×	×	×	64/32	80000h~8FFFFh	40000h~47FFFh
BA12	0	1	0	0	1	×	×	×	64/32	90000h~9FFFFh	48000h~4FFFFh
BA13	0	1	0	1	0	×	×	×	64/32	A0000h~AFFFFh	50000h~57FFFh
BA14	0	1	0	1	1	×	×	×	64/32	B0000h~BFFFFh	58000h~5FFFFh
BA15	0	1	1	0	0	×	×	×	64/32	C0000h~CFFFFh	60000h~67FFFh
BA16	0	1	1	0	1	×	×	×	64/32	D0000h~DFFFFh	68000h~6FFFFh
BA17	0	1	1	1	0	×	×	×	64/32	E0000h~EFFFFh	70000h~77FFFh
BA18	0	1	1	1	1	×	×	×	64/32	F0000h~FFFFFh	78000h~7FFFFh
BA19	1	0	0	0	0	×	×	×	64/32	100000h~10FFFFh	80000h~87FFFh
BA20	1	0	0	0	1	×	×	×	64/32	110000h~11FFFFh	88000h~8FFFFh
BA21	1	0	0	1	0	×	×	×	64/32	120000h~12FFFFh	90000h~97FFFh
BA22	1	0	0	1	1	×	×	×	64/32	130000h~13FFFFh	98000h~9FFFFh
BA23	1	0	1	0	0	×	×	×	64/32	140000h~14FFFFh	A0000h~A7FFFh
BA24	1	0	1	0	1	×	×	×	64/32	150000h~15FFFFh	A8000h~AFFFFh
BA25	1	0	1	1	0	×	×	×	64/32	160000h~16FFFFh	B0000h~B7FFFh
BA26	1	0	1	1	1	×	×	×	64/32	170000h~17FFFFh	B8000h~BFFFFh
BA27	1	1	0	0	0	×	×	×	64/32	180000h~18FFFFh	C0000h~C7FFFh
BA28	1	1	0	0	1	×	×	×	64/32	190000h~19FFFFh	C8000h~CFFFFh
BA29	1	1	0	1	0	×	×	×	64/32	1A0000h~1AFFFFh	D0000h~D7FFFh
BA30	1	1	0	1	1	×	×	×	64/32	1B0000h~1BFFFFh	D8000h~DFFFFh
BA31	1	1	1	0	0	×	×	×	64/32	1C0000h~1CFFFFh	E0000h~E7FFFh
BA32	1	1	1	0	1	×	×	×	64/32	1D0000h~1DFFFFh	E8000h~EFFFFh
BA33	1	1	1	1	0	×	×	×	64/32	1E0000h~1EFFFFh	F0000h~F7FFFh
BA34	1	1	1	1	1	×	×	×	64/32	1F0000h~1EFFFFh	F8000h~FFFFFh

PACKAGE DIMENSIONS

Unit: mm

TSOPI48-P-1220-0.50



PACKAGE DIMENSIONS

Unit: mm

P-TFBGA48-0608-0.80AZ

