

TENTATIVE

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

8,388,608-WORD × 8-BIT EDO (HYPER PAGE) DYNAMIC RAM

**DESCRIPTION**

The TC5164(5)805BJ/BFT/BJS/BFTS is an EDO (hyper page) dynamic RAM organized as 8,388,608 words by 8 bits. TC5164(5)805BJ/BFT/BJS/BFTS utilizes TOSHIBA's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC5164(5)805BJ/BFT/BJS/BFTS to be packaged in either a 32-pin plastic SOJ or a 32-pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. Other features include a single power supply of  $3.3V \pm 0.3V$  tolerance and direct interfacing with high performance logic families such as LVTTL.

**FEATURES**

- 8,388,608-word by 8-bit organization
- Fast access time and cycle time
- Single power supply of  $3.3V \pm 0.3V$  with a built-in  $V_{BB}$  generator
- Low power dissipation (max)
  - Operating : 306mW (TC5164805BJ/BFT/BJS/BFTS-40)
  - 252mW (TC5164805BJ/BFT/BJS/BFTS-50)
  - 432mW (TC5165805BJ/BFT/BJS/BFTS-40)
  - 360mW (TC5165805BJ/BFT/BJS/BFTS-50)
  - Standby : 1.8mW
  - 0.72mW (S-version)
- Outputs unlatched at cycle end, allowing two-dimensional chip selection
- Read-Modify-Write and EDO (Hyper Page mode) capability
- All inputs and outputs LVTTL-compatible
- Packages
  - BJ/BJS : SOJ32-P-400-1.27B, 1.27 grams
  - BFT/BFTS : TSOP II 32-P-400-1.27B, 0.50grams

|           |                              | TC5164(5)805<br>BJ/BFT/BJS/BFTS |      |
|-----------|------------------------------|---------------------------------|------|
|           |                              | -40                             | -50  |
| $t_{RAC}$ | $\overline{RAS}$ Access Time | 40ns                            | 50ns |
| $t_{AA}$  | Column Address Access Time   | 20ns                            | 25ns |
| $t_{CAC}$ | $\overline{CAS}$ Access Time | 11ns                            | 13ns |
| $t_{RC}$  | Cycle Time                   | 69ns                            | 84ns |
| $t_{HPC}$ | Hyper Page Mode Cycle Time   | 16ns                            | 20ns |

| Part No.                         | Row Add.  | Col. Add. | Refresh                                                                                                          | Refresh Cycle |
|----------------------------------|-----------|-----------|------------------------------------------------------------------------------------------------------------------|---------------|
| TC5164805BJ/BFT                  | A0 to A12 | A0 to A9  | $\overline{RAS}$ -Only refresh                                                                                   | 8192/64 ms    |
|                                  |           |           | $\overline{CAS}$ -before- $\overline{RAS}$ refresh, Hidden refresh                                               | 4096/64 ms    |
| TC5165805BJ/BFT                  | A0 to A11 | A0 to A10 | $\overline{RAS}$ -Only refresh, $\overline{CAS}$ -before- $\overline{RAS}$ refresh, Hidden refresh               | 4096/64 ms    |
| TC5164805BJS/BFTS<br>(S-version) | A0 to A12 | A0 to A9  | $\overline{RAS}$ -Only refresh                                                                                   | 8192/128 ms   |
|                                  |           |           | $\overline{CAS}$ -before- $\overline{RAS}$ refresh, Hidden refresh, Self-refresh                                 | 4096/128 ms   |
| TC5165805BJS/BFTS<br>(S-version) | A0 to A11 | A0 to A10 | $\overline{RAS}$ -Only refresh, $\overline{CAS}$ -before- $\overline{RAS}$ refresh, Hidden refresh, Self-refresh | 4096/128 ms   |

980910EBA1

- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

TC5164805BJ/BFT/BJS/BFTS

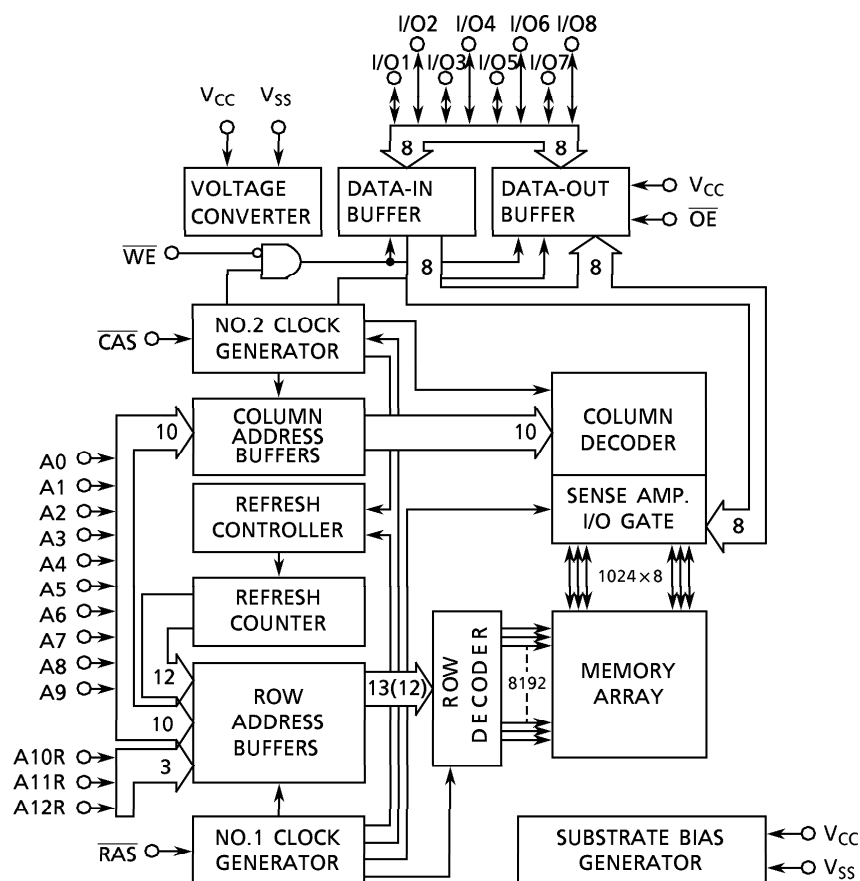
PIN ASSIGNMENT (TOP VIEW)

PIN NAMES

| Plastic SOJ     |    |    |                 | Plastic TSOP<br>(Normal Bend Type) |    |    |                 |
|-----------------|----|----|-----------------|------------------------------------|----|----|-----------------|
| V <sub>CC</sub> | 1  | 32 | V <sub>SS</sub> | V <sub>CC</sub>                    | 1  | 32 | V <sub>SS</sub> |
| I/O1            | 2  | 31 | I/O8            | I/O1                               | 2  | 31 | I/O8            |
| I/O2            | 3  | 30 | I/O7            | I/O2                               | 3  | 30 | I/O7            |
| I/O3            | 4  | 29 | I/O6            | I/O3                               | 4  | 29 | I/O6            |
| I/O4            | 5  | 28 | I/O5            | I/O4                               | 5  | 28 | I/O5            |
| NC              | 6  | 27 | V <sub>SS</sub> | NC                                 | 6  | 27 | V <sub>SS</sub> |
| V <sub>CC</sub> | 7  | 26 | CAS             | V <sub>CC</sub>                    | 7  | 26 | CAS             |
| WE              | 8  | 25 | OE              | WE                                 | 8  | 25 | OE              |
| RAS             | 9  | 24 | A12R            | RAS                                | 9  | 24 | A12R            |
| A0              | 10 | 23 | A11R            | A0                                 | 10 | 23 | A11R            |
| A1              | 11 | 22 | A10R            | A1                                 | 11 | 22 | A10R            |
| A2              | 12 | 21 | A9              | A2                                 | 12 | 21 | A9              |
| A3              | 13 | 20 | A8              | A3                                 | 13 | 20 | A8              |
| A4              | 14 | 19 | A7              | A4                                 | 14 | 19 | A7              |
| A5              | 15 | 18 | A6              | A5                                 | 15 | 18 | A6              |
| V <sub>CC</sub> | 16 | 17 | V <sub>SS</sub> | V <sub>CC</sub>                    | 16 | 17 | V <sub>SS</sub> |

|                         |                       |
|-------------------------|-----------------------|
| A0 to A12               | Address Inputs        |
| $\overline{\text{RAS}}$ | Row Address Strobe    |
| $\overline{\text{CAS}}$ | Column Address Strobe |
| $\overline{\text{WE}}$  | Write Enable          |
| $\overline{\text{OE}}$  | Output Enable         |
| I/O1 to I/O8            | Data Input/Output     |
| V <sub>CC</sub>         | Power (+ 3.3V)        |
| V <sub>SS</sub>         | Ground                |
| NC                      | No Connection         |

BLOCK DIAGRAM



## TC5165805BJ/BFT/BJS/BFTS

## PIN ASSIGNMENT (TOP VIEW)

Plastic SOJ

|                 |    |    |                 |
|-----------------|----|----|-----------------|
| V <sub>CC</sub> | 1  | 32 | V <sub>SS</sub> |
| I/O1            | 2  | 31 | I/O8            |
| I/O2            | 3  | 30 | I/O7            |
| I/O3            | 4  | 29 | I/O6            |
| I/O4            | 5  | 28 | I/O5            |
| NC              | 6  | 27 | V <sub>SS</sub> |
| V <sub>CC</sub> | 7  | 26 | CAS             |
| WE              | 8  | 25 | OE              |
| RAS             | 9  | 24 | NC              |
| A0              | 10 | 23 | A11R            |
| A1              | 11 | 22 | A10             |
| A2              | 12 | 21 | A9              |
| A3              | 13 | 20 | A8              |
| A4              | 14 | 19 | A7              |
| A5              | 15 | 18 | A6              |
| V <sub>CC</sub> | 16 | 17 | V <sub>SS</sub> |

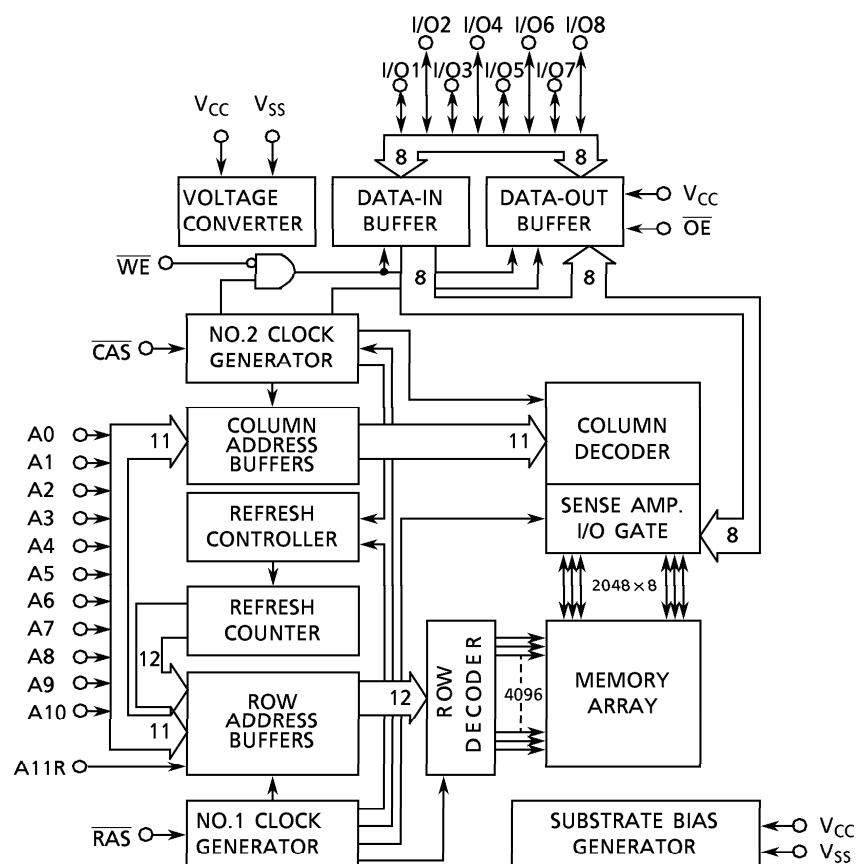
Plastic TSOP  
(Normal Bend Type)

|                 |    |    |                 |
|-----------------|----|----|-----------------|
| V <sub>CC</sub> | 1  | 32 | V <sub>SS</sub> |
| I/O1            | 2  | 31 | I/O8            |
| I/O2            | 3  | 30 | I/O7            |
| I/O3            | 4  | 29 | I/O6            |
| I/O4            | 5  | 28 | I/O5            |
| NC              | 6  | 27 | V <sub>SS</sub> |
| V <sub>CC</sub> | 7  | 26 | CAS             |
| WE              | 8  | 25 | OE              |
| RAS             | 9  | 24 | NC              |
| A0              | 10 | 23 | A11R            |
| A1              | 11 | 22 | A10             |
| A2              | 12 | 21 | A9              |
| A3              | 13 | 20 | A8              |
| A4              | 14 | 19 | A7              |
| A5              | 15 | 18 | A6              |
| V <sub>CC</sub> | 16 | 17 | V <sub>SS</sub> |

## PIN NAMES

|                 |                       |
|-----------------|-----------------------|
| A0 to A11       | Address Inputs        |
| RAS             | Row Address Strobe    |
| CAS             | Column Address Strobe |
| WE              | Write Enable          |
| OE              | Output Enable         |
| I/O1 to I/O8    | Data Input/Output     |
| V <sub>CC</sub> | Power (+ 3.3V)        |
| V <sub>SS</sub> | Ground                |
| NC              | No Connection         |

## BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

| ITEM                         | SYMBOL       | RATING                  | UNIT | NOTES |
|------------------------------|--------------|-------------------------|------|-------|
| Input Voltage                | $V_{IN}$     | - 0.3 to $V_{CC} + 0.3$ | V    | 1     |
| Output Voltage               | $V_{OUT}$    | - 0.3 to $V_{CC} + 0.3$ | V    | 1     |
| Power Supply Voltage         | $V_{CC}$     | - 0.3 to 4.6            | V    | 1     |
| Operating Temperature        | $T_{OPR}$    | 0 to 70                 | °C   | 1     |
| Storage Temperature          | $T_{STG}$    | - 55 to 150             | °C   | 1     |
| Soldering Temperature (10 s) | $T_{SOLDER}$ | 260                     | °C   | 1     |
| Power Dissipation            | $P_D$        | 1.0                     | W    | 1     |
| Short Circuit Output Current | $I_{OUT}$    | 50                      | mA   | 1     |

**RECOMMENDED DC OPERATING CONDITIONS ( $T_a = 0$  to  $70^{\circ}\text{C}$ )**

| SYMBOL   | PARAMETER          | MIN     | TYP. | MAX              | UNIT | NOTES |
|----------|--------------------|---------|------|------------------|------|-------|
| $V_{CC}$ | Supply Voltage     | 3.0     | 3.3  | 3.6              | V    | 2     |
| $V_{IH}$ | Input High Voltage | 2.0     | –    | $V_{CC} + 0.3^*$ | V    | 2     |
| $V_{IL}$ | Input Low Voltage  | - 0.3** | –    | 0.8              | V    | 2     |

\*  $V_{CC} + 1.2\text{V}$  at pulse width  $\leq 20\text{ns}$  (pulse width is measured at  $V_{CC}$ )

\*\* - 1.2V at pulse width  $\leq 20\text{ns}$  (pulse width is measured at  $V_{SS}$ )

**CAPACITANCE ( $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ ,  $f = 1\text{ MHz}$ ,  $T_a = 0$  to  $70^{\circ}\text{C}$ )**

| SYMBOL   | PARAMETER                                                                                                                 | MIN | MAX | UNIT |
|----------|---------------------------------------------------------------------------------------------------------------------------|-----|-----|------|
| $C_{I1}$ | Input Capacitance (Address)                                                                                               | –   | 5   | pF   |
| $C_{I2}$ | Input Capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ ) | –   | 7   | pF   |
| $C_O$    | I/O Capacitance (I/O1 to I/O8)                                                                                            | –   | 7   | pF   |

DC CHARACTERISTICS ( $V_{CC} = 3.3V \pm 0.3V$ ,  $T_a = 0$  to  $70^\circ C$ )

| SYMBOL     | PARAMETER                                                                                                                                                                                                                                                                                                                                                               | MIN                         | MAX                | UNIT    | NOTES         |
|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|--------------------|---------|---------------|
| $I_{CC1}$  | OPERATING CURRENT<br>Average Power Supply Operating Current<br>( $\overline{RAS}$ , $\overline{CAS}$ , Address Cycling: $t_{RC} = t_{RC \min}$ )                                                                                                                                                                                                                        | TC5164805BJ/BFT/BJ5/BFTS-40 | –                  | 85      | mA<br>3, 4, 5 |
|            |                                                                                                                                                                                                                                                                                                                                                                         | TC5164805BJ/BFT/BJ5/BFTS-50 | –                  | 70      |               |
|            |                                                                                                                                                                                                                                                                                                                                                                         | TC5165805BJ/BFT/BJ5/BFTS-40 | –                  | 120     |               |
|            |                                                                                                                                                                                                                                                                                                                                                                         | TC5165805BJ/BFT/BJ5/BFTS-50 | –                  | 100     |               |
| $I_{CC2}$  | STANDBY CURRENT<br>Power Supply Standby Current<br>( $\overline{RAS} = \overline{CAS} = V_{IH}$ )                                                                                                                                                                                                                                                                       | –                           | 1                  | mA      |               |
| $I_{CC3}$  | $\overline{RAS}$ -ONLY REFRESH CURRENT<br>Average Power Supply Current, $\overline{RAS}$ -Only Mode<br>( $\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$ : $t_{RC} = t_{RC \min}$ )                                                                                                                                                                                 | TC5164805BJ/BFT/BJ5/BFTS-40 | –                  | 85      | mA<br>3, 5    |
|            |                                                                                                                                                                                                                                                                                                                                                                         | TC5164805BJ/BFT/BJ5/BFTS-50 | –                  | 70      |               |
|            |                                                                                                                                                                                                                                                                                                                                                                         | TC5165805BJ/BFT/BJ5/BFTS-40 | –                  | 120     |               |
|            |                                                                                                                                                                                                                                                                                                                                                                         | TC5165805BJ/BFT/BJ5/BFTS-50 | –                  | 100     |               |
| $I_{CC4}$  | HYPER PAGE MODE CURRENT<br>Average Power Supply Current, Hyper Page Mode<br>( $\overline{RAS} = V_{IL}$ , $\overline{CAS}$ , Address Cycling: $t_{HPC} = t_{HPC \min}$ )                                                                                                                                                                                                | TC5164805BJ/BFT/BJ5/BFTS-40 | –                  | 90      | mA<br>3, 4, 5 |
|            |                                                                                                                                                                                                                                                                                                                                                                         | TC5164805BJ/BFT/BJ5/BFTS-50 | –                  | 75      |               |
|            |                                                                                                                                                                                                                                                                                                                                                                         | TC5165805BJ/BFT/BJ5/BFTS-40 | –                  | 90      |               |
|            |                                                                                                                                                                                                                                                                                                                                                                         | TC5165805BJ/BFT/BJ5/BFTS-50 | –                  | 75      |               |
| $I_{CC5}$  | STANDBY CURRENT<br>Power Supply Standby Current<br>( $\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$ )                                                                                                                                                                                                                                                                | –                           | 500                | $\mu A$ |               |
|            |                                                                                                                                                                                                                                                                                                                                                                         |                             | 200<br>(S-version) |         |               |
| $I_{CC6}$  | $\overline{CAS}$ -BEFORE- $\overline{RAS}$ REFRESH CURRENT<br>Average Power Supply Current, $\overline{CAS}$ -before- $\overline{RAS}$<br>Mode ( $\overline{RAS}$ , $\overline{CAS}$ Cycling: $t_{RC} = t_{RC \min}$ )                                                                                                                                                  | TC5164805BJ/BFT/BJ5/BFTS-40 | –                  | 120     | mA<br>3, 5    |
|            |                                                                                                                                                                                                                                                                                                                                                                         | TC5164805BJ/BFT/BJ5/BFTS-50 | –                  | 100     |               |
|            |                                                                                                                                                                                                                                                                                                                                                                         | TC5165805BJ/BFT/BJ5/BFTS-40 | –                  | 120     |               |
|            |                                                                                                                                                                                                                                                                                                                                                                         | TC5165805BJ/BFT/BJ5/BFTS-50 | –                  | 100     |               |
| $I_{CC7}$  | BATTERY BACK-UP CURRENT<br>Average Power Supply Current, Battery Back-up Mode<br>( $\overline{RAS}$ Cycling, $\overline{CAS} = \overline{CAS}$ -before- $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$ , $\overline{WE}$ , Address = $V_{CC} - 0.2V$ or 0.2V, I/O1 to I/O8 = $V_{CC} - 0.2V$ , 0.2V or Hi-Z: $t_{RC} = 31.2\mu s$ $t_{RAS} = t_{RAS \min}$ to 300ns) | –                           | 500<br>(S-version) | $\mu A$ |               |
| $I_{CCS}$  | SELF-REFRESH CURRENT<br>Average Power Supply Current, Self-Refresh Mode<br>( $\overline{RAS} = \overline{CAS} = V_{IL}$ , $\overline{OE}$ , $\overline{WE}$ , Address = $V_{CC} - 0.2V$ or 0.2V, I/O1 to I/O8 = $V_{CC} - 0.2V$ , 0.2V or Hi-Z)                                                                                                                         | –                           | 400<br>(S-version) | $\mu A$ |               |
| $I_{I(L)}$ | INPUT LEAKAGE CURRENT<br>Input Leakage Current, Any Input<br>( $0V \leq V_{IN} \leq V_{CC}$ , All Other Pins Not under Test = 0V)                                                                                                                                                                                                                                       | – 10                        | 10                 | $\mu A$ |               |
| $I_{O(L)}$ | OUTPUT LEAKAGE CURRENT<br>( $D_{OUT}$ Is Disabled, $0V \leq V_{OUT} \leq V_{CC}$ )                                                                                                                                                                                                                                                                                      | – 10                        | 10                 | $\mu A$ |               |
| $V_{OH}$   | OUTPUT LEVEL<br>Output H Level Voltage ( $I_{OUT} = -2mA$ )                                                                                                                                                                                                                                                                                                             | 2.4                         | –                  | V       |               |
| $V_{OL}$   | OUTPUT LEVEL<br>Output L Level Voltage ( $I_{OUT} = 2mA$ )                                                                                                                                                                                                                                                                                                              | –                           | 0.4                | V       |               |

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS(V<sub>CC</sub> = 3.3V ± 0.3V, T<sub>a</sub> = 0 to 70°C) (Notes 6, 7, 8)

| SYMBOL            | PARAMETER                                                                                  | TC5164(5)805BJ/BFT/BJ5/BFTS |         |     |         | UNIT | NOTES     |
|-------------------|--------------------------------------------------------------------------------------------|-----------------------------|---------|-----|---------|------|-----------|
|                   |                                                                                            | -40                         |         | -50 |         |      |           |
|                   |                                                                                            | MIN                         | MAX     | MIN | MAX     |      |           |
| t <sub>RC</sub>   | Random Read-or-Write Cycle Time                                                            | 69                          | –       | 84  | –       | ns   |           |
| t <sub>RMW</sub>  | Read-Modify-Write Cycle Time                                                               | 92                          | –       | 111 | –       | ns   |           |
| t <sub>RAC</sub>  | Access Time from $\overline{\text{RAS}}$                                                   | –                           | 40      | –   | 50      | ns   | 9, 14, 15 |
| t <sub>CAC</sub>  | Access Time from $\overline{\text{CAS}}$                                                   | –                           | 11      | –   | 13      | ns   | 9, 14     |
| t <sub>AA</sub>   | Access Time from Column Address                                                            | –                           | 20      | –   | 25      | ns   | 9, 15     |
| t <sub>CPA</sub>  | Access Time from $\overline{\text{CAS}}$ Precharge                                         | –                           | 22      | –   | 28      | ns   | 9         |
| t <sub>CLZ</sub>  | $\overline{\text{CAS}}$ to Output in Low-Z                                                 | 0                           | –       | 0   | –       | ns   |           |
| t <sub>OFF</sub>  | Output Buffer Turn-off Delay                                                               | 0                           | 11      | 0   | 13      | ns   | 10, 16    |
| t <sub>T</sub>    | Transition Time (Rise and Fall)                                                            | 1                           | 50      | 1   | 50      | ns   | 8         |
| t <sub>RP</sub>   | $\overline{\text{RAS}}$ Precharge Time                                                     | 25                          | –       | 30  | –       | ns   |           |
| t <sub>RAS</sub>  | $\overline{\text{RAS}}$ Pulse Width                                                        | 40                          | 10,000  | 50  | 10,000  | ns   |           |
| t <sub>RASP</sub> | $\overline{\text{RAS}}$ Pulse Width (Hyper Page Mode)                                      | 40                          | 100,000 | 50  | 100,000 | ns   |           |
| t <sub>RSH</sub>  | $\overline{\text{RAS}}$ Hold Time                                                          | 6                           | –       | 8   | –       | ns   |           |
| t <sub>RHCP</sub> | $\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge (Hyper Page Mode) | 22                          | –       | 28  | –       | ns   |           |
| t <sub>CSH</sub>  | $\overline{\text{CAS}}$ Hold Time                                                          | 30                          | –       | 35  | –       | ns   |           |
| t <sub>CAS</sub>  | $\overline{\text{CAS}}$ Pulse Width                                                        | 6                           | 10,000  | 8   | 10,000  | ns   |           |
| t <sub>RCD</sub>  | $\overline{\text{RAS}}$ -to- $\overline{\text{CAS}}$ Delay Time                            | 10                          | 29      | 12  | 37      | ns   | 14        |
| t <sub>RAD</sub>  | $\overline{\text{RAS}}$ -to-Column-Address Delay Time                                      | 8                           | 20      | 10  | 25      | ns   | 15        |
| t <sub>CRP</sub>  | $\overline{\text{CAS}}$ -to- $\overline{\text{RAS}}$ Precharge Time                        | 5                           | –       | 5   | –       | ns   |           |
| t <sub>CP</sub>   | $\overline{\text{CAS}}$ Precharge Time                                                     | 6                           | –       | 8   | –       | ns   |           |
| t <sub>ASR</sub>  | Row Address Set up Time                                                                    | 0                           | –       | 0   | –       | ns   |           |
| t <sub>RAH</sub>  | Row Address Hold Time                                                                      | 6                           | –       | 8   | –       | ns   |           |
| t <sub>ASC</sub>  | Column Address Set up Time                                                                 | 0                           | –       | 0   | –       | ns   |           |
| t <sub>CAH</sub>  | Column Address Hold Time                                                                   | 6                           | –       | 8   | –       | ns   |           |
| t <sub>RAL</sub>  | Column-Address-to- $\overline{\text{RAS}}$ Lead Time                                       | 20                          | –       | 25  | –       | ns   |           |
| t <sub>RCS</sub>  | Read Command Set up Time                                                                   | 0                           | –       | 0   | –       | ns   |           |
| t <sub>RCH</sub>  | Read Command Hold Time                                                                     | 0                           | –       | 0   | –       | ns   | 11        |
| t <sub>RRH</sub>  | Read Command Hold Time Referenced to $\overline{\text{RAS}}$                               | 0                           | –       | 0   | –       | ns   | 11        |
| t <sub>WCH</sub>  | Write Command Hold Time                                                                    | 6                           | –       | 8   | –       | ns   |           |
| t <sub>WP</sub>   | Write Command Pulse Width                                                                  | 6                           | –       | 8   | –       | ns   |           |
| t <sub>RWL</sub>  | Write-Command-to- $\overline{\text{RAS}}$ Lead Time                                        | 6                           | –       | 8   | –       | ns   |           |
| t <sub>CWL</sub>  | Write-Command-to- $\overline{\text{CAS}}$ Lead Time                                        | 6                           | –       | 8   | –       | ns   |           |
| t <sub>DS</sub>   | Data Set up Time                                                                           | 0                           | –       | 0   | –       | ns   | 12        |
| t <sub>DH</sub>   | Data Hold Time                                                                             | 6                           | –       | 8   | –       | ns   | 12        |

## AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(Continued)

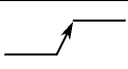
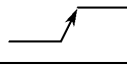
| SYMBOL             | PARAMETER                                                            | TC5164(5)805BJ/BFT/BJS/BFTS |                    |     |                    | UNIT | NOTES  |
|--------------------|----------------------------------------------------------------------|-----------------------------|--------------------|-----|--------------------|------|--------|
|                    |                                                                      | -40                         |                    | -50 |                    |      |        |
|                    |                                                                      | MIN                         | MAX                | MIN | MAX                |      |        |
| t <sub>REF</sub>   | Refresh Period                                                       | –                           | 64                 | –   | 64                 | ms   |        |
|                    |                                                                      | –                           | 128<br>(S-version) | –   | 128<br>(S-version) |      |        |
| t <sub>WCS</sub>   | Write Command Set up Time                                            | 0                           | –                  | 0   | –                  | ns   | 13     |
| t <sub>CWD</sub>   | CAS-to-WE Delay Time                                                 | 26                          | –                  | 30  | –                  | ns   | 13     |
| t <sub>RWD</sub>   | RAS-to-WE Delay Time                                                 | 55                          | –                  | 67  | –                  | ns   | 13     |
| t <sub>AWD</sub>   | Column-Address-to-WE Delay Time                                      | 35                          | –                  | 42  | –                  | ns   | 13     |
| t <sub>CPWD</sub>  | CAS-Precharge-to-WE Delay Time                                       | 37                          | –                  | 45  | –                  | ns   | 13     |
| t <sub>CSR</sub>   | CAS Set up Time (CAS-before-RAS Cycle)                               | 5                           | –                  | 5   | –                  | ns   |        |
| t <sub>CHR</sub>   | CAS Hold Time (CAS-before-RAS Cycle)                                 | 6                           | –                  | 8   | –                  | ns   |        |
| t <sub>RPC</sub>   | RAS-to-CAS Precharge Time                                            | 5                           | –                  | 5   | –                  | ns   |        |
| t <sub>ROH</sub>   | RAS Hold Time Referenced to OE                                       | 6                           | –                  | 8   | –                  | ns   |        |
| t <sub>OEA</sub>   | OE Access Time                                                       | –                           | 11                 | –   | 13                 | ns   | 9      |
| t <sub>OED</sub>   | OE-to-Data Delay                                                     | 11                          | –                  | 13  | –                  | ns   |        |
| t <sub>OLZ</sub>   | OE to Output in Low-Z                                                | 0                           | –                  | 0   | –                  | ns   |        |
| t <sub>OEZ</sub>   | Output Buffer Turn-off Delay Time from OE                            | 0                           | 11                 | 0   | 13                 | ns   | 10     |
| t <sub>OEH</sub>   | OE Command Hold Time                                                 | 6                           | –                  | 8   | –                  | ns   |        |
| t <sub>ODS</sub>   | Output Disable Set up Time                                           | 0                           | –                  | 0   | –                  | ns   |        |
| t <sub>WRP</sub>   | WE-to-RAS Precharge Time (CAS-before-RAS Cycle)                      | 5                           | –                  | 5   | –                  | ns   |        |
| t <sub>WRH</sub>   | WE-to-RAS Hold Time (CAS-before-RAS Cycle)                           | 6                           | –                  | 8   | –                  | ns   |        |
| t <sub>RNCD</sub>  | RAS-to-Next-CAS Delay Time (Hyper Page Mode)                         | 40                          | –                  | 50  | –                  | ns   |        |
| t <sub>HPC</sub>   | Hyper Page Mode Cycle Time                                           | 16                          | –                  | 20  | –                  | ns   |        |
| t <sub>HPRWC</sub> | Hyper Page Mode Read-Modify-Write Cycle Time                         | 47                          | –                  | 57  | –                  | ns   |        |
| t <sub>COH</sub>   | Output Data Hold Time                                                | 5                           | –                  | 5   | –                  | ns   |        |
| t <sub>REZ</sub>   | Output Buffer Turn-off Delay from RAS                                | 0                           | 11                 | 0   | 13                 | ns   | 10, 16 |
| t <sub>WEZ</sub>   | Output Buffer Turn-off Delay from WE                                 | 0                           | 11                 | 0   | 13                 | ns   | 10     |
| t <sub>WED</sub>   | WE-to-Data Delay                                                     | 11                          | –                  | 13  | –                  | ns   |        |
| t <sub>OE</sub>    | OE Pulse Width                                                       | 11                          | –                  | 13  | –                  | ns   |        |
| t <sub>OEP</sub>   | OE Precharge Time                                                    | 6                           | –                  | 8   | –                  | ns   |        |
| t <sub>CPO</sub>   | CAS-to-OE Precharge Time                                             | 5                           | –                  | 5   | –                  | ns   |        |
| t <sub>OCH</sub>   | CAS Hold Time Referenced to OE                                       | 6                           | –                  | 8   | –                  | ns   |        |
| t <sub>RASS</sub>  | RAS Pulse Width (CAS-before-RAS Self-Refresh)<br>(S-version only)    | 100                         | –                  | 100 | –                  | μs   |        |
| t <sub>RPS</sub>   | RAS Precharge Time (CAS-before-RAS Self-Refresh)<br>(S-version only) | 69                          | –                  | 84  | –                  | ns   |        |
| t <sub>CHS</sub>   | CAS Hold Time (CAS-before-RAS Self-Refresh)<br>(S-version only)      | -50                         | –                  | -50 | –                  | ns   |        |

## NOTES:

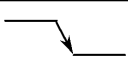
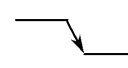
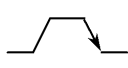
1. Conditions outside the limits listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to  $V_{SS}$ .
3.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC6}$  depend on the cycle rate.
4.  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
5. The address can be changed once at most while  $\overline{RAS}=V_{IL}$ . In the case of  $I_{CC4}$ , it can be changed once at most during a Hyper Page Mode cycle ( $t_{HPC}$ ).
6. An initial pause of  $200\mu s$  is required after power-up followed by a minimum of eight  $\overline{RAS}$ -Only refresh cycles before proper device operation is achieved. When using the internal refresh counter, a minimum of eight  $\overline{CAS}$ -before- $\overline{RAS}$  refresh cycles instead of eight  $\overline{RAS}$ -Only refresh cycles is required.
7. AC measurements assume  $t_T=2ns$ .
8.  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring the timing of input signals. Also, transition times are measured between the  $V_{IH}$  and  $V_{IL}$  levels.
9. This is measured with a load equivalent to  $100pF$  at  $V_{OH} = 2.0V$  ( $I_{OUT} = -2mA$ ),  $V_{OL} = 0.8V$  ( $I_{OUT} = 2mA$ ).
10.  $t_{OFF}$  (max),  $t_{OEZ}$  (max),  $t_{REZ}$  (max) and  $t_{WEZ}$  (max) define the time at which the output goes open circuit and are not referenced to output voltage levels.
11. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a Read cycle.
12. These parameters are referenced to the leading edge of  $\overline{CAS}$  in Early Write cycles and to the leading edge of  $\overline{WE}$  in Read-Modify-Write cycles.
13.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\min)$ , the cycle is an Early Write cycle and the Data-out pin will remain open circuit (high impedance) throughout the entire cycle. If  $t_{RWD} \geq t_{RWD}(\min)$ ,  $t_{CWD} \geq t_{CWD}(\min)$ ,  $t_{AWD} \geq t_{AWD}(\min)$  and  $t_{CPWD} \geq t_{CPWD}(\min)$  (Hyper Page mode), the cycle is a Read-Modify-Write cycle and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the data output (at access time) is indeterminate.
14. Operation within the  $t_{RCD}(\max)$  limit ensures that  $t_{RAC}(\max)$  can be met.  $t_{RCD}(\max)$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\max)$  limit, then the access time is determined by  $t_{CAC}$ .
15. Operation within the  $t_{RAD}(\max)$  limit ensures that  $t_{RAC}(\max)$  can be met.  $t_{RAD}(\max)$  is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\max)$  limit, then the access time is determined by  $t_{AA}$ .
16. If  $\overline{RAS}$  goes high before  $\overline{CAS}$  goes high, the output goes open circuit when  $\overline{CAS}$  goes high ( $t_{OFF}$ ). If  $\overline{CAS}$  goes high before  $\overline{RAS}$  goes high, the output goes open circuit when  $\overline{RAS}$  goes high ( $t_{REZ}$ ).



DATA-OUT HI-Z CONTROL LOGIC

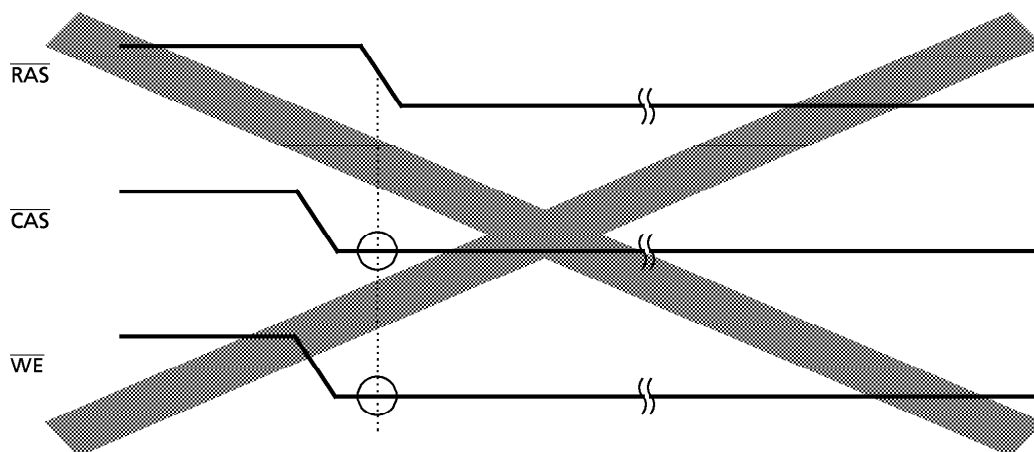
| RAS                                                                               | CAS                                                                               | OE                                                                                | WE                                                                                | Timing Specification |
|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|----------------------|
| H                                                                                 |  | L                                                                                 | H                                                                                 | $t_{OFF}$            |
|  | H                                                                                 | L                                                                                 | H                                                                                 | $t_{REZ}$            |
| L                                                                                 | L                                                                                 |  | H                                                                                 | $t_{OEZ}$            |
| L                                                                                 | H                                                                                 | L                                                                                 |  | $t_{WEZ}$            |

DATA-OUT LO-Z CONTROL LOGIC

| RAS | CAS                                                                               | OE                                                                                 | WE | Timing Specification |
|-----|-----------------------------------------------------------------------------------|------------------------------------------------------------------------------------|----|----------------------|
| L   |  | L                                                                                  | H  | $t_{CLZ}$            |
| L   | L                                                                                 |   | H  | $t_{OLZ}$            |
| L   | L                                                                                 |  | H  | $t_{OLZ}$            |

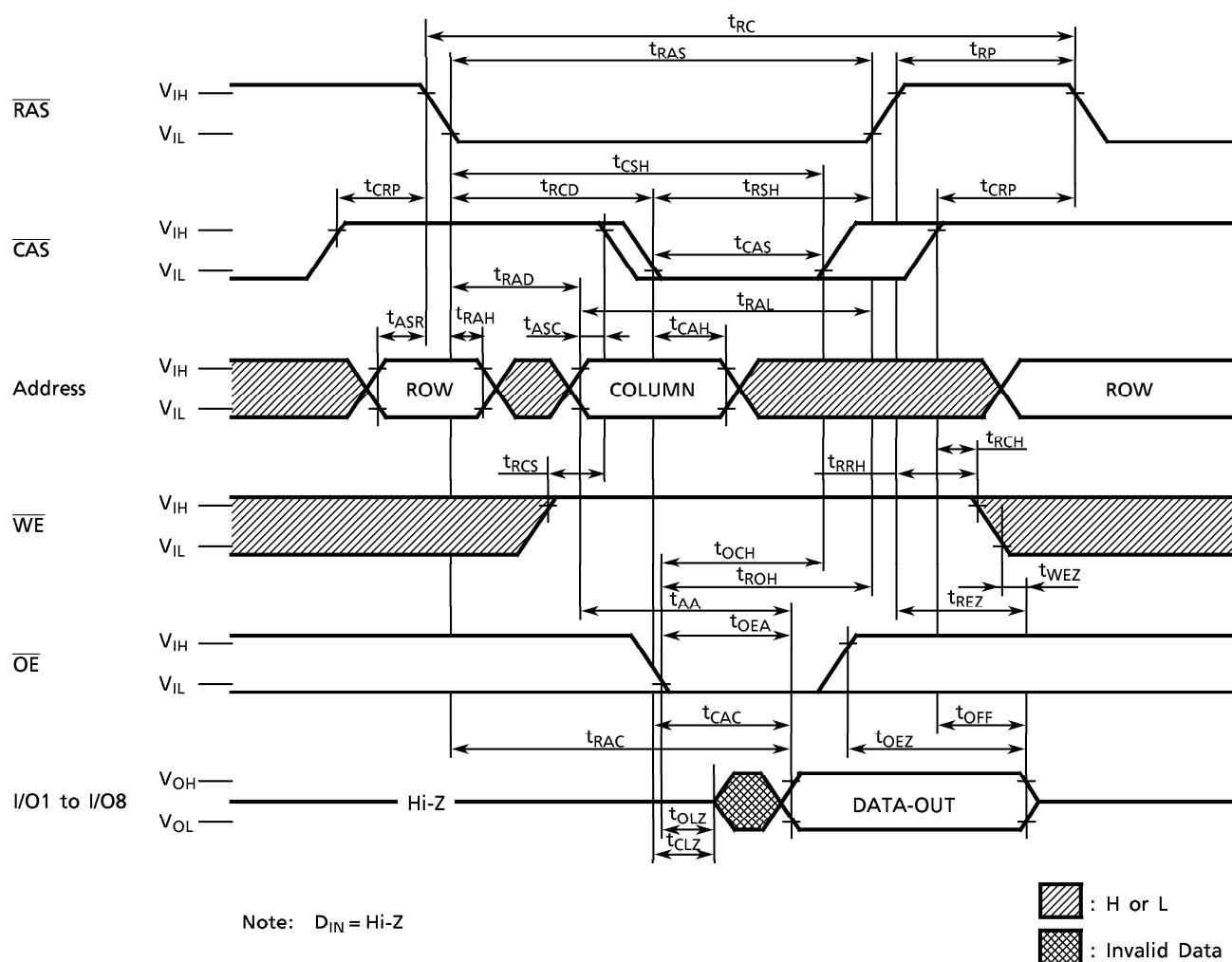
**CAUTION**

The WCBR ( $\overline{WE}$ ,  $\overline{CAS}$ -before- $\overline{RAS}$ ) timing shown below is not allowed during normal operation, such as during Read, Write and Refresh operations. When WCBR is input, a malfunction may occur due to the change in internal circuit operation status.

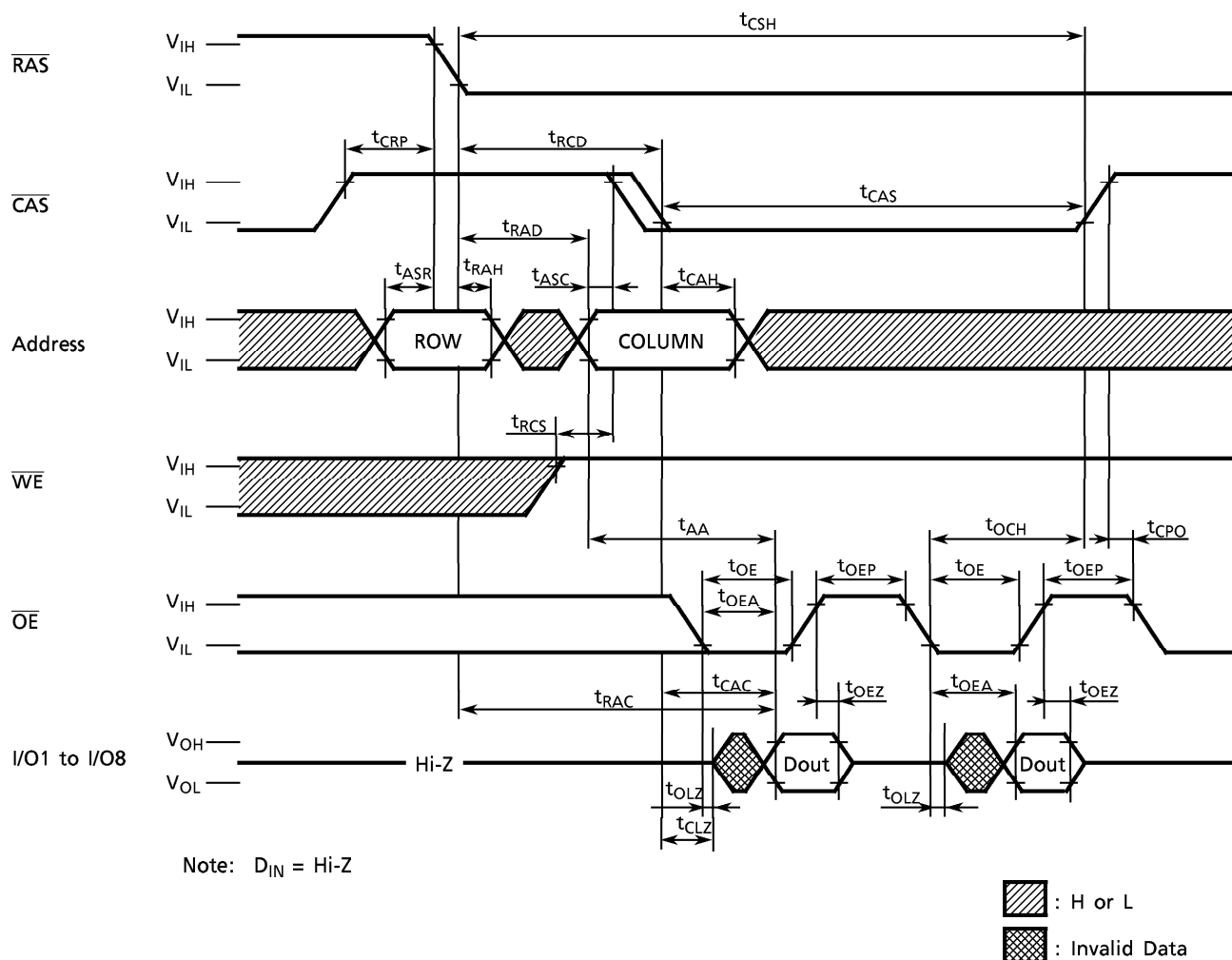
**WCBR timing**

# TIMING DIAGRAMS

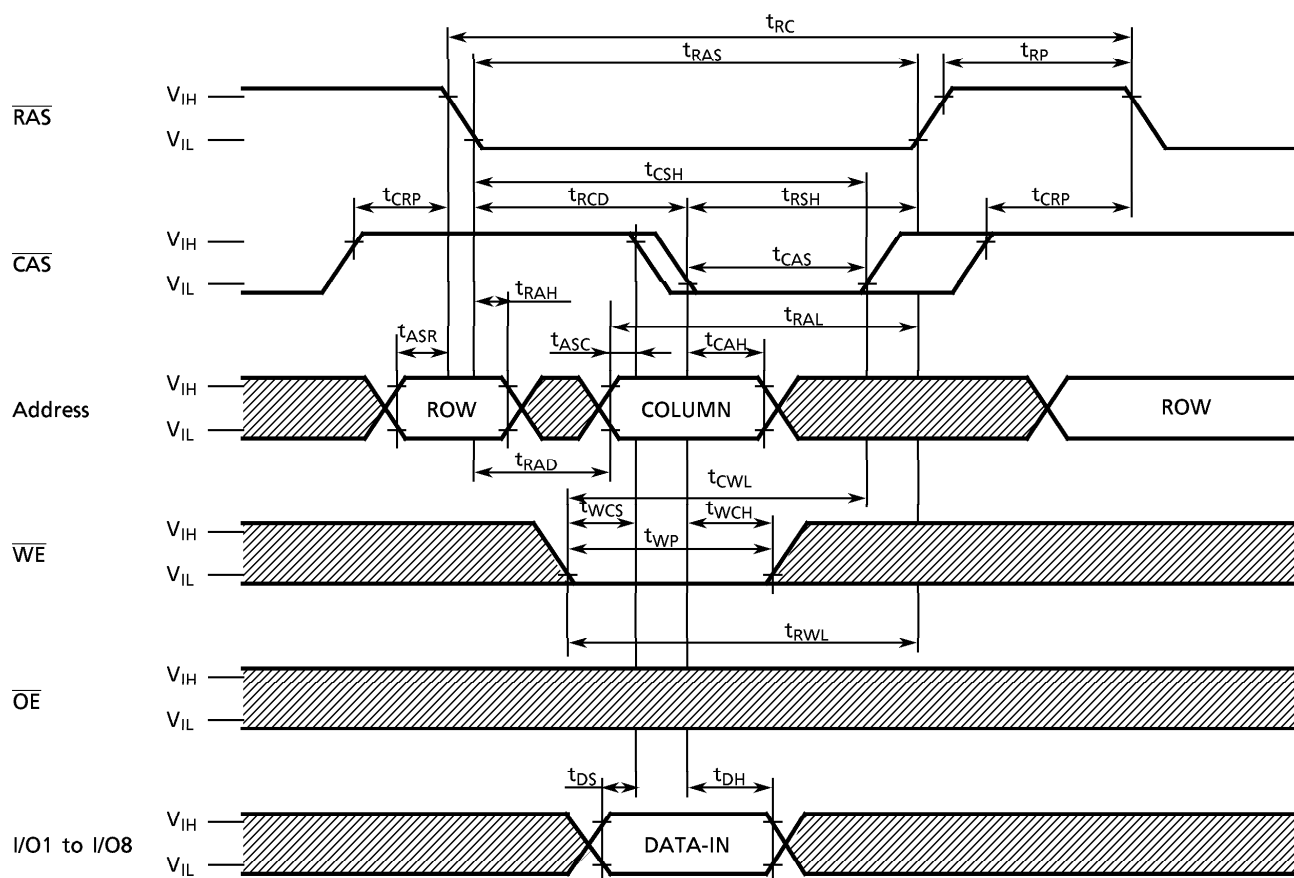
## READ CYCLE



**$\overline{OE}$ -CONTROLLED READ CYCLE**

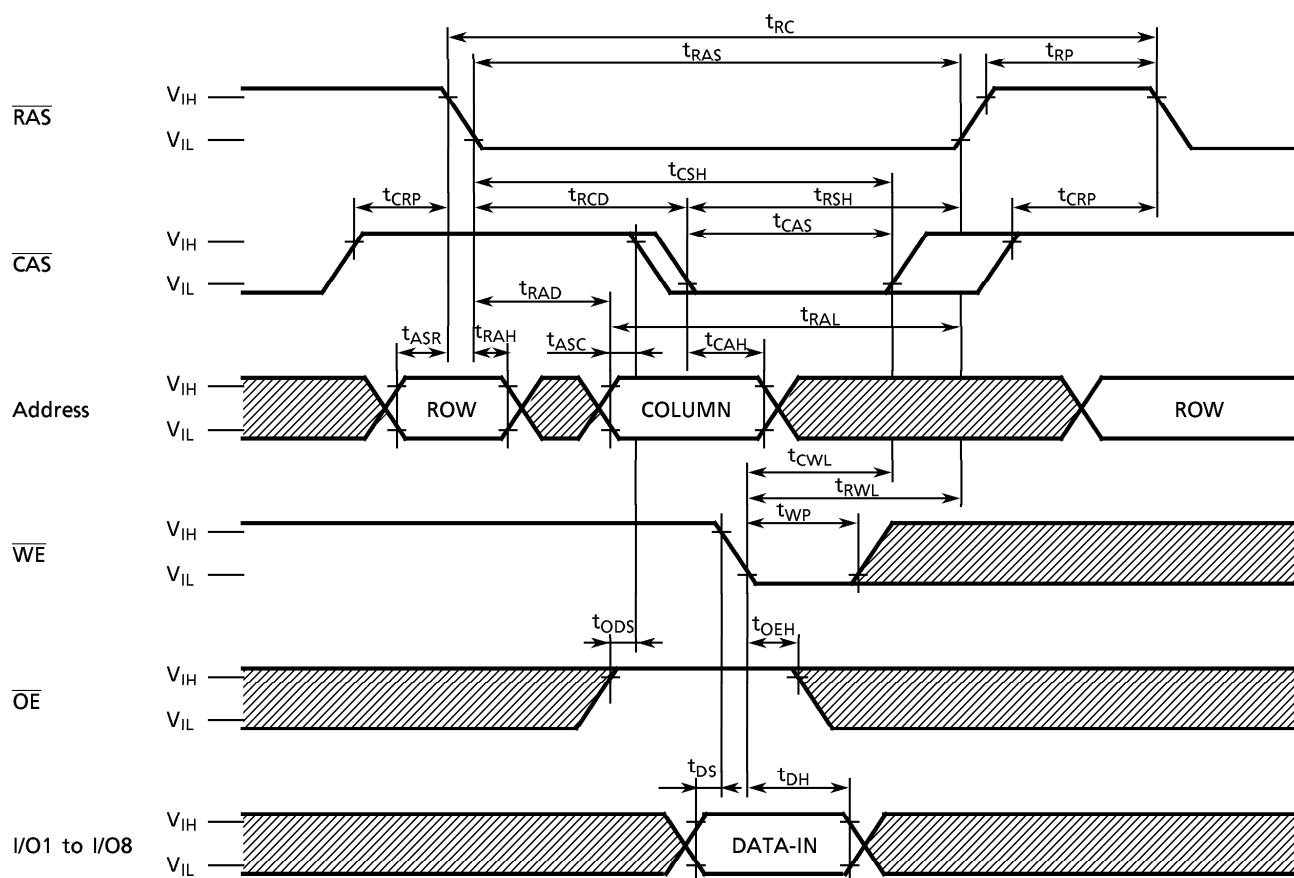


WRITE CYCLE (EARLY WRITE)

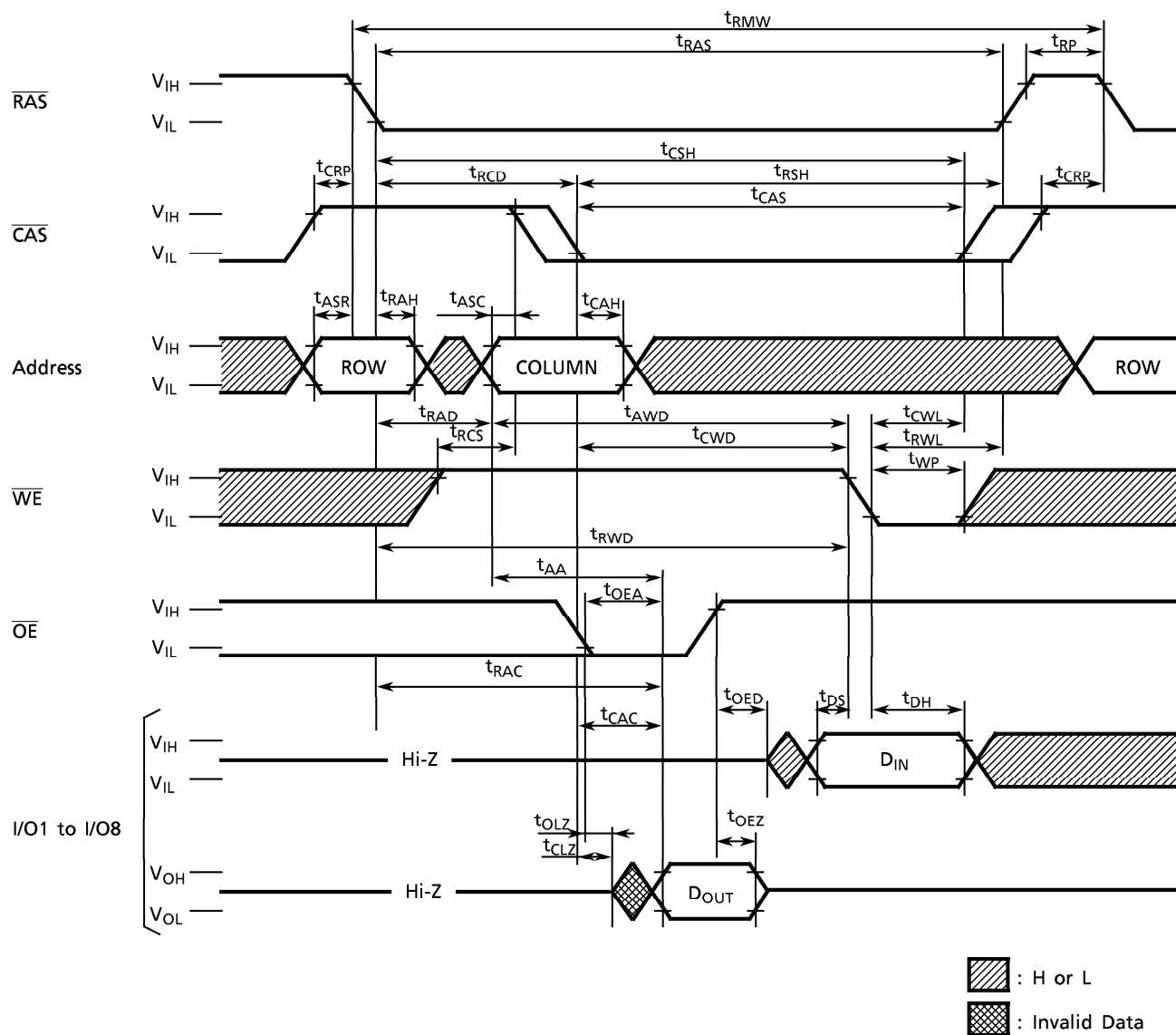


Note:  $D_{OUT} = \text{Hi-Z}$

 : H or L

OE-CONTROLLED WRITE CYCLENote:  $D_{OUT} = \text{Hi-Z}$ 
 : H or L

**READ-MODIFY-WRITE CYCLE**

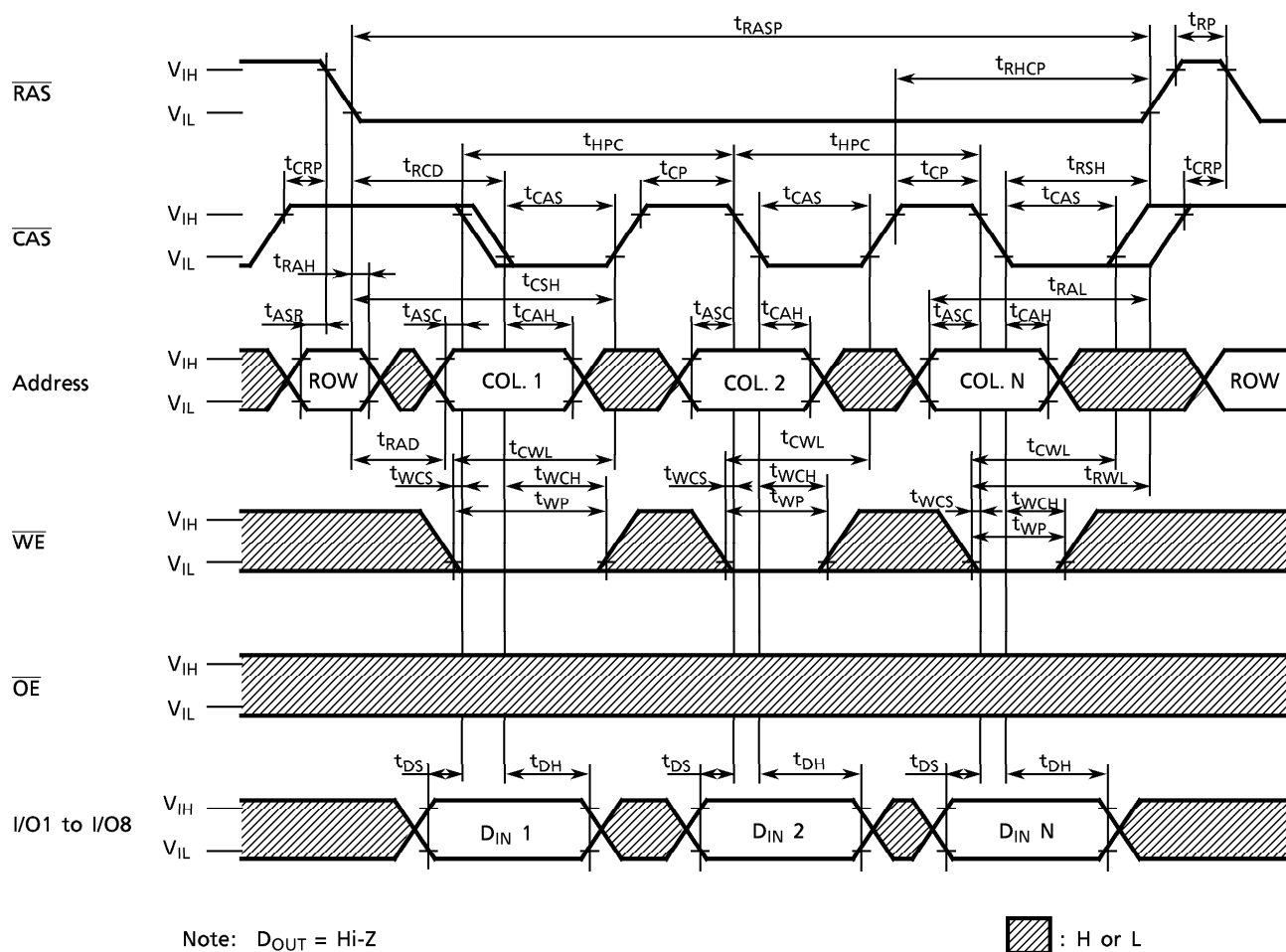


[illegible]

Note:  $D_{IN} = H_i - Z$

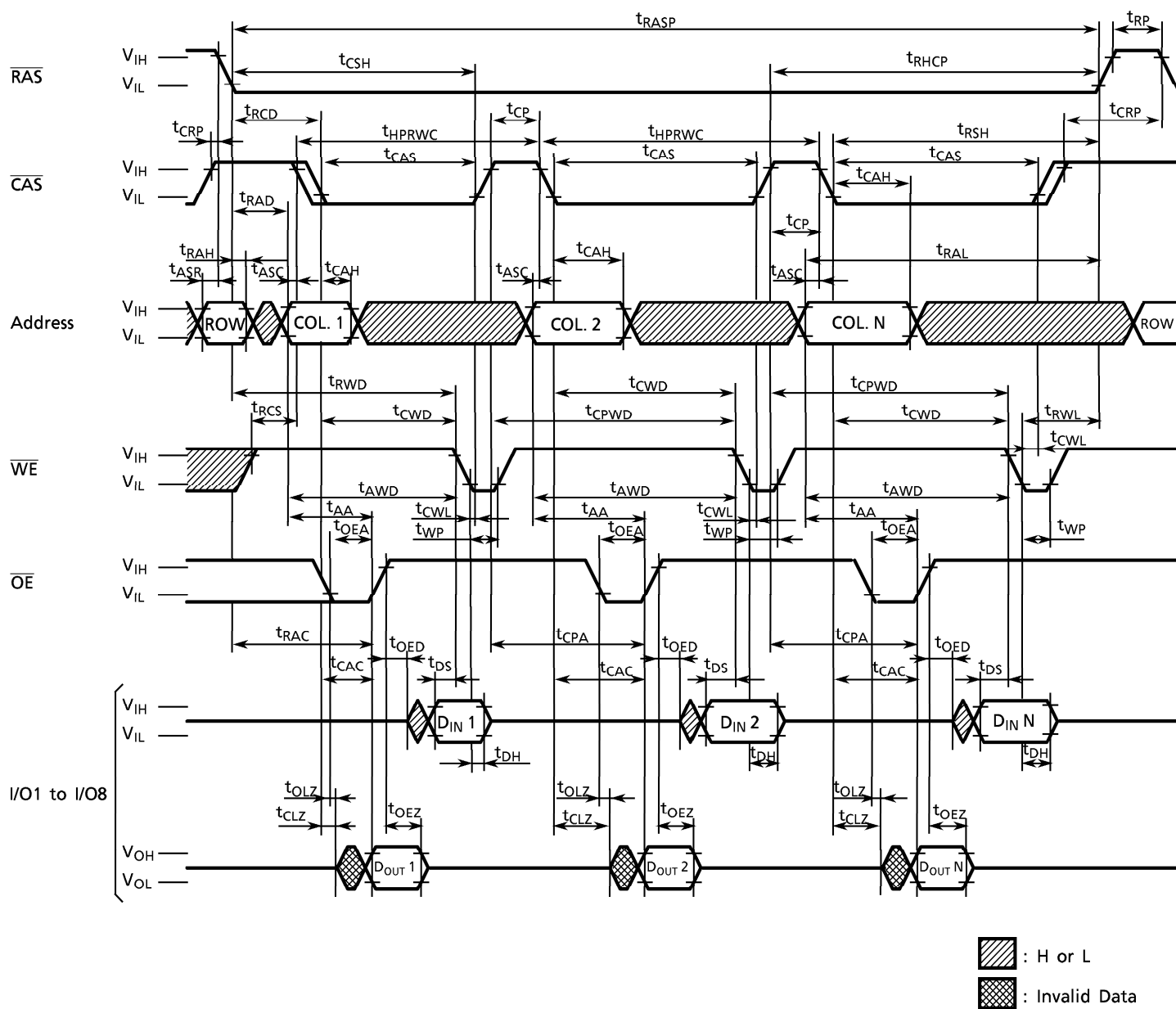
 : H or L  
 : Invalid Data

### HYPER PAGE MODE WRITE CYCLE (EARLY WRITE)



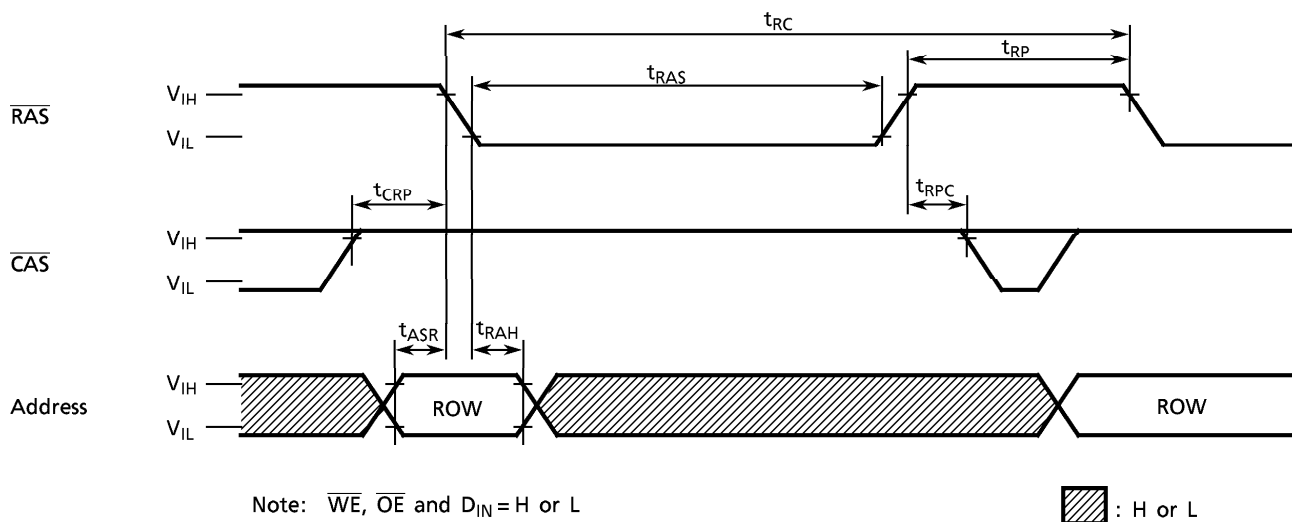


### HYPER PAGE MODE READ-MODIFY-WRITE CYCLE

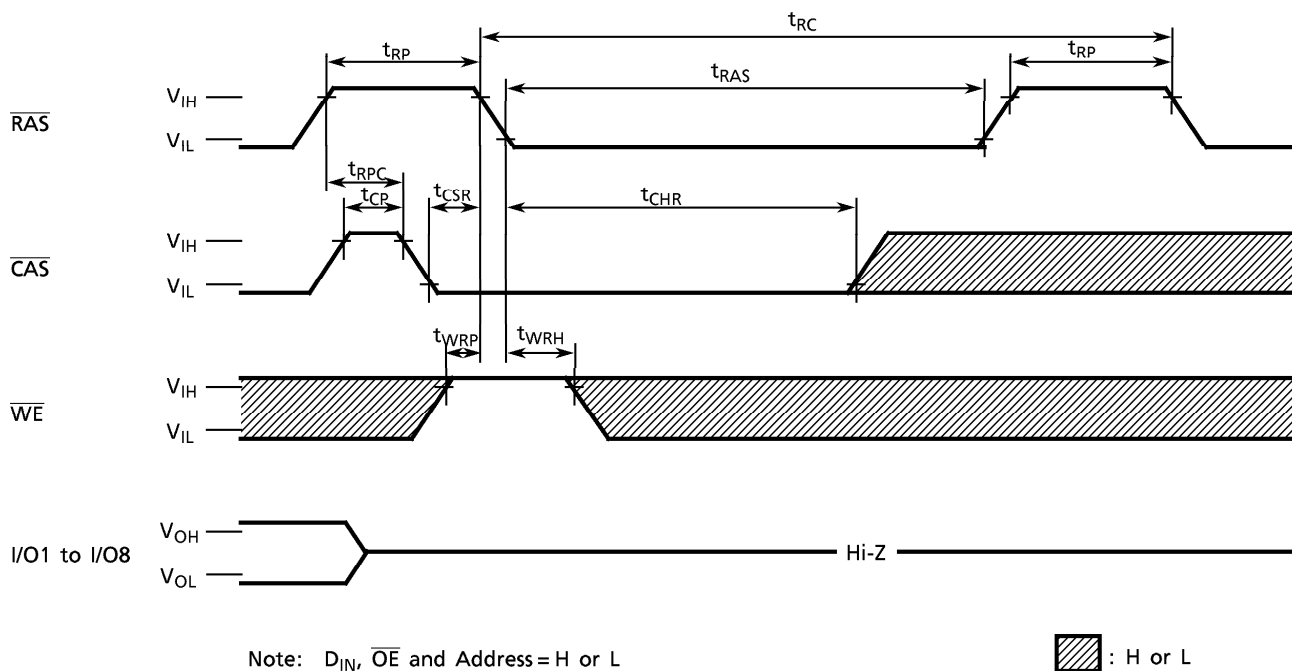




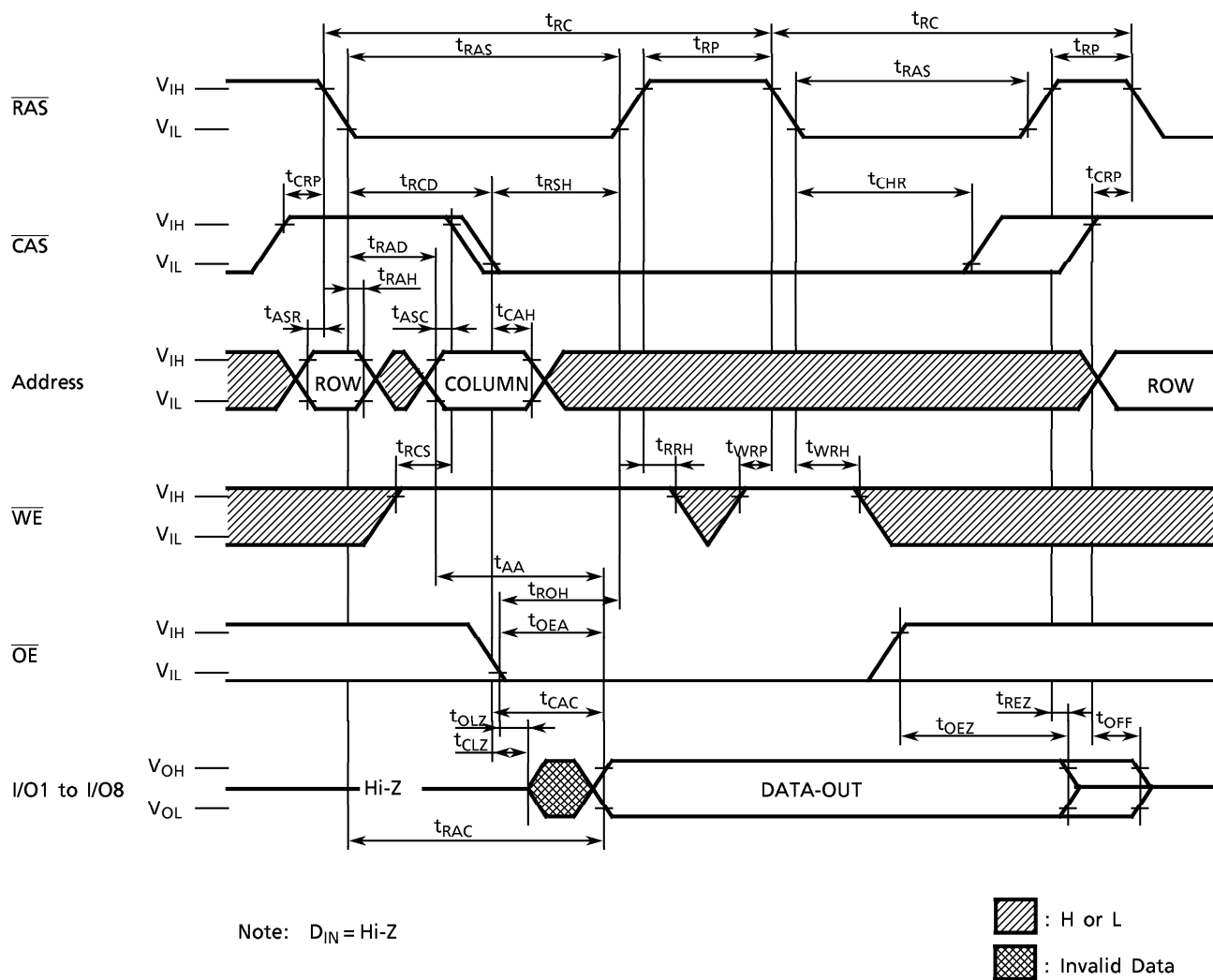
RAS-ONLY REFRESH CYCLE

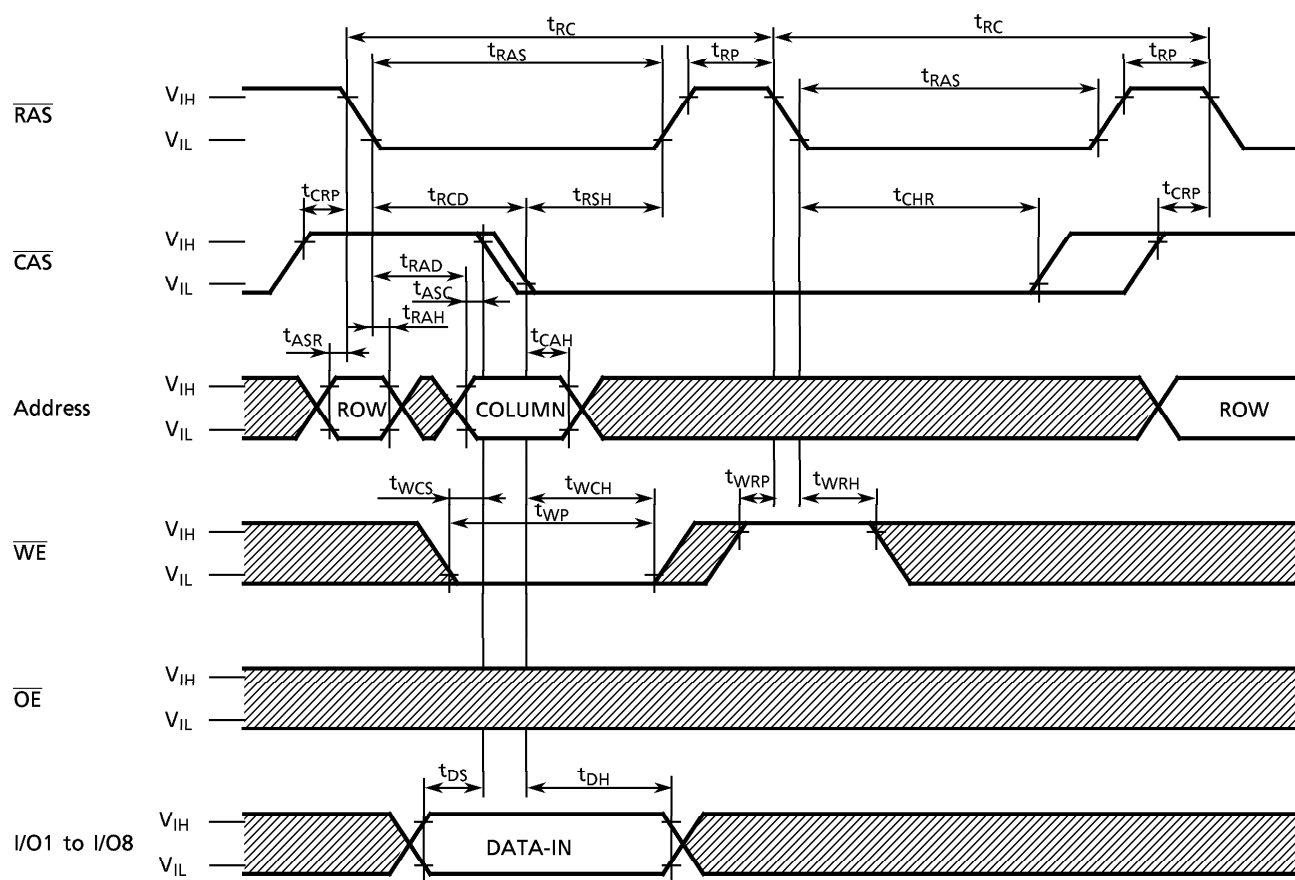


CAS-BEFORE-RAS REFRESH CYCLE

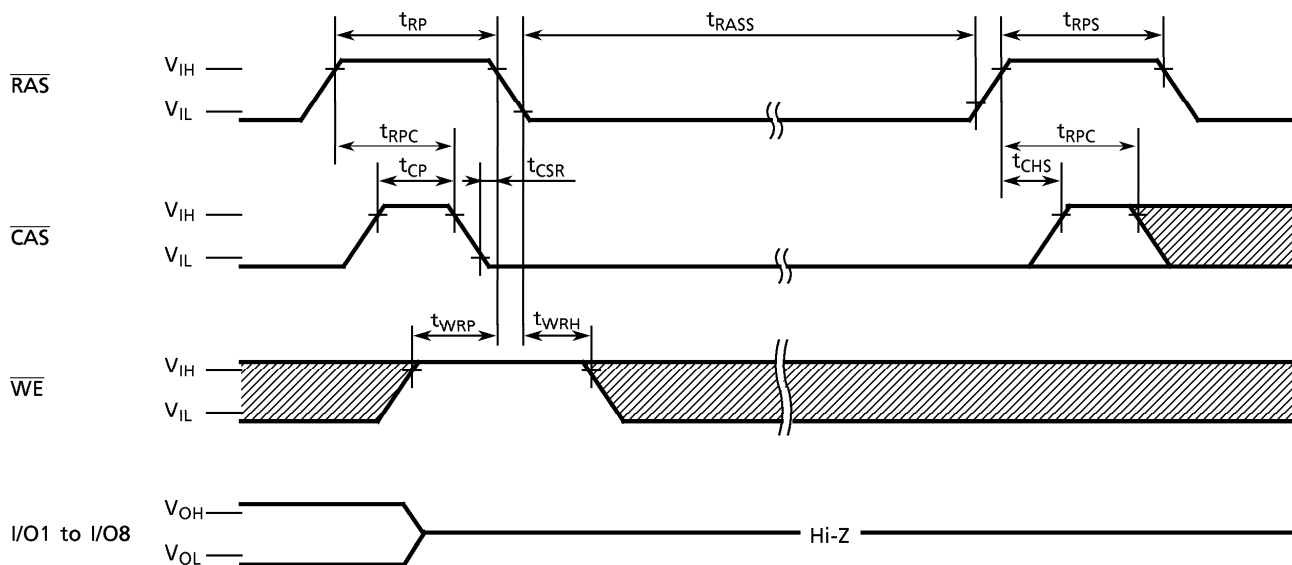


HIDDEN REFRESH CYCLE (READ)



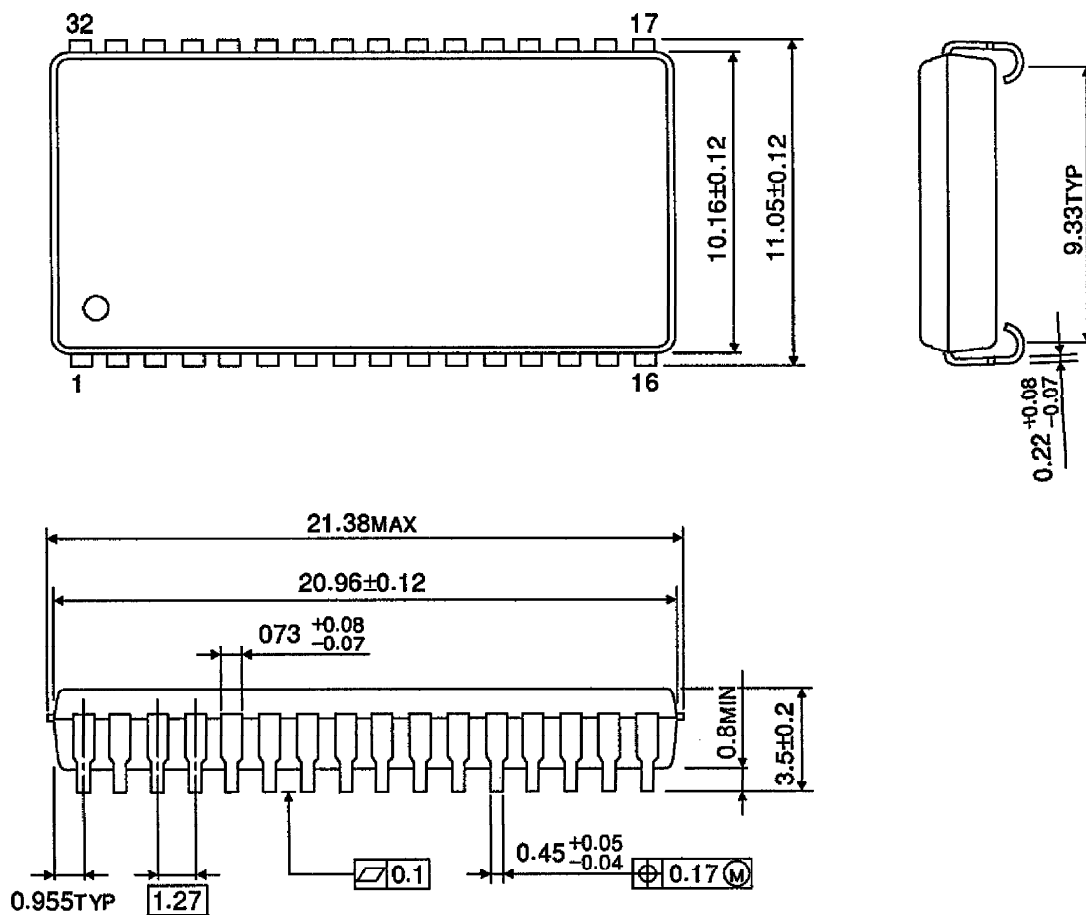
HIDDEN REFRESH CYCLE (WRITE)Note: D<sub>OUT</sub> = Hi-Z

: H or L

CAS-BEFORE-RAS SELF-REFRESH CYCLE (S-version only)

PACKAGE DIMENSIONS (SOJ32 – P – 400 – 1.27B)

Unit: mm



PACKAGE DIMENSIONS (TSOPII 32 – P – 400 – 1.27B)

Unit: mm

