# TC4421/TC4422

## 9A High-Speed MOSFET Drivers

### Features:

- High Peak Output Current: 9A
- Wide Input Supply Voltage Operating Range:
  - 4.5V to 18V
- High Continuous Output Current: 2A Maximum
- Fast Rise and Fall Times:
  - 30 ns with 4,700 pF Load
  - 180 ns with 47,000 pF Load
- Short Propagation Delays: 30 ns (Typical)
- Low Supply Current:
  - With Logic '1' Input – 200 µA (Typical)
  - With Logic '0' Input – 55 µA (Typical)
- Low Output Impedance: 1.4Ω (Typical)
- Latch-Up Protected: Will Withstand 1.5A Output Reverse Current
- Input Will Withstand Negative Inputs up to 5V
- Pin-Compatible with the TC4420/TC4429 6A MOSFET Driver
- Space-saving 8-Pin 6x5 DFN-S Package

### Applications:

- Line Drivers for Extra Heavily-Loaded Lines
- Pulse Generators
- Driving the Largest MOSFETs and IGBTs
- Local Power ON/OFF Switch
- Motor and Solenoid Driver

### General Description:

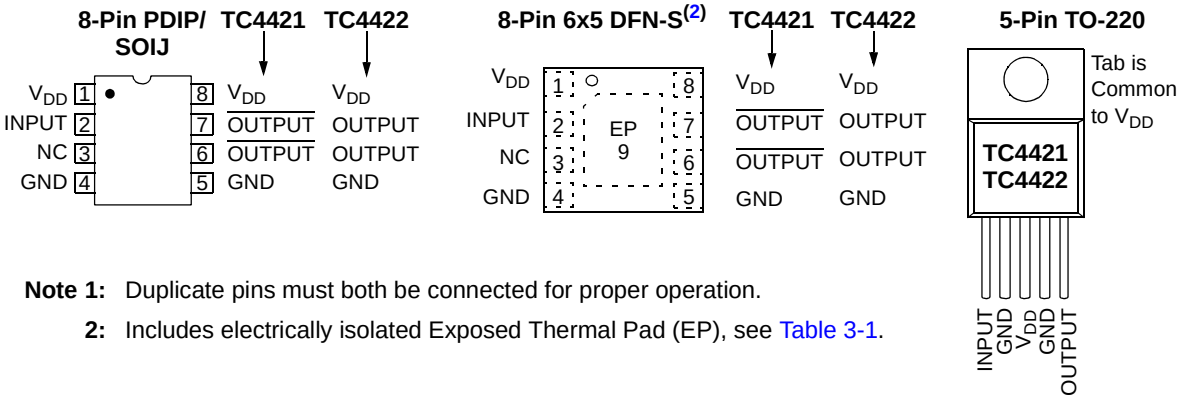
TC4421/TC4422 are high-current buffers/drivers capable of driving large MOSFETs and IGBTs.

These devices are essentially immune to any form of upset, except direct overvoltage or over-dissipation. They cannot be latched under any conditions within their power and voltage ratings. These parts are not subject to damage or improper operation when up to 5V of ground bounce is present on their ground terminals. They can accept, without damage or logic upset, more than 1A inductive current of either polarity being forced back into their outputs. In addition, all terminals are fully protected against up to 4 kV of electrostatic discharge.

The TC4421/TC4422 inputs may be driven directly from either TTL or CMOS (3V to 18V). In addition, 300 mV of hysteresis is built into the input, providing noise immunity and allowing the device to be driven from slowly rising or falling waveforms.

With both surface-mount and pin-through-hole packages and four operating temperature range offerings, the TC4421/TC4422 family of 9A MOSFET drivers fits into any application where high gate/line capacitance drive is required.

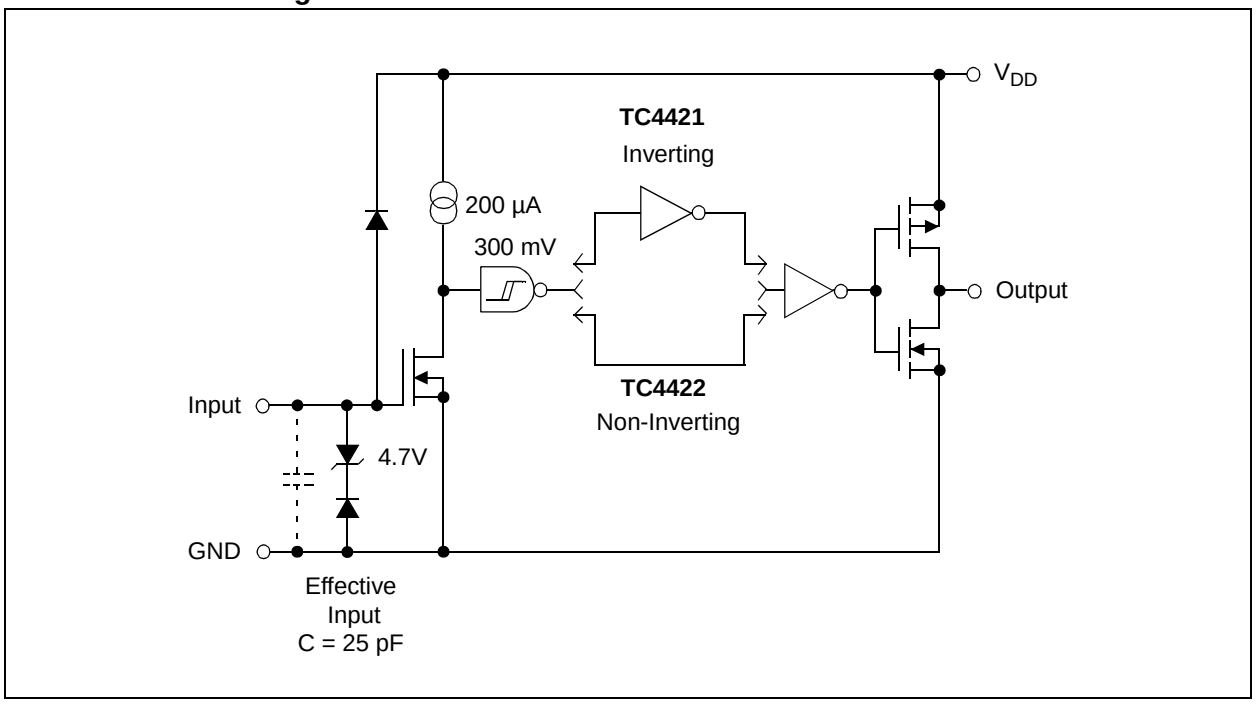
### Package Types(1)




**Note 1:** Duplicate pins must both be connected for proper operation.

**2:** Includes electrically isolated Exposed Thermal Pad (EP), see Table 3-1.

## Functional Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

Supply Voltage ..... +20V
Input Voltage ..... ($V_{DD}$ + 0.3V) to (GND – 5V)
Input Current ($V_{IN}$ > $V_{DD}$) ..... 50 mA
Package Power Dissipation ($T_A \leq 70°C$)
5-Pin TO-220 ..... 1.6W
DFN-S ..... **Note 2**
PDIP ..... 730 mW
SOIJ ..... 750 mW
Package Power Dissipation ($T_A \leq 25°C$)
5-Pin TO-220 (with heatsink) ..... 12.5W
Thermal Impedances (to case)
5-Pin TO-220 $R_{\theta J-C}$ ..... 10°C/W

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

## DC CHARACTERISTICS

**Electrical Specifications:** Unless otherwise noted, $T_A$ = +25°C with 4.5V ≤ $V_{DD}$ ≤ 18V.

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Input** | | | | | | |
| Logic '1', High-Input Voltage | $V_{IH}$ | 2.4 | 1.8 | — | V | |
| Logic '0', Low-Input Voltage | $V_{IL}$ | — | 1.3 | 0.8 | V | |
| Input Current | $I_{IN}$ | –10 | — | +10 | µA | 0V ≤ $V_{IN}$ ≤ $V_{DD}$ |
| **Output** | | | | | | |
| High-Output Voltage | $V_{OH}$ | $V_{DD}$ – 0.025 | — | — | V | DC test |
| Low-Output Voltage | $V_{OL}$ | — | — | 0.025 | V | DC test |
| Output Resistance, High | $R_{OH}$ | — | 1.4 | — | Ω | $I_{OUT}$ = 10 mA, $V_{DD}$ = 18V |
| Output Resistance, Low | $R_{OL}$ | — | 0.9 | 1.7 | Ω | $I_{OUT}$ = 10 mA, $V_{DD}$ = 18V |
| Peak Output Current | $I_{PK}$ | — | 9.0 | — | A | $V_{DD}$ = 18V |
| Continuous Output Current | $I_{DC}$ | 2 | — | — | A | 10V ≤ $V_{DD}$ ≤ 18V, $T_A$ = +25°C (**TC4421/TC4422** CAT only) **(Note 3)** |
| Latch-Up Protection Withstand Reverse Current | $I_{REV}$ | — | > 1.5 | — | A | Duty cycle ≤ 2%, t ≤ 300 µsec |
| **Switching Time (Note 1)** | | | | | | |
| Rise Time | $t_R$ | — | 60 | 75 | ns | **Figure 4-1**, $C_L$ = 10,000 pF |
| Fall Time | $t_F$ | — | 60 | 75 | ns | **Figure 4-1**, $C_L$ = 10,000 pF |
| Delay Time | $t_{D1}$ | — | 30 | 60 | ns | **Figure 4-1** |
| Delay Time | $t_{D2}$ | — | 33 | 60 | ns | **Figure 4-1** |
| **Power Supply** | | | | | | |
| Power Supply Current | $I_S$ | — | 0.2 | 1.5 | mA | $V_{IN}$ = 3V |
| | | — | 55 | 150 | µA | $V_{IN}$ = 0V |
| Operating Input Voltage | $V_{DD}$ | 4.5 | — | 18 | V | |

**Note 1:** Switching times ensured by design.
**2:** Package power dissipation is dependent on the copper pad area on the PCB.
**3:** Tested during characterization, not production tested.

## DC CHARACTERISTICS (OVER OPERATING TEMPERATURE RANGE)

**Electrical Specifications:** Unless otherwise noted, over the operating temperature range with 4.5V ≤ $V_{DD}$ ≤ 18V.

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Input** | | | | | | |
| Logic '1', High-Input Voltage | $V_{IH}$ | 2.4 | — | — | V | |
| Logic '0', Low-Input Voltage | $V_{IL}$ | — | — | 0.8 | V | |
| Input Current | $I_{IN}$ | –10 | — | +10 | µA | 0V ≤ $V_{IN}$ ≤ $V_{DD}$ |
| **Output** | | | | | | |
| High-Output Voltage | $V_{OH}$ | $V_{DD}$ – 0.025 | — | — | V | DC TEST |
| Low-Output Voltage | $V_{OL}$ | — | — | 0.025 | V | DC TEST |
| Output Resistance, High | $R_{OH}$ | — | 2.4 | 3.6 | Ω | $I_{OUT}$ = 10 mA, $V_{DD}$ = 18V |
| Output Resistance, Low | $R_{OL}$ | — | 1.8 | 2.7 | Ω | $I_{OUT}$ = 10 mA, $V_{DD}$ = 18V |
| **Switching Time (Note 1)** | | | | | | |
| Rise Time | $t_R$ | — | 60 | 120 | ns | **Figure 4-1**, $C_L$ = 10,000 pF |
| Fall Time | $t_F$ | — | 60 | 120 | ns | **Figure 4-1**, $C_L$ = 10,000 pF |
| Delay Time | $t_{D1}$ | — | 50 | 80 | ns | **Figure 4-1** |
| Delay Time | $t_{D2}$ | — | 65 | 80 | ns | **Figure 4-1** |
| **Power Supply** | | | | | | |
| Power Supply Current | $I_S$ | — | — | 3 | mA | $V_{IN}$ = 3V |
| | | — | — | 0.2 | | $V_{IN}$ = 0V |
| Operating Input Voltage | $V_{DD}$ | 4.5 | — | 18 | V | |

**Note 1:** Switching times ensured by design.

## TEMPERATURE CHARACTERISTICS

**Electrical Specifications:** Unless otherwise noted, all parameters apply with 4.5V ≤ $V_{DD}$ ≤ 18V.

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Specified Temperature Range (C) | $T_A$ | 0 | — | +70 | °C | |
| Specified Temperature Range (E) | $T_A$ | –40 | — | +85 | °C | |
| Specified Temperature Range (V) | $T_A$ | –40 | — | +125 | °C | |
| Maximum Junction Temperature | $T_J$ | — | — | +150 | °C | |
| Storage Temperature Range | $T_A$ | –65 | — | +150 | °C | |
| **Package Thermal Resistances** | | | | | | |
| Thermal Resistance, 5L-TO-220 | $\theta_{JA}$ | — | 39.5 | — | °C/W | |
| Thermal Resistance, 8L-6x5 DFN-S | $\theta_{JA}$ | — | 35.7 | — | °C/W | Typical 4-layer board with vias to ground plane |
| Thermal Resistance, 8L-PDIP | $\theta_{JA}$ | — | 89.3 | — | °C/W | |
| Thermal Resistance, 8L-SOIJ | $\theta_{JA}$ | — | 117 | — | °C/W | |

## 2.0 TYPICAL PERFORMANCE CURVES

| | |
|---|---|
| **Note:** | The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range. |

**Note:** Unless otherwise indicated, $T_A$ = +25°C with 4.5V ≤ $V_{DD}$ ≤ 18V.

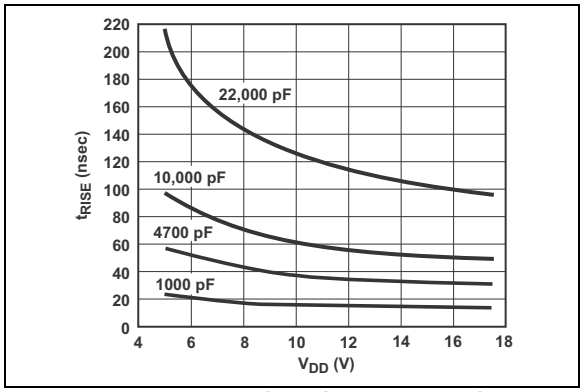



***FIGURE 2-1:*** *Rise Time vs. Supply Voltage.*

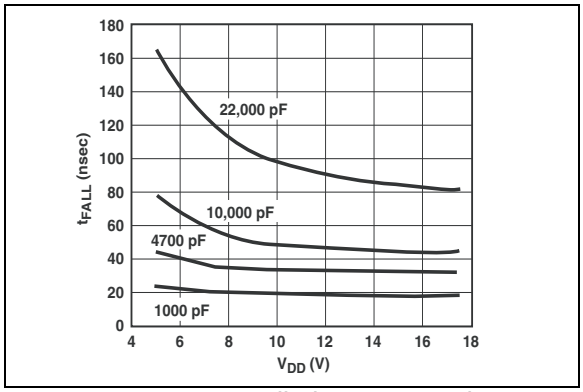



***FIGURE 2-4:*** *Fall Time vs. Supply Voltage.*

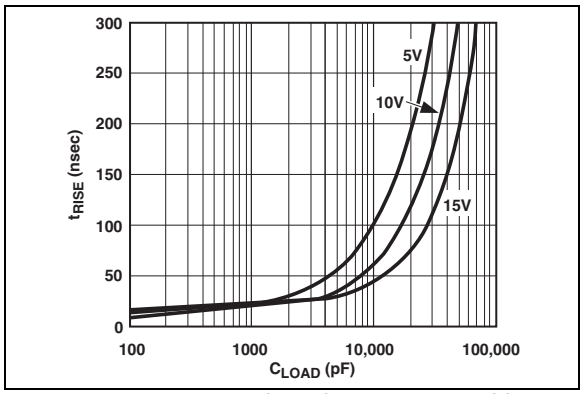



***FIGURE 2-2:*** *Rise Time vs. Capacitive Load.*

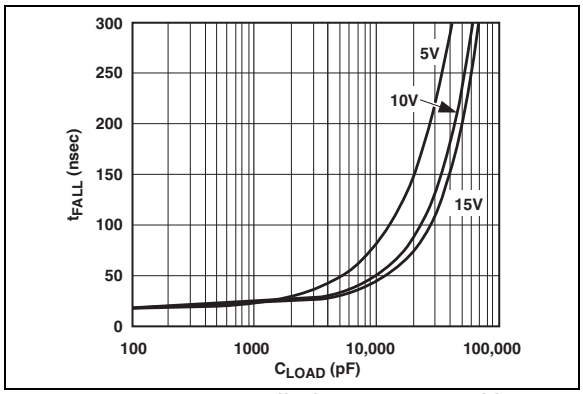



***FIGURE 2-5:*** *Fall Time vs. Capacitive Load.*

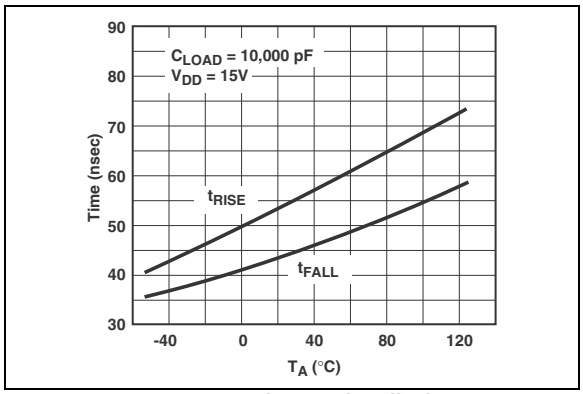



***FIGURE 2-3:*** *Rise and Fall Times vs. Temperature.*

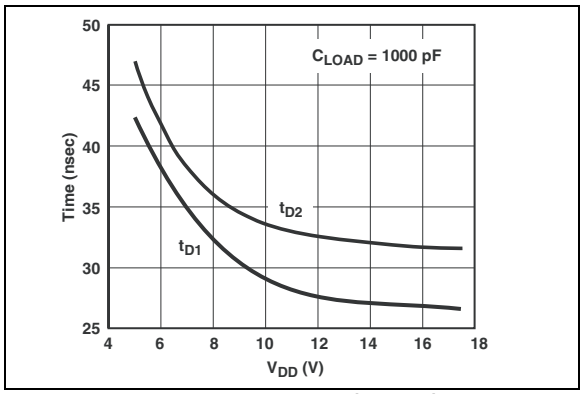



***FIGURE 2-6:*** *Propagation Delay vs. Supply Voltage.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C with 4.5V ≤ $V_{DD}$ ≤ 18V.

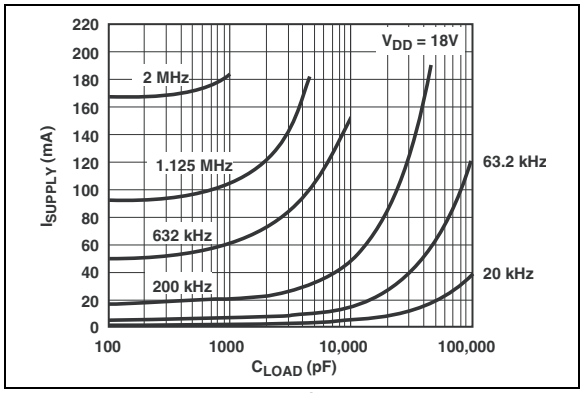



***FIGURE 2-7:*** *Supply Current vs. Capacitive Load ($V_{DD}$ = 18V).*

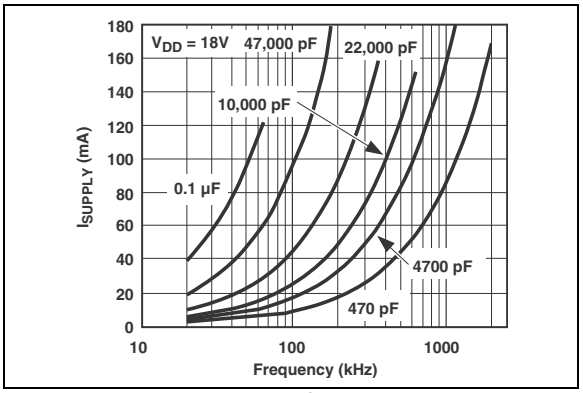



***FIGURE 2-10:*** *Supply Current vs. Frequency ($V_{DD}$ = 18V).*

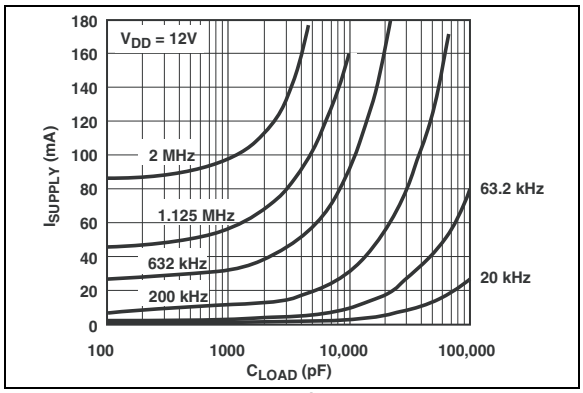



***FIGURE 2-8:*** *Supply Current vs. Capacitive Load ($V_{DD}$ = 12V).*

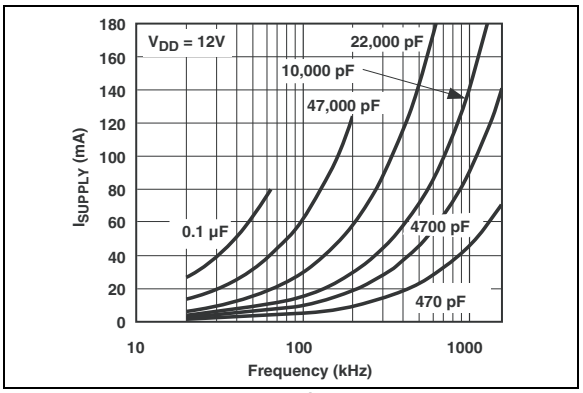



***FIGURE 2-11:*** *Supply Current vs. Frequency ($V_{DD}$ = 12V).*

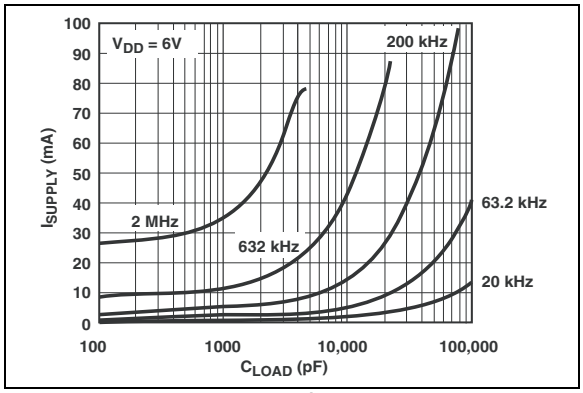



***FIGURE 2-9:*** *Supply Current vs. Capacitive Load ($V_{DD}$ = 6V).*

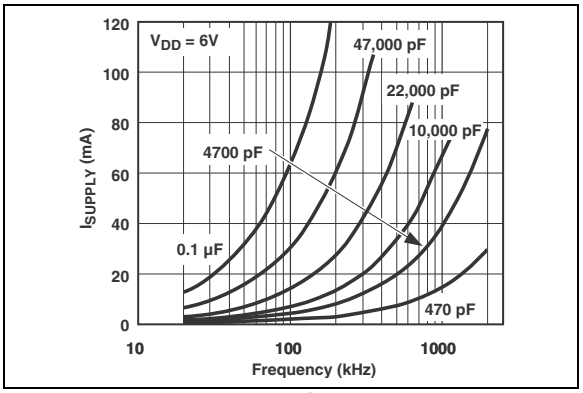



***FIGURE 2-12:*** *Supply Current vs. Frequency ($V_{DD}$ = 6V).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C with 4.5V ≤ $V_{DD}$ ≤ 18V.

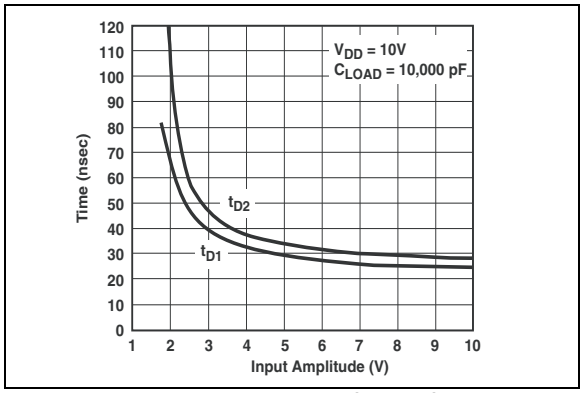



***FIGURE 2-13:*** *Propagation Delay vs. Input Amplitude.*

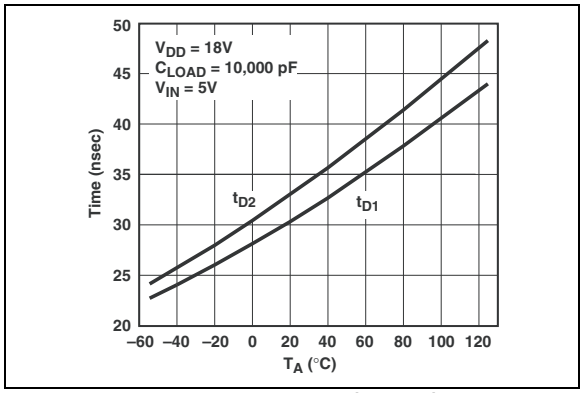



***FIGURE 2-16:*** *Propagation Delay vs. Temperature.*

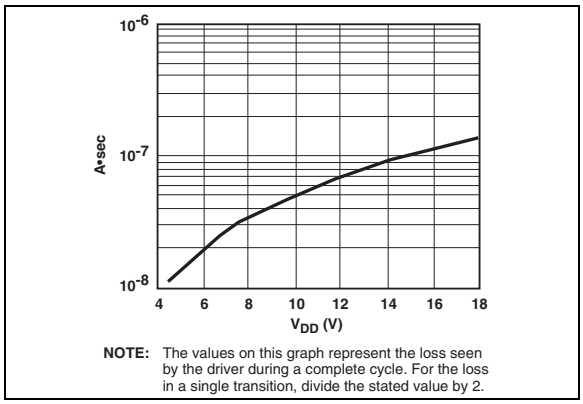



***FIGURE 2-14:*** *Crossover Energy vs. Supply Voltage.*

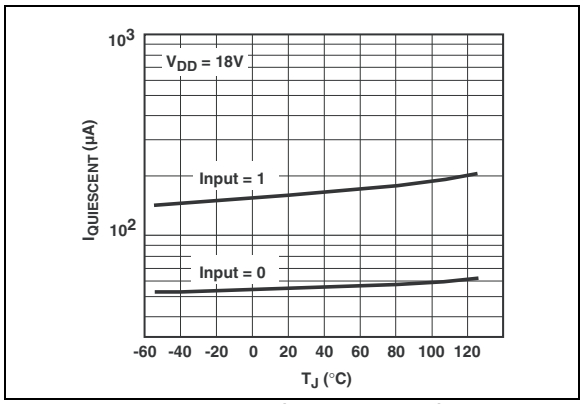



***FIGURE 2-17:*** *Quiescent Supply Current vs. Temperature.*

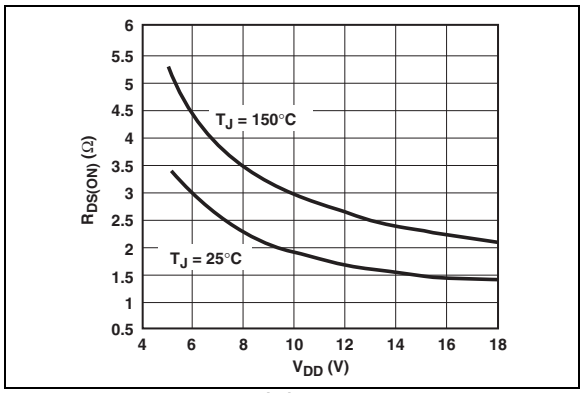



***FIGURE 2-15:*** *High-State Output Resistance vs. Supply Voltage.*

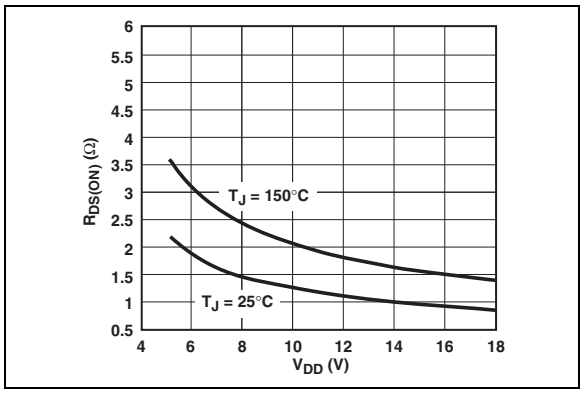



***FIGURE 2-18:*** *Low-State Output Resistance vs. Supply Voltage.*

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

**TABLE 3-1: PIN FUNCTION TABLE**

| Pin No. PDIP, SOIJ | Pin No. 6x5 DFN-S | Pin No. TO-220 | Symbol | Description |
|---|---|---|---|---|
| 1 | 1 | — | $V_{DD}$ | Supply input, 4.5V to 18V |
| 2 | 2 | 1 | INPUT | Control input, TTL/CMOS compatible input |
| 3 | 3 | — | NC | No connection |
| 4 | 4 | 2 | GND | Ground |
| 5 | 5 | 4 | GND | Ground |
| 6 | 6 | 5 | OUTPUT/$\overline{\text{OUTPUT}}$ | CMOS push-pull output |
| 7 | 7 | — | OUTPUT/$\overline{\text{OUTPUT}}$ | CMOS push-pull output |
| 8 | 8 | 3 | $V_{DD}$ | Supply input, 4.5V to 18V |
| — | 9 | — | EP | Exposed thermal pad |
| — | — | TAB | $V_{DD}$ | Thermal tab is at the $V_{DD}$ potential |

### 3.1 Supply Input ($V_{DD}$)

The $V_{DD}$ input is the bias supply for the MOSFET driver and is rated for 4.5V to 18V with respect to the ground pin. The $V_{DD}$ input should be bypassed to ground with a local ceramic capacitor. The value of the capacitor should be chosen based on the capacitive load that is being driven. A minimum value of 1.0 µF is suggested.

### 3.2 Control Input (INPUT)

The MOSFET driver input is a high-impedance, TTL/CMOS compatible input. The input also has 300 mV of hysteresis between the high and low thresholds that prevents output glitching even when the rise and fall time of the input signal is very slow.

### 3.3 CMOS Push-Pull Output (OUTPUT, $\overline{\text{OUTPUT}}$)

The MOSFET driver output is a low-impedance, CMOS, push-pull style output capable of driving a capacitive load with 9.0A peak currents. The MOSFET driver output is capable of withstanding 1.5A peak reverse currents of either polarity.

### 3.4 Ground (GND)

The ground pins are the return path for the bias current and for the high peak currents that discharge the load capacitor. The ground pins should be tied into a ground plane or have very short traces to the bias supply source return.

### 3.5 Exposed Thermal Pad (EP)

The exposed thermal pad of the 6x5 DFN-S package is not internally connected to any potential. Therefore, this pad can be connected to a ground plane or other copper plane on a printed circuit board to aid in heat removal from the package.

## 4.0 APPLICATIONS INFORMATION

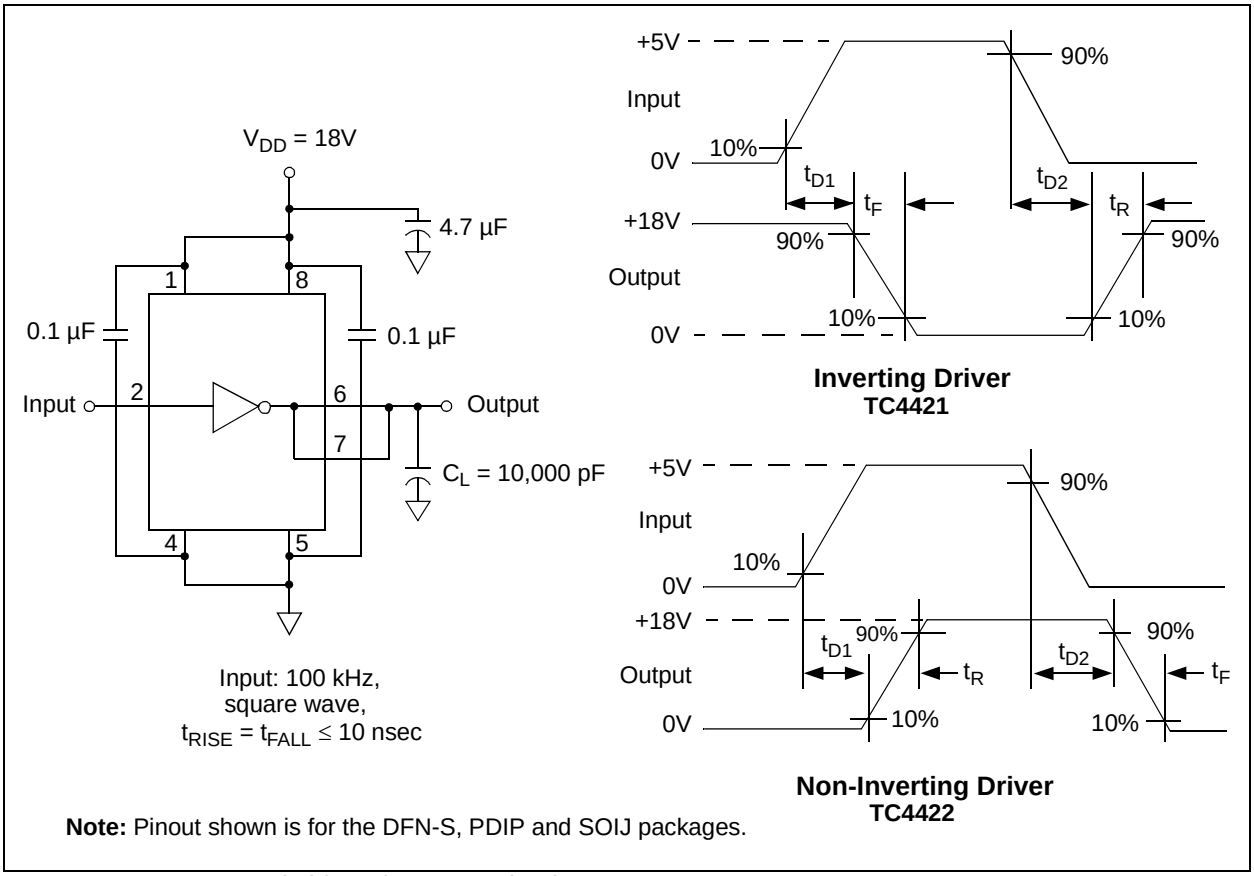
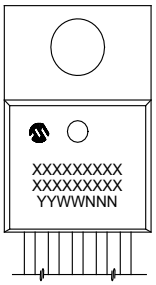



***FIGURE 4-1:*** *Switching Time Test Circuits.*

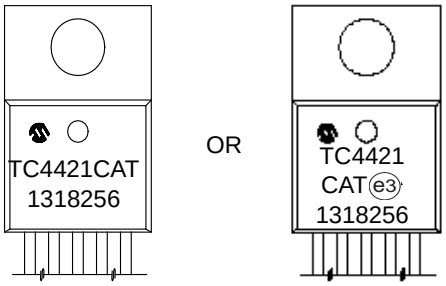
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

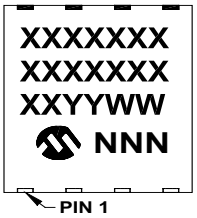
5-Lead TO-220



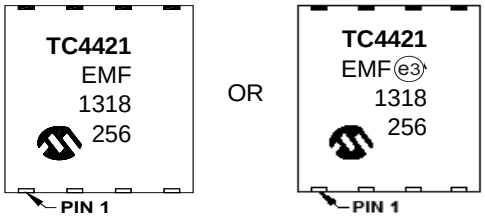

Example



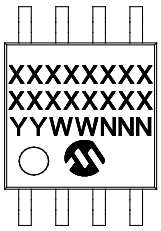

8-Lead DFN-S (6x5x0.9 mm)



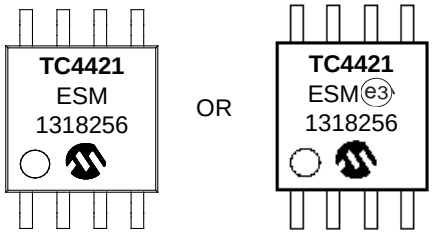

Example



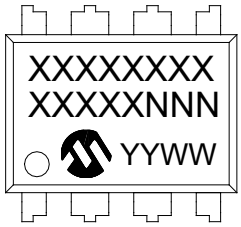

8-Lead SOIJ (5.28 mm)



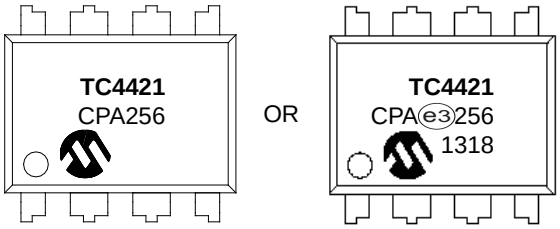

Example




8-Lead PDIP (300 mil)




Example

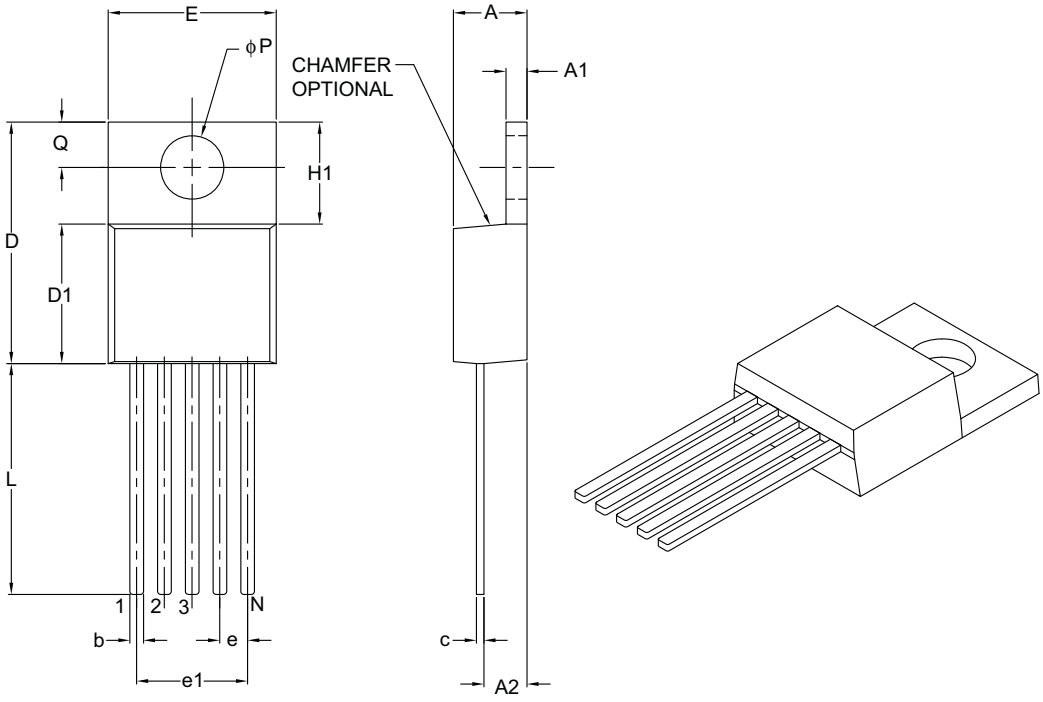



| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 5-Lead Plastic Transistor Outline (AT) [TO-220]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 5 | |
| Pitch | e | | .067 BSC | |
| Overall Pin Pitch | e1 | | .268 BSC | |
| Overall Height | A | .140 | – | .190 |
| Overall Width | E | .380 | – | .420 |
| Overall Length | D | .560 | – | .650 |
| Molded Package Length | D1 | .330 | – | .355 |
| Tab Length | H1 | .204 | – | .293 |
| Tab Thickness | A1 | .020 | – | .055 |
| Mounting Hole Center | Q | .100 | – | .120 |
| Mounting Hole Diameter | ϕP | .139 | – | .156 |
| Lead Length | L | .482 | – | .590 |
| Base to Bottom of Lead | A2 | .080 | – | .115 |
| Lead Thickness | c | .012 | – | .025 |
| Lead Width | b | .015 | .027 | .040 |

**Notes:**

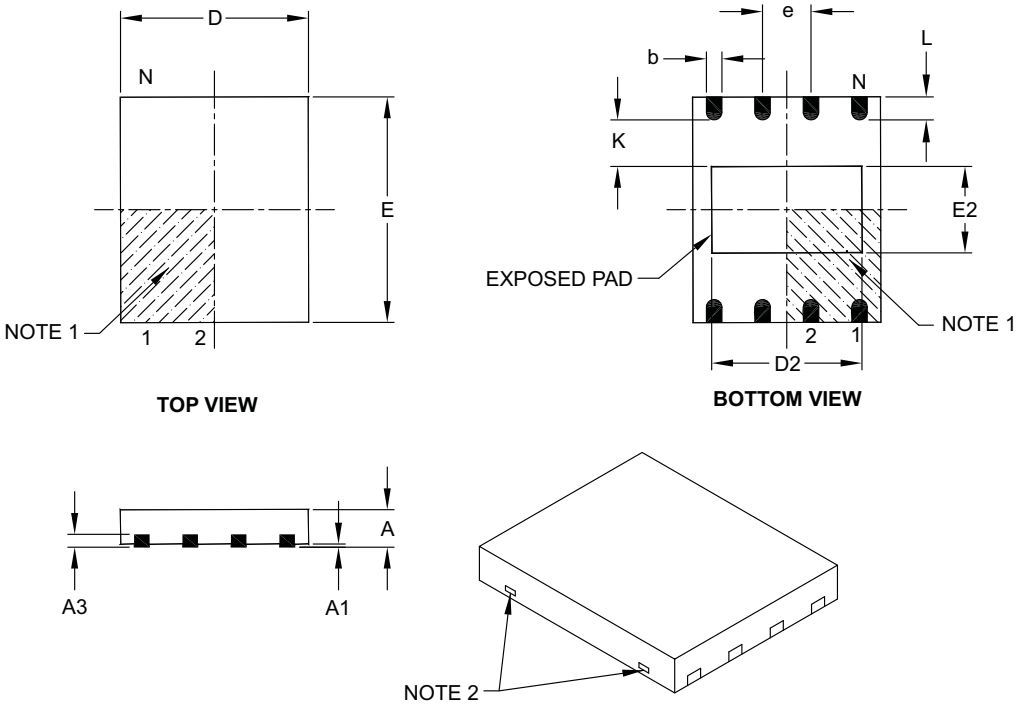
1. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-036B

## 8-Lead Plastic Dual Flat, No Lead Package (MF) – 6x5 mm Body [DFN-S]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | 0.80 | 0.85 | 1.00 |
| Standoff | A1 | 0.00 | 0.01 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 5.00 BSC | |
| Overall Width | E | | 6.00 BSC | |
| Exposed Pad Length | D2 | 3.90 | 4.00 | 4.10 |
| Exposed Pad Width | E2 | 2.20 | 2.30 | 2.40 |
| Contact Width | b | 0.35 | 0.40 | 0.48 |
| Contact Length | L | 0.50 | 0.60 | 0.75 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

**Notes:**

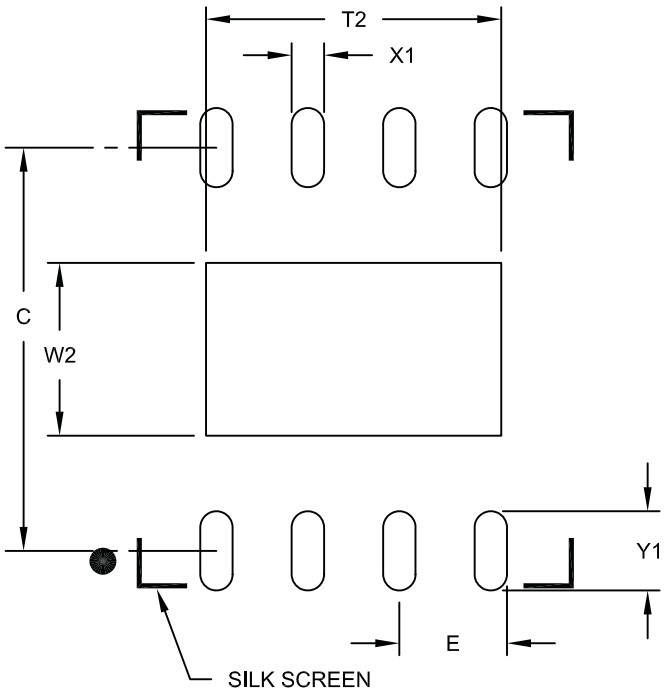
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

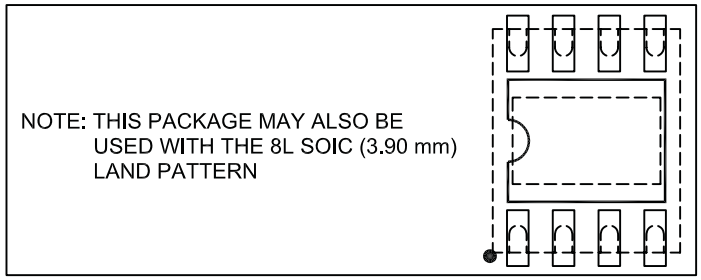
Microchip Technology Drawing C04-122B

8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Optional Center Pad Width | W2 | | | 2.40 |
| Optional Center Pad Length | T2 | | | 4.10 |
| Contact Pad Spacing | C | | 5.60 | |
| Contact Pad Width (X8) | X1 | | | 0.45 |
| Contact Pad Length (X8) | Y1 | | | 1.10 |

Notes:

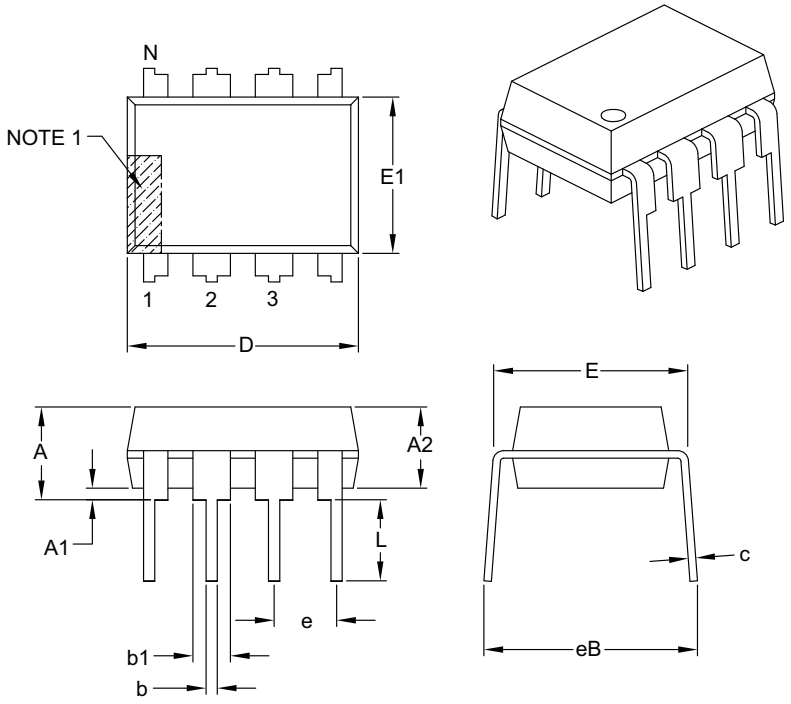
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2122A

## 8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

**Notes:**

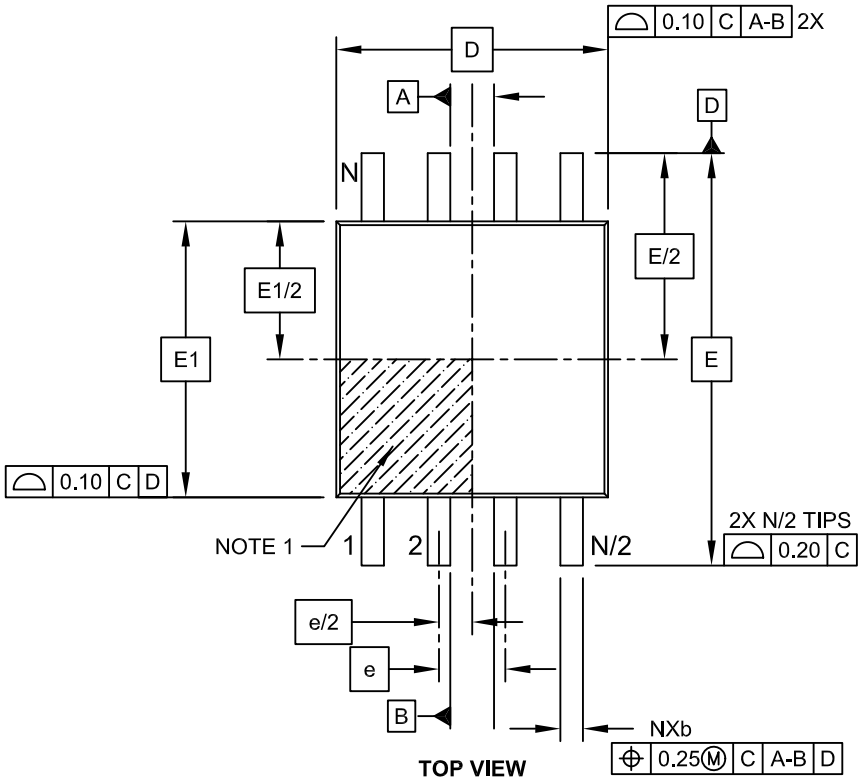
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

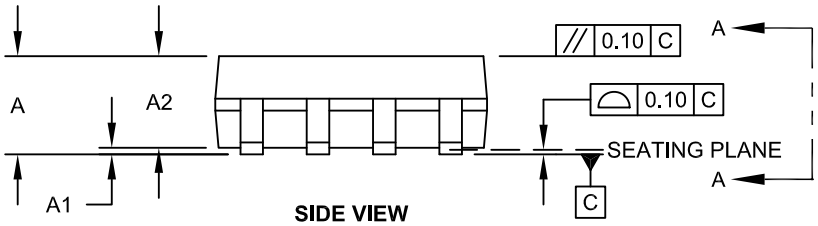
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

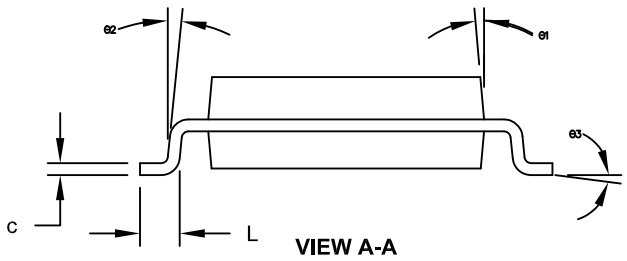
Microchip Technology Drawing C04-018B

### 8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



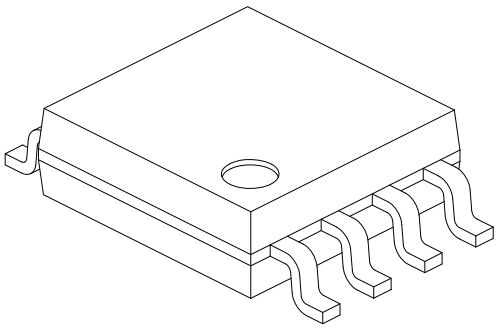




Microchip Technology Drawing C04-056C Sheet 1 of 2

### 8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | 1.77 | - | 2.03 |
| Standoff § | A1 | 0.05 | | 0.25 |
| Molded Package Thickness | A2 | 1.75 | - | 1.98 |
| Overall Width | E | | 7.94 BSC | |
| Molded Package Width | E1 | | 5.25 BSC | |
| Overall Length | D | | 5.26 BSC | |
| Foot Length | L | 0.51 | - | 0.76 |
| Lead Thickness | c | 0.15 | - | 0.25 |
| Lead Width | b | 0.36 | - | 0.51 |
| Mold Draft Angle | Θ1 | - | - | 15° |
| Lead Angle | Θ2 | 0° | - | 8° |
| Foot Angle | Θ3 | 0° | - | 8° |

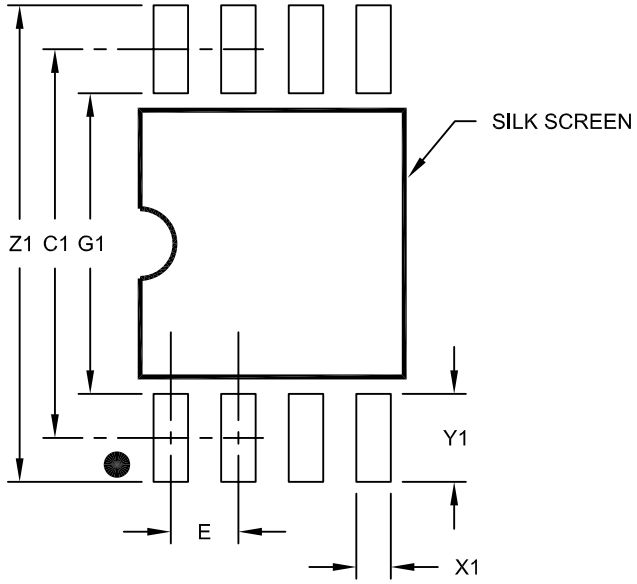
Notes:

1. SOIJ, JEITA/EIAJ Standard, Formerly called SOIC
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.

Microchip Technology Drawing No. C04-056C Sheet 2 of 2

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Overall Width | Z1 | | | 9.00 |
| Contact Pad Spacing | C1 | | 7.30 | |
| Contact Pad Width (X8) | X1 | | | 0.65 |
| Contact Pad Length (X8) | Y1 | | | 1.70 |
| Distance Between Pads | G1 | 5.60 | | |
| Distance Between Pads | G | 0.62 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2056C

**NOTES:**

# APPENDIX A: REVISION HISTORY

## Revision F (August 2013)

The following is the list of modifications:

1. Updated package type for 8-Pin 6x5 DFN-S in Package Types(1).
2. Updated the values in Temperature Characteristics.
3. Updated the markings in Section 5.0, Packaging Information.
4. Replaced all references to DFN and SOIC with DFN-S and SOIJ, respectively.

## Revision E (December 2012)

- Added a note to each package outline drawing.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | XX | XXX | X |
|---|---|---|---|---|
| Device | Temperature Range | Package | Tape & Reel | PB Free |

| | | |
|---|---|---|
| **Device:** | TC4421: | 9A High-Speed MOSFET Driver, Inverting |
| | TC4422: | 9A High-Speed MOSFET Driver, Non-Inverting |
| **Temperature Range:** | C = | 0°C to +70°C (PDIP and TO-220 Only) |
| | E = | -40°C to +85°C |
| | V = | -40°C to +125°C |
| **Package:** | AT = | TO-220, 5-lead (C-Temp Only) |
| | MF = | Dual, Flat, No-Lead (6x5 mm Body), 8-lead |
| | MF713 = | Dual, Flat, No-Lead (6x5 mm Body), 8-lead (Tape and Reel) |
| | PA = | Plastic DIP (300 mil Body), 8-lead |
| | SM = | Plastic SOIJ (208 mil Body), 8-lead |
| | SM713 = | Plastic SOIJ (208 mil Body), 8-lead (Tape and Reel) |
| **PB Free:** | G = | Lead-Free device |
| | = | Blank |

**Examples:**

a) TC4421CAT: 9A High-Speed Inverting MOSFET Driver, TO-220 package, 0°C to +70°C.

b) TC4421ESMG: 9A High-Speed Inverting MOSFET Driver, PB Free SOIJ package, -40°C to +85°C.

c) TC4421VMF: 9A High-Speed Inverting MOSFET Driver, DFN-S package, -40°C to +125°C.

a) TC4422VPA: 9A High-Speed Non-Inverting MOSFET Driver, PDIP package, -40°C to +125°C.

b) TC4422EPA: 9A High-Speed Non-Inverting MOSFET Driver, PDIP package, -40°C to +85°C.

c) TC4422EMF: 9A High-Speed Inverting MOSFET Driver, DFN-S package, -40°C to +85°C.

**NOTES:**

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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