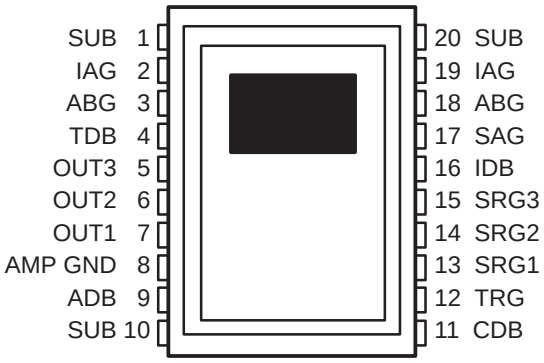
- **High-Resolution, Solid-State Image Sensor for PAL B/W TV Applications**
- **8-mm Image-Area Diagonal, Compatible With 1/2” Vidicon Optics**
- **699 (H) x 288 (V) Active Elements in Image-Sensing Area**
- **Low Dark Current**
- **Electron-Hole Recombination Antiblooming**
- **Dynamic Range . . . More Than 70 dB**
- **High Sensitivity**
- **High Photoresponse Uniformity**
- **High Blue Response**
- **Single-Phase Clocking**
- **Solid-State Reliability With No Image Burn-in, Residual Imaging, Image Distortion, Image Lag, or Microphonics**

DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TC277 is a frame-transfer charge-coupled device (CCD) image sensor designed for use in single-chip B/W PAL TV applications. The device is intended to replace a 1/2-inch vidicon tube in applications requiring small size, high reliability, and low cost.

The image-sensing area of the TC277 is configured into 288 lines with 699 elements in each line. Thirty-three elements are provided in each line for dark reference. The blooming-protection feature incorporated into the sensor is based on recombining excess charge with charge of opposite polarity in the substrate. This antiblooming is activated by supplying clocking pulses to the antiblooming gate, which is an integral part of each image-sensing element.

The sensor is designed to operate in an interlace mode, electronically displacing the image-sensing elements by one-half of a vertical line during the charge-integration period in alternate fields, and effectively increasing the vertical resolution and minimizing aliasing. The device can also be run as a 732 (H) by 288 (V) noninterlaced sensor with significant reduction in the dark signal. The image is read out through three outputs, each of which reads out every third column.

A gated floating-diffusion detection structure with an automatic reset and voltage reference incorporated on-chip converts charge to signal voltage. A low-noise, two-stage, source-follower amplifier buffers the output and provides high output-drive capability.

The TC277 is built using TI-proprietary virtual-phase technology, which provides devices with high blue response, low dark current, high photoresponse uniformity, and single-phase clocking. The TC277 is characterized for operation from –10°C to 45°C.



This MOS device contains limited built-in gate protection. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to SUB. Under no circumstances should pin voltages exceed absolute maximum ratings. Avoid shorting OUTn to ADB during operation to prevent damage to the amplifier. The device can also be damaged if the output terminals are reverse-biased and an excessive current is allowed to flow. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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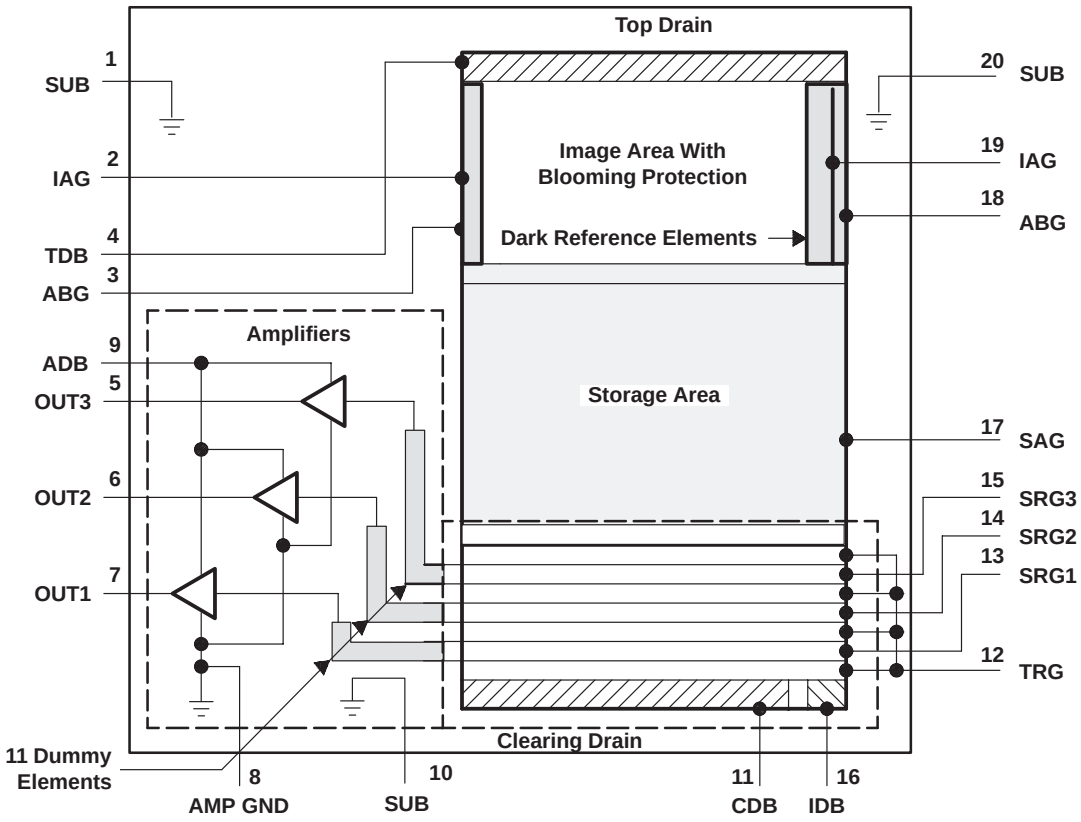
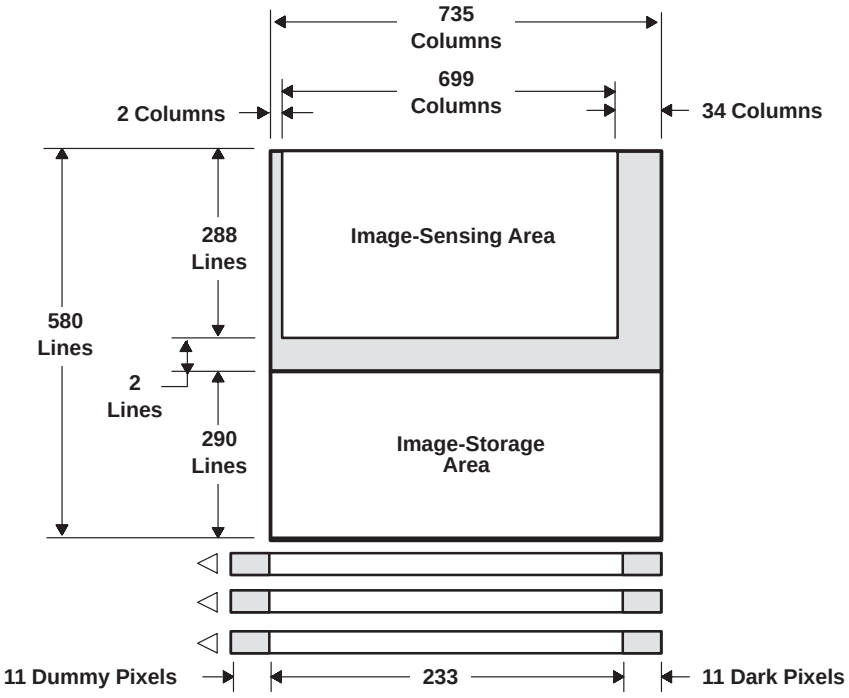
functional block diagram



sensor topology diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ABG†	3	I	Antiblooming gate
ABG†	18	I	Antiblooming gate
ADB	9	I	Supply voltage for amplifier-drain bias
AMP GND	8		Amplifier ground
CDB	11	I	Supply voltage for clearing-drain bias
IAG†	2	I	Image-area gate
IAG†	19	I	Image-area gate
IDB	16	I	Supply voltage for input-diode bias
OUT1	7	O	Output signal 1
OUT2	6	O	Output signal 2
OUT3	5	O	Output signal 3
SAG	17	I	Storage-area gate
SRG1	13	I	Serial-register gate 1
SRG2	14	I	Serial-register gate 2
SRG3	15	I	Serial-register gate 3
SUB†	1		Substrate and clock return
SUB†	10		Substrate and clock return
SUB†	20		Substrate and clock return
TDB	4	I	Supply voltage for top-drain bias
TRG	12	I	Transfer gate

† All pins of the same name should be connected together externally.

detailed description

The TC277 consists of four basic functional blocks: (1) the image-sensing area, (2) the image-storage area, (3) the multiplexer with serial registers and transfer gates, and (4) the low-noise signal-processing amplifier with charge-detection nodes. Location of each of these blocks is shown in the functional block diagram.

image-sensing and image-storage areas

Cross sections with potential-well diagrams and top views of image-sensing and storage-area elements are shown in Figure 1 and Figure 2. As light enters the silicon in the image-sensing area, free electrons are generated and collected in the potential wells of the sensing elements. During this time, the antiblooming gate is activated by the application of a burst of pulses every horizontal-blanking interval. This prevents blooming caused by the spilling of charge from overexposed elements into neighboring elements. After the completion of integration, the signal charge is transferred into the storage area.

Thirty-three full columns and one half-column of elements at the right edge of the image-sensing area are shielded from incident light; the 33 full columns of elements provide the dark reference used in subsequent video-processing circuits to restore the video-black level. There are also one full column and one half-column of light-shielded elements at the left edge of the image-sensing area and two lines of light-shielded elements between the image-sensing and image-storage areas. The latter prevent charge leakage from the image-sensing area into the image-storage area.

multiplexer with transfer gates and serial registers

The multiplexer and transfer gates transfers the charge line-by-line from each group of columns into the corresponding serial register and prepares it for readout. Multiplexing is activated during the horizontal-blanking interval by applying appropriate pulses to the transfer gates and serial registers. The required pulse timing is shown in Figure 3. A drain is included in this area to provide the capability to quickly clear the image-sensing and storage areas of unwanted charge. Such charge can accumulate in the imager during the start-up of operation or under special circumstances when nonstandard TV operation is desired.

correlated-clamp sample-and-hold amplifier with charge-detection nodes

Figure 4 illustrates the correlated-clamp sample-and-hold amplifier circuit. Charge is converted into a video signal by transferring the charge onto a floating-diffusion structure in detection node 1 that is connected to the gate of MOS transistor Q1. The proportional charge-induced signal is then processed by the circuit shown in Figure 4. This circuit consists of a low-pass filter formed by Q1 and C2, coupling-capacitor C1, dummy-detection node 2, which restores the dc bias on the gate of Q3, sampling-transistor Q5, holding capacitor C3, and output-buffer Q6. Transistors Q2, Q4, and Q7 are current sources for each corresponding stage of the amplifier. The parameters of this high-performance signal-processing amplifier have been optimized to minimize noise and maximize the video signal.

The signal processing begins with a reset of detection node 1 and restoration of the dc bias on the gate of Q3 through the clamping function of dummy-detection node 2. After the clamping is completed, the new charge packet is transferred onto detection node 1. The resulting signal is sampled by the sampling-transistor Q5 and is stored on the holding-capacitor C3. This process is repeated periodically and is correlated to the charge transfer in the registers. The correlation is achieved automatically since the same clock lines used in registers ϕ-S2 and ϕ-S3 for charge transport serve for reset and sample. The multiple use of the clock lines significantly reduces the number of signals required to operate the sensor. The amplifier also contains an internal voltage-reference generator that provides the reference bias for the reset and clamp transistors. Since the detection nodes and the corresponding amplifiers are located some distance from the edge of the storage area, eleven dummy elements are used at the end of each serial register to span the distance. The location of the dummy elements, which are considered to be part of the amplifiers, is shown on the functional block diagram.

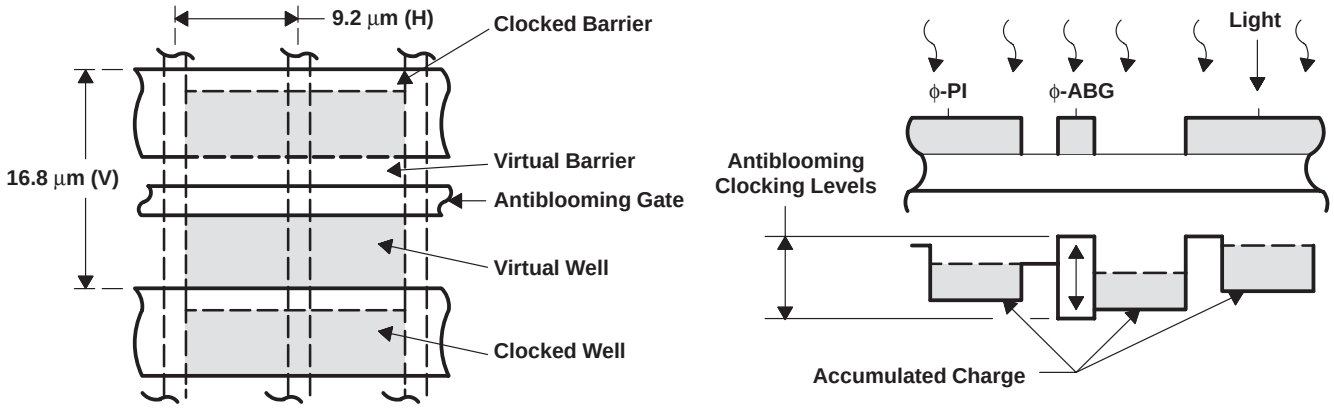


Figure 1. Charge-Accumulation Process

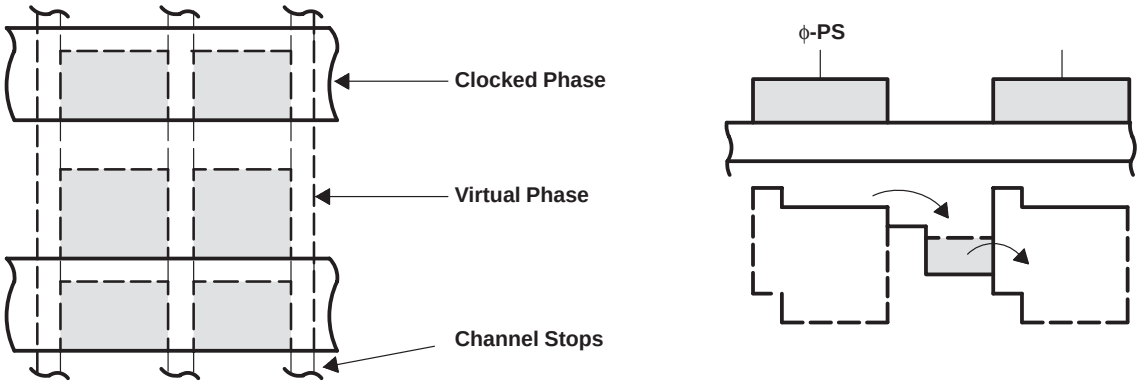


Figure 2. Charge-Transfer Process

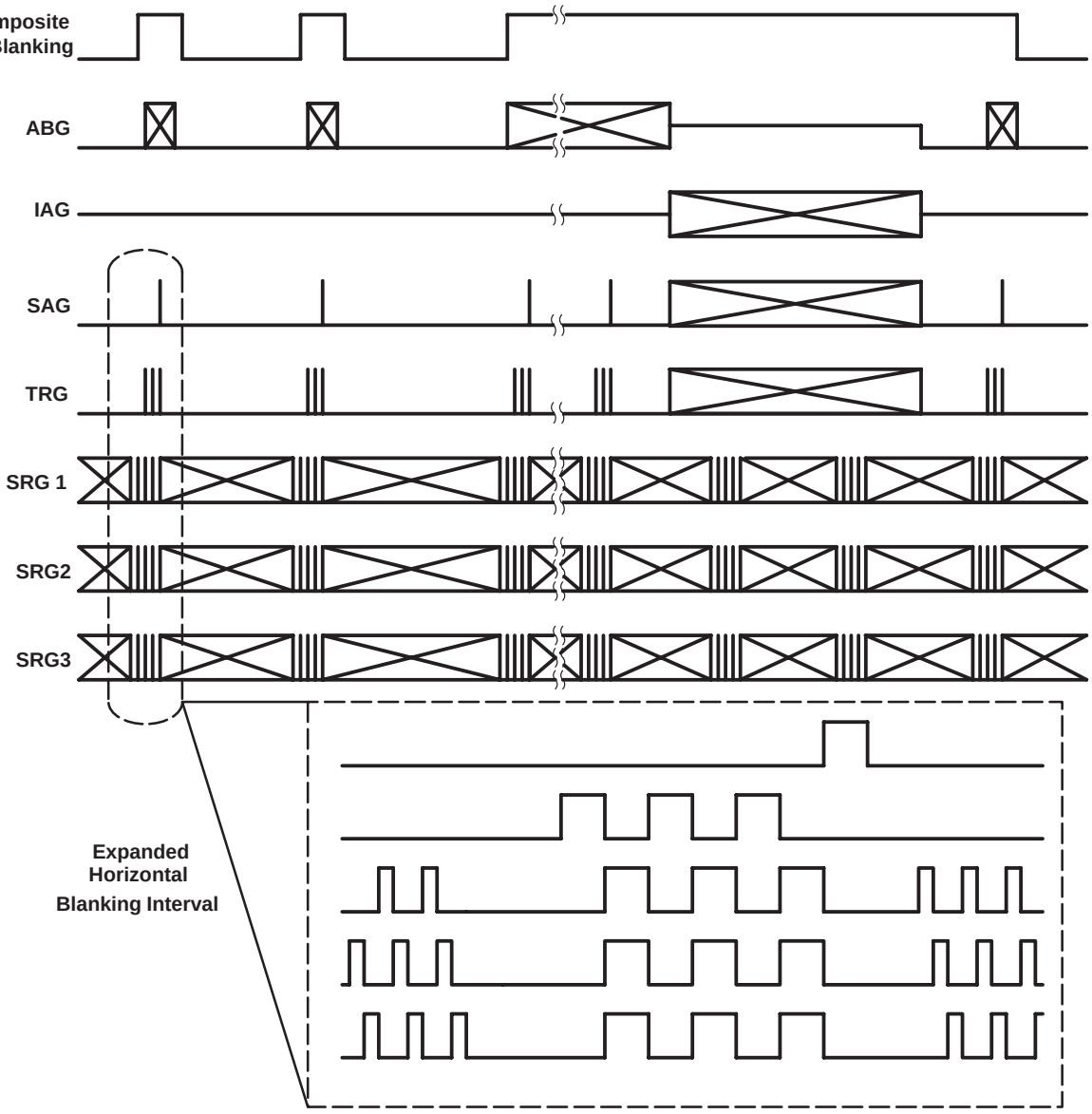


Figure 3. Timing Diagram

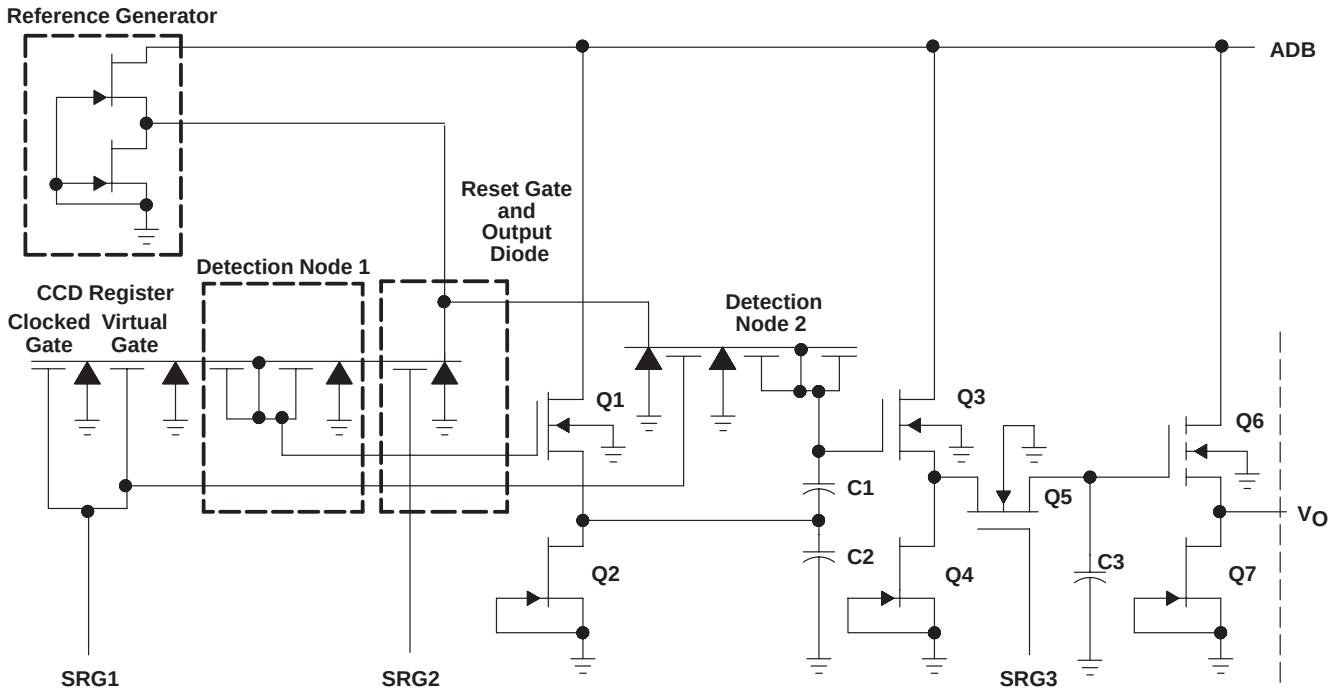


Figure 4. Correlated-Clamp Sample-and-Hold Amplifier and Charge-Detection Nodes

spurious-nonuniformity specification

The spurious-nonuniformity specification of the TC277 CCD grades –10, –20, –30, and –40 is based on several sensor characteristics.

- Amplitude of the nonuniform pixel
- Polarity of the nonuniform pixel
  - Black
  - White
- Location of the nonuniformity (see Figure 5)
  - Area A
    - Element columns near horizontal center of the area
    - Element rows near vertical center of the area
  - Area B
    - Up to the pixel or line border
    - Up to area A
  - Other
    - Edge of the imager
    - Up to area B
- Nonuniform pixel count
- Distance between nonuniform pixels
- Column amplitude

The CCD sensors are characterized in both an illuminated condition and a dark condition. In the dark condition, the nonuniformity is specified in terms of absolute amplitude as shown in Figure 6. In the illuminated condition, the nonuniformity is specified as a percentage of the total illumination as shown in Figure 7.

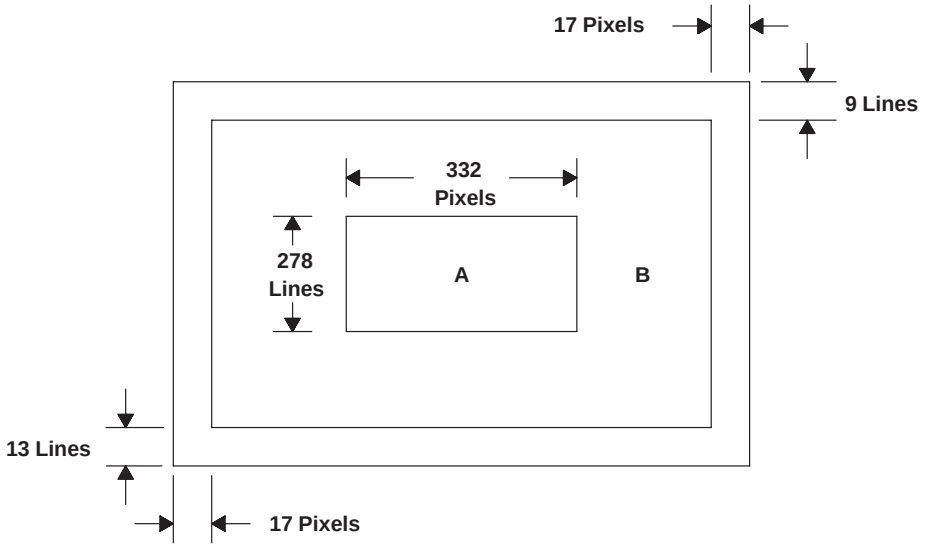


Figure 5. Sensor-Area Map

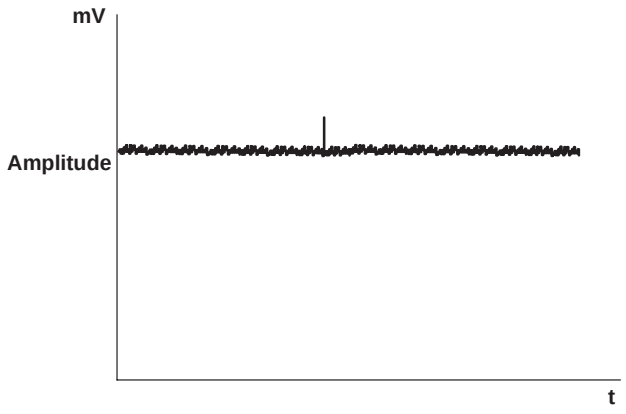


Figure 6. Pixel Nonuniformity, Dark Condition

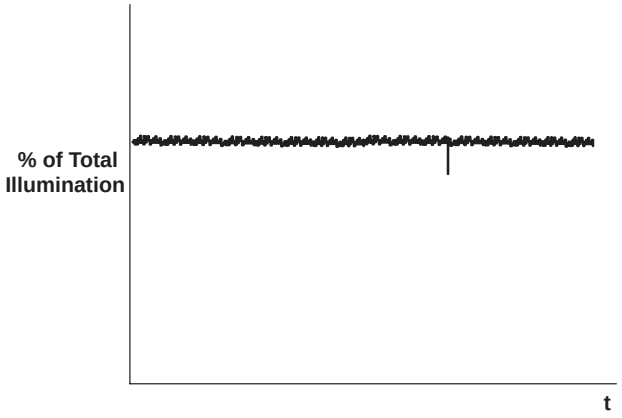


Figure 7. Pixel Nonuniformity, Illuminated Condition

The grade specification for the TC277 is as follows (CCD video-output signal is 50 mV ±10 mV):

Pixel nonuniformity:

PART NUMBER	DARK CONDITION							ILLUMINATED CONDITION			TOTAL COUNT‡	DISTANCE SEPARATION		
	PIXEL AMPLITUDE, x (mV)	NONUNIFORM PIXEL TYPE						% OF TOTAL ILLUMINATION	AREA A	AREA B		X	Y	AREA
		WHITE		BLACK		W/B†								
		AREA		AREA		AREA								
		A	B	A	B	A	B							
TC277-20	x > 3.5	0	0	0	0	0	0	x > 5	0	0	—	—	—	—
TC277-30	2.5 < x ≤ 3.5	2	5	2	5	2	5	5.0 < x ≤ 7.5	2	5	12	100	80	A
	x > 3.5	0	0	0	0	0	0	x > 7.5	0	0				
TC277-40	3.5 < x ≤ 7	3	7	3	7	3	7	7.5 < x ≤ 15	3	7	15	—	—	—
	x > 7	0	0	0	0	0	0	x > 15	0	0				

† White and black nonuniform pixel pair

‡ The total spot count is the sum of all nonuniform white, black, and white/black pairs in the dark condition added to the number of nonuniform black pixels in the illuminated condition. The sum of all nonuniform combinations do not exceed the total count.

Column nonuniformity:

PART NUMBER	COLUMN AMPLITUDE, x (mV)	WHITE	BLACK
		AREAS A AND B	AREAS A AND B
TC277-20	x > 0.3	0	0
TC277-30	x > 0.5	0	0
TC277-40	x > 0.7	0	0

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: ADB, CDB, IDB, TDB (see Note 1) . . . . . 0 V to 15 V
Input voltage range, V_I: ABG, IAG, SRG, SAG, TRG . . . . . –15 V to 15 V
Operating free-air temperature range, T_A . . . . . –10°C to 45°C
Storage temperature range, T_{STG} . . . . . –30°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the substrate terminal.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	ADB, CDB, IDB, TDB			12		V
Substrate bias voltage				0		V
Input voltage, V_I‡	IAG	High level	1.5	2	2.5	V
		Intermediate level§		–5.7		
		Low level	–11		–9	
	SRG1, SRG2, SRG3	High level	1.5	2	2.5	
		Low level	–11		–9	
	ABG	High level	2	4	6	
		Intermediate level§		–2.3		
		Low level		–7		
	SAG	High level	1.5	2	2.5	
		Low level	–11		–9	
	TRG	High level	1.5	2	2.5	
		Low level	–11		–9	
Clock frequency, f_{clock}	IAG, SAG				3.34	MHz
	SRG1, SRG2, SRG3, TRG				4.46	
	ABG				3.34	
Load capacitance	OUT1, OUT2, OUT3				6	pF
Operating free-air temperature, T_A			–10		45	°C

‡ The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for clock voltage levels.

§ Adjustment is required for optimal performance.

electrical characteristics over recommended operating ranges of supply voltage and operating free-temperature (unless otherwise noted)

PARAMETER		MIN	TYP†	MAX	UNIT
Dynamic range (see Note 2)	Antiblooming disabled (see Note 3)	60	70		dB
Charge-conversion factor		3.8	4	4.2	μV/e
Charge-transfer efficiency (see Note 4)		0.99990	0.99995	1	
Signal-response delay time, τ (see Note 5 and Figure 11)		18	20	22	ns
Gamma (see Note 6)		0.97	0.98	0.99	
Output resistance			700	800	Ω
Noise voltage	1/f noise (5 kHz)		0.1		μV/√Hz
	Random noise (f = 100 kHz)		0.08		
Noise-equivalent signal			25		electrons
Rejection ratio at 4.46 MHz	ADB (see Note 7)		20		dB
	SRG1, SRG2, SRG3 (see Note 8)		40		
	ABG (see Note 9)		20		
Supply current			5		mA
Input capacitance, C_i	IAG		6500		pF
	SRG1, SRG2, SRG3		68		
	ABG		2400		
	TRG		180		
	SAG		6800		

† All typical values are at T_A = 25 °C.

NOTES: 2. Dynamic range is –20 times the logarithm of the mean-noise signal divided by the saturation-output signal.
3. For this test, the antiblooming gate must be biased at the intermediate level.
4. Charge-transfer efficiency is one minus the charge loss per transfer in the output register. The test is performed in the dark using an electrical-input signal.
5. Signal-response delay time is the time between the falling edge of the SRG clock pulse and the output-signal valid state.
6. Gamma (γ) is the value of the exponent in the equation below for two points on the linear portion of the transfer-function curve (this value represents points near saturation):

$$\left(\frac{\text{Exposure (2)}}{\text{Exposure (1)}}\right)^{\gamma} = \left(\frac{\text{Output signal (2)}}{\text{Output signal (1)}}\right)$$

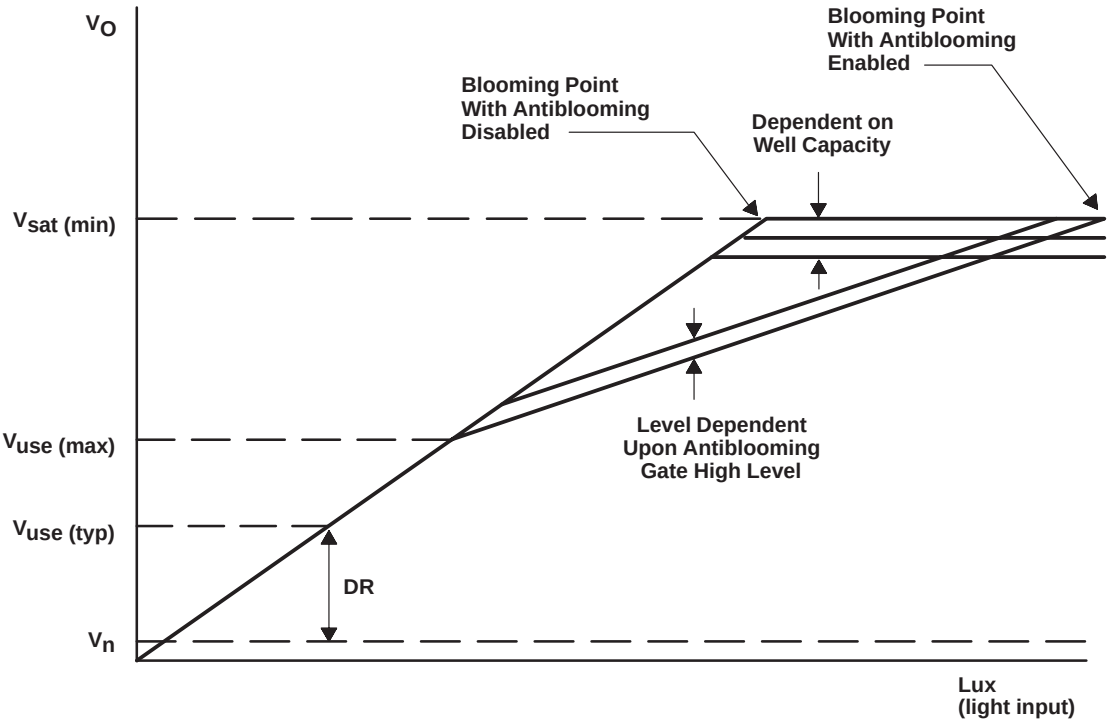
7. ADB rejection ratio is –20 times the logarithm of the ac amplitude at the output divided by the ac amplitude at ADB.
8. SRGn rejection ratio is –20 times the logarithm of the ac amplitude at the output divided by the ac amplitude at SRGn.
9. ABG rejection ratio is –20 times the logarithm of the ac amplitude at the output divided by the ac amplitude at ABG.

optical characteristics, T_A = 40°C (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
Sensitivity	No IR filter	Measured at V_U (see Notes 10 and 11)		242		mV/lx
	With IR filter			30		
Saturation signal, V_{sat} (see Note 12)	Antiblooming disabled, interlace off		320			mV
Maximum usable signal, V_{use}	Antiblooming enabled, interlace on		200			mV
Blooming-overload ratio (see Note 13)		Interlace on	150			
		Interlace off	300			
Image-area well capacity				80×10^3		electrons
Smear (see Note 14)		See Note 15			0.0004	
Dark current	Interlace off	T_A = 21°C		0.027		nA/cm^2
Dark signal (see Note 16)		TC277-30			6.6	mV
		TC277-40			7.2	
Pixel uniformity	Output signal = 50 mV ±10 mV	TC277-30			3.5	mV
		TC277-40			5	
Column uniformity	Output signal = 50 mV ±10 mV	TC277-30			0.5	mV
		TC277-40			0.7	
Shading	Output signal = 100 mV				15%	

NOTES: 10. Sensitivity is measured at an integration time of 20.03 ms with a source temperature of 2856 K. A CM-500 filter is used.
11. V_U is the output voltage that represents the threshold of operation of antiblooming. $V_U \approx$ 1/2 saturation signal.
12. Saturation is the condition in which further increase in exposure does not lead to further increase in output signal.
13. Blooming-overload ratio is the ratio of blooming exposure to saturation exposure.
14. Smear is a measure of the error induced by transferring charge through an illuminated pixel in shutterless operation. It is equivalent to the ratio of the single-pixel transfer time during a fast dump to the exposure time using an illuminated section that is 1/10 of the image-area vertical height with recommended clock frequencies.
15. Exposure time is 20 ms and the fast-dump clocking rate during vertical timing is 3.34 MHz.
16. Dark-signal level is measured from the dummy pixels.

PARAMETER MEASUREMENT INFORMATION



$$\text{DR (dynamic range)} = \frac{\text{camera white-clip voltage}}{V_n}$$

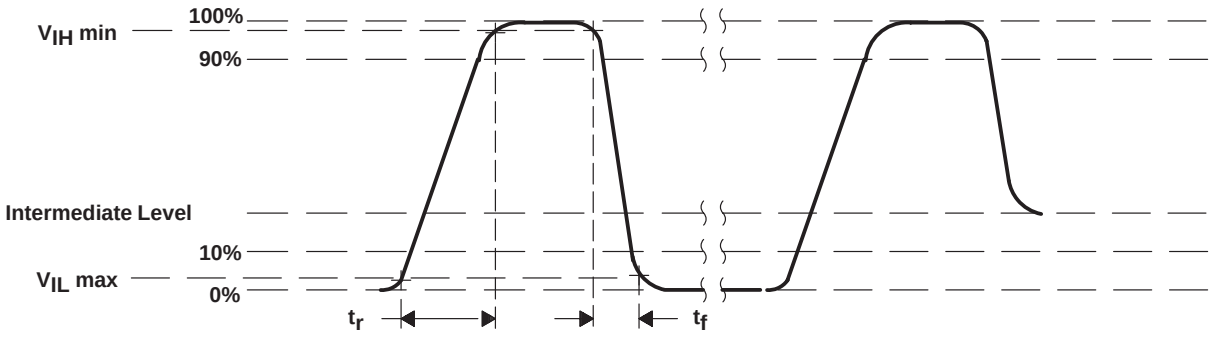
V_n = noise-floor voltage
$V_{sat\ (min)}$ = minimum saturation voltage
$V_{use\ (max)}$ = maximum usable voltage
$V_{use\ (typ)}$ = typical user voltage (camera white clip)

NOTES: A. $V_{use\ (typ)}$ is defined as the voltage determined to equal the camera white clip. This voltage must be less than $V_{use\ (max)}$.

B. A system trade-off is necessary to determine the system light sensitivity versus the signal/noise ratio. By lowering the $V_{use\ (typ)}$, the light sensitivity of the camera is increased; however, this sacrifices the signal/noise ratio of the camera.

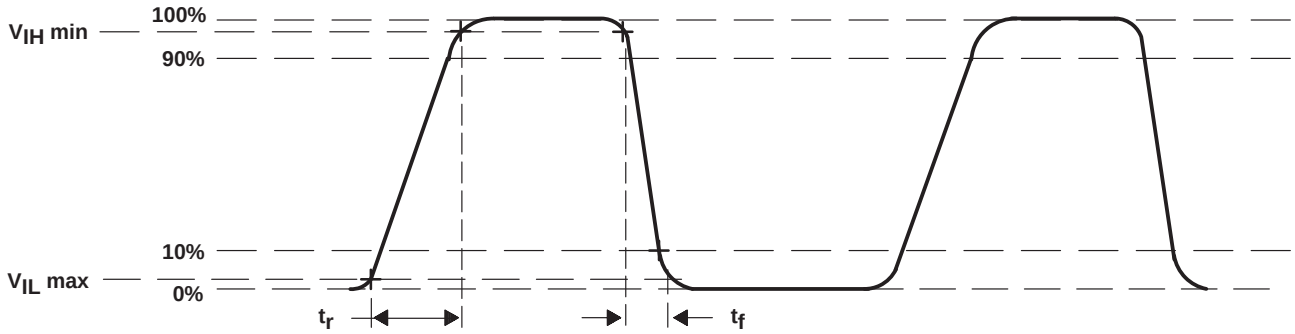
Figure 8. Typical V_{sat}, V_{use} Relationship

PARAMETER MEASUREMENT INFORMATION



Slew rate between 10% and 90% = 70 to 120 V/µs, t_r = 150 ns, t_f = 90 ns
Duty Cycle @ 2 MHz (13.375 MHz/7): 4:3
@ 3.3 MHz (13.375 MHz/4): 1:1

Figure 9. Typical Clock Waveform for ABG, IAG, and SAG



Slew rate between 10% and 90% = 300 V/µs, $t_r = t_f$ = 15 ns
Duty Cycle: 1:2

Figure 10. Typical Clock Waveform for SRG1, SRG2, SRG3, and TRG

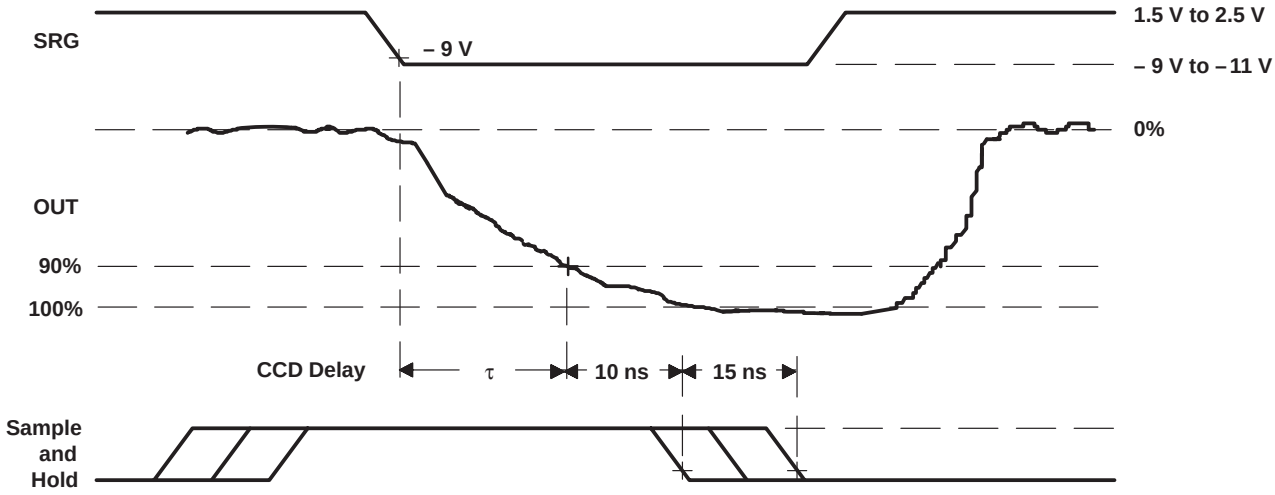


Figure 11. SRG and CCD Output Waveforms

TYPICAL CHARACTERISTICS

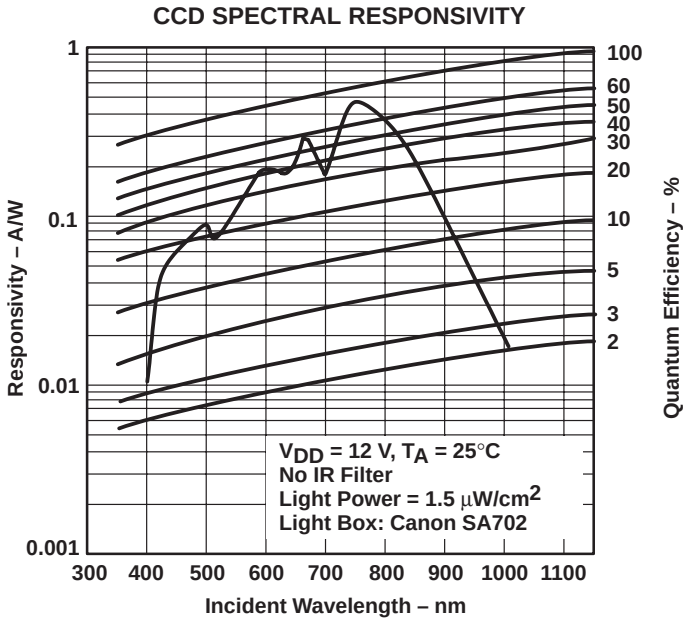


Figure 12

APPLICATION INFORMATION

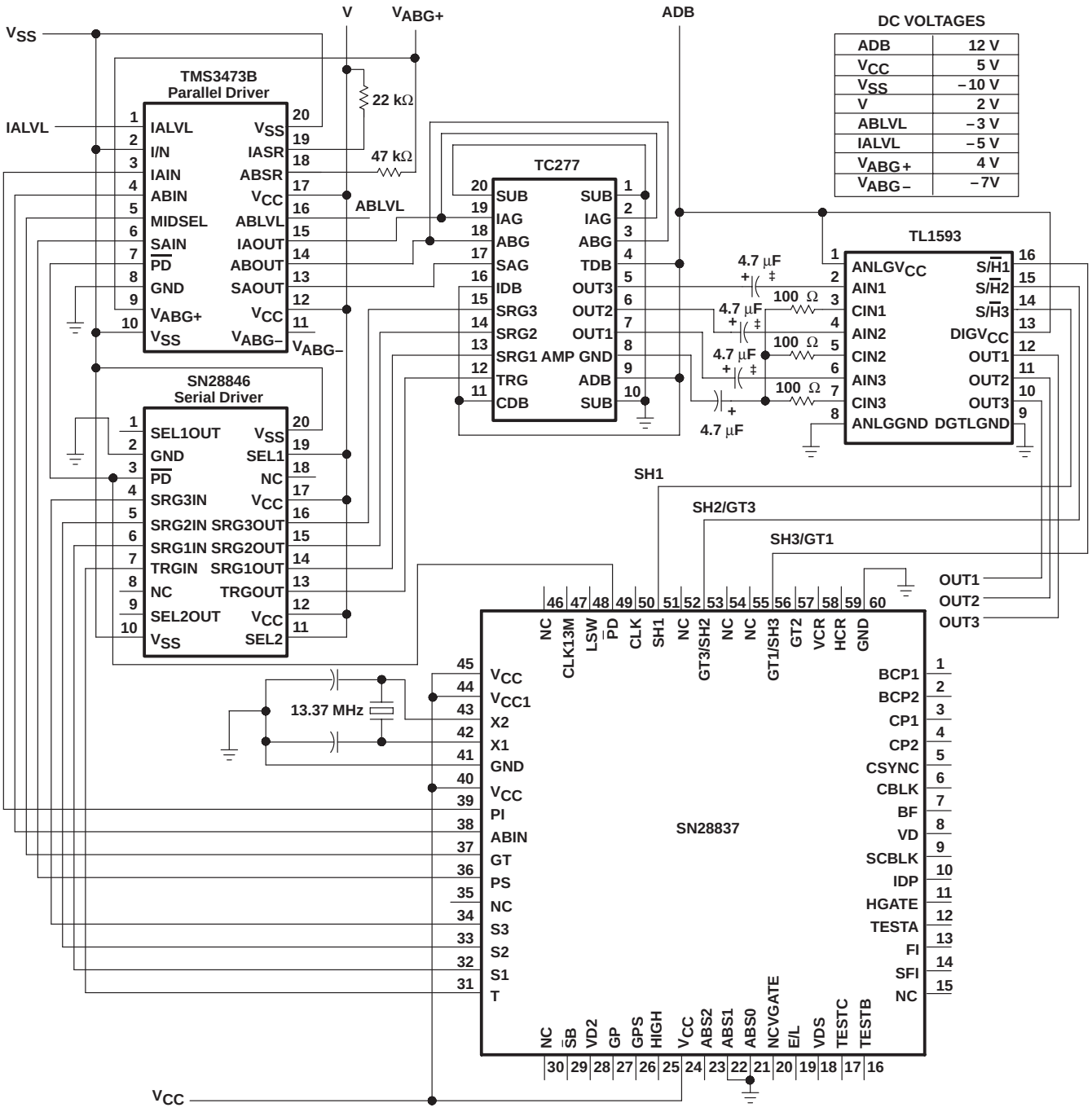


Figure 13. Typical Application Circuit Diagram

† Decoupling capacitors are not shown.
‡ TI recommends designing AC coupled systems.

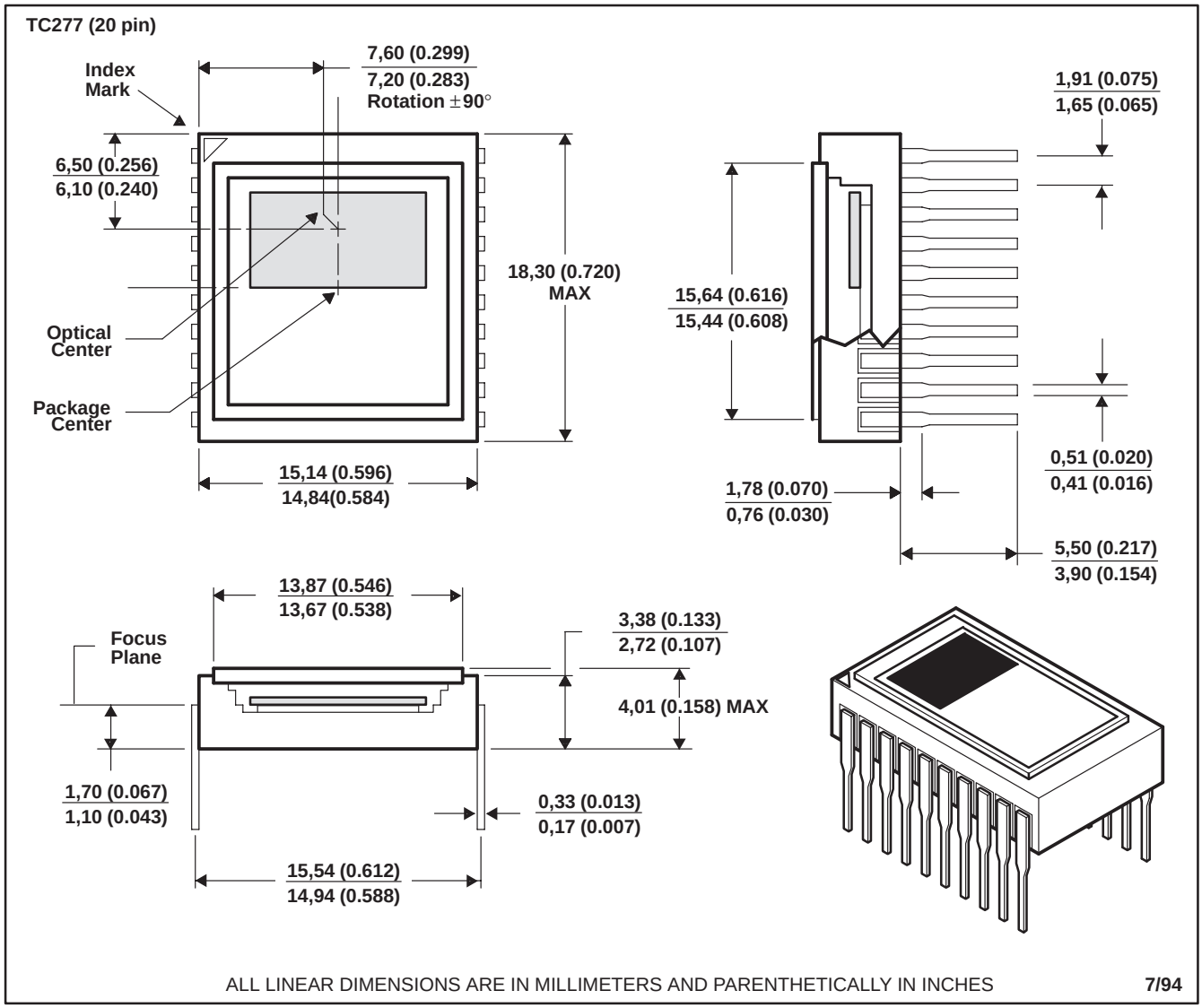
APPLICATION INFORMATION

SUPPORT CIRCUITS			
DEVICE	**PACKAGE**	**APPLICATION**	**FUNCTION**
SN28837FS	60 pin flatpack	Timing generator	PAL timing
SN28846DW	20 pin small outline	Serial driver	Driver for TRG, SRG1, SRG2, SRG3
TMS3473BDW	20 pin small outline	Parallel driver	Driver for IAG, SAG, and ABG
TL1593CNS	16 pin SO (EIAJ)	Sample and hold	Three-channel sample and hold

Figure 13. Typical Application Circuit Diagram (Continued)

MECHANICAL DATA

The package for the TC277 consists of a ceramic base, a glass window, and a 20-lead frame. The glass window is sealed to the package by an epoxy adhesive. The package leads are configured in a dual-in-line organization and fit into mounting holes with 1,78 mm (0.070 in) center-to-center spacings.



NOTES: A. The center of the package and the center of image area not coincident.
B. The distance from the top of the glass to the image-sensor surface is typically 1 mm (0.04 in). The glass is 0.95 ± 0.08 mm thick and has an index of refraction of 1.53.
C. Each pin centerline is located within 0.18 mm of its true longitudinal position.
D. Maximum rotation of the sensor within the package is 1.5°.

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