PTG: Extending Functionality for dsPIC® DSC Peripherals for Integration of PFC and FOC

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INTRODUCTION

Consumer's demand for improved power quality has constantly been driving the motor control industry to design power efficient motor control drives for various applications. The power quality can be enhanced by implementing Power Factor Correction (PFC); efficient and cost-effective control of a motor can be realized using sensorless Field-Oriented Control (FOC) techniques.

This document discusses how the dsPIC® Digital Signal Controllers (DSCs) from Microchip Technology deliver a development platform for motor drive, including the front-end PFC. Implementation of PFC and FOC algorithms in a single chip is challenging, considering the critical timing requirement and synchronization. The Peripheral Trigger Generator (PTG) module available in Microchip dsPIC DSCs simplifies the integration of PFC and FOC.

The proposed solution helps to:

- Improve efficiency
- Improve PF/THD
- Precisely regulate the DC bus

A detailed explanation for the proposed solution is demonstrated in the **"Usage Example"** section.

Power Factor Correction (PFC)

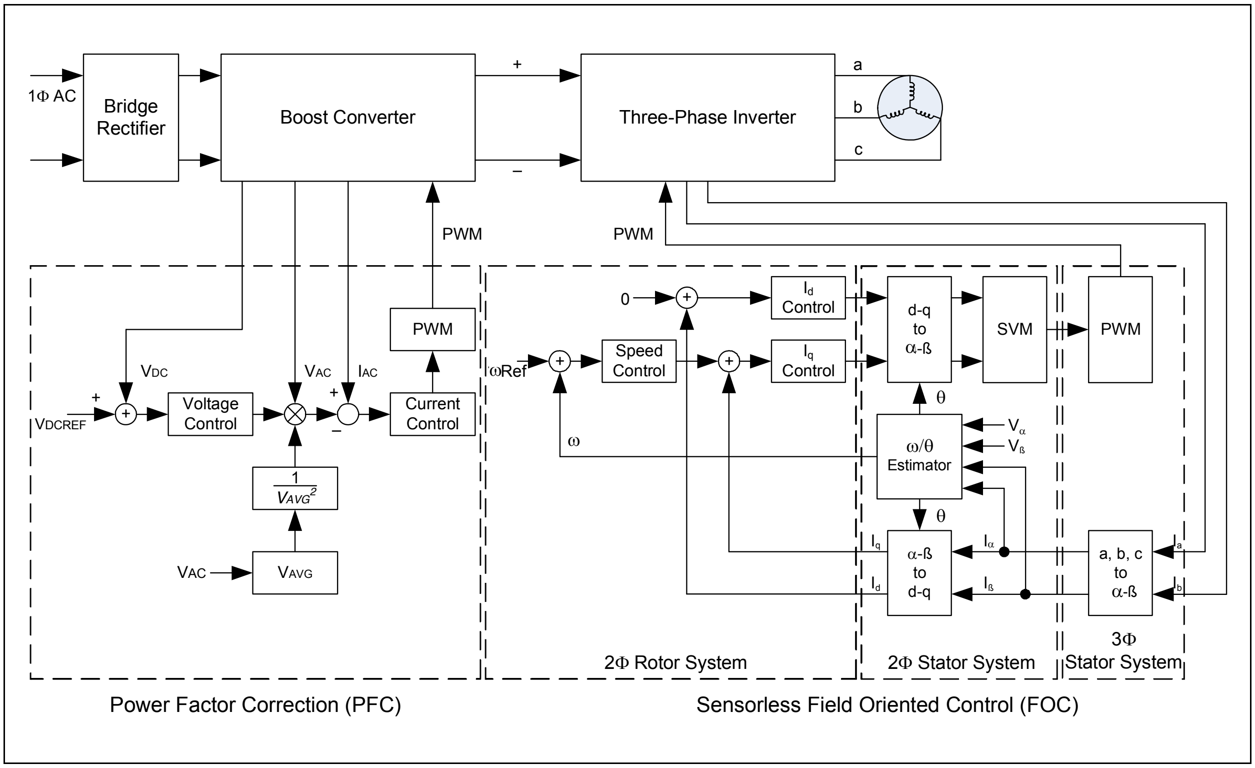
A majority of motor control drives consists of an input rectifier and capacitor filter (to derive DC from AC mains), which in turn, causes peaky currents to be drawn from the AC mains, and also contributes to a higher harmonic content on the mains grid. The PFC stage, which is a front-end converter, improves the Total Harmonic Distortion (THD) of the input current drawn and provides a better output voltage regulation.

In most applications, a Boost Converter is used as a PFC circuit and is operated using the Average Current mode control algorithm. This control topology has an inner current control loop and an outer voltage control loop (shown in Figure 1). The reference to the inner current controller is a scaled version of the rectified input AC voltage and is in a sinusoidal shape. Hence, the output of the current controller, which is the duty cycle input to the gate driver, is generated such that the Boost Converter draws a sinusoidal current.

Field-Oriented Control (FOC)

The FOC, also known as Vector Control, improves the dynamic performance of AC motor drives by independently controlling the torque and flux. The control of a synchronous machine in speed or torque drive applications is a complex mechanism, unlike the control of a separately excited DC machine. Therefore, to simplify the control of AC machines, it is necessary to resolve the stator current into an equivalent flux producing current and torque producing current leading to the control of the flux and torque independently (shown in Figure 1). All control algorithms for AC motors, such as Permanent Magnet Synchronous Motor (PMSM), requires the knowledge of the rotor position. The rotor position can be obtained from a shaft sensor or can be estimated from the motor phase currents and voltages. A FOC implemented without using a physical shaft sensor is called sensorless FOC.

FIGURE 1: BLOCK DIAGRAM – INTEGRATED PFC AND FOC



PERIPHERAL TRIGGER GENERATOR (PTG)

The PTG module is a user-programmable sequencer, which is capable of generating complex trigger signal sequences to coordinate the operation of peripherals, such as an Analog-to-Digital Converter (ADC), Output Compare (OC), Pulse-Width Modulation (PWM), timers, interrupt controllers and so on.

The PTG module operation sequence is programmable by writing its 8 bit commands, called Steps, into PTG Queue registers. Each command consists of command fields and option fields, as shown in the Table 1.

TABLE 1: STEP COMMAND FORMAT

Format	`STEPx<7:0> = CMD	OPTION`
Example	`_STEPn = PTGIRQ	0x2`

Option fields are used to indicate exactly which of the several possible input/output options the command executes. It specifies the trigger input to wait for the trigger or interrupts that are to be generated. For more information, refer to **"Peripheral Trigger Generator (PTG)"** (DS70669) in the "*dsPIC33/PIC24 Family Reference Manual*".

The PTG helps to:

- Synchronize motor control PWM and PFC PWM.
- Generate ADC triggers at the desired sampling instances, referenced to motor control PWM and PFC PWM.
- Monitor "ADC Conversion Done" interrupts and generate appropriate interrupts for executing PFC and FOC algorithms.

Challenges to Integrate PFC and FOC

Integrating the PFC and FOC algorithms in a single microcontroller poses inherent challenges. The first challenge is to synchronize the PWMs used for controlling the three-phase motor control inverter and the Boost PFC Converter. Another challenge is to use a single ADC module to sample and convert both PFC signals and FOC signals without any conflict.

SINGLE ANALOG-TO-DIGITAL CONVERTER

In a typical power conversion application, the efficacy of the control algorithm depends on the accuracy of the measured input signals.

As discussed in the **"Usage Example"** that appears later in this document, the PFC requires simultaneous sampling of input AC voltage, inductor current and PFC output voltage (DC bus voltage). The sensorless FOC requires simultaneous sampling of at least two motor phase currents and a DC bus voltage. The switching and control loop frequencies for PFC and FOC are different; hence, the triggers to ADC for sampling PFC and FOC signals are to be generated at different rates. In such a scenario, there will be a possibility of receiving concurrent requests at the ADC for sample and conversion which have to be carefully avoided.

Typically, an ADC produces only one interrupt after receiving the "ADC Conversion Done" message. Executing the PFC and FOC control loops at different frequencies, using a single ADC interrupt, is not a straight forward method as it does not support prioritization to execute algorithms at different rates; hence, it requires at least two interrupts with different priorities, which having two different interrupts makes the code modular.

SYNCHRONIZATION OF PFC PWM AND MOTOR CONTROL PWM

The dsPIC33EP DSC has one high-speed PWM module with three pairs of PWMH/L outputs, suitable for controlling a three-phase inverter. To run a Boost PFC Converter, an additional PWM output is required. The OC module of the dsPIC DSC is capable of generating PWM outputs, which can be used for controlling the PFC. In such a case, where the PWM signals are generated from two different modules (HSPWM and OC), the synchronization of these PWM signals is crucial.

Choosing an appropriate phase shift based on the ADC conversion time can avoid any conflict in the ADC sampling and conversion request. Providing a phase shift between the PWMs will also reduce the ground noise, as both motor control and PFC PWMs start at different instances. The PTG aids such an application requirement by precisely synchronizing and/or adding a phase shift between the motor control PWM and PFC PWM.

Usage Example

IMPLEMENTATION OF INTEGRATED PFC AND FOC IN dsPIC33EP256MC506

The switching frequency of the motor control PWM and PFC PWM are selected such that they are integral multiples of each other. This ensures that the control execution and interruption of the motor control algorithm is predictable in correlation with the PFC application. Also, generating a PTG sequence for coordination of peripherals becomes simpler. Typically, in motor control applications, switching frequency ranges from 10 kHz to 20 kHz and in PFC applications it is greater than 50 kHz.

The ADC in the dsPIC33EP256MC506 family of devices has a capability of sampling four channels simultaneously. Both PFC and FOC algorithms have a set of analog channels that are to be sampled simultaneously. The ADC in the dsPIC DSC devices is capable of switching between the analog input channels through the Channel Selection register, on-the-fly, and is utilized in the application for connecting PFC and motor control signals to an ADC.

In this application, by configuring the CH0SA/CH123SA bits in the AD1CHS0/AD1CHS123 registers, the motor control and PFC signals are connected to their respective Sample-and-Hold (S/H) circuits before triggering the ADC. Table 2 shows an example of ADC channel allocation.

TABLE 2: ANALOG CHANNEL CONNECTIONS

Sample-and-Hold Circuit	Motor Control CH123SA = 0; CH0SA = 13		PFC CH123SA = 1; CH0SA = 10	
	Analog Feedback Signal	ADC Channel	Analog Feedback Signal	ADC Channel
CH0	Speed Reference	AN13	PFC Output Voltage	AN10
CH1	Phase Current 2	AN0	AC Input Voltage	AN3
CH2	Phase Current 1	AN1	NA	
CH3	Bus Current	AN2	AC Input Current	AN6

Implementation details such as PTG Step commands, synchronization of PFC PWM and Motor Control PWM and triggering of the ADC module to sample the PFC and FOC signals are explained in the following diagram:

- Figure 2 shows PTG sequencer commands and function of each step
- Figure 3 depicts the peripheral integration to implement PFC and FOC in a single dsPIC DSC™ controller
- Figure 4 is the timing diagram of the sample application

Before starting the control execution, Motor Control PWM and PFC PWM are synchronized with a fixed phase shift of 5 µs, and will remain synchronized, as shown in Figure 4. The PTG Step commands _STEP0 to _STEP3 used for synchronization of the PWMs are shown in Figure 3.

Once the PWMs are synchronized, then starts the regular tasks such as ADC sampling and conversion, interrupt generation, and control loop execution. The PTG Step commands _STEP4 to _STEP14 perform these tasks. For simultaneously sampling and converting four channels the ADC takes approximately 4.6 µs. The PTG generates PTG1 Interrupt with low priority for executing FOC and PTG2 Interrupt with a high priority to execute the PFC algorithm.

The PTG waits for the "Motor Control PWM End of Cycle", once received it instantaneously generates a trigger for the ADC to sample motor control signals, then waits for an "ADC Conversion Done" event. After the occurrence of this event the PTG generates interrupt (PTG1 Interrupt) to execute the FOC algorithm. As this algorithm is executed in a lower priority interrupt, the ADC conversion results must be stored before switching the ADC channels to sample PFC signals. Considering the time taken for storing the results, ADC conversion time and ISR latency, the PFC PWM is phase shifted by 5 µs from the Motor Control PWM.

For implementing the Average Current mode control, the PFC signals must be sampled at half of the PFC duty cycle to measure the average inductor current in every switching cycle. In this application, another Output Compare (OC1) is configured such that its rising edge coincides with half the duty cycle of the PFC (OC2) PWM and it generates a trigger input to the PTG.

Once the PTG receives a trigger at the rising edge of OC1, it triggers the ADC to measure the PFC signals, then the PTG waits for "ADC Conversion Done" and generates interrupt (PTG2 Interrupt) to execute the PFC algorithm. As the PTG2 Interrupt generated after the conversion of PFC signals is of a higher priority, the FOC algorithm execution is put on hold and the PFC algorithm will start executing.

To ensure enough headroom for other tasks, the PFC algorithm is executed at every alternate PFC PWM cycle. In one motor control switching cycle (20 kHz) the PFC is executed twice and the FOC is executed once.

FIGURE 2: PTG STEP COMMANDS FOR INTEGRATION OF PFC AND FOC

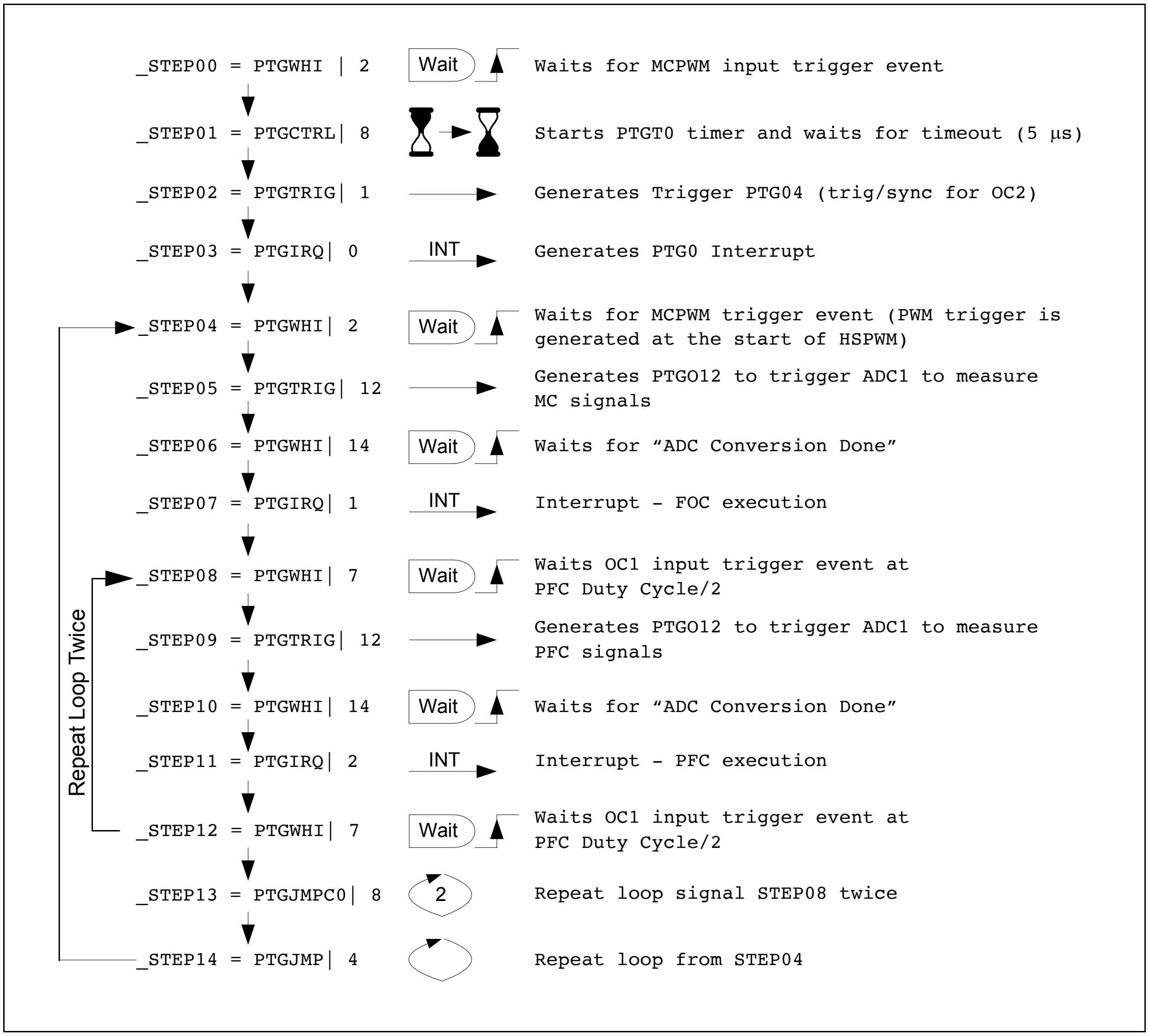


FIGURE 3: PERIPHERAL INTERCONNECTIONS – INTEGRATION OF PFC AND FOC

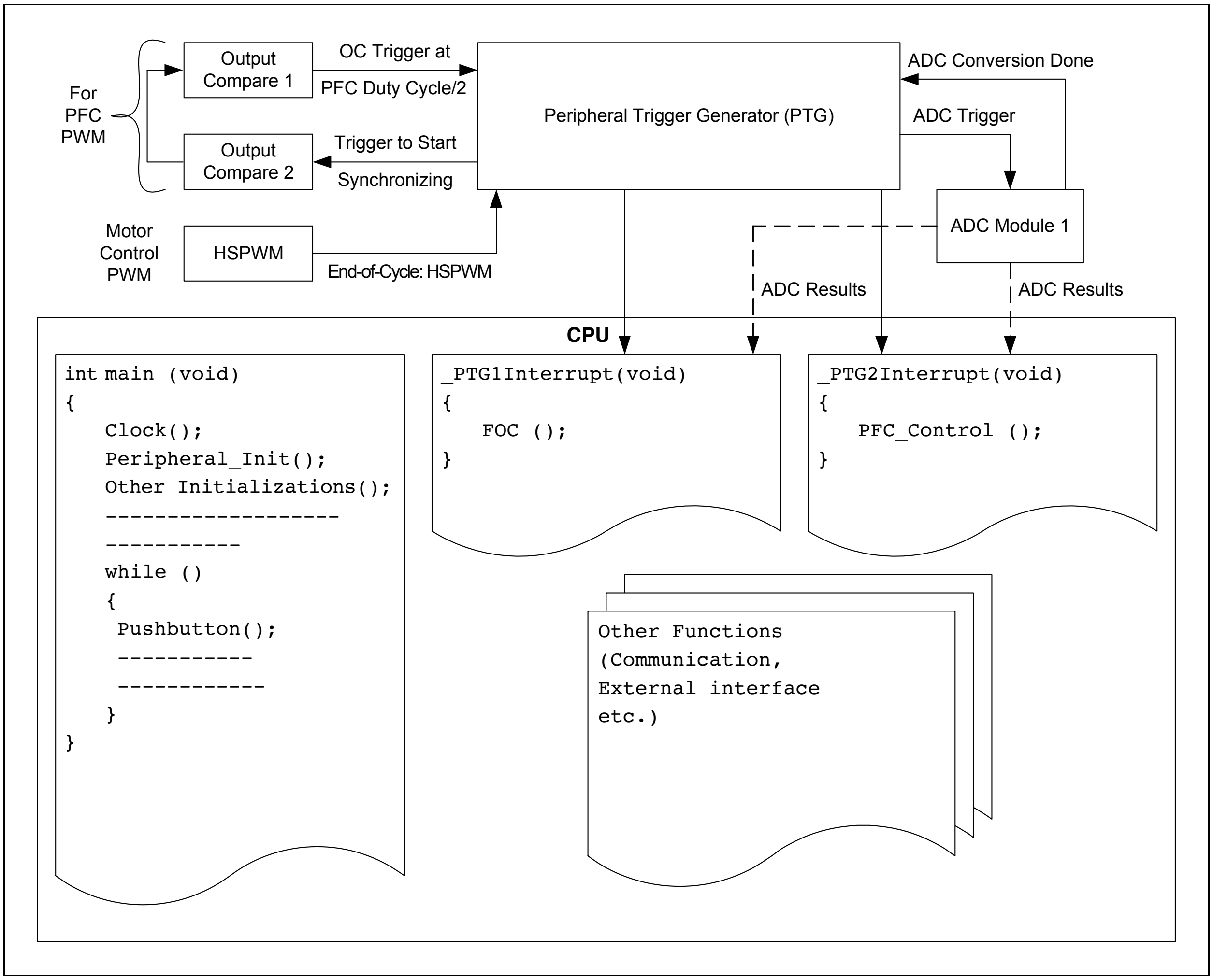
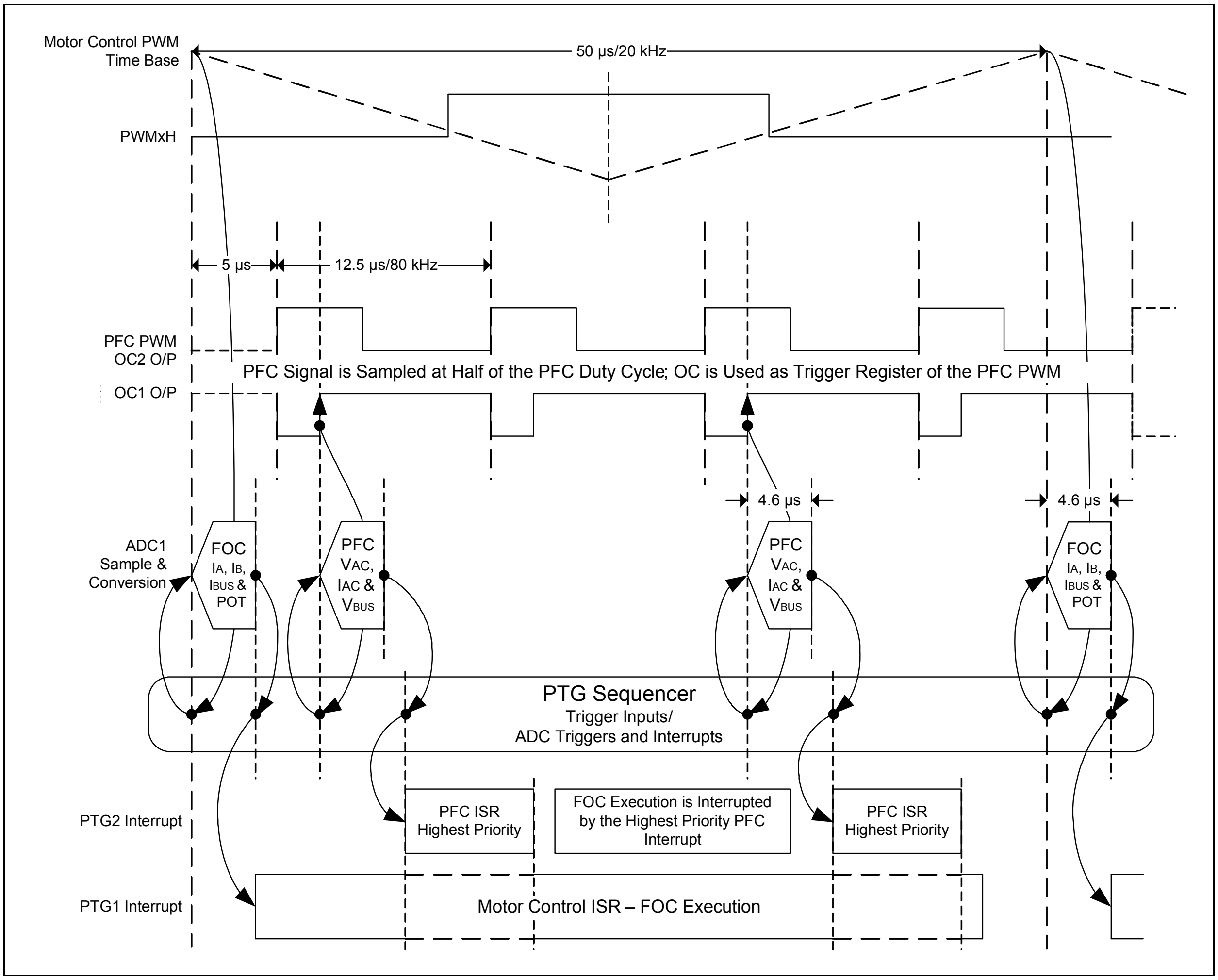


FIGURE 4: TIMING DIAGRAM FOR INTEGRATION OF PFC AND FOC



CONCLUSION

The Peripheral Trigger Generator (PTG), along with a **"Usage Example"** to leverage its capabilities in time-critical applications, and for coordinating and synchronizing peripherals without any intervention of the CPU has been discussed. The discussion, along with the **"Usage Example"**, has convincingly demonstrated that the functionalities of certain peripherals can be extended to execute complex tasks by deploying the module.

The presence of a powerful peripheral, such as the PTG, enables dsPIC DSC devices to implement the PFC functionalities in scenarios where an additional PWM module is not available. Thus, making these devices (with the developed code) ideal for those applications where cost reduction is essential, without compromising on the performance.

NOTES:

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