

## 20-W STEREO DIGITAL AUDIO POWER AMPLIFIER WITH EQ/DRC and FEEDBACK

### FEATURES

- **Audio Input/Output**
  - 20-W Into an 8-Ω Load From an 18-V Supply
  - Wide PVCC Range (10 V to 26 V)
  - Supports One Serial Audio Input (8 kHz - 48 kHz Sample Rates) (LJ/RJ/I<sup>2</sup>S)
  - Power-Stage Feedback Allows Operation From Poorly Regulated Power Supplies
- **Audio/PWM Processing**
  - Factory-Trimmed Internal Oscillator for Automatic Rate Detection
  - High-End 32-Bit Data Path Audio Processor
  - 18 Biquads for Speaker EQ
  - Dynamic Range Control (DRC)
  - Support for Pseudo Bass and 3D Effects
- **Benefits**
  - EQ: Speaker Equalization for Better Sound
  - 2-Band DRC: Improved Bass Performance, Enables Speaker Protection and Night mode Listening
  - Autobank Switching: Preloaded Coefficients for Three Different Sample Rates Eliminates the Need to Update Coefficients When Sample Rate Changes
  - Autodetect: Automatically Detects Sample-Rate Changes Eliminating the Need for External Microprocessor Intervention
  - Closed-Loop Power Stage: Enables Wide PVCC Operating Range and Reduced Power Supply Ripple Distortion

### DESCRIPTION

The TAS5710 is a 20-W, efficient, digital audio power amplifier for driving stereo bridge-tied speakers. A 32-bit datapath eliminates the need for pre-scaling before processing and preserves signal integrity without sacrificing dynamic range. A digital audio processor with fully programmable digital filters allows designers to custom tune speakers for optimum sound in small enclosures. A programmable DRC can adjust power levels for a scaleable design while also enabling night-mode listening modes.

The closed-loop architecture allows the device to operate from poorly regulated supplies. Figure 1 below shows the benefit of the feedback architecture when a noisy supply (1kHz, 500mVpp ripple) modulates a 10kHz audio input. The figure shows a 40dB improvement in sideband suppression when compared to an open-loop design. This correlates directly to a 24dB improvement in distortion as seen in Figure 2.

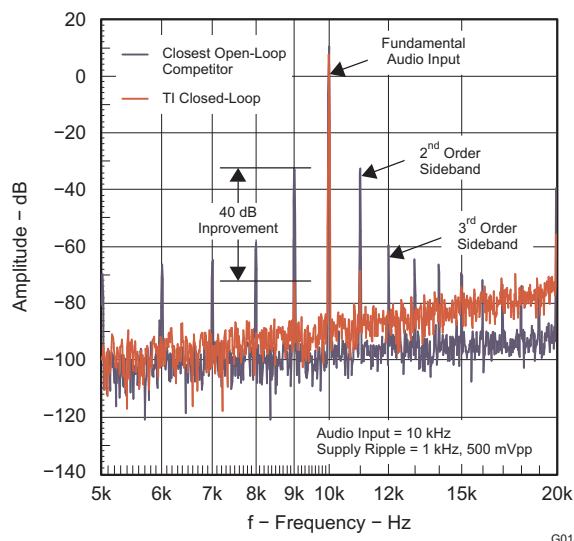


Figure 1. Supply Ripple Intermodulation Distortion

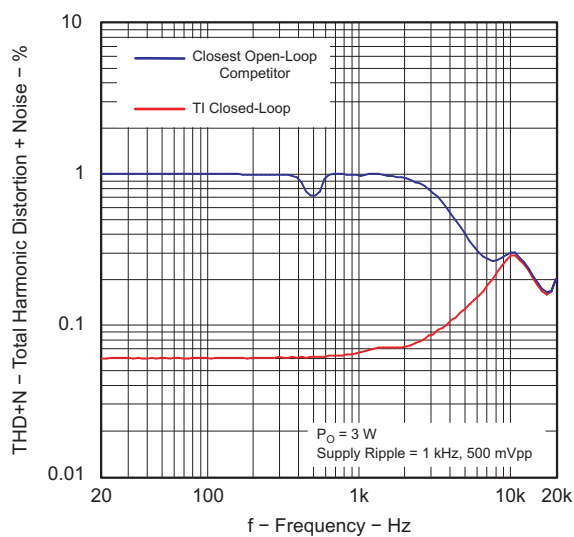


Figure 2. THD+N vs Frequency

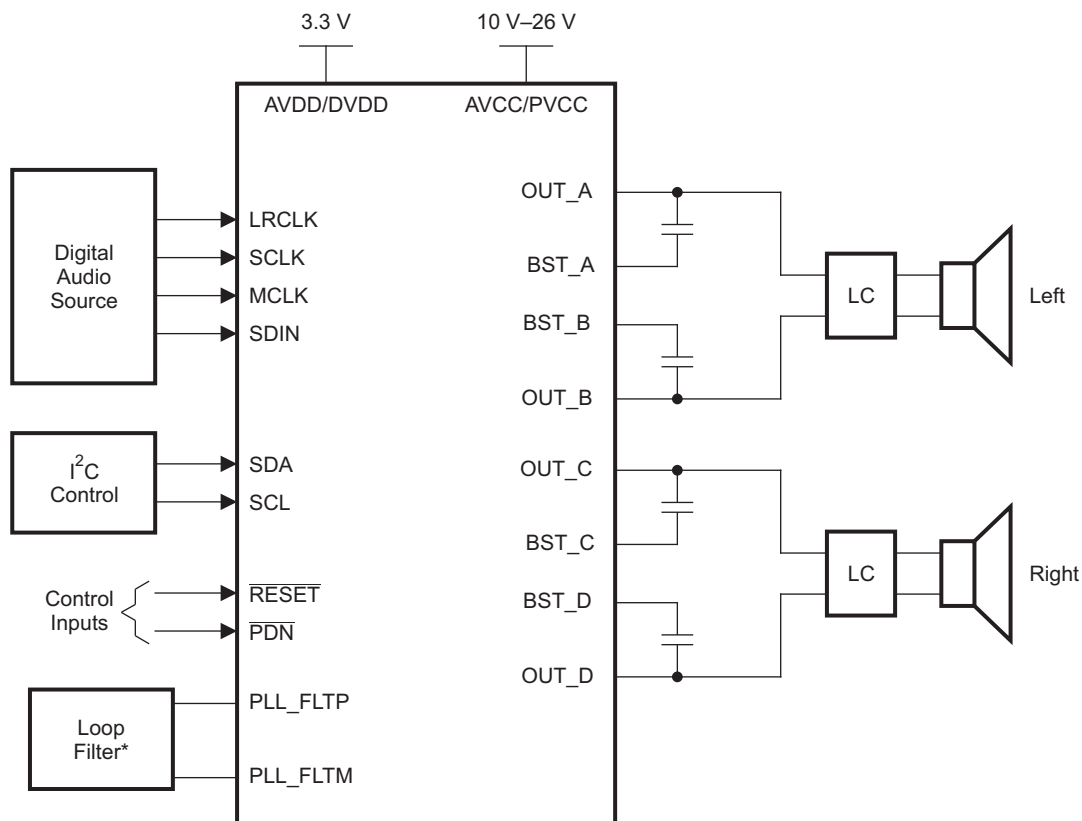


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

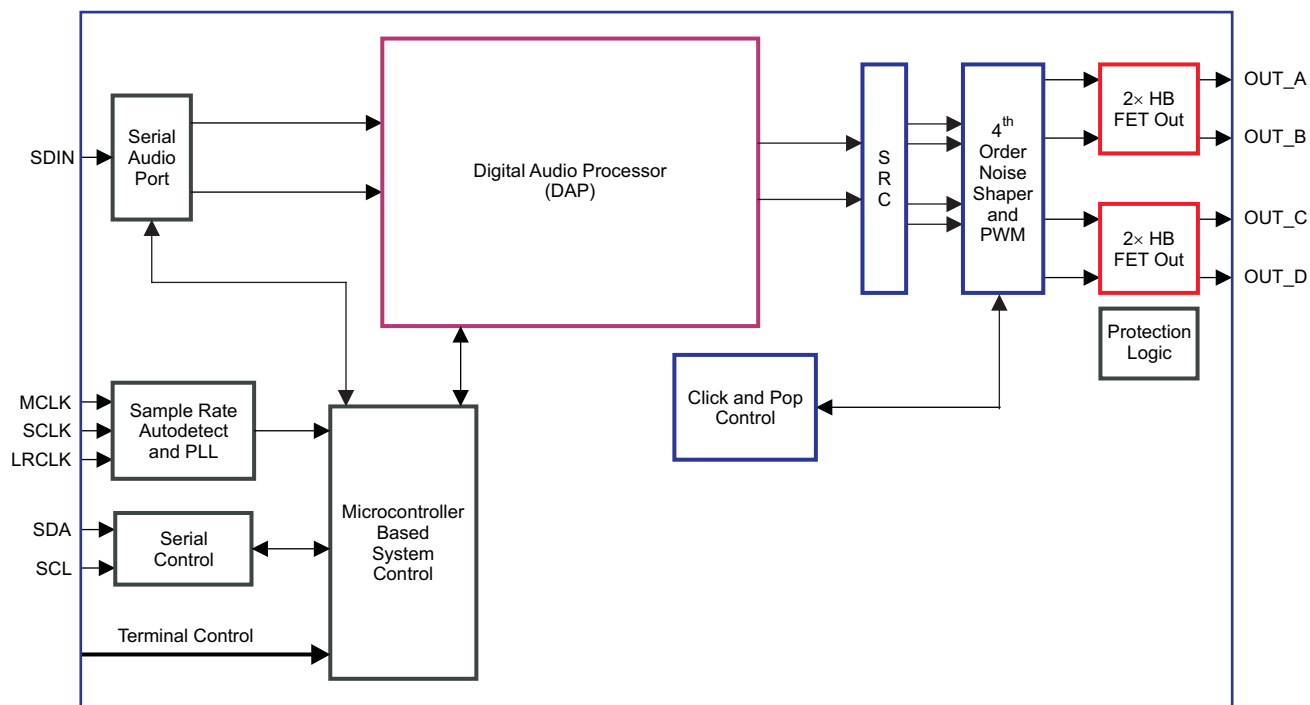
## SIMPLIFIED APPLICATION DIAGRAM



B0264-07

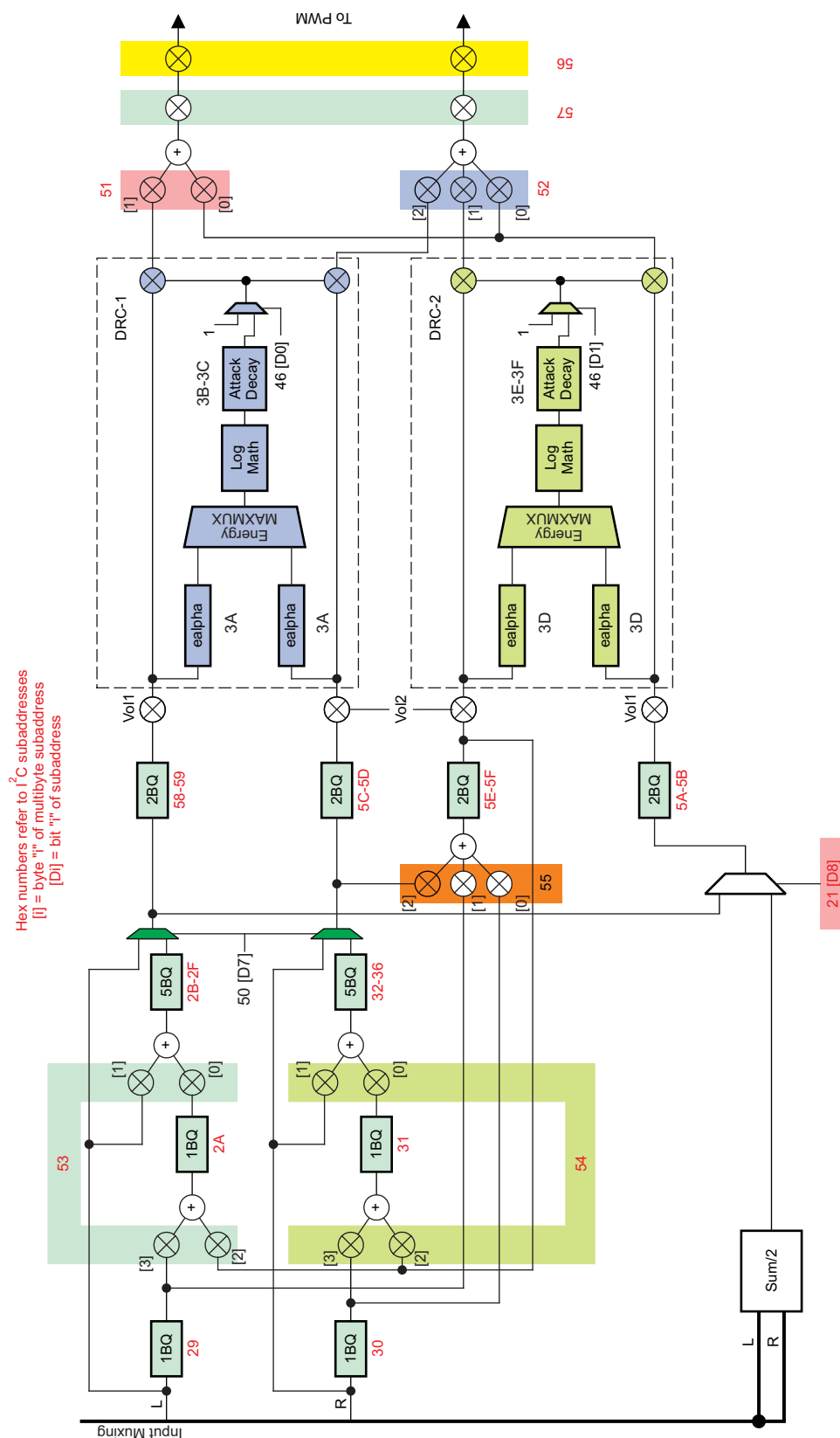
\*Refer to user's guide for Loop Filter details.

## FUNCTIONAL VIEW



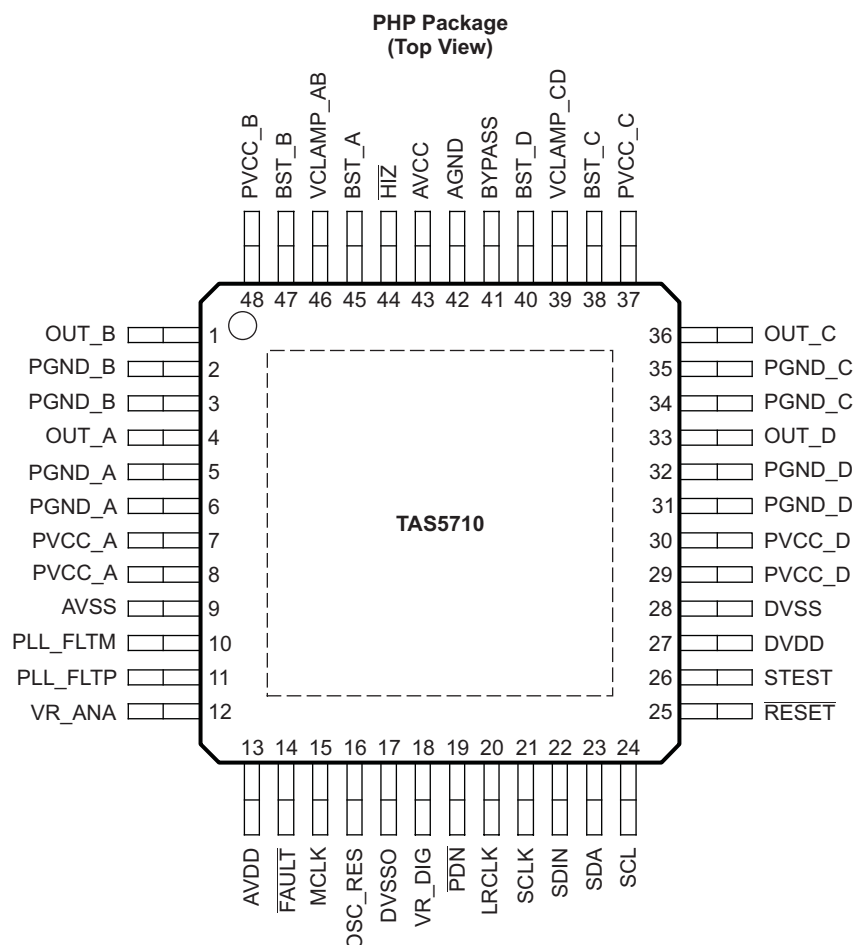
B0262-06

## DAP Process Flow



B0321-05

## 48-PIN, HTQFP PACKAGE (TOP VIEW)



P0075-03

## PIN FUNCTIONS

| PIN    |     | TYPE<br>(1) | 5-V<br>TOLERANT | TERMINATION<br>(2) | DESCRIPTION                                                                        |
|--------|-----|-------------|-----------------|--------------------|------------------------------------------------------------------------------------|
| NAME   | NO. |             |                 |                    |                                                                                    |
| AGND   | 42  | P           |                 |                    | Analog ground for power stage                                                      |
| AVCC   | 43  | P           |                 |                    | Analog power supply for power stage. Connect externally to same potential as PVCC. |
| AVDD   | 13  | P           |                 |                    | 3.3-V analog power supply                                                          |
| AVSS   | 9   | P           |                 |                    | Analog 3.3-V supply ground                                                         |
| BST_A  | 45  | P           |                 |                    | High-side bootstrap supply for half-bridge A                                       |
| BST_B  | 47  | P           |                 |                    | High-side bootstrap supply for half-bridge B                                       |
| BST_C  | 38  | P           |                 |                    | High-side bootstrap supply for half-bridge C                                       |
| BST_D  | 40  | P           |                 |                    | High-side bootstrap supply for half-bridge D                                       |
| BYPASS | 41  | AO          |                 |                    | Nominally equal to $V_{CC}/8$ . Internal reference voltage for analog cells        |
| DVDD   | 27  | P           |                 |                    | 3.3-V digital power supply                                                         |
| DVSS   | 28  | P           |                 |                    | Digital ground                                                                     |
| DVSSO  | 17  | P           |                 |                    | Oscillator Ground                                                                  |
| HIZ    | 44  | DI          |                 | Pullup             | Enable high-impedance (Hi-Z) mode (active low)                                     |

(1) TYPE: A = analog; D = 3.3-V digital; P = power/ground/decoupling; I = input; O = output

(2) All pullups are weak pullups and all pulldowns are weak pulldowns. The pullups and pulldowns are included to assure proper input logic levels if the pins are left unconnected (pullups → logic 1 input; pulldowns → logic 0 input).

**PIN FUNCTIONS (continued)**

| PIN                       |        | TYPE<br>(1) | 5-V<br>TOLERANT | TERMINATION<br>(2) | DESCRIPTION                                                                                                                                                                                                                                            |
|---------------------------|--------|-------------|-----------------|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                      | NO.    |             |                 |                    |                                                                                                                                                                                                                                                        |
| LRCLK                     | 20     | DI          | 5-V             | Pulldown           | Input serial audio data left/right clock (sample rate clock)                                                                                                                                                                                           |
| MCLK                      | 15     | DI          | 5-V             | Pulldown           | Master Clock Input                                                                                                                                                                                                                                     |
| OSC_RES                   | 16     | AO          |                 |                    | Oscillator trim resistor. Connect an 18.2-kΩ 1% resistor to DVSSO.                                                                                                                                                                                     |
| OUT_A                     | 4      | O           |                 |                    | Output, half-bridge A                                                                                                                                                                                                                                  |
| OUT_B                     | 1      | O           |                 |                    | Output, half-bridge B                                                                                                                                                                                                                                  |
| OUT_C                     | 36     | O           |                 |                    | Output, half-bridge C                                                                                                                                                                                                                                  |
| OUT_D                     | 33     | O           |                 |                    | Output, half-bridge D                                                                                                                                                                                                                                  |
| $\overline{\text{PDN}}$   | 19     | DI          | 5-V             | Pullup             | Power down, active-low. $\overline{\text{PDN}}$ prepares the device for loss of power supplies by shutting down the Noise Shaper and initiating PWM stop sequence.                                                                                     |
| PGND_A                    | 5, 6   | P           |                 |                    | Power ground for half-bridge A                                                                                                                                                                                                                         |
| PGND_B                    | 2, 3   | P           |                 |                    | Power ground for half-bridge B                                                                                                                                                                                                                         |
| PGND_C                    | 34, 35 | P           |                 |                    | Power ground for half-bridge C                                                                                                                                                                                                                         |
| PGND_D                    | 31, 32 | P           |                 |                    | Power ground for half-bridge D                                                                                                                                                                                                                         |
| PLL_FLTM                  | 10     | AO          |                 |                    | PLL negative loop filter terminal                                                                                                                                                                                                                      |
| PLL_FLTP                  | 11     | AO          |                 |                    | PLL positive loop filter terminal                                                                                                                                                                                                                      |
| PVCC_A                    | 7, 8   | P           |                 |                    | Power supply input for half-bridge output A                                                                                                                                                                                                            |
| PVCC_B                    | 48     | P           |                 |                    | Power supply input for half-bridge output B                                                                                                                                                                                                            |
| PVCC_C                    | 37     | P           |                 |                    | Power supply input for half-bridge output C                                                                                                                                                                                                            |
| PVCC_D                    | 29, 30 | P           |                 |                    | Power supply input for half-bridge output D                                                                                                                                                                                                            |
| $\overline{\text{RESET}}$ | 25     | DI          | 5-V             | Pullup             | Reset, active-low. A system reset is generated by applying a logic low to this pin. $\overline{\text{RESET}}$ is an asynchronous control signal that restores the DAP to its default conditions, and places the PWM in the hard mute state (3-stated). |
| SCL                       | 24     | DI          | 5-V             |                    | I <sup>2</sup> C serial control clock input                                                                                                                                                                                                            |
| SCLK                      | 21     | DI          | 5-V             | Pulldown           | Serial audio data clock (shift clock). SCLK is the serial audio port input data bit clock.                                                                                                                                                             |
| SDA                       | 23     | DIO         | 5-V             |                    | I <sup>2</sup> C serial control data interface input/output                                                                                                                                                                                            |
| SDIN                      | 22     | DI          | 5-V             | Pulldown           | Serial audio data input. SDIN supports three discrete (stereo) data formats.                                                                                                                                                                           |
| STEST                     | 26     | DI          |                 |                    | Factory test pin. Connect directly to DVSS.                                                                                                                                                                                                            |
| $\overline{\text{FAULT}}$ | 14     | DO          |                 |                    | Backend error indicator. Asserted LOW for over current errors. De-asserted upon recovery from error condition.                                                                                                                                         |
| VR_ANA                    | 12     | P           |                 |                    | Internally regulated 1.8-V analog supply voltage. This pin must not be used to power external devices.                                                                                                                                                 |
| VR_DIG                    | 18     | P           |                 |                    | Internally regulated 1.8-V digital supply voltage. This pin must not be used to power external devices.                                                                                                                                                |
| VCLAMP_AB                 | 46     | AO          |                 |                    | Internally generated voltage supply for channel A and B gate drive. This pin must not be used to power external devices. Connect only to external decoupling capacitor                                                                                 |
| VCLAMP_CD                 | 39     | AO          |                 |                    | Internally generated voltage supply for channel C and D gate drive. This pin must not be used to power external devices. Connect only to external decoupling capacitor                                                                                 |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)(2)</sup>

|                                             |                                                          | VALUE                             | UNIT |
|---------------------------------------------|----------------------------------------------------------|-----------------------------------|------|
| Supply voltage                              | DVDD, AVDD                                               | –0.3 to 3.6                       | V    |
|                                             | PVCC_X, AVCC                                             | –0.3 to 30                        | V    |
| Input voltage                               | 3.3-V digital inputs (except $\overline{\text{HIZ}}$ )   | –0.5 to DVDD + 0.5                | V    |
|                                             | 3.3-V $\overline{\text{HIZ}}$ input                      | –0.3 to AVDD + 0.3                | V    |
|                                             | 5-V tolerant <sup>(3)</sup> digital inputs (except MCLK) | –0.5 to DVDD + 2.5 <sup>(2)</sup> | V    |
|                                             | 5-V tolerant MCLK input                                  | –0.5 to AVDD + 2.5 <sup>(2)</sup> | V    |
| OUT_x to PGND_X                             |                                                          | 32 <sup>(4)</sup>                 | V    |
| BST_x to PGND_X                             |                                                          | 43 <sup>(4)</sup>                 | V    |
| Operating free-air temperature              |                                                          | 0 to 85                           | °C   |
| Operating junction temperature range        |                                                          | 0 to 150                          | °C   |
| Storage temperature range, T <sub>stg</sub> |                                                          | –40 to 125                        | °C   |

- (1) Stresses beyond those listed under *absolute ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operation conditions* are not implied. Exposure to absolute-maximum conditions for extended periods may affect device reliability.
- (2) Maximum pin voltage should not exceed 6.0V
- (3) 5-V tolerant inputs are  $\overline{\text{PDN}}$ ,  $\overline{\text{RESET}}$ , SCLK, LRCLK, MCLK, SDIN, SDA, and SCL.
- (4) DC voltage + peak ac waveform measured at the pin should be below the allowed limit for all conditions.

## DISSIPATION RATINGS<sup>(1)</sup>

| PACKAGE           | DERATING FACTOR<br>ABOVE T <sub>A</sub> = 25°C | T <sub>A</sub> ≤ 25°C<br>POWER RATING | T <sub>A</sub> = 45°C<br>POWER RATING | T <sub>A</sub> = 70°C<br>POWER RATING |
|-------------------|------------------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|
| 7-mm × 7-mm HTQFP | 40 mW/°C                                       | 5 W                                   | 4.2 W                                 | 3.2 W                                 |

- (1) This data was taken using 1 oz trace and copper pad that is soldered directly to a JEDEC standard high-k PCB. The thermal pad must be soldered to a thermal land on the printed-circuit board. See TI Technical Briefs SLMA002 for more information about using the HTQFP thermal pad

## RECOMMENDED OPERATING CONDITIONS

|                               |                                      |                                                         | MIN | NOM | MAX | UNIT |
|-------------------------------|--------------------------------------|---------------------------------------------------------|-----|-----|-----|------|
|                               | Digital/analog supply voltage        | DVDD, AVDD                                              | 3   | 3.3 | 3.6 | V    |
|                               | Half-bridge supply voltage           | PVCC_X, AVCC                                            | 10  |     | 26  | V    |
| V <sub>IH</sub>               | High-level input voltage             | Digital Inputs                                          | 2   |     |     | V    |
| V <sub>IL</sub>               | Low-level input voltage              | Digital Inputs                                          |     |     | 0.8 | V    |
| T <sub>A</sub>                | Operating ambient temperature range  |                                                         | 0   |     | 85  | °C   |
| T <sub>J</sub> <sup>(1)</sup> | Operating junction temperature range |                                                         | 0   |     | 125 | °C   |
| R <sub>L</sub> (BTL)          | Load impedance                       | Output filter: L = 33 μH, C = 1 μF.                     | 6   | 8   |     | Ω    |
| R <sub>L</sub> (PBTl)         | Load impedance                       | Output filter: L = 33 μH, C = 1 μF.                     | 3.2 | 4   |     | Ω    |
| L <sub>O</sub> (BTL)          | Output-filter inductance             | Minimum output inductance under short-circuit condition | 10  |     |     | μH   |
| L <sub>O</sub> (PBTl)         | Output-filter inductance             | Minimum output inductance under short-circuit condition | 10  |     |     | μH   |

- (1) Continuous operation above the recommended junction temperature may result in reduced reliability and/or lifetime of the device.

## PWM OPERATION AT RECOMMENDED OPERATING CONDITIONS

| PARAMETER          | TEST CONDITIONS                     | VALUE | UNIT |
|--------------------|-------------------------------------|-------|------|
| Output sample rate | 11.025/22.05/44.1-kHz data rate ±2% | 352.8 | kHz  |
|                    | 48/24/12/8/16/32-kHz data rate ±2%  | 384   |      |

## PLL INPUT PARAMETERS AND EXTERNAL FILTER COMPONENTS

| PARAMETER             |                                          | TEST CONDITIONS      | MIN    | TYP | MAX    | UNIT     |
|-----------------------|------------------------------------------|----------------------|--------|-----|--------|----------|
| $f_{\text{MCLKI}}$    | MCLK Frequency                           |                      | 2.8224 |     | 24.576 | MHz      |
|                       | MCLK duty cycle                          |                      | 40%    | 50% | 60%    |          |
| $t_r / t_f$<br>(MCLK) | Rise/fall time for MCLK                  |                      |        |     | 5      | ns       |
|                       | LRCLK allowable drift before LRCLK reset |                      |        |     | 4      | MCLKs    |
|                       | External PLL filter capacitor C1         | SMD 0603 Y5V         |        | 47  |        | nF       |
|                       | External PLL filter capacitor C2         | SMD 0603 Y5V         |        | 4.7 |        | nF       |
|                       | External PLL filter resistor R           | SMD 0603, metal film |        | 470 |        | $\Omega$ |

## ELECTRICAL CHARACTERISTICS

DC Characteristics, BD BTL Mode,  $F_S = 48 \text{ kHz}$ ,  $T_A = 25^\circ\text{C}$ ,  $PVCC\_X = AVCC = 18 \text{ V}$ ,  $DVDD=AVDD= 3.3\text{V}$ ,  $R_L = 8 \Omega$  (unless otherwise noted)

| PARAMETER                          |                                                       |                                   | TEST CONDITIONS                                                                                                 | MIN  | TYP  | MAX | UNIT |
|------------------------------------|-------------------------------------------------------|-----------------------------------|-----------------------------------------------------------------------------------------------------------------|------|------|-----|------|
| V <sub>OH</sub>                    | High-level output voltage                             | $\overline{\text{FAULT}}$ and SDA | I <sub>OH</sub> = −4 mA ,<br>DVDD=AVDD=3.0 V                                                                    | 2.4  |      |     | V    |
| V <sub>OL</sub>                    | Low-level output voltage                              | $\overline{\text{FAULT}}$ and SDA | I <sub>OL</sub> = 4 mA ,<br>DVDD=AVDD=3.0 V                                                                     |      |      | 0.5 | V    |
| VOS                                | Class-D output offset voltage                         |                                   |                                                                                                                 | 26   |      |     | mV   |
| V <sub>BYPASS</sub>                | PVCC/8 reference for analog section                   |                                   | No load                                                                                                         | 2.1  | 2.26 | 2.4 | V    |
| I <sub>IL</sub>                    | Low-level input current                               | Digital Inputs                    | V <sub>I</sub> ≤ V <sub>IL</sub><br>DVDD = AVDD = 3.6 V                                                         |      |      | 75  | μA   |
| I <sub>IH</sub>                    | High-level input current                              | Digital Inputs                    | V <sub>I</sub> ≥ V <sub>IH</sub><br>DVDD = AVDD = 3.6 V                                                         |      |      | 75  | μA   |
| I <sub>DD</sub>                    | 3.3-V supply current                                  | 3.3V Supply voltage (DVDD + AVDD) | Normal mode                                                                                                     | 43   | 77   |     | mA   |
|                                    |                                                       |                                   | Reset ( $\overline{\text{RESET}}$ = low, $\overline{\text{PDN}}$ = high)                                        | 19   | 24   |     |      |
| I <sub>CC</sub>                    | Half-Bridge supply current                            | No Load (PVCC + AVCC)             | Normal Mode                                                                                                     | 34   | 60   |     | mA   |
|                                    |                                                       |                                   | Reset ( $\overline{\text{RESET}}$ = low, $\overline{\text{PDN}}$ = high)                                        | 54   | 310  |     | μA   |
| r <sub>DS(on)</sub> <sup>(1)</sup> | Drain-to-source resistance, high-side                 |                                   | V <sub>CC</sub> = 18 V , I <sub>O</sub> = 500 mA,<br>T <sub>J</sub> = 25°C, includes<br>metalization resistance | 240  |      |     | mΩ   |
|                                    | Drain-to-source resistance, low-side                  |                                   |                                                                                                                 | 240  |      |     |      |
| Protection                         |                                                       |                                   |                                                                                                                 |      |      |     |      |
| V <sub>uvp</sub>                   | Undervoltage protection limit                         | PVCC_X = AVCC falling             |                                                                                                                 | 8.4  |      |     | V    |
| V <sub>uvp,hyst</sub>              | Undervoltage protection limit                         | PVCC_X = AVCC rising              |                                                                                                                 | 8.5  |      |     | V    |
| V <sub>ovp</sub>                   | Overvoltage protection limit                          | PVCC_X = AVCC rising              |                                                                                                                 | 27.5 |      |     | V    |
| V <sub>ovp,hyst</sub>              | Overvoltage protection limit                          | PVCC_X = AVCC falling             |                                                                                                                 | 27.2 |      |     | V    |
| OTE <sup>(2)</sup>                 | Over temperature error (output shutdown, unlatched)   |                                   |                                                                                                                 | 150  |      |     | °C   |
| OTE <sub>HYST</sub> <sup>(2)</sup> | Extra temperature drop required to recover from error |                                   |                                                                                                                 | 15   |      |     | °C   |

(1) This does not include bond-wire or pin resistance.

(2) Specified by design

## AC Characteristics

PVCC<sub>x</sub> = AVCC = 18V, BTL BD Mode, FS=48KHz, T<sub>A</sub> = 25°C, AVDD = DVDD = 3.3 V, R<sub>L</sub> = 8 Ω, C<sub>BST</sub> = 220 nF, Audio Frequency = 1 kHz, AES17 filter (unless otherwise noted). All performance is in accordance with recommended operating conditions (unless otherwise specified).

| PARAMETER        |                                      | TEST CONDITIONS                                      | MIN | TYP   | MAX | UNIT |
|------------------|--------------------------------------|------------------------------------------------------|-----|-------|-----|------|
| K <sub>SVR</sub> | Supply ripple rejection              | 200-mV <sub>PP</sub> ripple at 1 kHz, no audio input |     | –80   |     | dB   |
| P <sub>O</sub>   | Continuous output power              | THD+N = 10%, f = 1 kHz                               |     | 20.2  |     | W    |
|                  |                                      | THD+N = 7%, f = 1 kHz                                |     | 18.8  |     | W    |
| THD+N            | Total harmonic distortion + noise    | f = 1 kHz, P <sub>O</sub> = 1 W                      |     | 0.03% |     |      |
| V <sub>n</sub>   | Output integrated noise (rms)        | A-weighted                                           |     | 105   |     | μV   |
| Crosstalk        |                                      | P <sub>O</sub> = 1 W, f = 1 kHz                      |     | –63   |     | dB   |
| SNR              | Signal-to-noise ratio <sup>(1)</sup> | Maximum Power at THD+N < 1%, f = 1 kHz, A-weighted   |     | 100   |     | dB   |

(1) SNR is calculated relative to 0-dBFS Input Level

## AC Characteristics

PVCC<sub>x</sub> = AVCC = 12V, BTL BD Mode, FS=48KHz, T<sub>A</sub> = 25°C, AVDD = DVDD = 3.3 V, R<sub>L</sub> = 8 Ω, C<sub>BST</sub> = 220 nF, Audio Frequency = 1 kHz, AES17 filter (unless otherwise noted). All performance is in accordance with recommended operating conditions (unless otherwise specified).

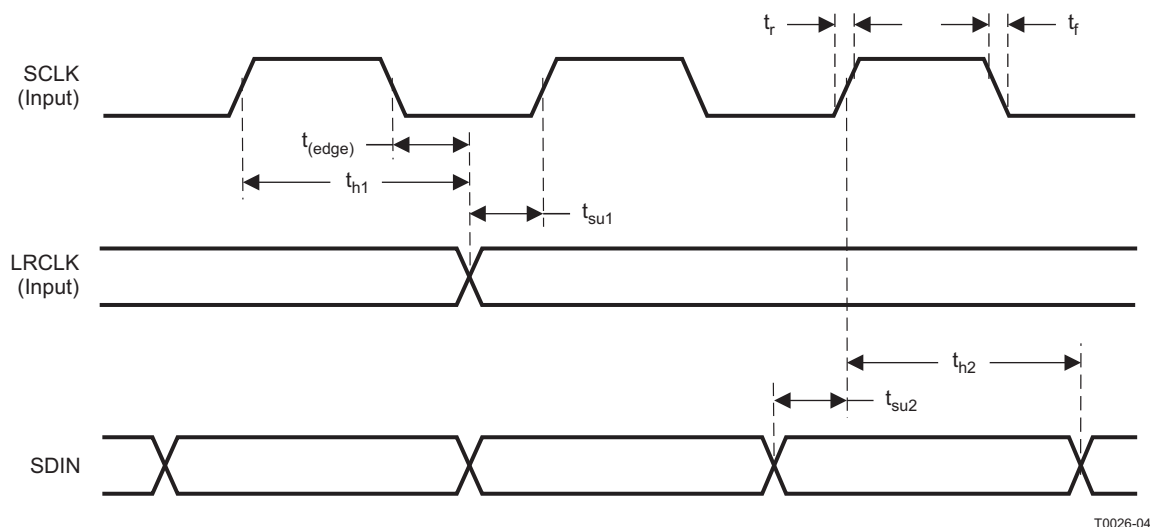
| PARAMETER        |                                      | TEST CONDITIONS                                      | MIN | TYP   | MAX | UNIT |
|------------------|--------------------------------------|------------------------------------------------------|-----|-------|-----|------|
| K <sub>SVR</sub> | Supply ripple rejection              | 200-mV <sub>PP</sub> ripple at 1 kHz, no audio input |     | –80   |     | dB   |
| P <sub>O</sub>   | Continuous output power              | THD+N = 10%, f = 1 kHz                               |     | 8.8   |     | W    |
|                  |                                      | THD+N = 7%, f = 1 kHz                                |     | 8.4   |     | W    |
| THD+N            | Total harmonic distortion + noise    | f = 1 kHz, P <sub>O</sub> = 1 W                      |     | 0.04% |     |      |
| V <sub>n</sub>   | Output integrated noise (rms)        | A-weighted                                           |     | 106   |     | μV   |
| Crosstalk        |                                      | f = 1 kHz, P <sub>O</sub> = 1 W                      |     | –63   |     | dB   |
| SNR              | Signal-to-noise ratio <sup>(1)</sup> | Maximum Power at THD+N < 1%, f = 1 kHz, A-weighted   |     | 97    |     | dB   |

(1) SNR is calculated relative to 0-dBFS Input Level

## SERIAL AUDIO PORTS SLAVE MODE

over recommended operating conditions (unless otherwise noted)

| PARAMETER                                |                                                                     | TEST CONDITIONS       | MIN   | TYP | MAX    | UNIT        |
|------------------------------------------|---------------------------------------------------------------------|-----------------------|-------|-----|--------|-------------|
| $f_{\text{SCLKIN}}$                      | Frequency, SCLK $32 \times f_s$ , $48 \times f_s$ , $64 \times f_s$ | $C_L = 30 \text{ pF}$ | 1.024 |     | 12.288 | MHz         |
| $t_{\text{su1}}$                         | Setup time, LRCLK to SCLK rising edge                               |                       | 10    |     |        | ns          |
| $t_{\text{h1}}$                          | Hold time, LRCLK from SCLK rising edge                              |                       | 10    |     |        | ns          |
| $t_{\text{su2}}$                         | Setup time, SDIN to SCLK rising edge                                |                       | 10    |     |        | ns          |
| $t_{\text{h2}}$                          | Hold time, SDIN from SCLK rising edge                               |                       | 10    |     |        | ns          |
|                                          | LRCLK frequency                                                     |                       | 8     | 48  | 48     | kHz         |
|                                          | SCLK duty cycle                                                     |                       | 40%   | 50% | 60%    |             |
|                                          | LRCLK duty cycle                                                    |                       | 40%   | 50% | 60%    |             |
|                                          | SCLK rising edges between LRCLK rising edges                        |                       | 32    |     | 64     | SCLK edges  |
| $t_{\text{(edge)}}$                      | LRCLK clock edge with respect to the falling edge of SCLK           |                       | -1/4  |     | 1/4    | SCLK period |
| $t_r / t_f$<br>$t_{\text{(SCLK/LRCLK)}}$ | Rise/fall time for SCLK/LRCLK                                       |                       |       |     | 8      | ns          |

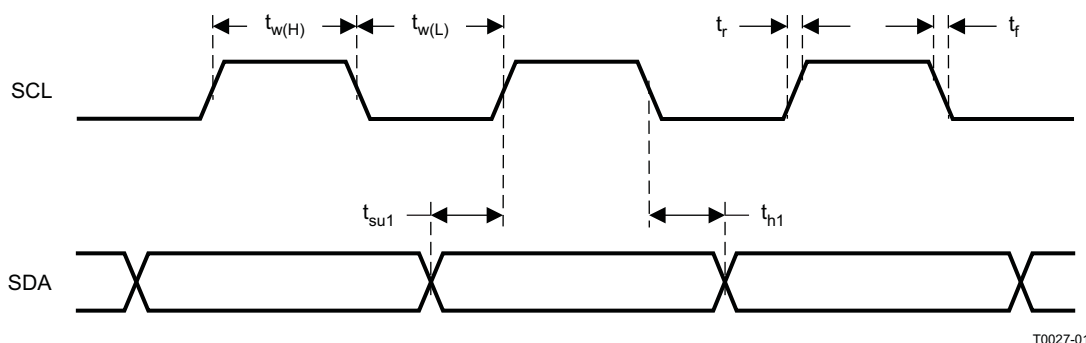


**Figure 3. Slave Mode Serial Data Interface Timing**

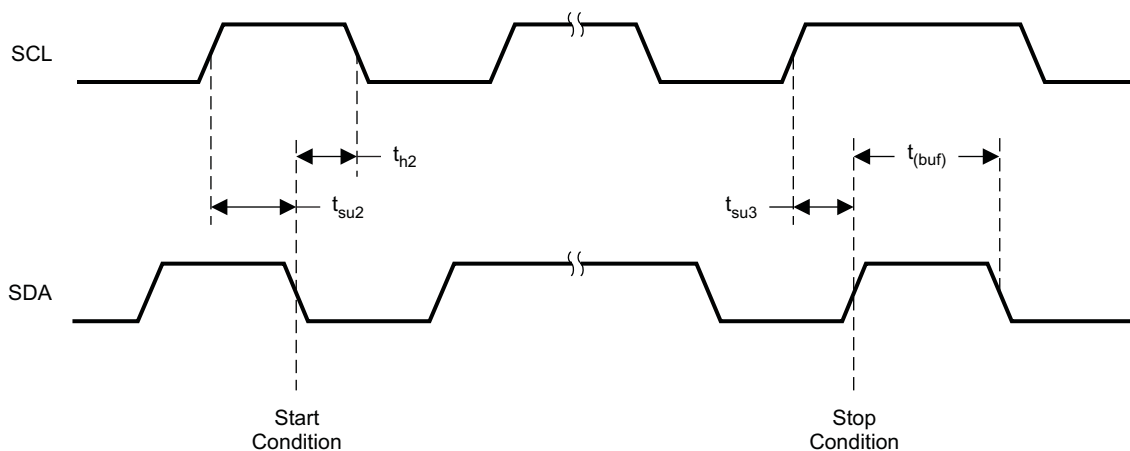
## I<sup>2</sup>C SERIAL CONTROL PORT OPERATION

Timing characteristics for I<sup>2</sup>C Interface signals over recommended operating conditions (unless otherwise noted)

| PARAMETER   |                                                | TEST CONDITIONS | MIN | MAX | UNIT    |
|-------------|------------------------------------------------|-----------------|-----|-----|---------|
| $f_{SCL}$   | Frequency, SCL                                 | No wait states  |     | 400 | kHz     |
| $t_{w(H)}$  | Pulse duration, SCL high                       |                 | 0.6 |     | $\mu$ s |
| $t_{w(L)}$  | Pulse duration, SCL low                        |                 | 1.3 |     | $\mu$ s |
| $t_r$       | Rise time, SCL and SDA                         |                 |     | 300 | ns      |
| $t_f$       | Fall time, SCL and SDA                         |                 |     | 300 | ns      |
| $t_{su1}$   | Setup time, SDA to SCL                         |                 | 100 |     | ns      |
| $t_{h1}$    | Hold time, SCL to SDA                          |                 | 0   |     | ns      |
| $t_{(buf)}$ | Bus free time between stop and start condition |                 | 1.3 |     | $\mu$ s |
| $t_{su2}$   | Setup time, SCL to start condition             |                 | 0.6 |     | $\mu$ s |
| $t_{h2}$    | Hold time, start condition to SCL              |                 | 0.6 |     | $\mu$ s |
| $t_{su3}$   | Setup time, SCL to stop condition              |                 | 0.6 |     | $\mu$ s |
| $C_L$       | Load capacitance for each bus line             |                 |     | 400 | pF      |



**Figure 4. SCL and SDA Timing**

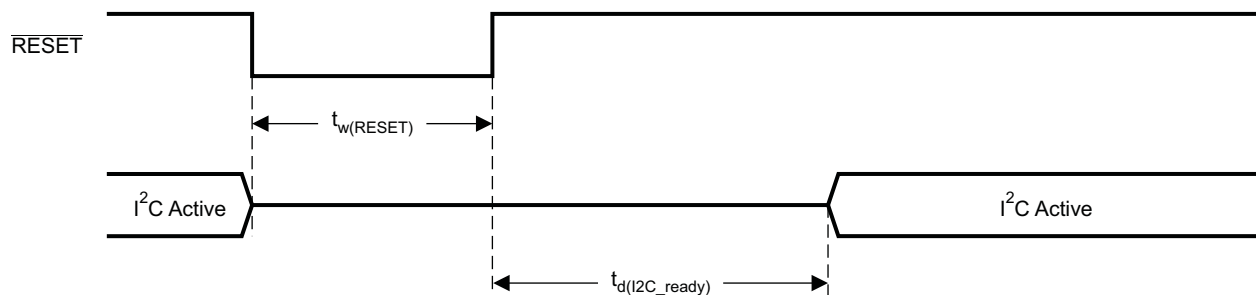


**Figure 5. Start and Stop Conditions Timing**

## RESET TIMING ( $\overline{\text{RESET}}$ )

Control signal parameters over recommended operating conditions (unless otherwise noted). Please refer to Recommended Use Model section on usage of all terminals.

| PARAMETER                          |                                                  | MIN | TYP | MAX  | UNIT |
|------------------------------------|--------------------------------------------------|-----|-----|------|------|
| $t_{w(\text{RESET})}$              | Pulse duration, $\overline{\text{RESET}}$ active | 100 |     |      | us   |
| $t_{d(\text{I}^2\text{C\_ready})}$ | Time to enable $\text{I}^2\text{C}$              |     |     | 13.5 | ms   |



System Initialization.

Enable via  $\text{I}^2\text{C}$ .

T0421-01

NOTE: On power up, it is recommended that the TAS5710  $\overline{\text{RESET}}$  be held LOW for at least 100  $\mu\text{s}$  after DVDD has reached 3.0 V

NOTE: If the  $\overline{\text{RESET}}$  is asserted LOW while  $\overline{\text{PDN}}$  is LOW, then the  $\overline{\text{RESET}}$  must continue to be held LOW for at least 100  $\mu\text{s}$  after  $\overline{\text{PDN}}$  is deasserted (HIGH).

Figure 6. Reset Timing

## TYPICAL CHARACTERISTICS, BTL CONFIGURATION

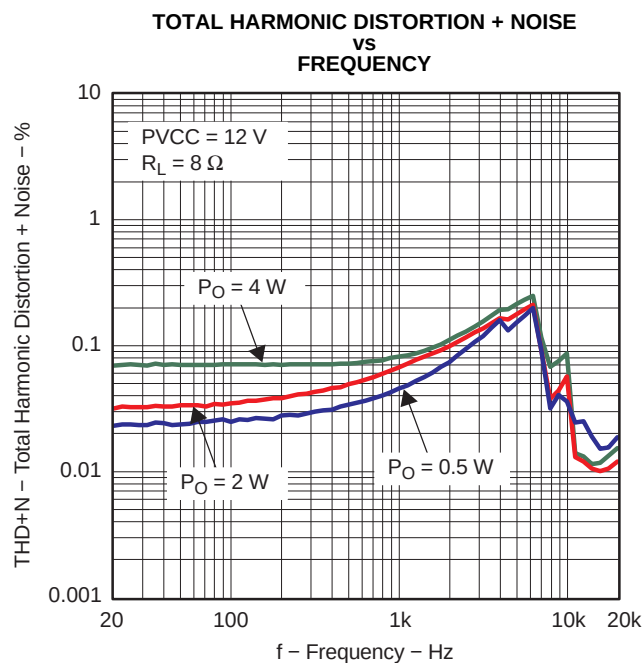


Figure 7.

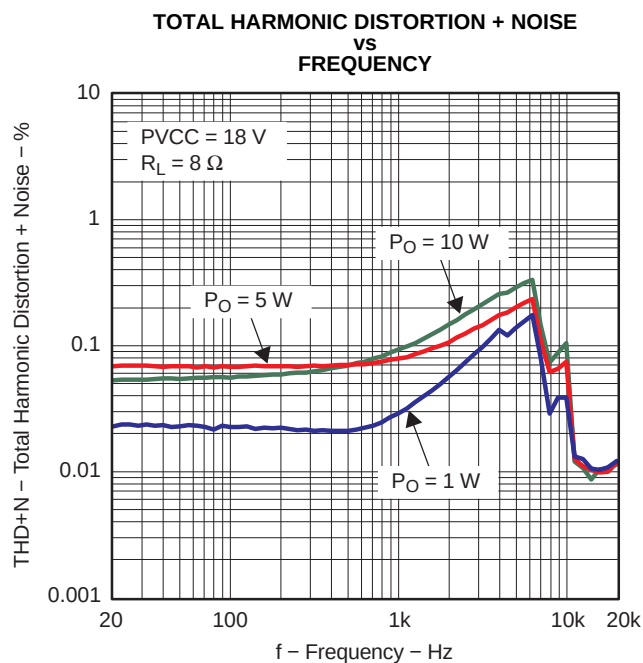
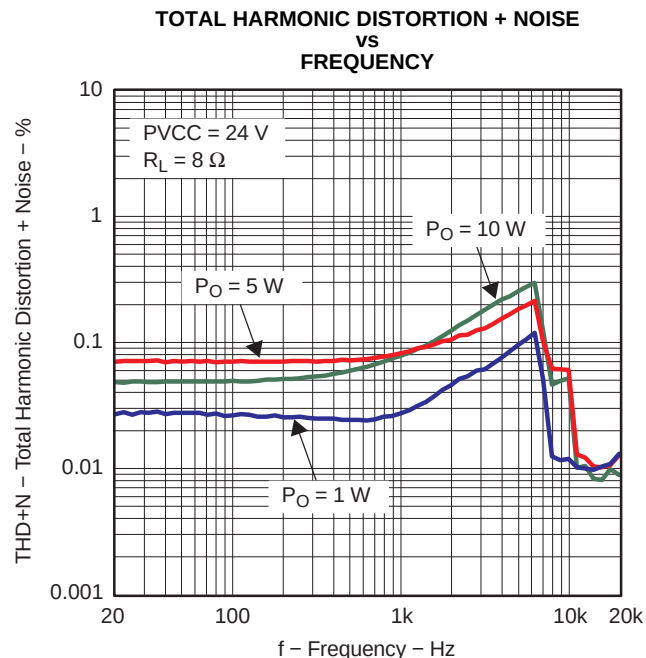
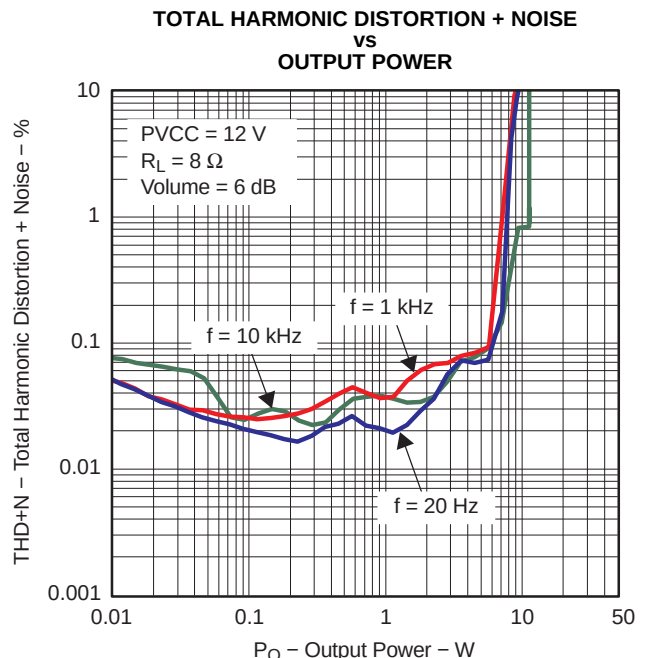


Figure 8.

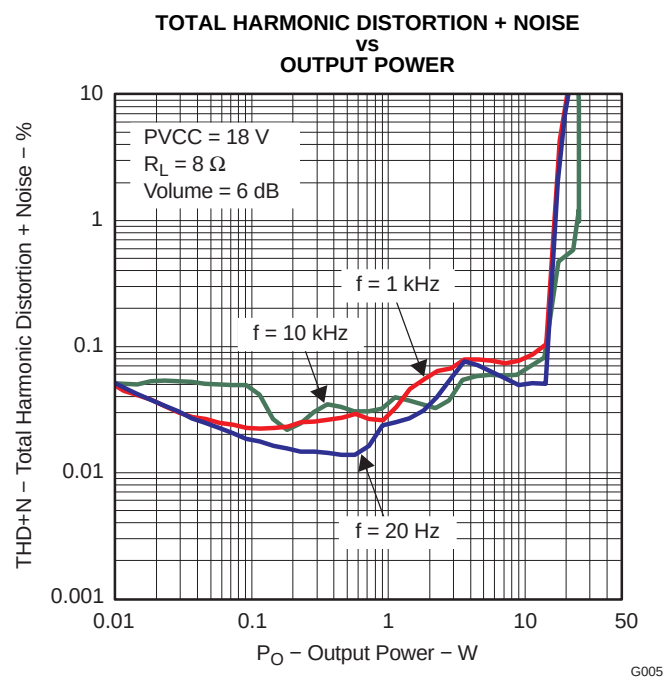
# **TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)**



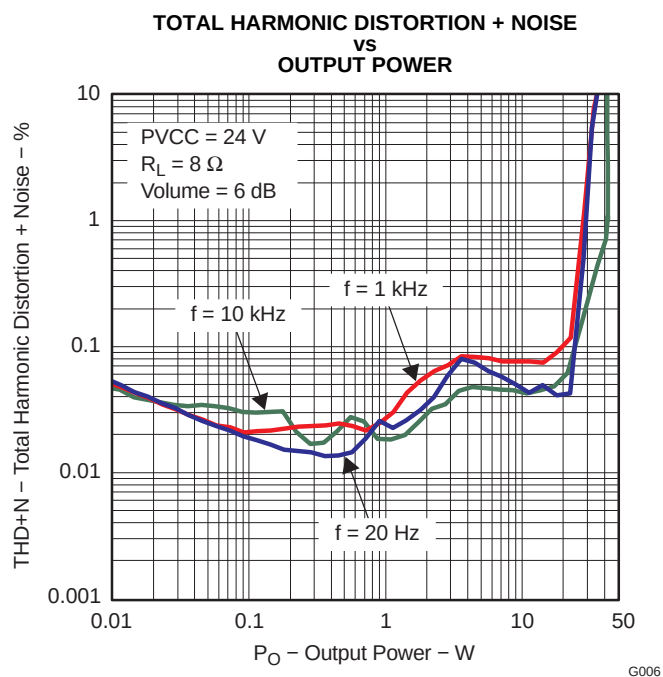
**Figure 9.**



**Figure 10.**



**Figure 11.**



**Figure 12.**

# TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

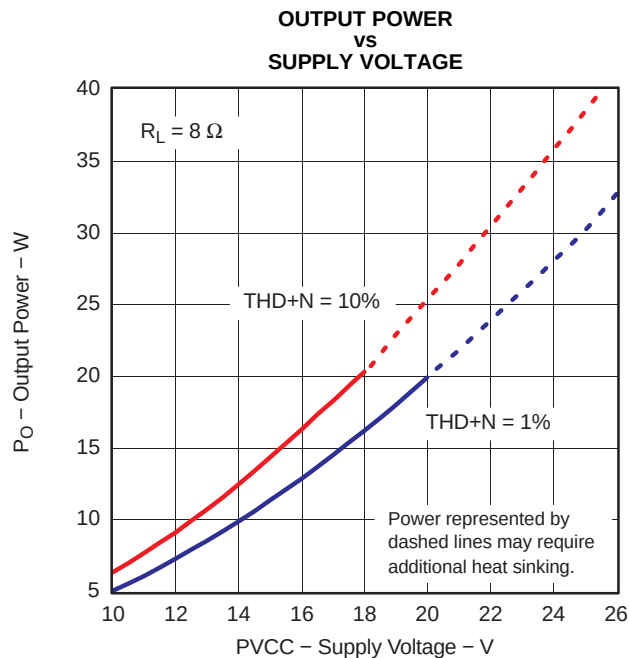


Figure 13.

G008

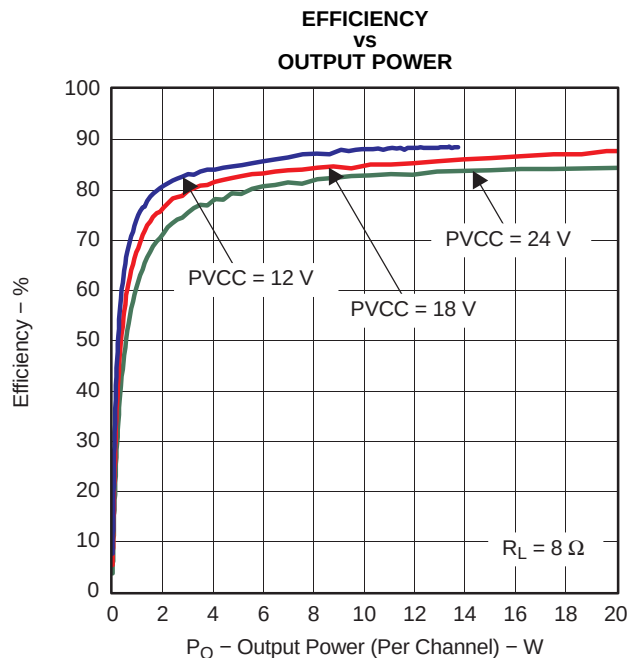


Figure 14.

G010

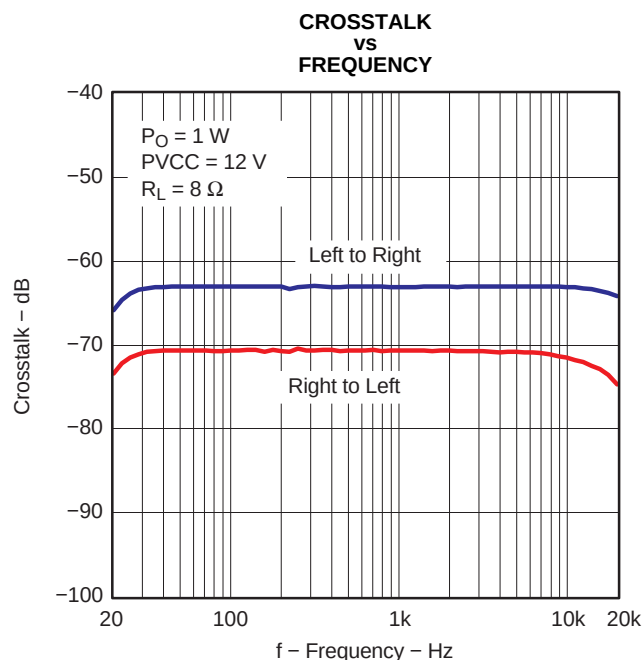


Figure 15.

G013

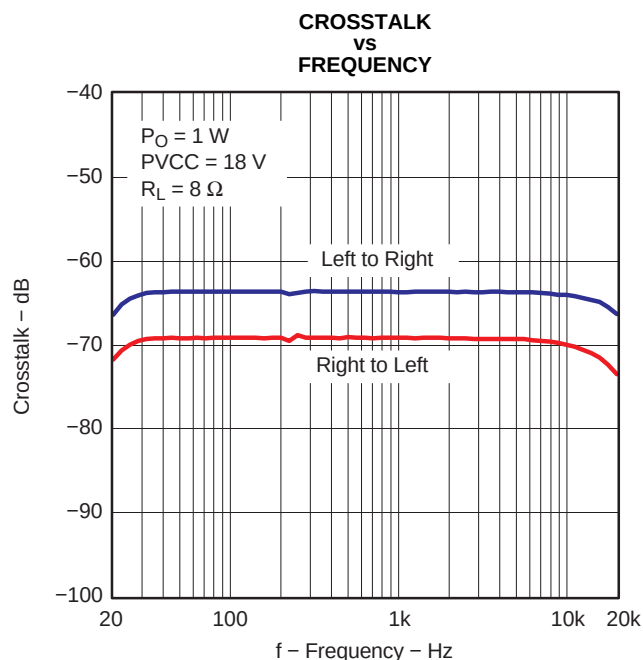


Figure 16.

G014

## TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

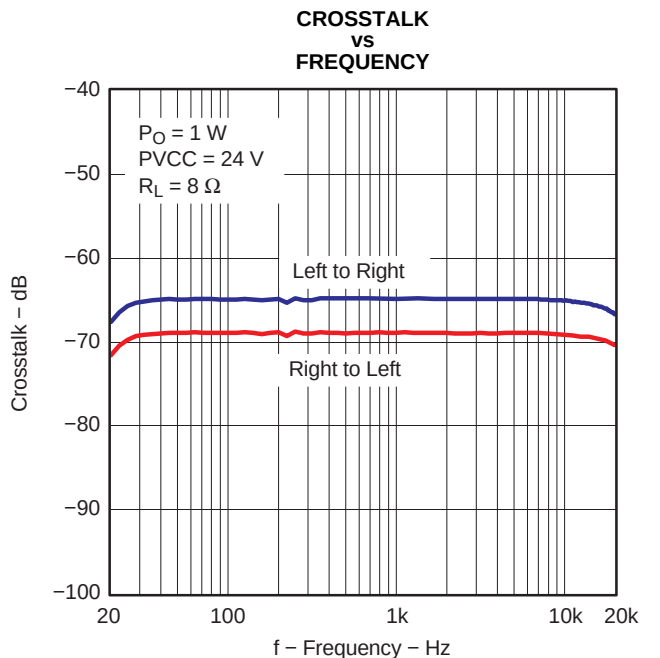


Figure 17.

## DETAILED DESCRIPTION

### POWER SUPPLY

To facilitate system design, the TAS5710 needs only a 3.3-V supply in addition to the 10-V to 26-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the gate drive circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors.

In order to provide good electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST\_X), and power-stage supply pins (PVCC\_X). The gate drive voltages (VCLAMP\_AB and VCLAMP\_CD) are derived from the PVCC voltage. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power-supply pins and decoupling capacitors must be avoided.

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST\_X) to the power-stage output pin (OUT\_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive regulator output pin (VCLAMP\_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 352 kHz to 384 kHz, it is recommended to use 220-nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 220-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVCC\_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVCC\_X pin is decoupled with a 100-nF ceramic capacitor placed as close as possible to each supply pin.

The TAS5710 is fully protected against erroneous power-stage turnon due to parasitic gate charging.

## ERROR REPORTING

Any fault resulting in device shutdown is signaled by the  $\overline{\text{FAULT}}$  pin going low (see [Table 1](#)). A sticky version of this pin is available on D1 of register 0X02.

**Table 1.  $\overline{\text{FAULT}}$  Output States**

| $\overline{\text{FAULT}}$ | DESCRIPTION                  |
|---------------------------|------------------------------|
| 0                         | Overcurrent (OC) ERROR       |
| 1                         | No faults (normal operation) |

## DEVICE PROTECTION SYSTEM

### Overcurrent (OC) Protection

The device has independent, fast-reacting current detectors on all high-side and low-side power-stage FETs, which protects against shorts across the load, to GND, or to PVCC. The protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state and  $\overline{\text{FAULT}}$  being asserted low. The device returns to normal operation once the fault condition (i.e., a short circuit on the output) is removed. Current limiting and overcurrent protection are not independent for half-bridges. That is, if the bridge-tied load between half-bridges A and B causes an overcurrent fault, half-bridges A, B, C, and D are shut down.

### Overtemperature Protection

The TAS5710 has an over-temperature protection system. If the device junction temperature exceeds 150°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state. The TAS5710 recovers automatically once the temperature drops approximately 15°.

### Undervoltage Protection (UVP) and Overvoltage Protection (OVP)

THE UVP circuits of the TAS5710 fully protect the device in any power-up/down and brownout situation. The UVP engages if PVCC\_X = AVCC drops below 8.4-V (typical) and disengages when PVCC\_X = AVCC exceeds 8.5-V. The OVP circuits protect against voltage spikes and engage when PVCC\_X = AVCC exceeds 27.5-V (typical). The OVP circuits disengage when PVCC\_X = AVCC drops below 27.2-V. When the protection circuits engage, all half-bridge outputs are immediately placed in the high-impedance (Hi-Z) state.

## SERIAL DATA INTERFACE

Serial data is input on SDIN. The PWM outputs are derived from SDIN. The TAS5710 DAP accepts serial data in 16-, 20-, or 24-bit left-justified, right-justified, and I<sup>2</sup>S serial data formats.

## CLOCK, AUTO DETECTION, and PLL

The TAS5710 is a slave device. It accepts MCLK, SCLK, and LRCLK. The digital audio processor (DAP) supports all the sample rates and MCLK rates that are defined in the [clock control register](#).

The TAS5710 checks to verify that SCLK is a specific value of 32 f<sub>s</sub>, 48 f<sub>s</sub>, or 64 f<sub>s</sub>. The DAP only supports a 1 × f<sub>s</sub> LRCLK. The timing relationship of these clocks to SDIN is shown in subsequent sections. The clock section uses MCLK or the internal oscillator clock (when MCLK is unstable, out of range, or absent) to produce the internal clock (DCLK) running at 512 times the PWM switching frequency.

The DAP can autodetect and set the internal clock control logic to the appropriate settings for all supported clock rates as defined in the clock control register.

TAS5710 has robust clock error handling that uses the built-in trimmed oscillator clock to quickly detect changes/errors. Once the system detects a clock change/error, it will mute the audio (through a single step mute) and then force PLL to limp using the internal oscillator as a reference clock. Once the clocks are stable, the system will auto detect the new rate and revert to normal operation. During this process, the default volume will be restored in a single step (also called hard unmute). The ramp process can be programmed to ramp back slowly (also called soft unmute) as defined in volume register (0X0E).

## PWM Section

The TAS5710 DAP device uses noise-shaping and sophisticated non-linear correction algorithms to achieve high power efficiency and high-performance digital audio reproduction. The DAP uses a fourth-order noise shaper to increase dynamic range and SNR in the audio band. The PWM section accepts 24-bit PCM data from the DAP and outputs two BTL PWM audio output channels.

The PWM section has individual channel dc blocking filters that can be enabled and disabled. The filter cutoff frequency is less than 1 Hz. Individual channel de-emphasis filters for 44.1- and 48-kHz are included and can be enabled and disabled.

Finally, the PWM section has an adjustable maximum modulation limit of 93.8% to 99.2%.

For detailed description of using audio processing features like DRC and EQ, please refer to User's Guide and TAS570X GDE software development tool documentation. Also refer to GDE software development tool for device data path.

## I<sup>2</sup>C COMPATIBLE SERIAL CONTROL INTERFACE

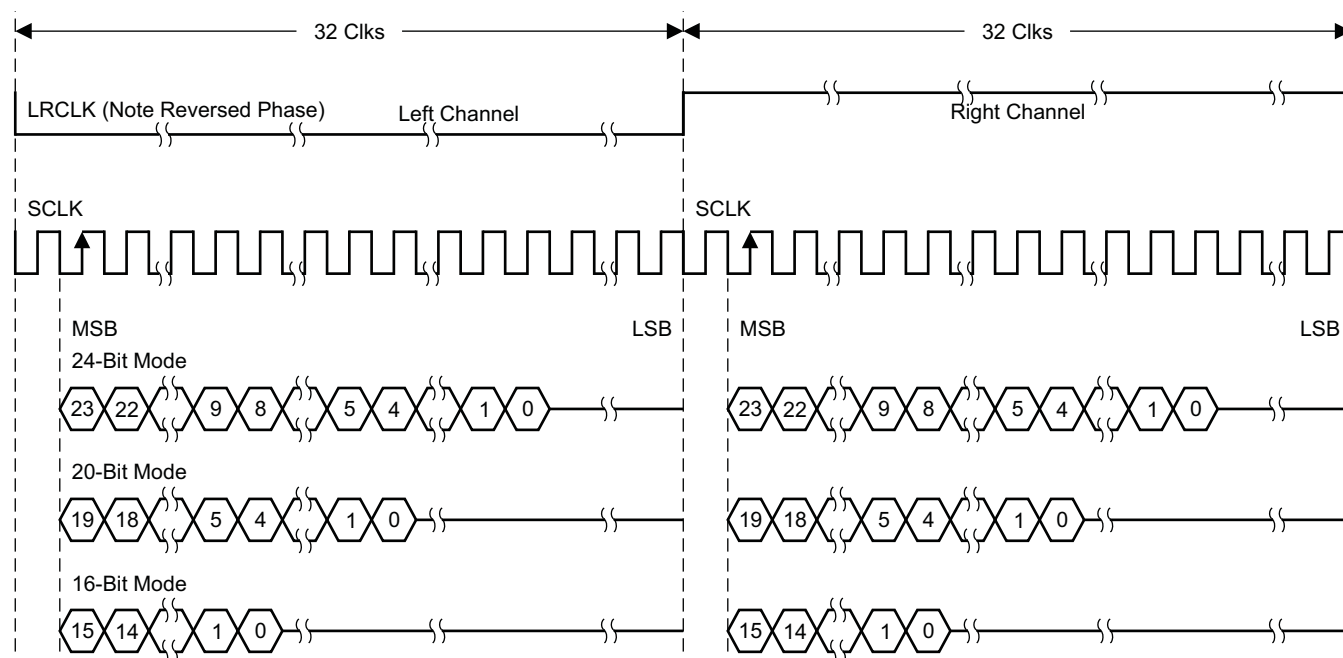
The TAS5710 DAP has an I<sup>2</sup>C serial control slave interface to receive commands from a system controller. The serial control interface supports both normal-speed (100-kHz) and high-speed (400-kHz) operations without wait states. As an added feature, this interface operates even if MCLK is absent.

The serial control interface supports both single-byte and multi-byte read and write operations for status registers and the general control registers associated with the PWM.

## SERIAL INTERFACE CONTROL AND TIMING

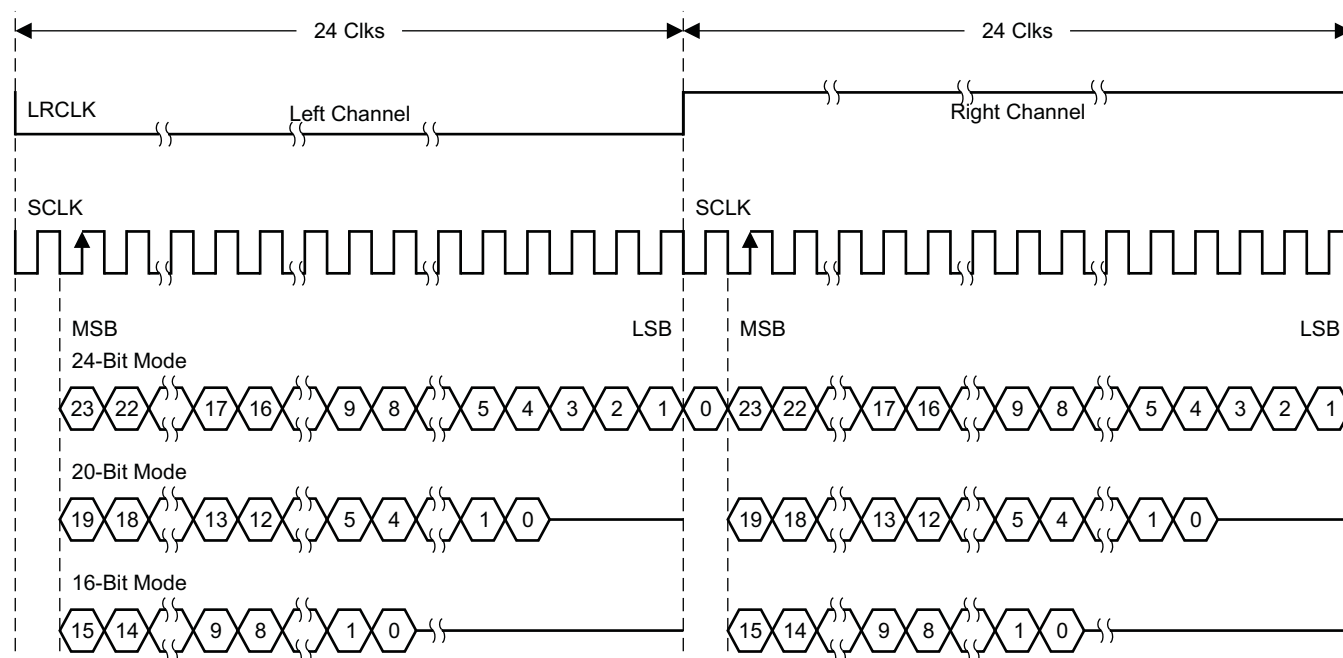
### I<sup>2</sup>S Timing

I<sup>2</sup>S timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is low for the left channel and high for the right channel. A bit clock running at 32, 48, or  $64 \times f_s$  is used to clock in the data. There is a delay of one bit clock from the time the LRCLK signal changes state to the first bit of data on the data lines. The data is written MSB first and is valid on the rising edge of bit clock. The DAP masks unused trailing data bit positions.

2-Channel I<sup>2</sup>S (Philips Format) Stereo Input

T0034-01

NOTE: All data presented in 2s-complement form with MSB first.

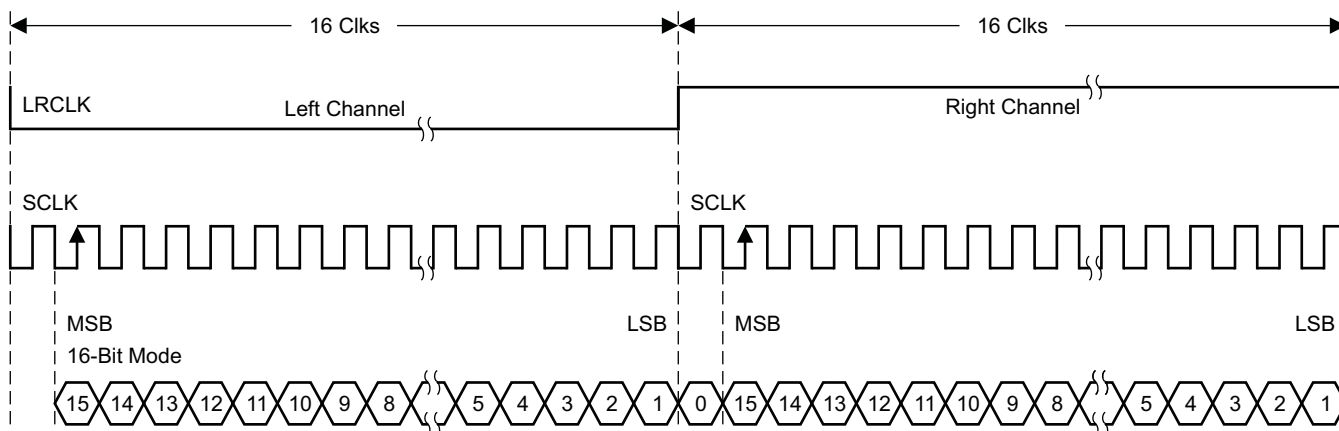
**Figure 18. I<sup>2</sup>S 64-f<sub>s</sub> Format**2-Channel I<sup>2</sup>S (Philips Format) Stereo Input/Output (24-Bit Transfer Word Size)

T0092-01

NOTE: All data presented in 2s-complement form with MSB first.

**Figure 19. I<sup>2</sup>S 48-f<sub>s</sub> Format**

## 2-Channel I<sup>2</sup>S (Philips Format) Stereo Input



T0266-01

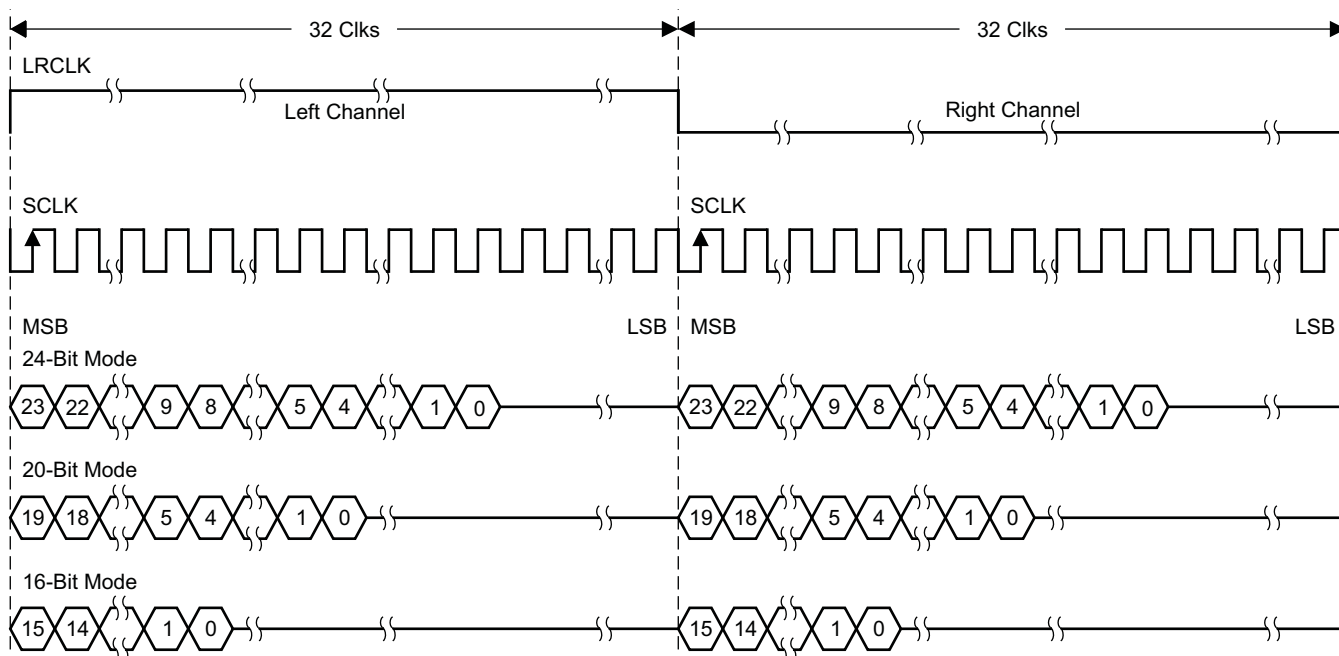
NOTE: All data presented in 2s-complement form with MSB first.

**Figure 20. I<sup>2</sup>S 32-f<sub>s</sub> Format**

## Left-Justified

Left-justified (LJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at  $32, 48, \text{ or } 64 \times f_s$  is used to clock in the data. The first bit of data appears on the data lines at the same time LRCLK toggles. The data is written MSB first and is valid on the rising edge of the bit clock. The DAP masks unused trailing data bit positions.

## 2-Channel Left-Justified Stereo Input

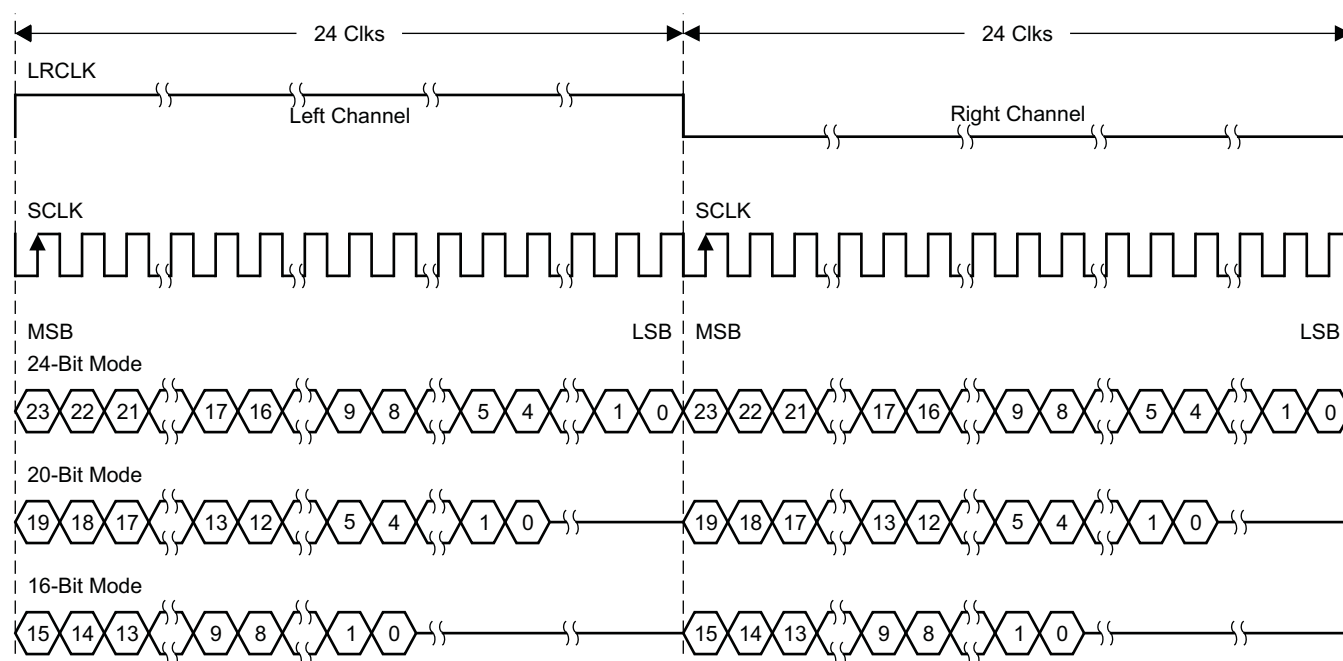


T0034-02

NOTE: All data presented in 2s-complement form with MSB first.

**Figure 21. Left-Justified 64-f<sub>s</sub> Format**

## 2-Channel Left-Justified Stereo Input (24-Bit Transfer Word Size)

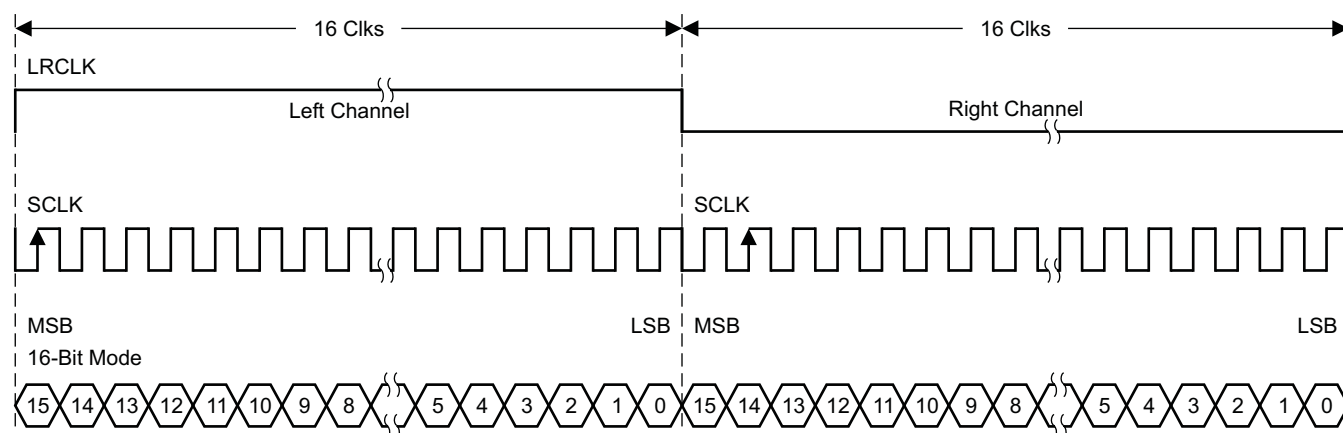


T0092-02

NOTE: All data presented in 2s-complement form with MSB first.

**Figure 22. Left-Justified 48- $f_s$  Format**

## 2-Channel Left-Justified Stereo Input



T0266-02

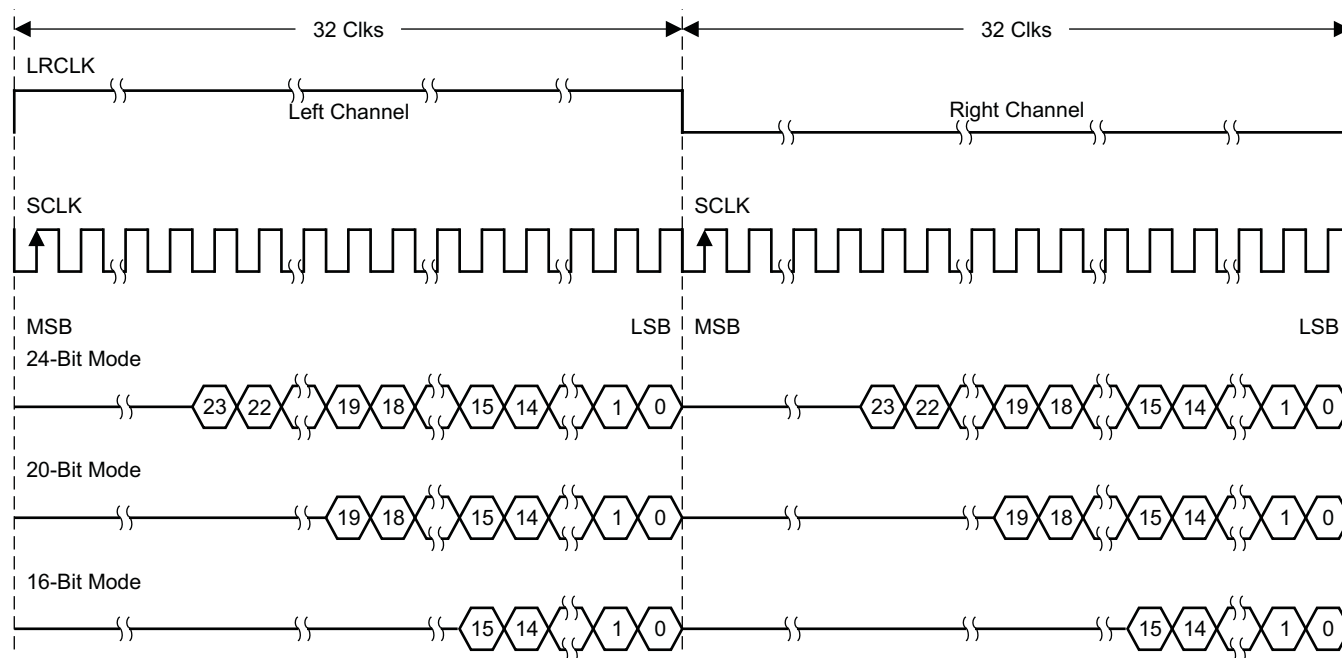
NOTE: All data presented in 2s-complement form with MSB first.

**Figure 23. Left-Justified 32- $f_s$  Format****Right-Justified**

Right-justified (RJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when

it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at  $32, 48, \text{ or } 64 \times f_s$  is used to clock in the data. The first bit of data appears on the data 8 bit-clock periods (for 24-bit data) after LRCLK toggles. In RJ mode the LSB of data is always clocked by the last bit clock before LRCLK transitions. The data is written MSB first and is valid on the rising edge of bit clock. The DAP masks unused leading data bit positions.

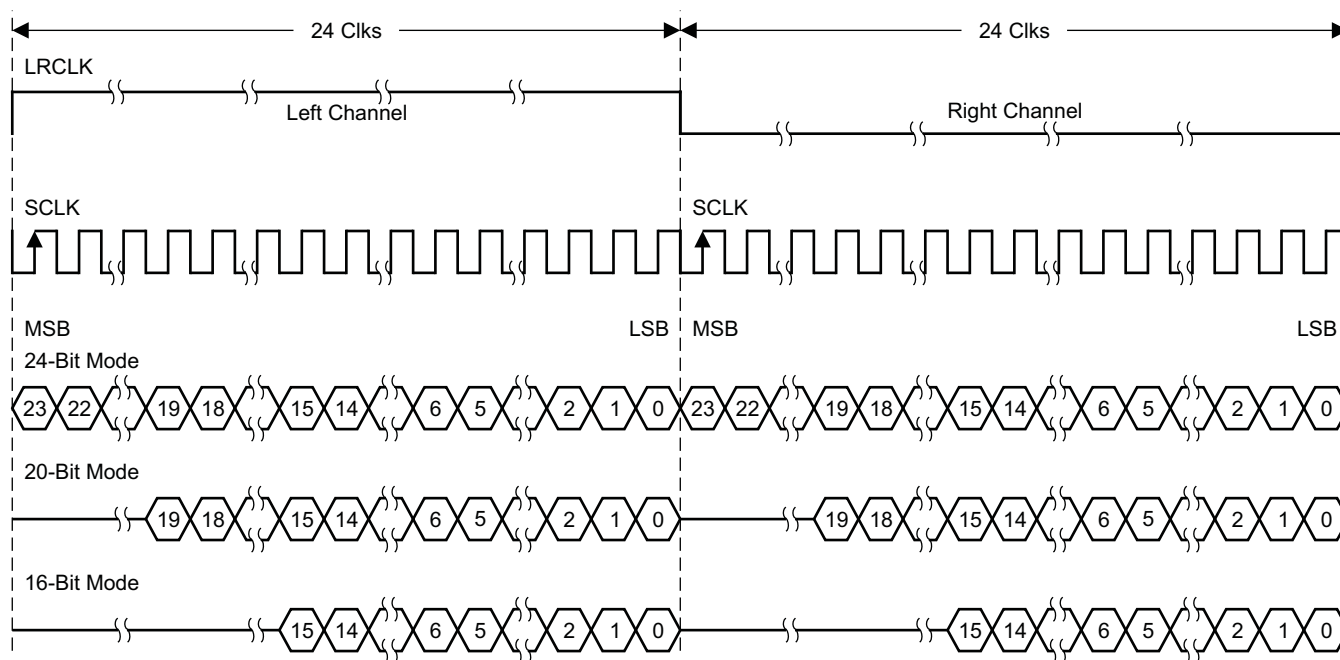
2-Channel Right-Justified (Sony Format) Stereo Input



T0034-03

**Figure 24. Right Justified 64- $f_s$  Format**

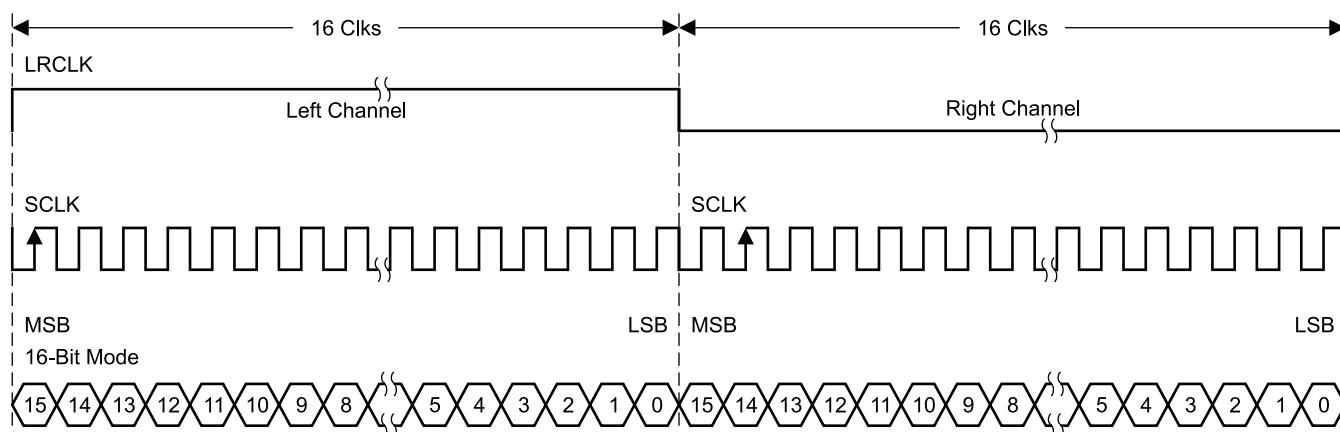
## 2-Channel Right-Justified Stereo Input (24-Bit Transfer Word Size)



T0092-03

Figure 25. Right Justified 48-f<sub>s</sub> Format

## 2-Channel Right-Justified (Sony Format) Stereo Input



T0266-03

Figure 26. Right Justified 32-f<sub>s</sub> Format

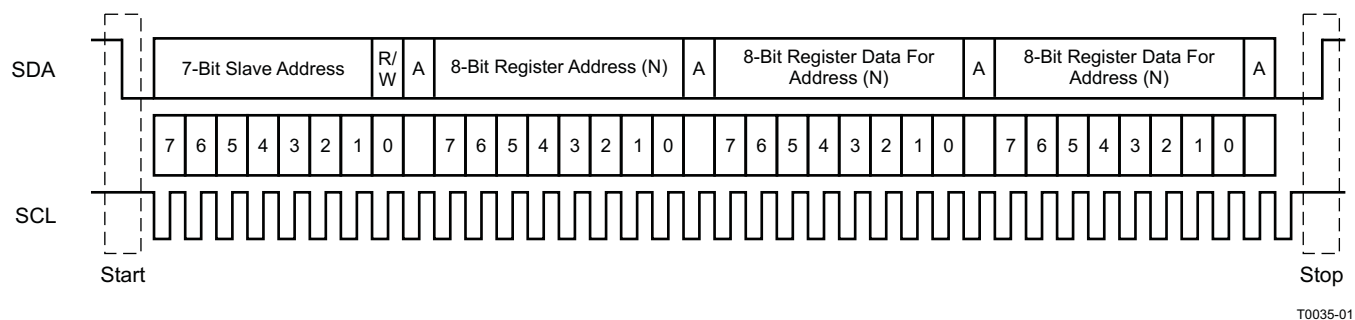
## I<sup>2</sup>C SERIAL CONTROL INTERFACE

The TAS5710 DAP has a bidirectional I<sup>2</sup>C interface that compatible with the I<sup>2</sup>C (Inter IC) bus protocol and supports both 100-kHz and 400-kHz data transfer rates for single and multiple byte write and read operations. This is a slave only device that does not support a multimaster bus environment or wait state insertion. The control interface is used to program the registers of the device and to read device status.

The DAP supports the standard-mode I<sup>2</sup>C bus operation (100 kHz maximum) and the fast I<sup>2</sup>C bus operation (400 kHz maximum). The DAP performs all I<sup>2</sup>C operations without I<sup>2</sup>C wait cycles.

### General I<sup>2</sup>C Operation

The I<sup>2</sup>C bus employs two signals; SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is high to indicate a start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 27. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The TAS5710 holds SDA low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the high level for the bus.



**Figure 27. Typical I<sup>2</sup>C Sequence**

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 27.

The 7-bit address for TAS5710 is 0011 011 (0x36).

TAS5710 address can be changed from 0x36 to 0x38 by writing 0x38 to device address register 0xF9.

### Single- and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte read/write operations for subaddresses 0x00 to 0x1F. However, for the subaddresses 0x20 to 0xFF, the serial control interface supports only multiple-byte read/write operations (in multiples of 4 bytes).

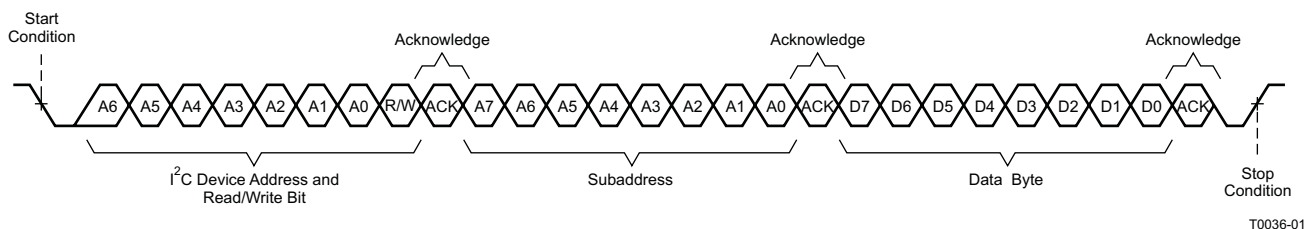
During multiple-byte read operations, the DAP responds with data, a byte at a time, starting at the subaddress assigned, as long as the master device continues to respond with acknowledges. If a particular subaddress does not contain 32 bits, the unused bits are read as logic 0.

During multiple-byte write operations, the DAP compares the number of bytes transmitted to the number of bytes that are required for each specific subaddress. For example, if a write command is received for a biquad subaddress, the DAP expects to receive five 32-bit words. If fewer than five 32-bit data words have been received when a stop command (or another start command) is received, the data received is discarded.

Supplying a subaddress for each subaddress transaction is referred to as random I<sup>2</sup>C addressing. The TAS5710 also supports sequential I<sup>2</sup>C addressing. For write transactions, if a subaddress is issued followed by data for that subaddress and the 15 subaddresses that follow, a sequential I<sup>2</sup>C write transaction has taken place, and the data for all 16 subaddresses is successfully received by the TAS5710. For I<sup>2</sup>C sequential write transactions, the subaddress then serves as the start address, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many subaddresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last subaddress is discarded. However, all other data written is accepted; only the incomplete data is discarded.

### Single-Byte Write

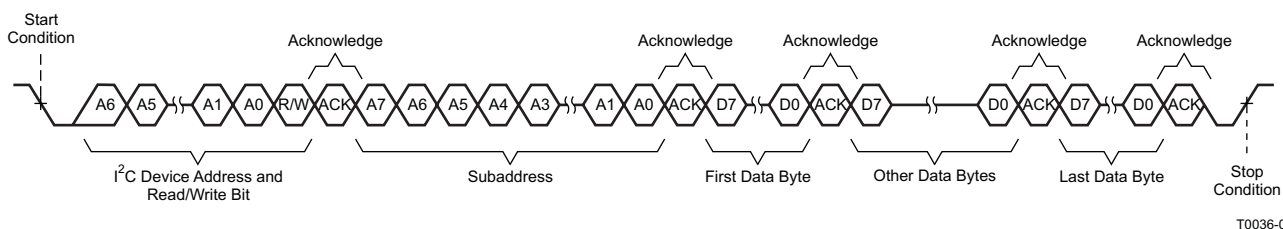
As shown in Figure 28, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I<sup>2</sup>C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit will be a 0. After receiving the correct I<sup>2</sup>C device address and the read/write bit, the DAP responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the TAS5710 internal memory address being accessed. After receiving the address byte, the TAS5710 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5710 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.



**Figure 28. Single-Byte Write Transfer**

### Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the DAP as shown in Figure 29. After receiving each data byte, the TAS5710 responds with an acknowledge bit.



**Figure 29. Multiple-Byte Write Transfer**

## Single-Byte Read

As shown in Figure 30, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I<sup>2</sup>C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit becomes a 0. After receiving the TAS5710 address and the read/write bit, TAS5710 responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the TAS5710 address and the read/write bit again. This time the read/write bit becomes a 1, indicating a read transfer. After receiving the address and the read/write bit, the TAS5710 again responds with an acknowledge bit. Next, the TAS5710 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not acknowledge followed by a stop condition to complete the single byte data read transfer.

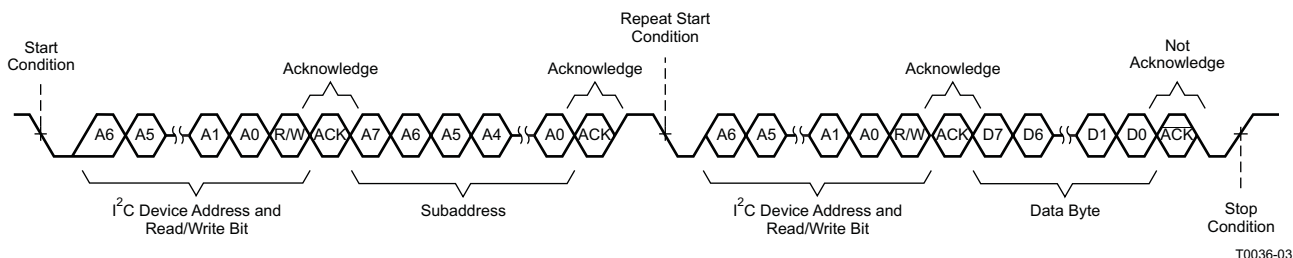


Figure 30. Single-Byte Read Transfer

## Multiple-Byte Read

A multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the TAS5710 to the master device as shown in Figure 31. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

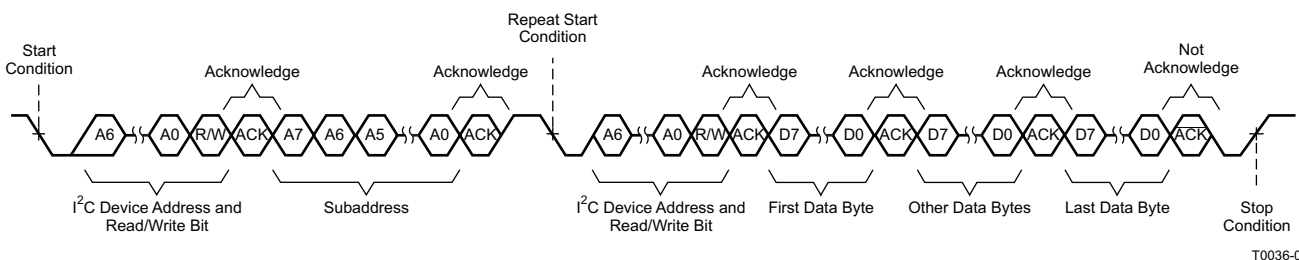
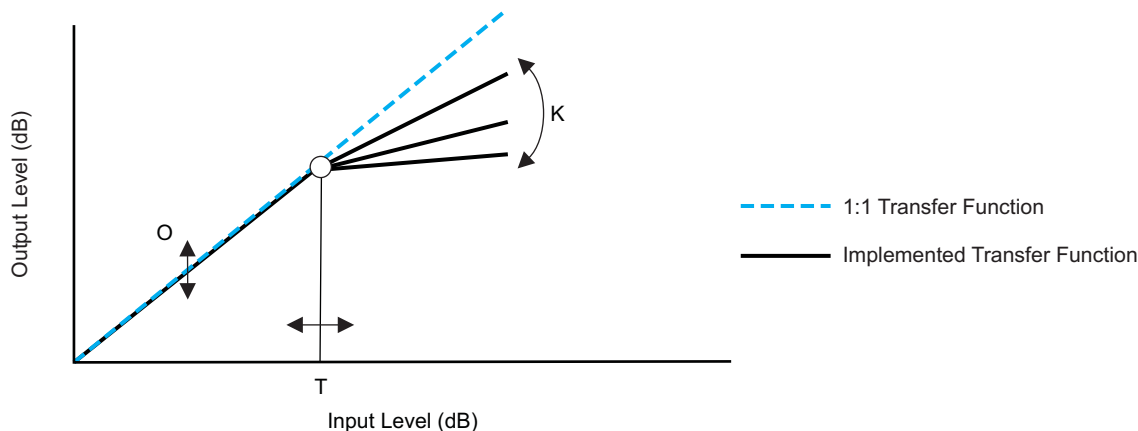


Figure 31. Multiple Byte Read Transfer

## Dynamic Range Control (DRC)

The DRC scheme has a single threshold, offset, and slope (all programmable). There is one ganged DRC for the left/right channels and one DRC for the subwoofer channel.

The DRC input/output diagram is shown in Figure 32.

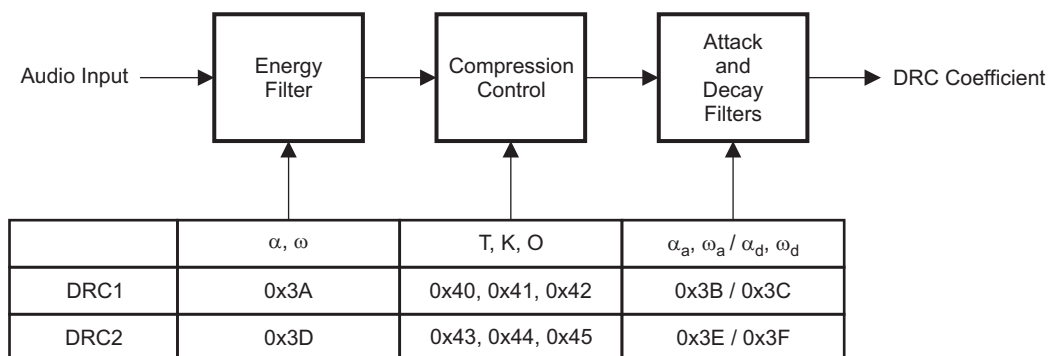


M0091-02

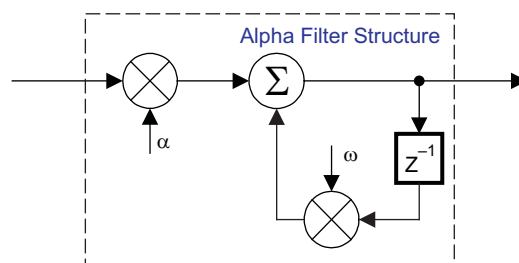
Professional-quality dynamic range compression automatically adjusts volume to flatten volume level.

- One DRC for left/right and one DRC for subwoofer
- Each DRC has adjustable threshold, offset, and compression levels
- Programmable energy, attack, and decay time constants
- *Transparent compression*: compressors can attack fast enough to avoid apparent clipping before engaging, and decay times can be set slow enough to avoid pumping.

**Figure 32. Dynamic Range Control**



NOTE:  
 $\omega = 1 - \alpha$

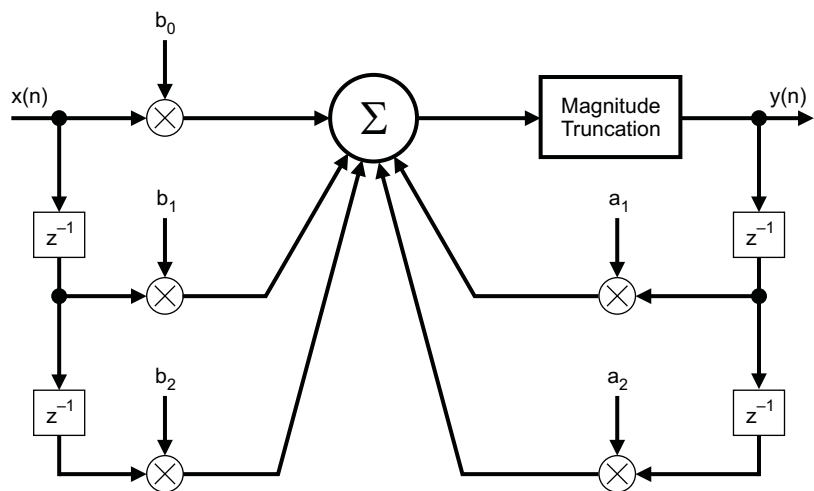


B0265-01

**Figure 33. DRC Structure**

## BiQuad Structure

All biquads use a 2nd order IIR filter structure as shown below. Each biquad has 3 coefficients on the direct path ( $b_0, b_1, b_2$ ) and 2 coefficients on feedback path ( $a_1$  and  $a_2$ ) as shown in the diagram.



M0012-02

Figure 34. BiQuad Filter

## BANK SWITCHING

The TAS5710 uses an approach called *bank switching* together with automatic sample-rate detection. All processing features that must be changed for different sample rates are stored internally in the TAS5710. The TAS5710 has three full banks storing information, one for 32-48 kHz, one for 16-24 kHz, and one for all other data rates. Combined with the clock-rate autodetection feature, bank switching allows the TAS5710 to detect automatically a change in the input sample rate and switch to the appropriate bank without any MCU intervention.

An external controller updates the three banks (see the I<sup>2</sup>C register mapping table for bankable locations) during the initialization sequence.

If the autobank switch is enabled (register 0x50, bits 2:0), then the TAS5710 automatically swaps the coefficients for subsequent sample rate changes, avoiding the need for any external controller intervention for a sample rate change.

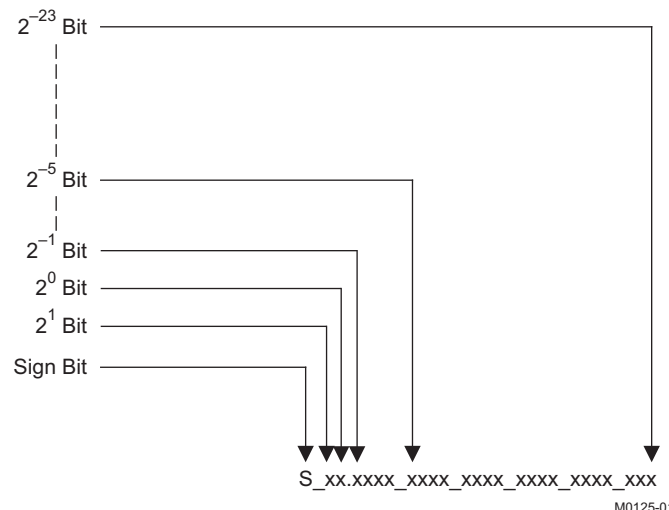
By default, bits 2:0 have the value 000; that means the bank switch is disabled. In that state, any update to locations 0x29–0x3F and 0x58–0x5F go into the DAP. A write to register 0x50 with bits 2:0 being 001, 010, or 011 brings the system into the coefficient-bank-update state *update bank1*, *update bank2*, or *update bank3*, respectively. Any subsequent write to locations 0x29–0x3F and 0x58–0x5F updates the coefficient banks stored outside the DAP. After updating all the three banks, the system controller should issue a write to register 0x50 with bits 2:0 being 100; this changes the system state to automatic bank update. In automatic bank update, the TAS5710 automatically swaps banks based on the sample rate.

**Command sequences for initialization can be summarized as follows:**

1. **Enable factory trim for internal oscillator:** Write to register 0x1B with a value 0x00.
2. **Update coefficients:** Coefficients can be loaded into DAP RAM using the manual bank mode.  
OR  
**Use automatic bank mode.**
  - a. Enable bank-1 mode: Write to register 0x50 with 0x01. Load the 32 kHz coefficients.
  - b. Enable bank-2 mode: Write to register 0x50 with 0x02. Load the 48 kHz coefficients.
  - c. Enable bank-3 mode: Write to register 0x50 with 0x03. Load the other coefficients.
  - d. Enable automatic bank switching by writing to register 0x50 with 0x04.
3. **Bring the system out of all-channel shutdown:** Write 0 to bit 6 of register 0x05.
4. **Issue master volume:** Write to register 0x07 with the volume value (0 db = 0x30).

## 26-Bit 3.23 Number Format

All mixer gain coefficients are 26-bit coefficients using a 3.23 number format. Numbers formatted as 3.23 numbers means that there are 3 bits to the left of the decimal point and 23 bits to the right of the decimal point. This is shown in [Figure 35](#).



**Figure 35. 3.23 Format**

The decimal value of a 3.23 format number can be found by following the weighting shown in Figure 35. If the most significant bit is logic 0, the number is a positive number, and the weighting shown yields the correct number. If the most significant bit is a logic 1, then the number is a negative number. In this case every bit must be inverted, a 1 added to the result, and then the weighting shown in Figure 36 applied to obtain the magnitude of the negative number.

$$\begin{array}{c}
 2^1 \text{ Bit} \quad 2^0 \text{ Bit} \quad 2^{-1} \text{ Bit} \quad 2^{-4} \text{ Bit} \quad 2^{-23} \text{ Bit} \\
 \downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow \\
 (1 \text{ or } 0) \times 2^1 + (1 \text{ or } 0) \times 2^0 + (1 \text{ or } 0) \times 2^{-1} + \dots (1 \text{ or } 0) \times 2^{-4} + \dots (1 \text{ or } 0) \times 2^{-23}
 \end{array}$$

M0126-01

Figure 36. Conversion Weighting Factors—3.23 Format to Floating Point

Gain coefficients, entered via the I2C bus, must be entered as 32-bit binary numbers. The format of the 32-bit number (4-byte or 8-digit hexadecimal number) is shown in Figure 37

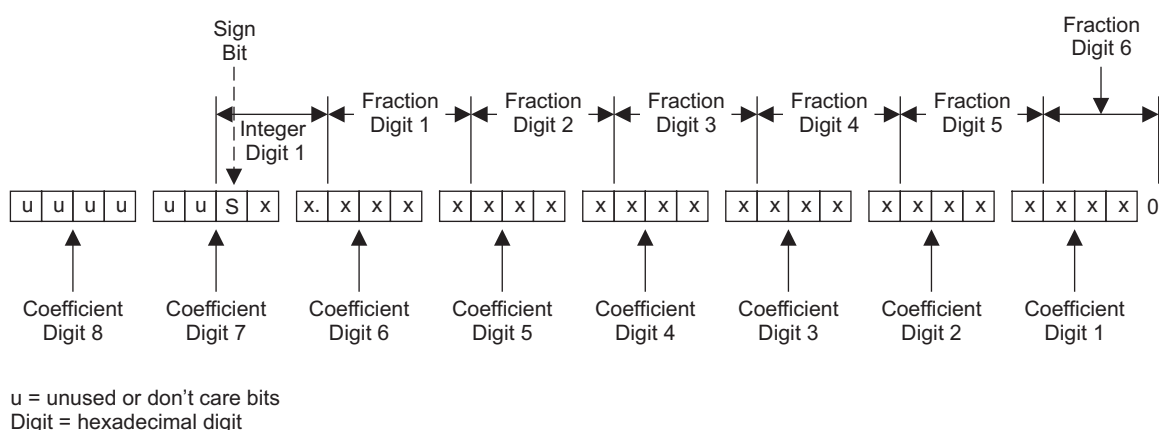


Figure 37. Alignment of 3.23 Coefficient in 32-Bit I2C Word

#### Sample calculation for 3.23 format

| db | Linear            | Decimal                | Hex (3.23 Format)          |
|----|-------------------|------------------------|----------------------------|
| 0  | 1                 | 8388608                | 00800000                   |
| 5  | 1.7782794         | 14917288               | 00E39EA8                   |
| -5 | 0.5623413         | 4717260                | 0047FACC                   |
| X  | $L = 10^{(X/20)}$ | $D = 8388608 \times L$ | $H = \text{dec2hex}(D, 8)$ |

#### Sample calculation for 9.17 format

| db | Linear            | Decimal               | Hex (9.17 Format)          |
|----|-------------------|-----------------------|----------------------------|
| 0  | 1                 | 131072                | 00020000                   |
| 5  | 1.7782794         | 233082.6              | 00038E7A                   |
| -5 | 0.5623413         | 73707.2               | 00011FEB                   |
| X  | $L = 10^{(X/20)}$ | $D = 131072 \times L$ | $H = \text{dec2hex}(D, 8)$ |

## APPLICATION INFORMATION

### Calculation of Output Signal Level of TAS5710 Feedback Power Stage (Gain Is independent of PVCC)

The gain of the TAS5710 is the total digital gain of the controller multiplied by the gain of the power stage.

For a half-bridge channel of the TAS5710 power stage, the gain is simply:

$$\text{Power stage gain} = 13 \times V_{\text{RMS}} / \text{Modulation Level}$$

Modulation level = fraction of full-scale modulation of the PWM signal at the input of the power stage.

$$V_{\text{RMS}}(\text{SE}) = \text{Audio voltage level at the output of the power stage} = 13 \times \text{Modulation Level}$$

$$V_{\text{RMS}}(\text{BTL}) = 2 \times \text{Audio voltage level at the output of the power stage} = 26 \times \text{Modulation Level}$$

For the TAS5710 controller, the gain is the programmed digital gain multiplied by a scaling factor, called the *maximum modulation level*. The maximum modulation level is derived from the modulation limit programmed in the controller, which limits duty cycle to a set number of percent above 0% and below 100%. Setting the modulation limit to 97.7% (default) limits the duty cycle between 2.3% and 97.7%.

$$\text{Controller gain} = \text{digital gain} \times \text{maximum modulation level} \times (\text{modulation level/digital FFS})$$

$$\text{Digital FFS} = \text{digital input fraction of full scale}$$

$$\text{Modulation limit} = 97.7\%$$

$$\text{Maximum modulation level} = 2 \times \text{modulation limit} - 1 = 0.954$$

The output signal level of the TAS5710 can now be calculated:

$$V_{\text{RMS}}(\text{SE}) = \text{digital FFS} \times \text{digital gain} \times \text{maximum modulation level} \times 13$$

$$V_{\text{RMS}}(\text{BTL}) = 2 \times V_{\text{RMS}}(\text{SE})$$

With the modulation limit set at the default level of 97.7%, this becomes:

$$V_{\text{RMS}}(\text{BTL}) = \text{digital FFS} \times \text{digital gain} \times 24.8$$

Example: Input = -20 dBFS; volume = 0 dB; biquads = ALL PASS; modulation index = 97.7%; mode = BTL

$$\text{Output } V_{\text{RMS}}(\text{BTL}) = 24.8 \times 0.1 \times 1 = 2.48 \text{ V.}$$

### Figure 38. Recommended Command Sequence

| PARAMETER               | DESCRIPTION                                                                                                                                                                     | MIN                               | TYP | MAX | UNIT    |
|-------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|-----|-----|---------|
| $t_{VDDH-DL}$           | Time digital inputs must remain low after AVDD/DVDD goes above 3V                                                                                                               | 0                                 |     |     | $\mu$ s |
| $t_{DL-VDDH}$           | Time digital inputs must be low before AVDD/DVDD goes below 3V                                                                                                                  | 0                                 |     |     | $\mu$ s |
| $t_{VDDH-PVCCL}$        | Time PVCC/AVCC remains below 7.5V after AVDD/DVDD goes above 3V                                                                                                                 | 100                               |     |     | $\mu$ s |
| $t_{PVCCL-VDDH}$        | Time PVCC/AVCC must be below 7.5V before AVDD/DVDD goes below 3V                                                                                                                | 0                                 |     |     | $\mu$ s |
| $t_{PVCCH-I2C}$         | Time PVCC/AVCC must be above 10V before I2C commands may address device                                                                                                         | 10                                |     |     | $\mu$ s |
| $t_{RL-PVCCH}$          | Time PVCC/AVCC must remain above 10V after $\overline{\text{RESET}}$ goes low                                                                                                   | 2                                 |     |     | $\mu$ s |
| $t_{RH-I2C}$            | Time $\overline{\text{RESET}}$ must be high before I2C commands may address device                                                                                              | 13.5                              |     |     | ms      |
| $t_{DV-RH}$             | Time digital inputs must be valid (driven as recommended) before $\overline{\text{RESET}}$ goes high                                                                            | 100                               |     |     | $\mu$ s |
| $t_{RL-DV}$             | Time digital inputs must remain valid (driven as recommended) after $\overline{\text{RESET}}$ goes low                                                                          | 2                                 |     |     | $\mu$ s |
| $t_{\text{autodetect}}$ | Autodetect completion wait time (given stable and valid clocks) before issuing further commands                                                                                 | 50                                |     |     | ms      |
| $t_{\text{exitSD}}$     | Exit shutdown wait time before issuing further commands to device ( $t_{\text{start}}$ given by register 0x1A)                                                                  | $1+1.3 \times t_{\text{start}}$   |     |     | ms      |
| $t_{\text{enterSD}}$    | Enter shutdown wait time before issuing further commands to device ( $t_{\text{stop}}$ given by register 0x1A)                                                                  | $1+1.3 \times t_{\text{stop}}$    |     |     | ms      |
| $t_{\text{POR}}$        | Power-on-reset wait time after 1st trim following AVDD/DVDD power-up ( $t_{\text{start}}$ given by register 0x1A) (does not apply to trim commands following subsequent resets) | $240+1.3 \times t_{\text{start}}$ |     |     | ms      |

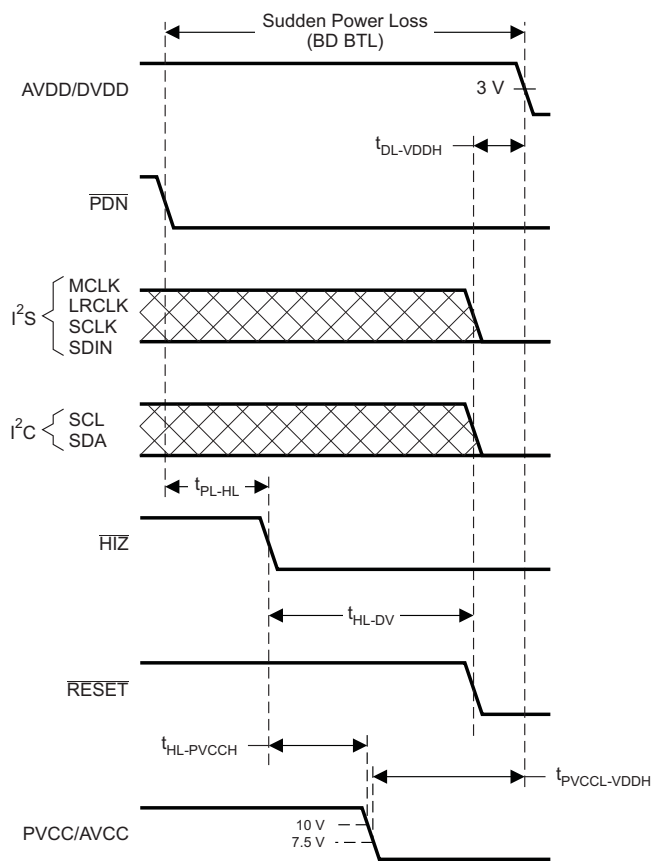


Figure 39. BD BTL Power Loss Sequence

T0420-02

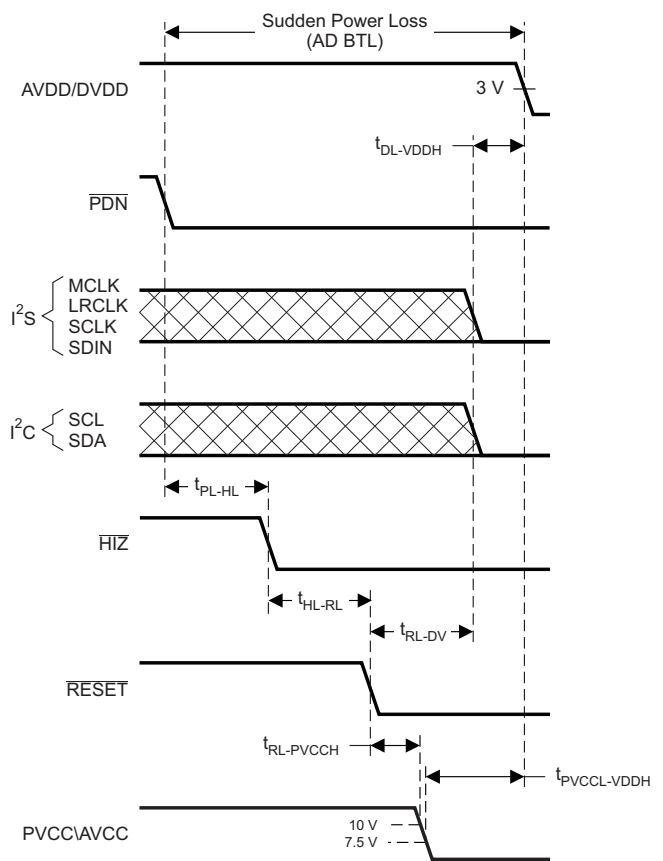


Figure 40. AD BTL Power Loss Sequence

T0420-03

| PARAMETER         | DESCRIPTION                                                                                     | MIN | TYP | MAX | UNIT    |
|-------------------|-------------------------------------------------------------------------------------------------|-----|-----|-----|---------|
| $t_{PL-HL}$       | Time $\overline{HIZ}$ must remain high after $\overline{PDN}$ goes low                          | 2   |     |     | ms      |
| $t_{HL-RL}$       | Time $\overline{RESET}$ must remain high after $\overline{HIZ}$ goes low                        | 4   |     |     | $\mu$ s |
| $t_{HL-DV}$       | Time digital inputs must remain valid (driven as recommended) after $\overline{HIZ}$ goes low   | 4   |     |     | $\mu$ s |
| $t_{RL-DV}$       | Time digital inputs must remain valid (driven as recommended) after $\overline{RESET}$ goes low | 2   |     |     | $\mu$ s |
| $t_{DL-VDDH}$     | Time digital inputs must be low before AVDD/DVDD goes below 3V                                  | 0   |     |     | $\mu$ s |
| $t_{HL-PVCC}$     | Time PVCC/AVCC must remain above 10V after $\overline{HIZ}$ goes low                            | 4   |     |     | $\mu$ s |
| $t_{RL-PVCC}$     | Time PVCC/AVCC must remain above 10V after $\overline{RESET}$ goes low                          | 2   |     |     | $\mu$ s |
| $t_{PVCC-L-VDDH}$ | Time PVCC/AVCC must be below 7.5V before AVDD/DVDD goes below 3V                                | 0   |     |     | $\mu$ s |

## Recommended Command Sequences

The DAP has two groups of commands. One set is for configuration and is intended for use only during initialization. The other set has built-in click and pop protection and may be used during normal operation while audio is streaming. The following supported command sequences illustrate how to initialize, operate, and shutdown the device.

### Initialization Sequence

Use the following sequence to power-up and initialize the device:

1. Hold all digital inputs low and ramp up AVDD/DVDD to at least 3V.
2. Initialize digital inputs and PVCC/AVCC supply as follows:
  - Drive  $\overline{RESET}=0$ ,  $\overline{PDN}=1$ ,  $\overline{HIZ}=1$ , and other digital inputs to their desired state, observing absolute maximum ratings relative to AVDD/DVDD. Provide stable and valid I2S clocks (MCLK, LRCLK, and SCLK). Wait at least 100 $\mu$ s, drive  $\overline{RESET}=1$ , and wait at least another 13.5ms.
  - Ramp up PVCC/AVCC to at least 10V while ensuring it remains below 7.5V for at least 100 $\mu$ s after AVDD/DVDD reaches 3V. Then wait at least another 10 $\mu$ s.
3. Trim oscillator (write 0x00 to register 0x1B) and wait at least 50ms.
4. Configure the DAP via I2C (see Users's Guide for typical values):
  - Biquads (0x29-36)
  - DRC parameters (0x3A-3C, 0x40-42, and 0x46)
  - Bank select (0x50)
5. Configure remaining registers
6. Exit shutdown (sequence defined below).

### Normal Operation

The following are the only events supported during normal operation:

- (a) Writes to master/channel volume registers
- (b) Writes to soft mute register
- (c) Enter and exit shutdown (sequence defined below)
- (d) Clock errors and rate changes

**Note:** Events (c) and (d) are not supported for  $240\text{ms} + 1.3 \times t_{\text{start}}$  after trim following AVDD/DVDD powerup ramp (where  $t_{\text{start}}$  is specified by register 0x1A).

## Shutdown Sequence

Enter:

1. Ensure I2S clocks have been stable and valid for at least 50ms.
2. Write 0x40 to register 0x05.
3. Wait at least  $1\text{ms} + 1.3 \times t_{\text{stop}}$  (where  $t_{\text{stop}}$  is specified by register 0x1A).
4. Once in shutdown, stable clocks are not required while device remains idle.
5. If desired, reconfigure by ensuring that clocks have been stable and valid for at least 50ms before returning to step 4 of initialization sequence.

Exit:

1. Ensure I2S clocks have been stable and valid for at least 50ms.
2. Write 0x00 to register 0x05 (exit shutdown command may not be serviced for as much as 240ms after trim following AVDD/DVDD powerup ramp).
3. Wait at least  $1\text{ms} + 1.3 \times t_{\text{start}}$  (where  $t_{\text{start}}$  is specified by register 0x1A).
4. Proceed with normal operation.

## Controlled Powerdown Sequence

Use the following sequence to powerdown the device and its supplies when time permits a controlled shutdown:

1. Enter shutdown (sequence defined above).
2. Assert  $\overline{\text{RESET}}=0$ .
3. Drive digital inputs low and ramp down PVCC/AVCC supply as follows:
  - Drive all digital inputs low after  $\overline{\text{RESET}}$  has been low for at least 2 $\mu\text{s}$ .
  - Ramp down PVCC/AVCC while ensuring that it remains above 10V until  $\overline{\text{RESET}}$  has been low for at least 2 $\mu\text{s}$ .
4. Ramp down AVDD/DVDD while ensuring that it remains above 3V until PVCC/AVCC is below 7.5V and observing absolute maximum ratings for digital inputs.

## Power Loss Sequence (BD BTL)

Use the following sequence to powerdown a BD BTL device and its supplies in case of sudden power loss when time does not permit a controlled shutdown:

1. Assert  $\overline{\text{PDN}} = 0$  and wait at least 2ms.
2. Assert  $\overline{\text{HIZ}} = 0$ .
3. Drive digital inputs low and ramp down PVCC/AVCC supply as follows:
  - Drive all digital inputs low after  $\overline{\text{HIZ}}$  has been low for at least 4 $\mu\text{s}$ .
  - Ramp down PVCC/AVCC while ensuring that it remains above 10V until  $\overline{\text{HIZ}}$  has been low for at least 4 $\mu\text{s}$ .
4. Ramp down AVDD/DVDD while ensuring that it remains above 3V until PVCC/AVCC is below 7.5V and observing absolute maximum ratings for digital inputs.

## Power Loss Sequence (AD BTL)

Use the following sequence to powerdown an AD BTL device and its supplies in case of sudden power loss when time does not permit a controlled shutdown:

1. Assert  $\overline{\text{PDN}} = 0$  and wait at least 2ms then assert  $\overline{\text{HIZ}} = 0$  and wait at least 4 $\mu\text{s}$ .
2. Assert  $\overline{\text{RESET}} = 0$ .
3. Drive digital inputs low and ramp down PVCC/AVCC supply as follows:
  - Drive all digital inputs low after  $\overline{\text{RESET}}$  has been low for at least 2 $\mu\text{s}$ .
  - Ramp down PVCC/AVCC while ensuring that it remains above 10V until  $\overline{\text{RESET}}$  has been low for at least 2 $\mu\text{s}$ .
4. Ramp down AVDD/DVDD while ensuring that it remains above 3V until PVCC/AVCC is below 7.5V and observing absolute maximum ratings for digital inputs.

**Table 2. Serial Control Interface Register Summary<sup>(1)</sup>**

| SUBADDRESS  | REGISTER NAME                  | NO. OF BYTES | CONTENTS                                | INITIALIZATION VALUE |
|-------------|--------------------------------|--------------|-----------------------------------------|----------------------|
|             |                                |              | A u indicates unused bits.              |                      |
| 0x00        | Clock control register         | 1            | Description shown in subsequent section | 0x6C                 |
| 0x01        | Device ID register             | 1            | Description shown in subsequent section | 0x70                 |
| 0x02        | Error status register          | 1            | Description shown in subsequent section | 0x00                 |
| 0x03        | System control register 1      | 1            | Description shown in subsequent section | 0xA0                 |
| 0x04        | Serial data interface register | 1            | Description shown in subsequent section | 0x05                 |
| 0x05        | System control register 2      | 1            | Description shown in subsequent section | 0x40                 |
| 0x06        | Soft mute register             | 1            | Description shown in subsequent section | 0x00                 |
| 0x07        | Master volume                  | 1            | Description shown in subsequent section | 0xFF (mute)          |
| 0x08        | Channel 1 vol                  | 1            | Description shown in subsequent section | 0x30 (0 dB)          |
| 0x09        | Channel 2 vol                  | 1            | Description shown in subsequent section | 0x30 (0 dB)          |
| 0x0A        | Fine master volume             | 1            | Description shown in subsequent section | 0x00 (0 dB)          |
| 0x0B - 0x0D |                                | 1            | Reserved <sup>(2)</sup>                 |                      |
| 0x0E        | Volume configuration register  | 1            | Description shown in subsequent section | 0x91                 |
| 0x0F        |                                | 1            | Reserved <sup>(2)</sup>                 |                      |
| 0x10        | Modulation limit register      | 1            | Description shown in subsequent section | 0x02                 |
| 0x11        | IC delay channel 1             | 1            | Description shown in subsequent section | 0xAC                 |
| 0x12        | IC delay channel 2             | 1            | Description shown in subsequent section | 0x54                 |
| 0x13        | IC delay channel 3             | 1            | Description shown in subsequent section | 0xAC                 |
| 0x14        | IC delay channel 4             | 1            | Description shown in subsequent section | 0x54                 |
| 0x15-0x19   |                                | 1            | Reserved <sup>(2)</sup>                 |                      |
| 0x1A        | Start/stop period register     | 1            |                                         | 0x0F                 |
| 0x1B        | Oscillator trim register       | 1            |                                         | 0x82                 |
| 0x1C        | BKND_ERR register              | 1            |                                         | 0x02                 |
| 0x1D–0x1F   |                                | 1            | Reserved <sup>(2)</sup>                 |                      |
| 0x20        | Input MUX register             | 4            | Description shown in subsequent section | 0x0001 7772          |
| 0x21        | Ch 4 source select register    | 4            | Description shown in subsequent section | 0x0000 4303          |
| 0x22 -0x24  |                                | 4            | Reserved <sup>(2)</sup>                 |                      |
| 0x25        | PWM MUX register               | 4            | Description shown in subsequent section | 0x0102 1345          |
| 0x26-0x28   |                                | 4            | Reserved <sup>(2)</sup>                 |                      |

(1) "ae" stands for  $\infty$  of energy filter, "aa" stands for  $\infty$  of attack filter and "ad" stands for  $\infty$  of decay filter and  $1 - \infty = \omega$ .

(2) Reserved registers should not be accessed.

**Table 2. Serial Control Interface Register Summary (continued)**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS           | INITIALIZATION VALUE |
|------------|---------------|--------------|--------------------|----------------------|
| 0x29       | ch1_bq[0]     | 20           | u[31:26], b0[25:0] | 0x0080 0000          |
|            |               |              | u[31:26], b1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], b2[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a2[25:0] | 0x0000 0000          |
| 0x2A       | ch1_bq[1]     | 20           | u[31:26], b0[25:0] | 0x0080 0000          |
|            |               |              | u[31:26], b1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], b2[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a2[25:0] | 0x0000 0000          |
| 0x2B       | ch1_bq[2]     | 20           | u[31:26], b0[25:0] | 0x0080 0000          |
|            |               |              | u[31:26], b1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], b2[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a2[25:0] | 0x0000 0000          |
| 0x2C       | ch1_bq[3]     | 20           | u[31:26], b0[25:0] | 0x0080 0000          |
|            |               |              | u[31:26], b1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], b2[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a2[25:0] | 0x0000 0000          |
| 0x2D       | ch1_bq[4]     | 20           | u[31:26], b0[25:0] | 0x0080 0000          |
|            |               |              | u[31:26], b1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], b2[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a2[25:0] | 0x0000 0000          |
| 0x2E       | ch1_bq[5]     | 20           | u[31:26], b0[25:0] | 0x0080 0000          |
|            |               |              | u[31:26], b1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], b2[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a2[25:0] | 0x0000 0000          |
| 0x2F       | ch1_bq[6]     | 20           | u[31:26], b0[25:0] | 0x0080 0000          |
|            |               |              | u[31:26], b1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], b2[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a2[25:0] | 0x0000 0000          |
| 0x30       | ch2_bq[0]     | 20           | u[31:26], b0[25:0] | 0x0080 0000          |
|            |               |              | u[31:26], b1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], b2[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a2[25:0] | 0x0000 0000          |
| 0x31       | ch2_bq[1]     | 20           | u[31:26], b0[25:0] | 0x0080 0000          |
|            |               |              | u[31:26], b1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], b2[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a1[25:0] | 0x0000 0000          |
|            |               |              | u[31:26], a2[25:0] | 0x0000 0000          |

**Table 2. Serial Control Interface Register Summary (continued)**

| SUBADDRESS  | REGISTER NAME          | NO. OF BYTES | CONTENTS                               | INITIALIZATION VALUE |
|-------------|------------------------|--------------|----------------------------------------|----------------------|
| 0x32        | ch2_bq[2]              | 20           | u[31:26], b0[25:0]                     | 0x0080 0000          |
|             |                        |              | u[31:26], b1[25:0]                     | 0x0000 0000          |
|             |                        |              | u[31:26], b2[25:0]                     | 0x0000 0000          |
|             |                        |              | u[31:26], a1[25:0]                     | 0x0000 0000          |
|             |                        |              | u[31:26], a2[25:0]                     | 0x0000 0000          |
| 0x33        | ch2_bq[3]              | 20           | u[31:26], b0[25:0]                     | 0x0080 0000          |
|             |                        |              | u[31:26], b1[25:0]                     | 0x0000 0000          |
|             |                        |              | u[31:26], b2[25:0]                     | 0x0000 0000          |
|             |                        |              | u[31:26], a1[25:0]                     | 0x0000 0000          |
|             |                        |              | u[31:26], a2[25:0]                     | 0x0000 0000          |
| 0x34        | ch2_bq[4]              | 20           | u[31:26], b0[25:0]                     | 0x0080 0000          |
|             |                        |              | u[31:26], b1[25:0]                     | 0x0000 0000          |
|             |                        |              | u[31:26], b2[25:0]                     | 0x0000 0000          |
|             |                        |              | u[31:26], a1[25:0]                     | 0x0000 0000          |
|             |                        |              | u[31:26], a2[25:0]                     | 0x0000 0000          |
| 0x35        | ch2_bq[5]              | 20           | u[31:26], b0[25:0]                     | 0x0080 0000          |
|             |                        |              | u[31:26], b1[25:0]                     | 0x0000 0000          |
|             |                        |              | u[31:26], b2[25:0]                     | 0x0000 0000          |
|             |                        |              | u[31:26], a1[25:0]                     | 0x0000 0000          |
|             |                        |              | u[31:26], a2[25:0]                     | 0x0000 0000          |
| 0x36        | ch2_bq[6]              | 20           | u[31:26], b0[25:0]                     | 0x0080 0000          |
|             |                        |              | u[31:26], b1[25:0]                     | 0x0000 0000          |
|             |                        |              | u[31:26], b2[25:0]                     | 0x0000 0000          |
|             |                        |              | u[31:26], a1[25:0]                     | 0x0000 0000          |
|             |                        |              | u[31:26], a2[25:0]                     | 0x0000 0000          |
| 0x37 - 0x39 |                        | 4            | Reserved <sup>(3)</sup>                |                      |
| 0x3A        | DRC1 ae <sup>(4)</sup> | 8            | u[31:26], ae[25:0]                     | 0x0080 0000          |
|             | DRC1 (1 – ae)          |              | u[31:26], (1 – ae)[25:0]               | 0x0000 0000          |
| 0x3B        | DRC1 aa                | 8            | u[31:26], aa[25:0]                     | 0x0080 0000          |
|             | DRC1 (1 – aa)          |              | u[31:26], (1 – aa)[25:0]               | 0x0000 0000          |
| 0x3C        | DRC1 ad                | 8            | u[31:26], ad[25:0]                     | 0x0080 0000          |
|             | DRC1 (1 – ad)          |              | u[31:26], (1 – ad)[25:0]               | 0x0000 0000          |
| 0x3D        | DRC2 ae                | 8            | u[31:26], ae[25:0]                     | 0x0080 0000          |
|             | DRC 2 (1 – ae)         |              | u[31:26], (1 – ae)[25:0]               | 0x0000 0000          |
| 0x3E        | DRC2 aa                | 8            | u[31:26], aa[25:0]                     | 0x0080 0000          |
|             | DRC2 (1 – aa)          |              | u[31:26], (1 – aa)[25:0]               | 0x0000 0000          |
| 0x3F        | DRC2 ad                | 8            | u[31:26], ad[25:0]                     | 0x0080 0000          |
|             | DRC2 (1 – ad)          |              | u[31:26], (1 – ad)[25:0]               | 0x0000 0000          |
| 0x40        | DRC1-T                 | 4            | T1[31:0] (9.23 format)                 | 0xFDA2 1490          |
| 0x41        | DRC1-K                 | 4            | u[31:26], K1[25:0]                     | 0x0384 2109          |
| 0x42        | DRC1-O                 | 4            | u[31:26], O1[25:0]                     | 0x0008 4210          |
| 0x43        | DRC2-T                 | 4            | T2[31:0] (9.23 format)                 | 0xFDA2 1490          |
| 0x44        | DRC2-K                 | 4            | u[31:26], K2[25:0]                     | 0x0384 2109          |
| 0x45        | DRC2-O                 | 4            | u[31:26], O2[25:0]                     | 0x0008 4210          |
| 0x46        | DRC control            | 4            | Description show in subsequent section | 0x0000 0000          |

(3) Reserved registers should not be accessed.

(4) "ae" stands for  $\infty$  of energy filter, "aa" stands for  $\infty$  of attack filter and "ad" stands for  $\infty$  of decay filter and  $1 - \infty = \omega$ .

**Table 2. Serial Control Interface Register Summary (continued)**

| SUBADDRESS | REGISTER NAME         | NO. OF BYTES | CONTENTS                               | INITIALIZATION VALUE |
|------------|-----------------------|--------------|----------------------------------------|----------------------|
| 0x47–0x4F  |                       | 4            | Reserved <sup>(3)</sup>                |                      |
| 0x50       | Bank switch control   | 4            | Description show in subsequent section | 0x0F70 8000          |
| 0x51       | Ch 1 output mixer     | 8            | Ch 1 output mix1[1]                    | 0x0080 0000          |
|            |                       |              | Ch 1 output mix1[0]                    | 0x0000 0000          |
| 0x52       | Ch 2 output mixer     | 12           | Ch 2 output mix2[2]                    | 0x0080 0000          |
|            |                       |              | Ch 2 output mix2[1]                    | 0x0000 0000          |
|            |                       |              | Ch 2 output mix2[0]                    | 0x0000 0000          |
| 0x53       | Ch 1 input mixer      | 16           | Ch 1 input mixer[3]                    | 0x0080 0000          |
|            |                       |              | Ch 1 input mixer[2]                    | 0x0000 0000          |
|            |                       |              | Ch 1 input mixer[1]                    | 0x0000 0000          |
|            |                       |              | Ch 1 input mixer[0]                    | 0x0080 0000          |
| 0x54       | Ch 2 input mixer      | 16           | Ch 2 input mixer[3]                    | 0x0080 0000          |
|            |                       |              | Ch 2 input mixer[2]                    | 0x0000 0000          |
|            |                       |              | Ch 2 input mixer[1]                    | 0x0000 0000          |
|            |                       |              | Ch 2 input mixer[0]                    | 0x0080 0000          |
| 0x55       | Channel 3 input mixer | 12           | Channel 3 input mixer [2]              | 0x0080 0000          |
|            |                       |              | Channel 3 input mixer [1]              | 0x0000 0000          |
|            |                       |              | Channel 3 input mixer [0]              | 0x0000 0000          |
| 0x56       | Output post-scale     | 4            | u[31:26], post[25:0]                   | 0x0080 0000          |
| 0x57       | Output pre-scale      | 4            | u[31:26], pre[25:0] (9.17 format)      | 0x0002 0000          |
| 0x58       | ch1 BQ[7]             | 20           | u[31:26], b0[25:0]                     | 0x0080 0000          |
|            |                       |              | u[31:26], b1[25:0]                     | 0x0000 0000          |
|            |                       |              | u[31:26], b2[25:0]                     | 0x0000 0000          |
|            |                       |              | u[31:26], a1[25:0]                     | 0x0000 0000          |
|            |                       |              | u[31:26], a2[25:0]                     | 0x0000 0000          |
| 0x59       | ch1 BQ[8]             | 20           | u[31:26], b0[25:0]                     | 0x0080 0000          |
|            |                       |              | u[31:26], b1[25:0]                     | 0x0000 0000          |
|            |                       |              | u[31:26], b2[25:0]                     | 0x0000 0000          |
|            |                       |              | u[31:26], a1[25:0]                     | 0x0000 0000          |
|            |                       |              | u[31:26], a2[25:0]                     | 0x0000 0000          |
| 0x5A       | ch4 BQ[0]             | 20           | u[31:26], b0[25:0]                     | 0x0080 0000          |
|            |                       |              | u[31:26], b1[25:0]                     | 0x0000 0000          |
|            |                       |              | u[31:26], b2[25:0]                     | 0x0000 0000          |
|            |                       |              | u[31:26], a1[25:0]                     | 0x0000 0000          |
|            |                       |              | u[31:26], a2[25:0]                     | 0x0000 0000          |
| 0x5B       | ch4 BQ[1]             | 20           | u[31:26], b0[25:0]                     | 0x0080 0000          |
|            |                       |              | u[31:26], b1[25:0]                     | 0x0000 0000          |
|            |                       |              | u[31:26], b2[25:0]                     | 0x0000 0000          |
|            |                       |              | u[31:26], a1[25:0]                     | 0x0000 0000          |
|            |                       |              | u[31:26], a2[25:0]                     | 0x0000 0000          |
| 0x5C       | ch2 BQ[7]             | 20           | u[31:26], b0[25:0]                     | 0x0080 0000          |
|            |                       |              | u[31:26], b1[25:0]                     | 0x0000 0000          |
|            |                       |              | u[31:26], b2[25:0]                     | 0x0000 0000          |
|            |                       |              | u[31:26], a1[25:0]                     | 0x0000 0000          |
|            |                       |              | u[31:26], a2[25:0]                     | 0x0000 0000          |

**Table 2. Serial Control Interface Register Summary (continued)**

| SUBADDRESS | REGISTER NAME          | NO. OF BYTES | CONTENTS                                                 | INITIALIZATION VALUE |
|------------|------------------------|--------------|----------------------------------------------------------|----------------------|
| 0x5D       | ch2 BQ[8]              | 20           | u[31:26], b0[25:0]                                       | 0x0080 0000          |
|            |                        |              | u[31:26], b1[25:0]                                       | 0x0000 0000          |
|            |                        |              | u[31:26], b2[25:0]                                       | 0x0000 0000          |
|            |                        |              | u[31:26], a1[25:0]                                       | 0x0000 0000          |
|            |                        |              | u[31:26], a2[25:0]                                       | 0x0000 0000          |
| 0x5E       | ch3 BQ[0]              | 20           | u[31:26], b0[25:0]                                       | 0x0080 0000          |
|            |                        |              | u[31:26], b1[25:0]                                       | 0x0000 0000          |
|            |                        |              | u[31:26], b2[25:0]                                       | 0x0000 0000          |
|            |                        |              | u[31:26], a1[25:0]                                       | 0x0000 0000          |
|            |                        |              | u[31:26], a2[25:0]                                       | 0x0000 0000          |
| 0x5F       | ch3 BQ[1]              | 20           | u[31:26], b0[25:0]                                       | 0x0080 0000          |
|            |                        |              | u[31:26], b1[25:0]                                       | 0x0000 0000          |
|            |                        |              | u[31:26], b2[25:0]                                       | 0x0000 0000          |
|            |                        |              | u[31:26], a1[25:0]                                       | 0x0000 0000          |
|            |                        |              | u[31:26], a2[25:0]                                       | 0x0000 0000          |
| 0x60–0xF8  |                        | 4            | Reserved <sup>(5)</sup>                                  | 0x0000 0000          |
| 0XF9       | Update Dev Address Reg | 4            | u[31:8], New Dev Id[7:0] (New Dev Id = 0X38 for TAS5710) | 0x0000 0036          |
| 0xFA–0xFF  |                        | 4            | Reserved <sup>(5)</sup>                                  | 0x0000 0000          |

(5) Reserved registers should not be accessed.

**Note:** All DAP coefficients are 3.23 format unless specified otherwise

## CLOCK CONTROL REGISTER (0x00)

The clocks and data rates are automatically determined by the TAS5710. The clock control register contains the auto-detected clock status. Bits D7–D5 reflect the sample rate. Bits D4–D2 reflect the MCLK frequency. TAS5710 accepts a 64 Fs or 32 Fs SCLK rate for all MCLK ratios, but accepts a 48Fs SCLK rate only for MCLK ratios of 192 Fs and 384 Fs.

**Table 3. Clock Control Register (0x00)**

| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                                                                |
|----------|----------|----------|----------|----------|----------|----------|----------|-------------------------------------------------------------------------|
| 0        | 0        | 0        | –        | –        | –        | –        | –        | $f_s = 32\text{-kHz}$ sample rate                                       |
| 0        | 0        | 1        | –        | –        | –        | –        | –        | Reserved <sup>(1)</sup>                                                 |
| 0        | 1        | 0        | –        | –        | –        | –        | –        | Reserved <sup>(1)</sup>                                                 |
| <b>0</b> | <b>1</b> | <b>1</b> | –        | –        | –        | –        | –        | <b><math>f_s = 44.1/48\text{-kHz}</math> sample rate</b> <sup>(2)</sup> |
| 1        | 0        | 0        | –        | –        | –        | –        | –        | $f_s = 16\text{-kHz}$ sample rate                                       |
| 1        | 0        | 1        | –        | –        | –        | –        | –        | $f_s = 22.05/24\text{-kHz}$ sample rate                                 |
| 1        | 1        | 0        | –        | –        | –        | –        | –        | $f_s = 8\text{-kHz}$ sample rate                                        |
| 1        | 1        | 1        | –        | –        | –        | –        | –        | $f_s = 11.025/12\text{-kHz}$ sample rate                                |
| –        | –        | –        | 0        | 0        | 0        | –        | –        | MCLK frequency = $64 \times f_s$ <sup>(3)</sup>                         |
| –        | –        | –        | 0        | 0        | 1        | –        | –        | MCLK frequency = $128 \times f_s$ <sup>(3)</sup>                        |
| –        | –        | –        | 0        | 1        | 0        | –        | –        | MCLK frequency = $192 \times f_s$ <sup>(4)</sup>                        |
| –        | –        | –        | <b>0</b> | <b>1</b> | <b>1</b> | –        | –        | <b>MCLK frequency = <math>256 \times f_s</math></b> <sup>(2)(5)</sup>   |
| –        | –        | –        | 1        | 0        | 0        | –        | –        | MCLK frequency = $384 \times f_s$                                       |
| –        | –        | –        | 1        | 0        | 1        | –        | –        | MCLK frequency = $512 \times f_s$                                       |
| –        | –        | –        | 1        | 1        | 0        | –        | –        | Reserved <sup>(1)</sup>                                                 |
| –        | –        | –        | 1        | 1        | 1        | –        | –        | Reserved <sup>(1)</sup>                                                 |
| –        | –        | –        | –        | –        | –        | <b>0</b> | –        | <b>Reserved<sup>(1)</sup></b>                                           |
| –        | –        | –        | –        | –        | –        | –        | <b>0</b> | Reserved <sup>(1)</sup>                                                 |

(1) Reserved registers should not be accessed.

(2) Default values are in **bold**.

(3) Only available for 44.1 kHz and 48 kHz rates.

(4) Rate only available for 32/44.1/48 KHz sample rates

(5) Not available at 8 kHz

## DEVICE ID REGISTER (0x01)

The device ID register contains the ID code for the firmware revision.

**Table 4. General Status Register (0x01)**

| D7 | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                   |
|----|----------|----------|----------|----------|----------|----------|----------|----------------------------|
| X  | –        | –        | –        | –        | –        | –        | –        | Reserved                   |
| –  | <b>1</b> | <b>1</b> | <b>1</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>Identification code</b> |

## ERROR STATUS REGISTER (0x02)

The error bits are sticky and are not cleared by the hardware. This means that the software must clear the register (write zeroes) and then read them to determine if they are persistent errors.

Error Definitions:

- MCLK Error : MCLK frequency is changing. The number of MCLKs per LRCLK is changing.
- SCLK Error: The number of SCLKs per LRCLK is changing.
- LRCLK Error: LRCLK frequency is changing.
- Frame Slip: LRCLK phase is drifting with respect to internal Frame Sync.

**Table 5. Error Status Register (0x02)**

| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0 | FUNCTION                        |
|----------|----------|----------|----------|----------|----------|----------|----|---------------------------------|
| 1        | -        | -        | -        | -        | -        | -        | -  | MCLK error                      |
| -        | 1        | -        | -        | -        | -        | -        | -  | PLL autolock error              |
| -        | -        | 1        | -        | -        | -        | -        | -  | SCLK error                      |
| -        | -        | -        | 1        | -        | -        | -        | -  | LRCLK error                     |
| -        | -        | -        | -        | 1        | -        | -        | -  | Frame slip                      |
| -        | -        | -        | -        | -        | -        | 1        | -  | Over current error              |
| <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | -  | <b>No errors <sup>(1)</sup></b> |

(1) Default values are in **bold**.

## SYSTEM CONTROL REGISTER 1 (0x03)

The system control register 1 has several functions:

Bit D7: If 0, the dc-blocking filter for each channel is disabled.

If 1, the dc-blocking filter (–3 dB cutoff <1 Hz) for each channel is enabled (default).

Bit D5: If 0, use soft unmute on recovery from clock error. This is a slow recovery. Unmute takes same time as volume ramp defined in reg 0X0E.

If 1, use hard unmute on recovery from clock error (default). This is a fast recovery, a single step volume ramp

Bits D1–D0: Select de-emphasis

**Table 6. System Control Register 1 (0x03)**

| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                                                       |
|----------|----------|----------|----------|----------|----------|----------|----------|----------------------------------------------------------------|
| 0        | -        | -        | -        | -        | -        | -        | -        | PWM high-pass (dc blocking) disabled                           |
| <b>1</b> | -        | -        | -        | -        | -        | -        | -        | <b>PWM high-pass (dc blocking) enabled <sup>(1)</sup></b>      |
| -        | <b>0</b> | -        | -        | -        | -        | -        | -        | <b>Reserved <sup>(1)</sup></b>                                 |
| -        | -        | 0        | -        | -        | -        | -        | -        | Soft unmute on recovery from clock error                       |
| -        | -        | <b>1</b> | -        | -        | -        | -        | -        | <b>Hard unmute on recovery from clock error <sup>(1)</sup></b> |
| -        | -        | -        | <b>0</b> | -        | -        | -        | -        | <b>Reserved <sup>(1)</sup></b>                                 |
| -        | -        | -        | -        | <b>0</b> | -        | -        | -        | <b>Reserved <sup>(1)</sup></b>                                 |
| -        | -        | -        | -        | -        | <b>0</b> | -        | -        | <b>Reserved <sup>(1)</sup></b>                                 |
| -        | -        | -        | -        | -        | -        | <b>0</b> | <b>0</b> | <b>No de-emphasis <sup>(1)</sup></b>                           |
| -        | -        | -        | -        | -        | -        | 0        | 1        | Reserved                                                       |
| -        | -        | -        | -        | -        | -        | 1        | 0        | De-emphasis for $f_S = 44.1$ kHz                               |
| -        | -        | -        | -        | -        | -        | 1        | 1        | De-emphasis for $f_S = 48$ kHz                                 |

(1) Default values are in **bold**.

## SERIAL DATA INTERFACE REGISTER (0x04)

As shown in Table 7, the TAS5710 supports 9 serial data modes. The default is 24-bit, I<sup>2</sup>S mode,

**Table 7. Serial Data Interface Control Register (0x04) Format**

| RECEIVE SERIAL DATA<br>INTERFACE FORMAT | WORD<br>LENGTH | D7–D4       | D3       | D2       | D1       | D0       |
|-----------------------------------------|----------------|-------------|----------|----------|----------|----------|
| Right-justified                         | 16             | 0000        | 0        | 0        | 0        | 0        |
| Right-justified                         | 20             | 0000        | 0        | 0        | 0        | 1        |
| Right-justified                         | 24             | 0000        | 0        | 0        | 1        | 0        |
| I <sup>2</sup> S                        | 16             | 000         | 0        | 0        | 1        | 1        |
| I <sup>2</sup> S                        | 20             | 0000        | 0        | 1        | 0        | 0        |
| <b>I<sup>2</sup>S</b> <sup>(1)</sup>    | <b>24</b>      | <b>0000</b> | <b>0</b> | <b>1</b> | <b>0</b> | <b>1</b> |
| Left-justified                          | 16             | 0000        | 0        | 1        | 1        | 0        |
| Left-justified                          | 20             | 0000        | 0        | 1        | 1        | 1        |
| Left-justified                          | 24             | 0000        | 1        | 0        | 0        | 0        |
| Reserved                                |                | 0000        | 1        | 0        | 0        | 1        |
| Reserved                                |                | 0000        | 1        | 0        | 1        | 0        |
| Reserved                                |                | 0000        | 1        | 0        | 1        | 1        |
| Reserved                                |                | 0000        | 1        | 1        | 0        | 0        |
| Reserved                                |                | 0000        | 1        | 1        | 0        | 1        |
| Reserved                                |                | 0000        | 1        | 1        | 1        | 0        |
| Reserved                                |                | 0000        | 1        | 1        | 1        | 1        |

(1) Default values are in **bold**.

## SYSTEM CONTROL REGISTER 2 (0x05)

When bit D6 is set low, the system exits all channel shutdown and starts playing audio; otherwise, the outputs are shut down(hard mute).

**Table 8. System Control Register 2 (0x05)**

| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                                                       |
|----------|----------|----------|----------|----------|----------|----------|----------|----------------------------------------------------------------|
| <b>0</b> | –        | –        | –        | –        | –        | –        | –        | <b>Reserved</b> <sup>(1)</sup>                                 |
| –        | <b>1</b> | –        | –        | –        | –        | –        | –        | <b>Enter all channel shut down (hard mute).</b> <sup>(1)</sup> |
| –        | 0        | –        | –        | –        | –        | –        | –        | Exit all channel shutdown (normal operation)                   |
| –        | –        | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>Reserved</b> <sup>(1)</sup>                                 |

(1) Default values are in **bold**.

## SOFT MUTE REGISTER (0x06)

Writing a 1 to any of the following bits sets the output of the respective channel to 50% duty cycle (soft mute).

**Table 9. Soft Mute Register (0x06)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                     |
|----|----|----|----|----|----|----|----|------------------------------|
| –  | –  | –  | –  | –  | –  | –  | 1  | Soft mute channel 1          |
| –  | –  | –  | –  | –  | –  | –  | 0  | <b>Soft unmute channel 1</b> |
| –  | –  | –  | –  | –  | –  | 1  | –  | Soft mute channel 2          |
| –  | –  | –  | –  | –  | –  | 0  | –  | <b>Soft unmute channel 2</b> |
| 0  | 0  | 0  | 0  | 0  | 0  | –  | –  | Reserved                     |

## VOLUME REGISTERS (0x07, 0x08, 0x09)

Step size is 0.5 dB.

Master volume – 0x07 (default is mute)

Channel-1 volume – 0x08 (default is 0 dB)

Channel-2 volume – 0x09 (default is 0 dB)

**Table 10. Volume Registers (0x07, 0x08, 0x09)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                                                           |
|----|----|----|----|----|----|----|----|--------------------------------------------------------------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 24 dB                                                              |
| 0  | 0  | 1  | 1  | 0  | 0  | 0  | 0  | <b>0 dB (default for individual channel volume)</b> <sup>(1)</sup> |
| 1  | 1  | 0  | 0  | 1  | 1  | 0  | 1  | –78.5 dB                                                           |
| 1  | 1  | 0  | 0  | 1  | 1  | 1  | 0  | –79.0 dB                                                           |
| 1  | 1  | 0  | 0  | 1  | 1  | 1  | 1  | Values between 0xCF and 0xFE are Reserved                          |
| 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | MUTE (default for master volume)                                   |

(1) Default values are in **bold**.

## MASTER FINE VOLUME REGISTER (0x0A)

This register can be used to provide precision tuning of master volume. If fine master volume is used, output mixers (0x51 and 0x52) should not be used. Similarly, this feature cannot be used if features like 2-band DRC or Bass Boost are being used. Write a "1" to bit D7 to enable changes to this register.

**Table 11. Master Fine Volume Register (0x0A)**

| D7       | D6 | D5 | D4 | D3 | D2 | D1       | D0       | FUNCTION                             |
|----------|----|----|----|----|----|----------|----------|--------------------------------------|
| –        | –  | –  | –  | –  | –  | <b>0</b> | <b>0</b> | <b>0 dB</b> <sup>(1)</sup>           |
| –        | –  | –  | –  | –  | –  | 0        | 1        | 0.125 dB                             |
| –        | –  | –  | –  | –  | –  | 1        | 0        | 0.25 dB                              |
| –        | –  | –  | –  | –  | –  | 1        | 1        | 0.375 dB                             |
| 1        | –  | –  | –  | –  | –  | –        | –        | Write enable bit                     |
| <b>0</b> | –  | –  | –  | –  | –  | –        | –        | <b>Ignore Write to register 0X0A</b> |

(1) Default values are in **bold**.

## VOLUME CONFIGURATION REGISTER (0x0E)

Bits D2–D0: Volume slew rate (Used to control volume change and MUTE ramp rates). These bits control the number of steps in a volume ramp. Volume steps occur at a rate that depends on the sample rate of the I2S data as follows

| Sample Rate (KHz) | Approximate Ramp Rate |
|-------------------|-----------------------|
| 8/16/32           | 125 us/step           |
| 11.025/22.05/44.1 | 90.7 us/step          |
| 12/24/48          | 83.3 us/step          |

**Table 12. Volume Control Register (0x0E)**

| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                                                                       |
|----------|----------|----------|----------|----------|----------|----------|----------|--------------------------------------------------------------------------------|
| <b>1</b> | <b>0</b> | <b>0</b> | <b>1</b> | <b>0</b> | –        | –        | –        | <b>Reserved</b> <sup>(1)</sup>                                                 |
| –        | –        | –        | –        | –        | 0        | 0        | 0        | Volume slew 512 steps (43 ms volume ramp time at 48kHz)                        |
| –        | –        | –        | –        | –        | <b>0</b> | <b>0</b> | <b>1</b> | <b>Volume slew 1024 steps (85 ms volume ramp time at 48kHz)</b> <sup>(1)</sup> |
| –        | –        | –        | –        | –        | 0        | 1        | 0        | Volume slew 2048 steps (171 ms volume ramp time at 48kHz)                      |
| –        | –        | –        | –        | –        | 0        | 1        | 1        | Volume slew 256 steps (21ms volume ramp time at 48kHz)                         |
| –        | –        | –        | –        | –        | 1        | X        | X        | Reserved                                                                       |

(1) Default values are in **bold**.

## MODULATION LIMIT REGISTER (0x10)

**Table 13. Modulation Limit Register (0x10)**

| D7 | D6 | D5 | D4 | D3 | D2       | D1       | D0       | MODULATION LIMIT |
|----|----|----|----|----|----------|----------|----------|------------------|
| –  | –  | –  | –  | –  | 0        | 0        | 0        | 99.2%            |
| –  | –  | –  | –  | –  | 0        | 0        | 1        | 98.4%            |
| –  | –  | –  | –  | –  | <b>0</b> | <b>1</b> | <b>0</b> | <b>97.7%</b>     |
| –  | –  | –  | –  | –  | 0        | 1        | 1        | 96.9%            |
| –  | –  | –  | –  | –  | 1        | 0        | 0        | 96.1%            |
| –  | –  | –  | –  | –  | 1        | 0        | 1        | 95.3%            |
| –  | –  | –  | –  | –  | 1        | 1        | 0        | 94.5%            |
| –  | –  | –  | –  | –  | 1        | 1        | 1        | 93.8%            |
| 0  | 0  | 0  | 0  | 0  | –        | –        | –        | RESERVED         |

## INTERCHANNEL DELAY REGISTERS (0x11, 0x12, 0x13, and 0x14)

Internal PWM Channels 1, 2,  $\bar{1}$ , and  $\bar{2}$  are mapped into registers 0x11, 0x12, 0x13, and 0x14.

**Table 14. Channel Interchannel Delay Register Format**

| BITS DEFINITION | D7       | D6       | D5       | D4       | D3       | D2       | D1 | D0 | FUNCTION                                           |
|-----------------|----------|----------|----------|----------|----------|----------|----|----|----------------------------------------------------|
|                 | 0        | 0        | 0        | 0        | 0        | 0        | –  | –  | Minimum absolute delay, 0 DCLK cycles              |
|                 | 0        | 1        | 1        | 1        | 1        | 1        | –  | –  | Maximum positive delay, $31 \times 4$ DCLK cycles  |
|                 | 1        | 0        | 0        | 0        | 0        | 0        | –  | –  | Maximum negative delay, $-32 \times 4$ DCLK cycles |
|                 |          |          |          |          |          |          | 0  | 0  | RESERVED                                           |
| SUBADDRESS      | D7       | D6       | D5       | D4       | D3       | D2       | D1 | D0 | Delay = (value) $\times 4$ DCLKs                   |
| <b>0x11</b>     | <b>0</b> | <b>1</b> | <b>0</b> | <b>0</b> | <b>1</b> | <b>1</b> | –  | –  | <b>Default value for channel 1</b> <sup>(1)</sup>  |
| <b>0x12</b>     | <b>0</b> | <b>1</b> | <b>1</b> | <b>1</b> | <b>0</b> | <b>0</b> | –  | –  | <b>Default value for channel 2</b> <sup>(1)</sup>  |
| <b>0x13</b>     | <b>0</b> | <b>0</b> | <b>0</b> | <b>1</b> | <b>1</b> | <b>1</b> | –  | –  | <b>Default value for channel 1</b> <sup>(1)</sup>  |
| <b>0x14</b>     | <b>0</b> | <b>1</b> | <b>1</b> | <b>0</b> | <b>0</b> | <b>1</b> | –  | –  | <b>Default value for channel 2</b> <sup>(1)</sup>  |

(1) Default values are in **bold**.

ICD settings have high impact on audio performance (eg: Dynamic Range, THD, Cross talk etc.) Therefore, appropriate ICD settings must be used. By default device has ICD settings for BD mode. If used in AD mode, then update these registers before coming out of all channel shutdown. Contact factory for AD Mode ICD settings.

| MODE | BD MODE |
|------|---------|
| 0x11 | 4C      |
| 0x12 | 34      |
| 0x13 | 1C      |
| 0x14 | 64      |

## START/STOP PERIOD REGISTER (0x1A)

This register is used to control the soft-start and soft-stop period following an enter/exit all channel shut down command or change in the  $\overline{\text{PDN}}$  state. This helps reduce pops and clicks at start-up and shutdown. The times are only approximate and vary depending on device activity level and I2S clock stability.

**Table 15. Start/Stop Period Register (0x1A)**

| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                                                       |
|----------|----------|----------|----------|----------|----------|----------|----------|----------------------------------------------------------------|
| <b>0</b> | <b>0</b> | <b>0</b> | –        | –        | –        | –        | –        | <b>Reserved</b>                                                |
| –        | –        | –        | 0        | 0        | –        | –        | –        | No 50% duty cycle start/stop period                            |
| –        | –        | –        | 0        | 1        | 0        | 0        | 0        | 16.5-ms 50% duty cycle start/stop period                       |
| –        | –        | –        | 0        | 1        | 0        | 0        | 1        | 23.9-ms 50% duty cycle start/stop period                       |
| –        | –        | –        | 0        | 1        | 0        | 1        | 0        | 31.4-ms 50% duty cycle start/stop period                       |
| –        | –        | –        | 0        | 1        | 0        | 1        | 1        | 40.4-ms 50% duty cycle start/stop period                       |
| –        | –        | –        | 0        | 1        | 1        | 0        | 0        | 53.9-ms 50% duty cycle start/stop period                       |
| –        | –        | –        | 0        | 1        | 1        | 0        | 1        | 70.3-ms 50% duty cycle start/stop period                       |
| –        | –        | –        | 0        | 1        | 1        | 1        | 0        | 94.2-ms 50% duty cycle start/stop period                       |
| –        | –        | –        | <b>0</b> | <b>1</b> | <b>1</b> | <b>1</b> | <b>1</b> | <b>125.7-ms 50% duty cycle start/stop period<sup>(1)</sup></b> |
| –        | –        | –        | 1        | 0        | 0        | 0        | 0        | 164.6-ms 50% duty cycle start/stop period                      |
| –        | –        | –        | 1        | 0        | 0        | 0        | 1        | 239.4-ms 50% duty cycle start/stop period                      |
| –        | –        | –        | 1        | 0        | 0        | 1        | 0        | 314.2-ms 50% duty cycle start/stop period                      |
| –        | –        | –        | 1        | 0        | 0        | 1        | 1        | 403.9-ms 50% duty cycle start/stop period                      |
| –        | –        | –        | 1        | 0        | 1        | 0        | 0        | 538.6-ms 50% duty cycle start/stop period                      |
| –        | –        | –        | 1        | 0        | 1        | 0        | 1        | 703.1-ms 50% duty cycle start/stop period                      |
| –        | –        | –        | 1        | 0        | 1        | 1        | 0        | 942.5-ms 50% duty cycle start/stop period                      |
| –        | –        | –        | 1        | 0        | 1        | 1        | 1        | 1256.6-ms 50% duty cycle start/stop period                     |
| –        | –        | –        | 1        | 1        | 0        | 0        | 0        | 1728.1-ms 50% duty cycle start/stop period                     |
| –        | –        | –        | 1        | 1        | 0        | 0        | 1        | 2513.6-ms 50% duty cycle start/stop period                     |
| –        | –        | –        | 1        | 1        | 0        | 1        | 0        | 3299.1-ms 50% duty cycle start/stop period                     |
| –        | –        | –        | 1        | 1        | 0        | 1        | 1        | 4241.7-ms 50% duty cycle start/stop period                     |
| –        | –        | –        | 1        | 1        | 1        | 0        | 0        | 5655.6-ms 50% duty cycle start/stop period                     |
| –        | –        | –        | 1        | 1        | 1        | 0        | 1        | 7383.7-ms 50% duty cycle start/stop period                     |
| –        | –        | –        | 1        | 1        | 1        | 1        | 0        | 9897.3-ms 50% duty cycle start/stop period                     |
| –        | –        | –        | 1        | 1        | 1        | 1        | 1        | 13,196.4-ms 50% duty cycle start/stop period                   |

(1) Default values are in **bold**.

## OSCILLATOR TRIM REGISTER (0x1B)

The TAS5710 PWM processor contains an internal oscillator to support autodetect of I2S clock rates. This reduces system cost because an external reference is not required. Currently, TI recommends a reference resistor value of 18.2 kΩ (1%). This should be connected between OSC\_RES and DVSSO.

Writing 0X00 to reg 0X1B enables the trim that was programmed at the factory.

Note that trim must always be run following reset of the device.

**Table 16. Oscillator Trim Register (0x1B)**

| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                                                              |
|----------|----------|----------|----------|----------|----------|----------|----------|-----------------------------------------------------------------------|
| <b>1</b> | –        | –        | –        | –        | –        | –        | –        | <b>Reserved</b> <sup>(1)</sup>                                        |
| –        | <b>0</b> | –        | –        | –        | –        | –        | –        | <b>Oscillator trim not done (read-only)</b> <sup>(1)</sup>            |
| –        | <b>1</b> | –        | –        | –        | –        | –        | –        | Oscillator trim done (read only)                                      |
| –        | –        | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | –        | –        | <b>Reserved</b> <sup>(1)</sup>                                        |
| –        | –        | –        | –        | –        | –        | <b>0</b> | –        | Select factory trim (Write a 0 to select factory trim; default is 1.) |
| –        | –        | –        | –        | –        | –        | <b>1</b> | –        | <b>Factory trim disabled</b> <sup>(1)</sup>                           |
| –        | –        | –        | –        | –        | –        | –        | <b>0</b> | <b>Reserved</b> <sup>(1)</sup>                                        |

(1) Default values are in **bold**.

## BKND\_ERR REGISTER (0x1C)

When a back-end error signal is received from the internal power stage, the power stage is reset stopping all PWM activity. Subsequently, the modulator waits approximately for the time listed in [Table 17](#) before attempting to re-start the power stage.

**Table 17. BKND\_ERR Register (0x1C)** <sup>(1)</sup>

| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                                                  |
|----------|----------|----------|----------|----------|----------|----------|----------|-----------------------------------------------------------|
| <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>X</b> | Reserved                                                  |
| –        | –        | –        | –        | <b>0</b> | <b>0</b> | <b>1</b> | <b>0</b> | <b>Set back-end reset period to 299 ms</b> <sup>(2)</sup> |
| –        | –        | –        | –        | <b>0</b> | <b>0</b> | <b>1</b> | <b>1</b> | Set back-end reset period to 449 ms                       |
| –        | –        | –        | –        | <b>0</b> | <b>1</b> | <b>0</b> | <b>0</b> | Set back-end reset period to 598 ms                       |
| –        | –        | –        | –        | <b>0</b> | <b>1</b> | <b>0</b> | <b>1</b> | Set back-end reset period to 748 ms                       |
| –        | –        | –        | –        | <b>0</b> | <b>1</b> | <b>1</b> | <b>0</b> | Set back-end reset period to 898 ms                       |
| –        | –        | –        | –        | <b>0</b> | <b>1</b> | <b>1</b> | <b>1</b> | Set back-end reset period to 1047 ms                      |
| –        | –        | –        | –        | <b>1</b> | <b>0</b> | <b>0</b> | <b>0</b> | Set back-end reset period to 1197 ms                      |
| –        | –        | –        | –        | <b>1</b> | <b>0</b> | <b>0</b> | <b>1</b> | Set back-end reset period to 1346 ms                      |
| –        | –        | –        | –        | <b>1</b> | <b>0</b> | <b>1</b> | <b>X</b> | Set back-end reset period to 1496 ms                      |
| –        | –        | –        | –        | <b>1</b> | <b>1</b> | <b>X</b> | <b>X</b> | Set back-end reset period to 1496 ms                      |

(1) This register can be written only with a "non-Reserved" value. Also this register can be written once after the reset.

(2) Default values are in **bold**.

## INPUT MULTIPLEXER REGISTER (0x20)

This register controls the modulation scheme (AD or BD mode) as well as the routing of I2S audio to the internal channels.

**Table 18. Input Multiplexer Register (0x20)**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION                                  |
|-----|-----|-----|-----|-----|-----|-----|-----|-------------------------------------------|
| 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | Reserved <sup>(1)</sup>                   |
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | FUNCTION                                  |
| 0   | –   | –   | –   | –   | –   | –   | –   | <b>Channel-1 AD mode</b>                  |
| 1   | –   | –   | –   | –   | –   | –   | –   | Channel-1 BD mode                         |
| –   | 0   | 0   | 0   | –   | –   | –   | –   | <b>SDIN-L to channel 1 <sup>(1)</sup></b> |
| –   | 0   | 0   | 1   | –   | –   | –   | –   | SDIN-R to channel 1                       |
| –   | 0   | 1   | 0   | –   | –   | –   | –   | Reserved                                  |
| –   | 0   | 1   | 1   | –   | –   | –   | –   | Reserved                                  |
| –   | 1   | 0   | 0   | –   | –   | –   | –   | Reserved                                  |
| –   | 1   | 0   | 1   | –   | –   | –   | –   | Reserved                                  |
| –   | 1   | 1   | 0   | –   | –   | –   | –   | Ground (0) to channel 1                   |
| –   | 1   | 1   | 1   | –   | –   | –   | –   | Reserved                                  |
| –   | –   | –   | –   | 0   | –   | –   | –   | <b>Channel 2 AD mode</b>                  |
| –   | –   | –   | –   | 1   | –   | –   | –   | Channel 2 BD mode                         |
| –   | –   | –   | –   | –   | 0   | 0   | 0   | SDIN-L to channel 2                       |
| –   | –   | –   | –   | –   | 0   | 0   | 1   | <b>SDIN-R to channel 2 <sup>(1)</sup></b> |
| –   | –   | –   | –   | –   | 0   | 1   | 0   | Reserved                                  |
| –   | –   | –   | –   | –   | 0   | 1   | 1   | Reserved                                  |
| –   | –   | –   | –   | –   | 1   | 0   | 0   | Reserved                                  |
| –   | –   | –   | –   | –   | 1   | 0   | 1   | Reserved                                  |
| –   | –   | –   | –   | –   | 1   | 1   | 0   | Ground (0) to channel 2                   |
| –   | –   | –   | –   | –   | 1   | 1   | 1   | Reserved                                  |
| D15 | D14 | D13 | D12 | D11 | D10 | D9  | D8  | FUNCTION                                  |
| 0   | 1   | 1   | 1   | 0   | 1   | 1   | 1   | Reserved <sup>(1)</sup>                   |
| D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  | FUNCTION                                  |
| 0   | 1   | 1   | 1   | 0   | 0   | 1   | 0   | Reserved <sup>(1)</sup>                   |

(1) Default values are in **bold**.

## CHANNEL 4 SOURCE SELECT REGISTER (0x21)

This register selects the channel 4 source.

**Table 19. Subchannel Control Register (0x21)**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION                |
|-----|-----|-----|-----|-----|-----|-----|-----|-------------------------|
| 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | Reserved <sup>(1)</sup> |
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | FUNCTION                |
| 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | Reserved <sup>(1)</sup> |
| D15 | D14 | D13 | D12 | D11 | D10 | D9  | D8  | FUNCTION                |
| 0   | 1   | 0   | 0   | 0   | 0   | 1   |     | Reserved <sup>(1)</sup> |
| –   | –   | –   | –   | –   | –   | –   | 0   | (L + R)/2               |
| –   | –   | –   | –   | –   | –   | –   | 1   | Left-channel post-BQ    |
| D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  | FUNCTION                |
| 0   | 0   | 0   | 0   | 0   | 0   | 1   | 1   | Reserved <sup>(1)</sup> |

(1) Default values are in **bold**.

## PWM OUTPUT MUX REGISTER (0x25)

This DAP output mux selects which internal PWM channel is output to the external pins. Any channel can be output to any external output pin.

Bits D21–D20: Selects which PWM channel is output to OUT\_A

Bits D17–D16: Selects which PWM channel is output to OUT\_B

Bits D13–D12: Selects which PWM channel is output to OUT\_C

Bits D09–D08: Selects which PWM channel is output to OUT\_D

Note that channels are enclosed so that channel 1 = 0x00, channel 2 = 0x01,  $\overline{\text{channel 1}}$  = 0x02, and  $\overline{\text{channel 2}}$  = 0x03.

**Table 20. PWM Output Mux Register (0x25)**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION                                                 |
|-----|-----|-----|-----|-----|-----|-----|-----|----------------------------------------------------------|
| 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | Reserved <sup>(1)</sup>                                  |
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | FUNCTION                                                 |
| 0   | 0   | –   | –   | –   | –   | –   | –   | Reserved <sup>(1)</sup>                                  |
| –   | –   | 0   | 0   | –   | –   | –   | –   | Multiplex channel 1 to OUT_A <sup>(1)</sup>              |
| –   | –   | 0   | 1   | –   | –   | –   | –   | Multiplex channel 2 to OUT_A                             |
| –   | –   | 1   | 0   | –   | –   | –   | –   | Multiplex channel $\overline{1}$ to OUT_A                |
| –   | –   | 1   | 1   | –   | –   | –   | –   | Multiplex channel $\overline{2}$ to OUT_A                |
| –   | –   | –   | –   | 0   | 0   | –   | –   | Reserved <sup>(1)</sup>                                  |
| –   | –   | –   | –   | –   | –   | 0   | 0   | Multiplex channel 1 to OUT_B                             |
| –   | –   | –   | –   | –   | –   | 0   | 1   | Multiplex channel 2 to OUT_B                             |
| –   | –   | –   | –   | –   | –   | 1   | 0   | Multiplex channel $\overline{1}$ to OUT_B <sup>(1)</sup> |
| –   | –   | –   | –   | –   | –   | 1   | 1   | Multiplex channel $\overline{2}$ to OUT_B                |

(1) Default values are in **bold**.

**Table 20. PWM Output Mux Register (0x25) (continued)**

| D15      | D14      | D13      | D12      | D11      | D10      | D9       | D8       | FUNCTION                                           |
|----------|----------|----------|----------|----------|----------|----------|----------|----------------------------------------------------|
| <b>0</b> | <b>0</b> | –        | –        | –        | –        | –        | –        | <b>Reserved</b> <sup>(2)</sup>                     |
| –        | –        | 0        | 0        | –        | –        | –        | –        | Multiplex channel 1 to OUT_C                       |
| –        | –        | <b>0</b> | <b>1</b> | –        | –        | –        | –        | <b>Multiplex channel 2 to OUT_C</b> <sup>(2)</sup> |
| –        | –        | 1        | 0        | –        | –        | –        | –        | Multiplex channel 1 to OUT_C                       |
| –        | –        | 1        | 1        | –        | –        | –        | –        | Multiplex channel 2 to OUT_C                       |
| –        | –        | –        | –        | <b>0</b> | <b>0</b> | –        | –        | <b>Reserved</b> <sup>(2)</sup>                     |
| –        | –        | –        | –        | –        | –        | 0        | 0        | Multiplex channel 1 to OUT_D                       |
| –        | –        | –        | –        | –        | –        | 0        | 1        | Multiplex channel 2 to OUT_D                       |
| –        | –        | –        | –        | –        | –        | 1        | 0        | Multiplex channel 1 to OUT_D                       |
| –        | –        | –        | –        | –        | –        | <b>1</b> | <b>1</b> | <b>Multiplex channel 2 to OUT_D</b> <sup>(2)</sup> |
| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                                           |
| 0        | 1        | 0        | 0        | 0        | 1        | 0        | 1        | RESERVED                                           |

(2) Default values are in **bold**.**DRC CONTROL (0x46)**

| D31      | D30      | D29      | D28      | D27      | D26      | D25      | D24      | FUNCTION                              |
|----------|----------|----------|----------|----------|----------|----------|----------|---------------------------------------|
| <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>Reserved</b> <sup>(1)</sup>        |
| D23      | D22      | D21      | D20      | D19      | D18      | D17      | D16      | FUNCTION                              |
| <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>Reserved</b> <sup>(1)</sup>        |
| D15      | D14      | D13      | D12      | D11      | D10      | D9       | D8       | FUNCTION                              |
| <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>Reserved</b> <sup>(1)</sup>        |
| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       | FUNCTION                              |
| –        | –        | –        | –        | –        | –        | –        | <b>0</b> | <b>DRC1 turned OFF</b> <sup>(1)</sup> |
| –        | –        | –        | –        | –        | –        | –        | 1        | DRC1 turned ON                        |
| –        | –        | –        | –        | –        | –        | <b>0</b> | –        | <b>DRC2 turned OFF</b> <sup>(1)</sup> |
| –        | –        | –        | –        | –        | –        | 1        | –        | DRC2 turned ON                        |
| <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | –        | –        | <b>Reserved</b> <sup>(1)</sup>        |

(1) Default values are in **bold**.

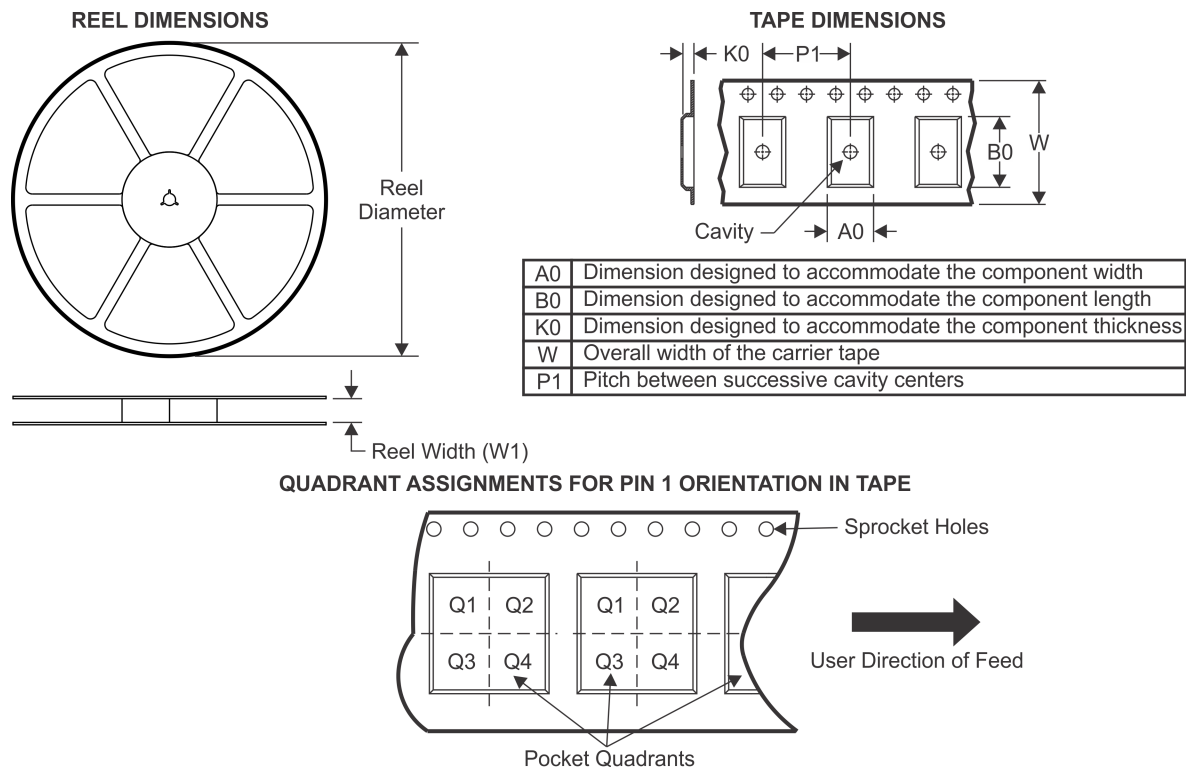
**BANK SWITCH AND EQ CONTROL (0x50)**
**Table 21. Bank Switching Command**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION                                          |
|-----|-----|-----|-----|-----|-----|-----|-----|---------------------------------------------------|
| 0   | –   | –   | –   | –   | –   | –   | –   | 32 kHz, does not use bank 3 <sup>(1)</sup>        |
| 1   | –   | –   | –   | –   | –   | –   | –   | 32 kHz, uses bank 3                               |
| –   | 0   | –   | –   | –   | –   | –   | –   | Reserved                                          |
| –   | –   | 0   | –   | –   | –   | –   | –   | Reserved                                          |
| –   | –   | –   | 0   | –   | –   | –   | –   | 44.1/48 kHz, does not use bank 3 <sup>(1)</sup>   |
| –   | –   | –   | 1   | –   | –   | –   | –   | 44.1/48 kHz, uses bank 3                          |
| –   | –   | –   | –   | 0   | –   | –   | –   | 16 kHz, does not use bank 3                       |
| –   | –   | –   | –   | 1   | –   | –   | –   | 16 kHz, uses bank 3 <sup>(1)</sup>                |
| –   | –   | –   | –   | –   | 0   | –   | –   | 22.025/24 kHz, does not use bank 3                |
| –   | –   | –   | –   | –   | 1   | –   | –   | 22.025/24 kHz, uses bank 3 <sup>(1)</sup>         |
| –   | –   | –   | –   | –   | –   | 0   | –   | 8 kHz, does not use bank 3                        |
| –   | –   | –   | –   | –   | –   | 1   | –   | 8 kHz, uses bank 3 <sup>(1)</sup>                 |
| –   | –   | –   | –   | –   | –   | –   | 0   | 11.025 kHz/12, does not use bank 3                |
| –   | –   | –   | –   | –   | –   | –   | 1   | 11.025/12 kHz, uses bank 3 <sup>(1)</sup>         |
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | FUNCTION                                          |
| 0   | –   | –   | –   | –   | –   | –   | –   | 32 kHz, does not use bank 2 <sup>(1)</sup>        |
| 1   | –   | –   | –   | –   | –   | –   | –   | 32 kHz, uses bank 2                               |
| –   | 1   | –   | –   | –   | –   | –   | –   | Reserved <sup>(1)</sup>                           |
| –   | –   | 1   | –   | –   | –   | –   | –   | Reserved <sup>(1)</sup>                           |
| –   | –   | –   | 0   | –   | –   | –   | –   | 44.1/48 kHz, does not use bank 2                  |
| –   | –   | –   | 1   | –   | –   | –   | –   | 44.1/48 kHz, uses bank 2 <sup>(1)</sup>           |
| –   | –   | –   | –   | 0   | –   | –   | –   | 16 kHz, does not use bank 2 <sup>(1)</sup>        |
| –   | –   | –   | –   | 1   | –   | –   | –   | 16 kHz, uses bank 2                               |
| –   | –   | –   | –   | –   | 0   | –   | –   | 22.025/24 kHz, does not use bank 2 <sup>(1)</sup> |
| –   | –   | –   | –   | –   | 1   | –   | –   | 22.025/24 kHz, uses bank 2                        |
| –   | –   | –   | –   | –   | –   | 0   | –   | 8 kHz, does not use bank 2 <sup>(1)</sup>         |
| –   | –   | –   | –   | –   | –   | 1   | –   | 8 kHz, uses bank 2                                |
| –   | –   | –   | –   | –   | –   | –   | 0   | 11.025/12 kHz, does not use bank 2 <sup>(1)</sup> |
| –   | –   | –   | –   | –   | –   | –   | 1   | 11.025/12 kHz, uses bank 2                        |
| D15 | D14 | D13 | D12 | D11 | D10 | D9  | D8  | FUNCTION                                          |
| 0   | –   | –   | –   | –   | –   | –   | –   | 32 kHz, does not use bank 1                       |
| 1   | –   | –   | –   | –   | –   | –   | –   | 32 kHz, uses bank 1 <sup>(1)</sup>                |
| –   | 0   | –   | –   | –   | –   | –   | –   | Reserved                                          |
| –   | –   | 0   | –   | –   | –   | –   | –   | Reserved                                          |
| –   | –   | –   | 0   | –   | –   | –   | –   | 44.1/48 kHz, does not use bank 1 <sup>(1)</sup>   |
| –   | –   | –   | 1   | –   | –   | –   | –   | 44.1/48 kHz, uses bank 1                          |
| –   | –   | –   | –   | 0   | –   | –   | –   | 16 kHz, does not use bank 1 <sup>(1)</sup>        |
| –   | –   | –   | –   | 1   | –   | –   | –   | 16 kHz, uses bank 1                               |
| –   | –   | –   | –   | –   | 0   | –   | –   | 22.025/24 kHz, does not use bank 1 <sup>(1)</sup> |
| –   | –   | –   | –   | –   | 1   | –   | –   | 22.025/24 kHz, uses bank 1                        |
| –   | –   | –   | –   | –   | –   | 0   | –   | 8 kHz, does not use bank 1 <sup>(1)</sup>         |
| –   | –   | –   | –   | –   | –   | 1   | –   | 8 kHz, uses bank 1                                |
| –   | –   | –   | –   | –   | –   | –   | 0   | 11.025/12 kHz, does not use bank 1 <sup>(1)</sup> |
| –   | –   | –   | –   | –   | –   | –   | 1   | 11.025/12 kHz, uses bank 1                        |

(1) Default values are in **bold**.

**Table 21. Bank Switching Command (continued)**

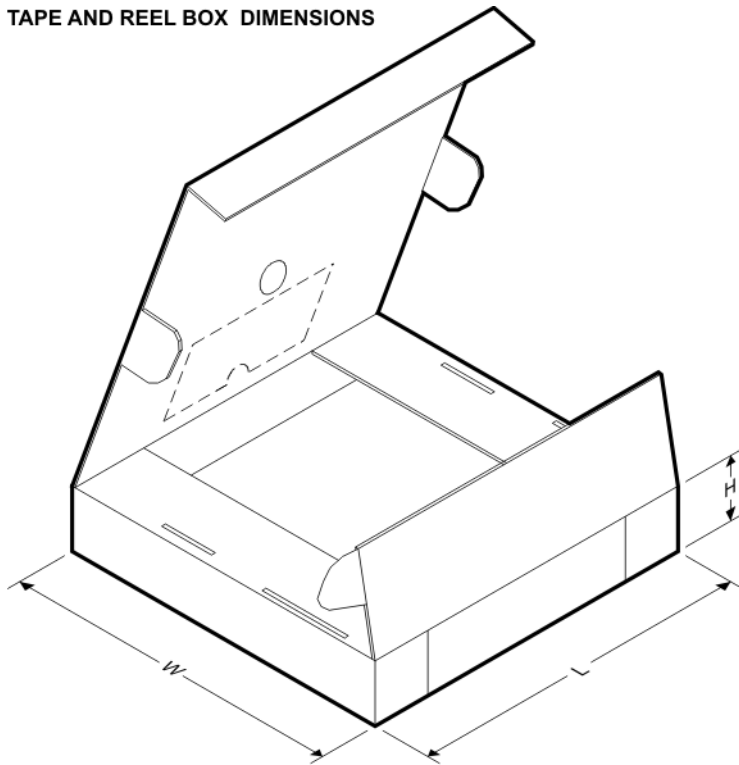
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                                                                                                                             |
|----|----|----|----|----|----|----|----|--------------------------------------------------------------------------------------------------------------------------------------|
| 0  |    |    |    |    |    |    |    | EQ ON                                                                                                                                |
| 1  | –  | –  | –  | –  | –  | –  | –  | EQ OFF (bypass BQ 0-6 of channels 1 and 2)                                                                                           |
| –  | 0  | –  | –  | –  | –  | –  | –  | Reserved <sup>(1)</sup>                                                                                                              |
| –  | –  | 0  | –  | –  | –  | –  | –  | Ignore bank-mapping in bits D31–D8. Use default mapping. <sup>(1)</sup>                                                              |
|    |    | 1  |    |    |    |    |    | Use bank-mapping in bits D31–D8.                                                                                                     |
| –  | –  | –  | 0  | –  | –  | –  | –  | L and R can be written independently. <sup>(1)</sup>                                                                                 |
| –  | –  | –  | 1  | –  | –  | –  | –  | L and R are ganged for EQ biquads; a write to Left channel BQ is also written to Right channel BQ. (0X29-2F is ganged to 0X30-0X36). |
| –  | –  | –  | –  | 0  | –  | –  | –  | Reserved <sup>(1)</sup>                                                                                                              |
| –  | –  | –  | –  | –  | 0  | 0  | 0  | No bank switching. All updates to DAP <sup>(1)</sup>                                                                                 |
| –  | –  | –  | –  | –  | 0  | 0  | 1  | Configure bank 1 (32 kHz by default)                                                                                                 |
| –  | –  | –  | –  | –  | 0  | 1  | 0  | Configure bank 2 (44.1/48 kHz by default)                                                                                            |
| –  | –  | –  | –  | –  | 0  | 1  | 1  | Configure bank 3 (other sample rates by default)                                                                                     |
| –  | –  | –  | –  | –  | 1  | 0  | 0  | Automatic bank selection                                                                                                             |
| –  | –  | –  | –  | –  | 1  | 0  | 1  | Reserved                                                                                                                             |
| –  | –  | –  | –  | –  | 1  | 1  | X  | Reserved                                                                                                                             |

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TAS5710PHPR | HTQFP        | PHP             | 48   | 1000 | 330.0              | 16.4               | 9.6     | 9.6     | 1.5     | 12.0    | 16.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS

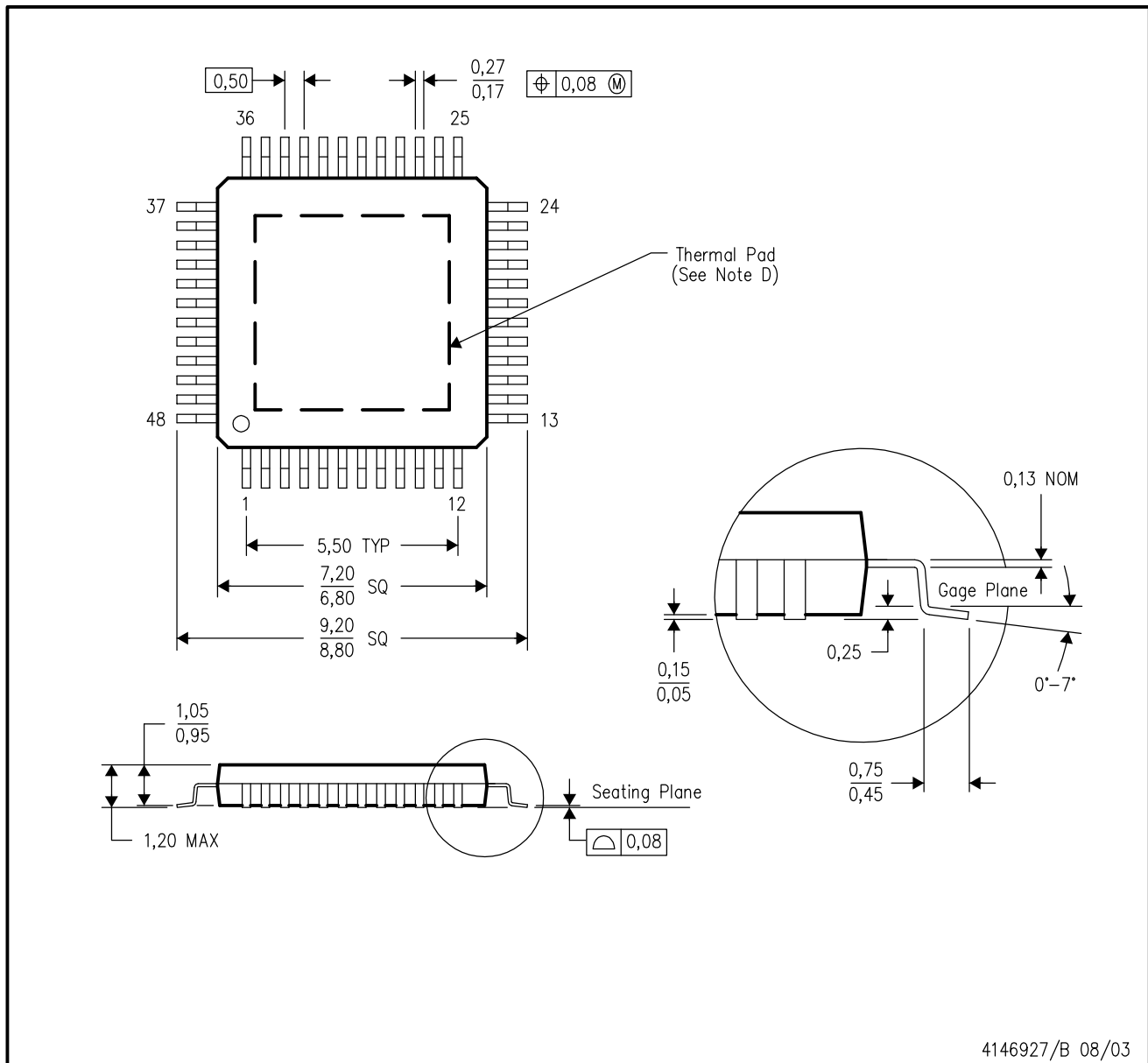


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TAS5710PHPR | HTQFP        | PHP             | 48   | 1000 | 336.6       | 336.6      | 31.8        |

PHP (S-PQFP-G48)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

PHP (S-PQFP-G48)

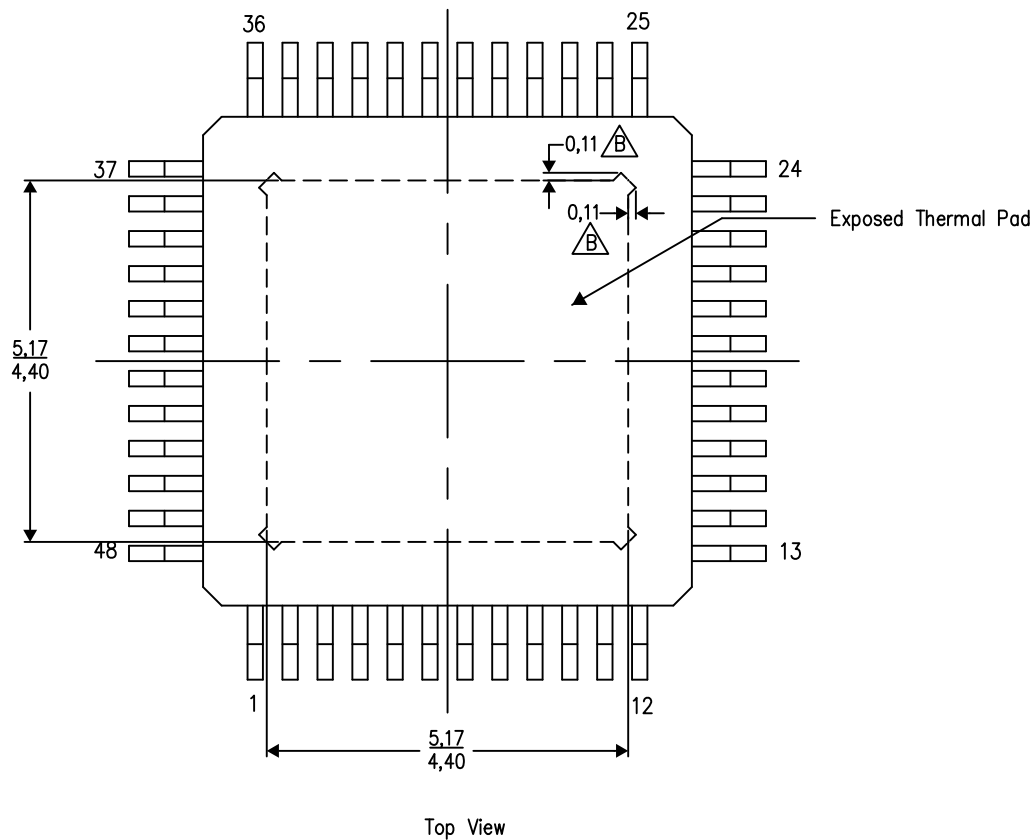
PowerPAD™ PLASTIC QUAD FLATPACK

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206329-7/P 03/15

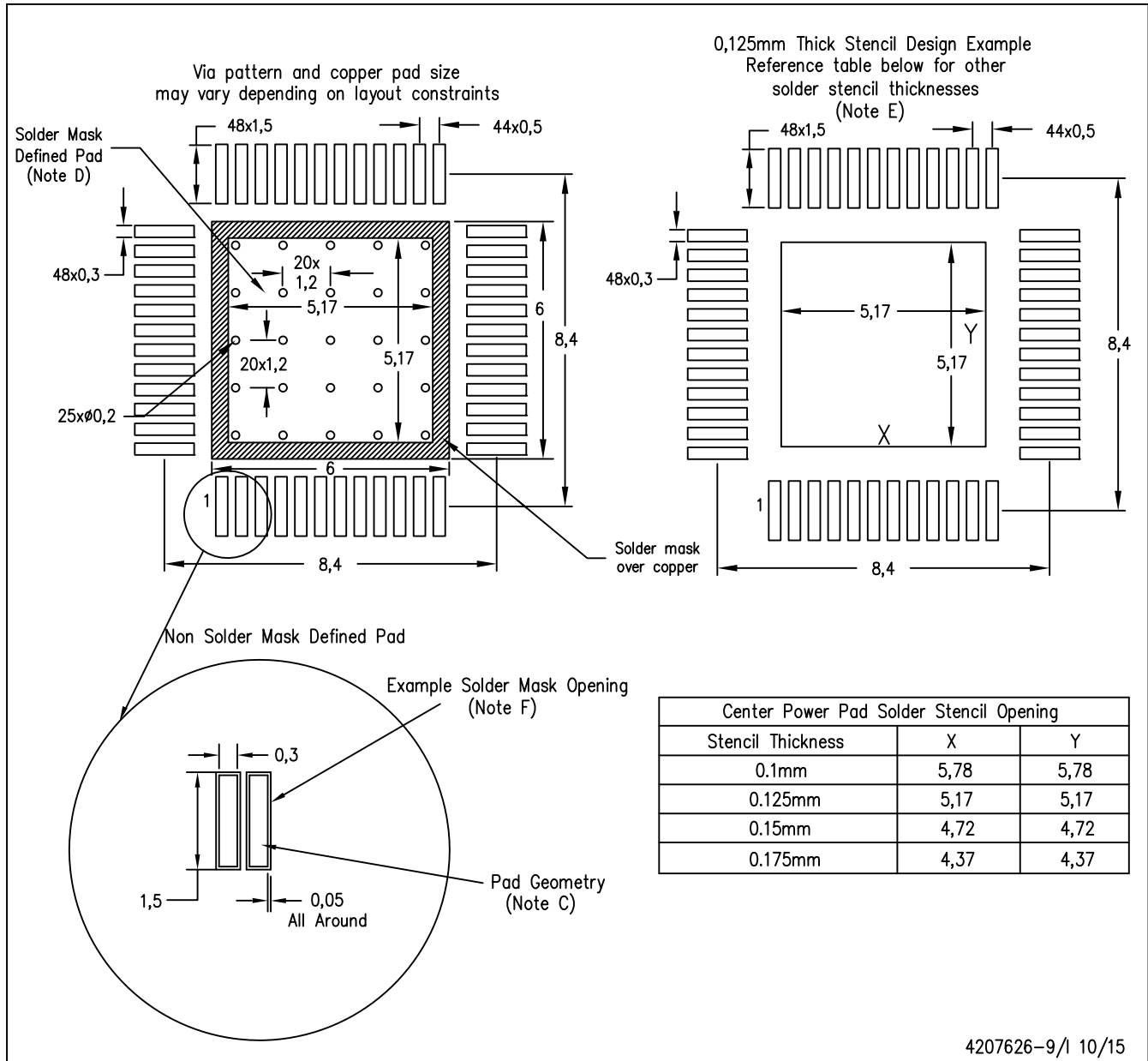
NOTE: A. All linear dimensions are in millimeters

 Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PHP (S-PQFP-G48)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting options for vias placed in the thermal pad.

PowerPAD is a trademark of Texas Instruments

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.