20W STEREO DIGITAL AMPLIFIER POWER STAGE

FEATURES

- **Supports Multiple Output Configurations**
  - **2×20-W into a 8-Ω BTL Load at 18 V**
  - **4×10-W into a 4-Ω SE Load at 18 V**
  - **2×10W (SE) + 1×20W (BTL) at 18 V**
- **Thermally Enhanced Package**
  - **DCA (56-pin HTTSOP)**
- **Wide Voltage Range: 10V–26V**
  - **No Separate Supply Required for Gate Drive**
- **Efficient Class-D Operation Eliminates Need for Heat Sinks**
- **Closed Loop Power Stage Architecture**
  - **Improved PSRR Reduces Power Supply Performance Requirements**
  - **High Damping Factor Provides for Tighter, More Accurate Sound With Improved Bass Response**
  - **Constant Output Power Over Variation in Supply Voltage**
- **Single Ended Inputs**
- **Integrated Self-Protection Circuits Including Overvoltage, Undervoltage, Overtemperature, and Short Circuit With Error Reporting**

APPLICATIONS

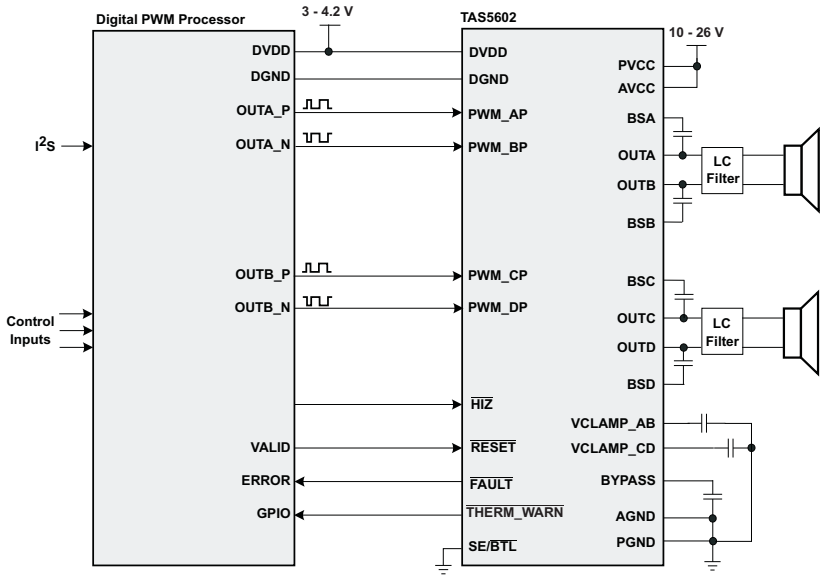
- **Flat-Panel, Rear-Projection, and CRT TV**
- **Consumer Audio Applications**

DESCRIPTION

The TAS5602 is a 20-W (per channel) efficient, stereo digital amplifier power stage for driving 4 single-ended speakers, 2 bridge-tied speakers, or combination of single and bridge-tied loads. The TAS5602 can drive a speaker with an impedance as low as 4Ω. The high efficiency of the TAS5602 eliminates the need for an external heat sink.

A simple interface to a digital audio PWM processor is shown below. The TAS5602 is fully protected against faults with short-circuit protection and thermal protection as well as overvoltage and undervoltage protection. Faults are reported back to the processor to prevent devices from being damaged during overload conditions.

SIMPLIFIED APPLICATION CIRCUIT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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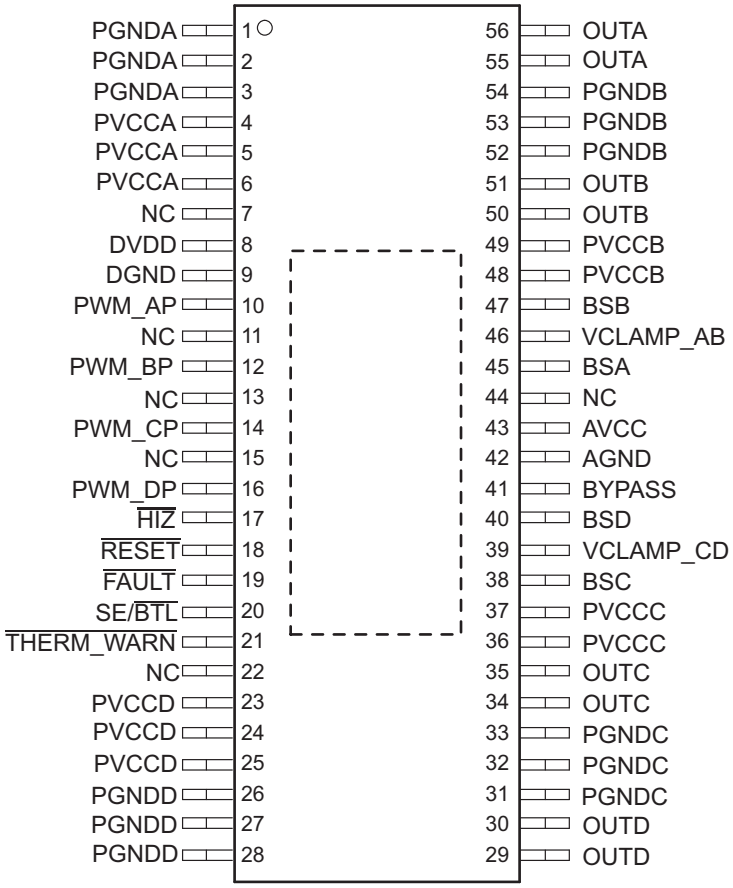
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PINOUT

DCA PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NO.	NAME		
40	BSD	I/O	Bootstrap I/O for channel D high-side FET
39	VCLAMP_CD	–	Internally generated voltage supply for channel C and D bootstrap. Not to be used as a supply or connected to any component other than the decoupling capacitor.
38	BSC	I/O	Bootstrap I/O for channel C high-side FET
43	AVCC	–	Analog power supply
42	AGND		Analog ground
8	DVDD	I	Digital supply (3V–4.2V). Supply for PWM input signal conditioning, $\overline{\text{FAULT}}$ and $\overline{\text{RST}}$ I/O buffers
9	DGND	I	Ground reference input for PWM and digital inputs
10	PWM_AP	I	Positive audio signal PWM input for channel A
12	PWM_BP	I	Positive audio signal PWM input for channel B
14	PWM_CP	I	Positive audio signal PWM input for channel C
16	PWM_DP	I	Positive audio signal PWM input for channel D

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TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NO.	NAME		
17	$\overline{\text{HIZ}}$	–	Forces the output to high impedance state. Use this terminal to quickly (<1 ms) disable the output switching in cases like power fail. If $\overline{\text{HIZ}}$ is tied to $\overline{\text{RESET}}$, the volume ramps up slowly at start-up, but the output switching is stopped quickly at power down. $\overline{\text{HIZ}}$ = High, normal operation. HIZ = Low, the outputs held in high impedance state. No switching at output.
18	$\overline{\text{RESET}}$	I	Enable/Disable pin. Use this terminal for pop-free start/stop. $\overline{\text{RESET}}$ = High, normal operation $\overline{\text{RESET}}$ = Low, held in reset mode
19	$\overline{\text{FAULT}}$	O	Short circuit fault $\overline{\text{FAULT}}$ = High, normal operation $\overline{\text{FAULT}}$ = Low, short circuit at output detected. $\overline{\text{FAULT}}$ will latch if short circuit detected and will be reset if the $\overline{\text{RESET}}$ pin is pulled low or the VCC power supplies are turned off. Thermal fault will not be reported by the $\overline{\text{FAULT}}$ pin.
20	SE/$\overline{\text{BTL}}$	I	Single-ended or Bridge-tied output select terminal. If any output is configured as a single-ended load, this pin should be connected to DVDD. For 2-channel, BTL operation, connect to GND.
21	$\overline{\text{THERM_WARN}}$	O	Thermal warning output flag. $\overline{\text{THERM_WARN}}$ = HIGH, normal operation. $\overline{\text{THERM_WARN}}$ = LOW, die temperature has reached 125 deg. C. Automatically resets when temperature falls back to normal range. TTL compatible push-pull output.
41	BYPASS	O	VCC/8 reference for analog cells
47	BSB	I/O	Bootstrap I/O for channel B high-side FET
46	VCLAMP_AB	–	Internally generated voltage supply for channel A and B bootstrap. Not to be used as a supply or connected to any component other than the decoupling capacitor.
45	BSA	I/O	Bootstrap I/O for channel A high-side FET
4–6	PVCCA	–	Positive power supply for channel A output
55, 56	OUTA	O	Channel A = H-bridge output
1–3	PGNDA	–	Power ground reference for channel A output
48, 49	PVCCB	–	Positive power supply for channel B output
52–54	PGNDB	–	Power ground reference for channel B output
50, 51	OUTB	O	Channel B = H-bridge output
34, 35	OUTC	O	Channel C = H-bridge output
31–33	PGNDC	–	Power ground reference for channel C output
36, 37	PVCCC	–	Positive power supply for channel C output
26–28	PGNDD	–	Power ground reference for channel D output
29, 30	OUTD	O	Channel D = H-bridge output
23–25	PVCCD	–	Positive power supply for channel D output
7, 11, 13, 15, 22, 44	NC	–	No internal connection.
–	Thermal Pad		Connect to PGNDx

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
Supply Voltage	DV_{DD}	–0.3 to 5	V
	AV_{CC}, PV_{CC}	–0.3 to 30	V
Input Voltage	$\overline{RESET}$, SE/$\overline{BTL}$, PWM_xP, PWM_xN	–0.3 to DV_{DD} + 0.3	V
Operating free-air temperature, T_A		–40 to 85	°C
Operating junction temperature range, T_J		–40 to 150	°C
Storage temperature range, T_{stg}		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE(1)	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
DCA (56 pin HTSSOP)	5.5 W	44 mW/°C	3.52 W	2.86 W

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		PVCCx, AVCC (minimum series inductance of 5uH for full output short circuit protection)	10		26	V
		PVCCx, AVCC (output is fully protected from shorts with no inductance between short and terminal)	10		20	
Digital reference voltage		DVDD	3	3.3	4.2	V
High-level input voltage, V_{IH}		PWM_xx, $\overline{RESET}$, SE/ $\overline{BTL}$, $\overline{HIZ}$	2			V
Low-level input voltage, V_{IL}		PWM_xx, $\overline{RESET}$, SE/ $\overline{BTL}$, $\overline{HIZ}$			0.8	V
High-level output voltage, V_{OH}		$\overline{FAULT}$, $\overline{THERM_WARN}$, I_{OH} = 10 µA	DVDD–0.4V			V
Low-level output voltage, V_{OL}		$\overline{FAULT}$, $\overline{THERM_WARN}$, I_{OL} = –10 µA			DGND+0.4V	V
PWM input frequency, f_{PWM}		PWM_xx	200		400	kHz
Operating free-air temperature, T_A			–40		85	°C
R_L(BTL)	Load Impedance	Output filter: L= 22 µH, C = 680 nF	6.0	8		Ω
R_L(SE)			3.2	4		
R_L(PBTL)			3.2			
Lo(BTL)	Output-filter Inductance	Minimum output inductance under short-circuit condition		10		µH
Lo (SE)				10		
Lo (PBTL)				10		

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DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 24 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured with respect to $V_{CC}/2$ for SE and output-to-output for BTL)	50% duty cycle PWM at PWM_xx inputs			26	80	mV
V_{BYPASS}	$V_{CC}/8$ reference for analog section	No load			$V_{CC}/8$		V
I_{IH}	High-level input current	PWM_xx, $\overline{RESET}$, SE/$\overline{BTL}$, $\overline{HIZ}$, V_I = DVDD, DVDD = 5 V				5	µA
I_{IL}	Low-level input current	PWM_xx, $\overline{RESET}$, SE/$\overline{BTL}$, $\overline{HIZ}$, V_I = 0, DVDD = 5 V				5	µA
I_{DVDD}	DVDD supply current	$\overline{RESET}$ = 2.0 V, DVDD = 3.3 V, No load			20	50	µA
I_{CC}	Quiescent supply current	$\overline{RESET}$ = 2.0 V No load, PV_{CC} = 18 V		19	35	60	mA
$I_{CC(RESET)}$	Quiescent supply current in reset mode	$\overline{RESET}$ = 0.8 V, No load, PV_{CC} = 18 V			64	216	µA
$R_{DS(on)}$	Drain-source on-state resistance	VCC = 24 V, Io = 500 mA, T_J = 25°C, includes metallization resistance	High side		240		mΩ
			Low side		240		
			Total		480		
t_{ON}	Turn-on time (SE mode), voltage on BYPASS pin reaches final value of PVCC/8	$C_{(BYPASS)}$ = 1µF, $\overline{RESET}$ = 2 V, SE/$\overline{BTL}$ = 2V			800		ms
	Turn-on time (BTL mode) , voltage on BYPASS pin reaches final value of PVCC/8	$C_{(BYPASS)}$ = 1µF, $\overline{RESET}$ = 2 V, SE/$\overline{BTL}$ = 0.8 V			420		
t_{OFF}	Turn-off time (SE mode), voltage on BYPASS pin reaches final value of PVCC/8	$C_{(BYPASS)}$ = 1 µF, $\overline{RESET}$ = 0.8 V, SE/$\overline{BTL}$ = 2 V			800		ms
	Turn-off time (BTL mode) , voltage on BYPASS pin reaches final value of PVCC/8	$C_{(BYPASS)}$ = 1 µF, $\overline{RESET}$= 0.8 V, SE/$\overline{BTL}$ = 0.8 V			50		
$t_{on/off}$	Turn-on and turn-off time when $\overline{HIZ}$ goes low				<1		ms

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured with respect to $V_{CC}/2$ for SE and output-to-output for BTL)	50% duty cycle PWM at PWM_xx inputs			26	80	mV
$\lvert V_{OS\ start\text{-}up} \rvert$	Class-D Start-up output offset voltage	50% duty cycle PWM at PWM_xx inputs. V_{Bypass} = 0.75V			30	100	mV
V_{BYPASS}	$V_{CC}/8$ reference for analog section	No load			$V_{CC}/8$		V
I_{DVDD}	DVDD supply current	$\overline{RESET}$ = 2.0 V, DVDD = 3.3 V, No load			20	50	µA
I_{CC}	Quiescent supply current	$\overline{RESET}$ = 2.0 V, No load		14	28	51	mA
$I_{CC(RESET)}$	Quiescent supply current in reset mode	$\overline{RESET}$ = 0.8 V, No load			64	216	µA
$R_{DS(on)}$	Drain-source on-state resistance	VCC = 12 V, Io = 500 mA, T_J = 25°C, includes metallization resistance	High side		240		mΩ
			Low side		240		
			Total		480		
t_{ON}	Turn-on time (SE mode), voltage on BYPASS pin reaches final value of PVCC/8	$C_{(BYPASS)}$ = 1µF, $\overline{RESET}$ = 2 V, SE/$\overline{BTL}$ = 2V			800		ms
	Turn-on time (BTL mode), voltage on BYPASS pin reaches final value of PVCC/8	$C_{(BYPASS)}$ = 1µF, $\overline{RESET}$ = 2 V, SE/$\overline{BTL}$ = 0.8 V			420		
t_{OFF}	Turn-off time (SE mode), voltage on BYPASS pin reaches final value of PVCC/8	$C_{(BYPASS)}$ = 1 µF, $\overline{RESET}$ = 0.8 V, SE/$\overline{BTL}$ = 2 V			800		ms
	Turn-off time (BTL mode), voltage on BYPASS pin reaches final value of PVCC/8	$C_{(BYPASS)}$ = 1 µF, $\overline{RESET}$= 0.8 V, SE/$\overline{BTL}$ = 0.8 V			50		
$t_{on/off}$	Turn-on and turn-off time when $\overline{HIZ}$ goes low				<1		ms

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AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 24 V, R_L = 8Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Supply Ripple Rejection	200 mV_{PP} ripple at 20 Hz–20 kHz, BTL 50% duty cycle PWM at inputs		–60		dB
P_O	Continuous output power	BTL – R_L = 8Ω, THD+N = 7%, f = 1 kHz, V_{CC} = 18 V		20		W
		SE – R_L = 4Ω, THD+N = 10%, f = 1 kHz, V_{CC} = 24 V		19		
THD+N	Total Harmonic Distortion + Noise (SE)	V_{CC} = 24 V, f = 1 kHz, P_O = 10 W		0.08%		
	Total Harmonic Distortion + Noise (BTL)	V_{CC} = 18 V, R_L = 8Ω, f = 1 kHz, Po = 10 W (half-power)		0.04%		
V_n	Output Integrated Noise	20 Hz to 22 kHz, A-weighted filter, BD modulation		125		µV
				–78		dBv
	Crosstalk	Po = 1 W, f = 1 kHz		–70		dB
SNR	Signal-to-noise ratio	Max. Output at THD+N <1%, f = 1 kHz, A-weighted, V_{CC} = 18 V		99		dB
	Thermal trip point (output shutdown, unlatched fault)			150		°C
	Thermal warning trip ($\overline{\text{THERM_WARN}}$ = Low)			125		°C
	Thermal hysteresis			20		°C
t_r	PWM Input rise time	PWM_xx pins			5	ns
t_f	PWM Input fall time	PWM_xx pins			5	ns

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 12 V, R_L = 8Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Supply Ripple Rejection	200 mV_{PP} ripple at 20 Hz–20 kHz, BTL 50% duty cycle PWM at inputs		–60		dB
P_O	Continuous output power	BTL – R_L = 8Ω, THD+N = 10%, f = 1 kHz,		9.5		W
		SE – R_L = 4Ω, THD+N = 10%, f = 1 kHz,		4.5		
THD+N	Total Harmonic Distortion + Noise (SE)	V_{CC} = 12 V, f = 1 kHz, P_O = 2 W (half-power)		0.04 %		
	Total Harmonic Distortion + Noise (BTL)	V_{CC} = 12 V, R_L = 8Ω, f = 1 kHz, P_O = 5 W (half-power)		0.07 %		
V_n	Output Integrated Noise	20 Hz to 22 kHz, A-weighted filter, BD modulation		125		µV
				–78		dBv
	Crosstalk	P_O = 1 W, f = 1 kHz		–70		dB
SNR	Signal-to-noise ratio	Max. Output at THD+N <1%, f = 1 kHz, A-weighted		96		dB
	Thermal trip point (output shutdown, unlatched fault)			150		°C
	Thermal warning trip ($\overline{\text{THERM_WARN}}$ = Low)			125		°C
	Thermal hysteresis			20		°C
t_r	PWM Input rise time	PWM_xx pins			5	ns
t_f	PWM Input fall time	PWM_xx pins			5	ns

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APPLICATION CIRCUITS

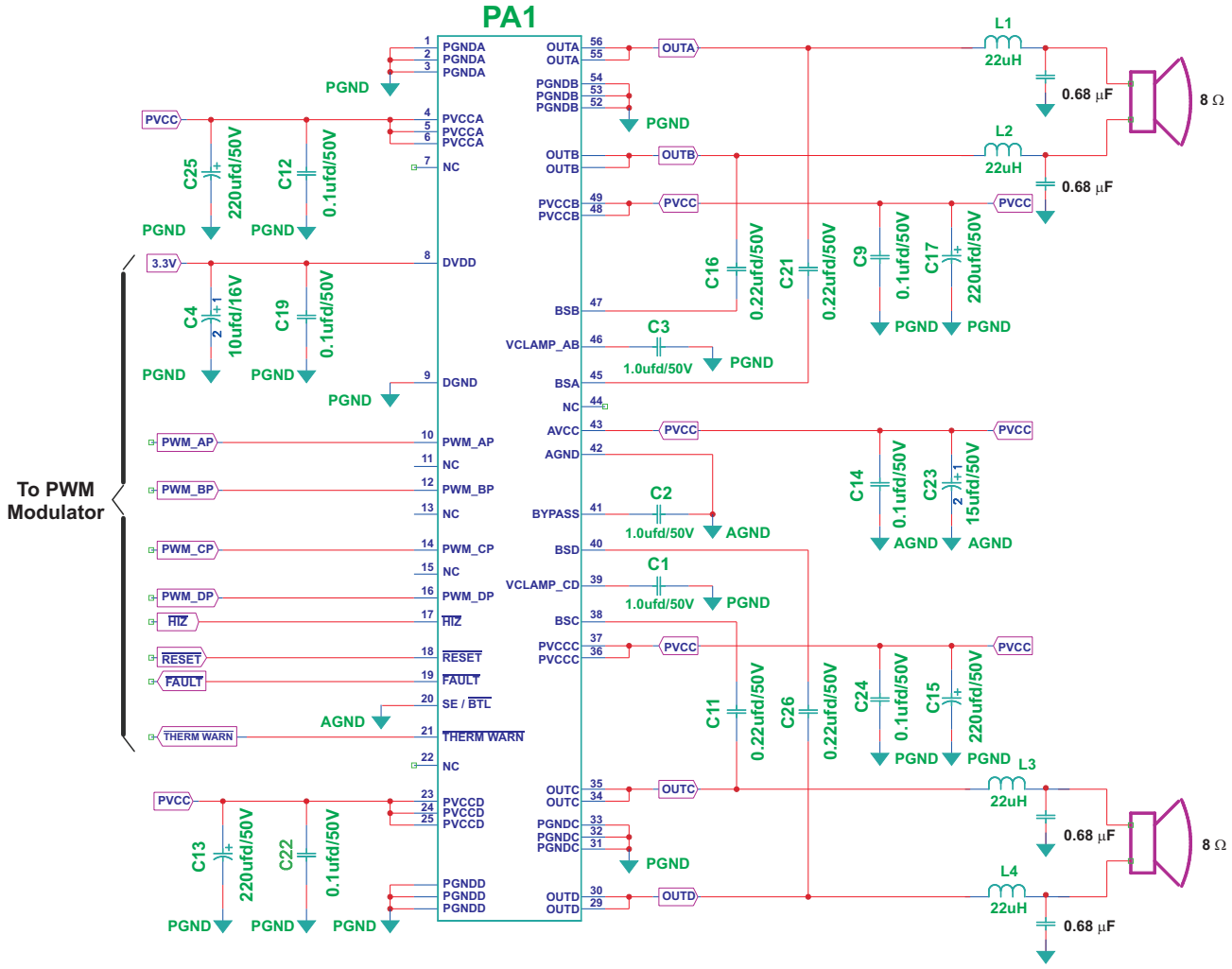


Figure 1. Bridge Tied Load (BTL) Application Schematic

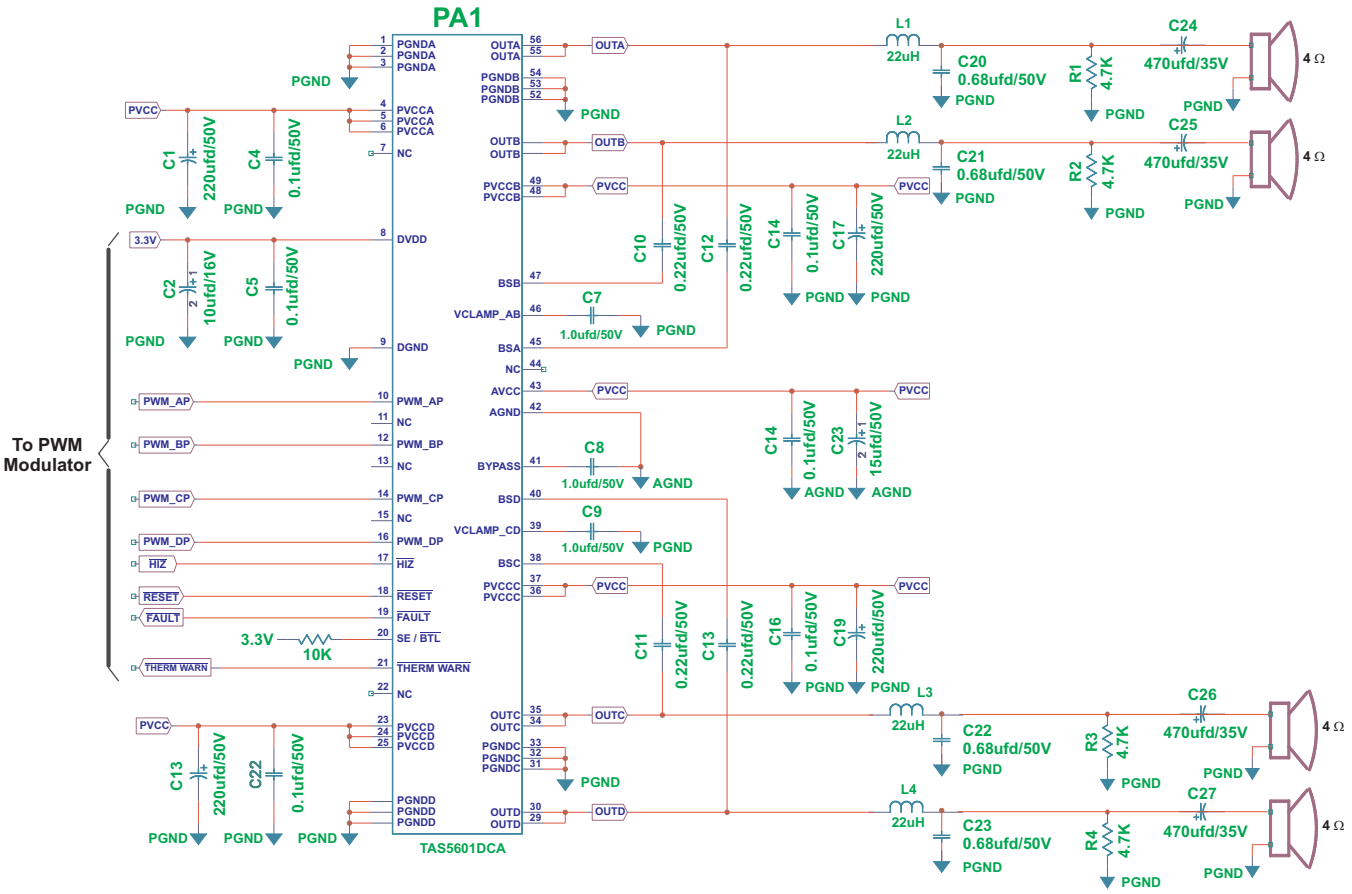


Figure 2. Single Ended (SE) Application Schematic

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TYPICAL CHARACTERISTICS

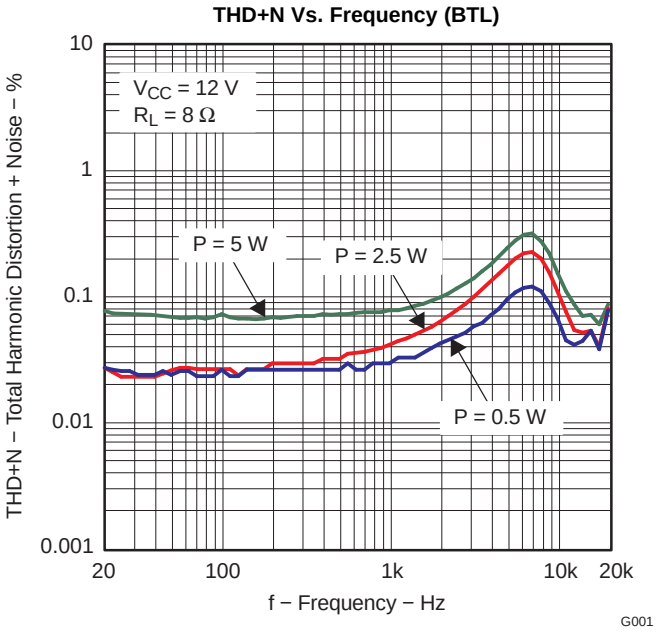


Figure 3.

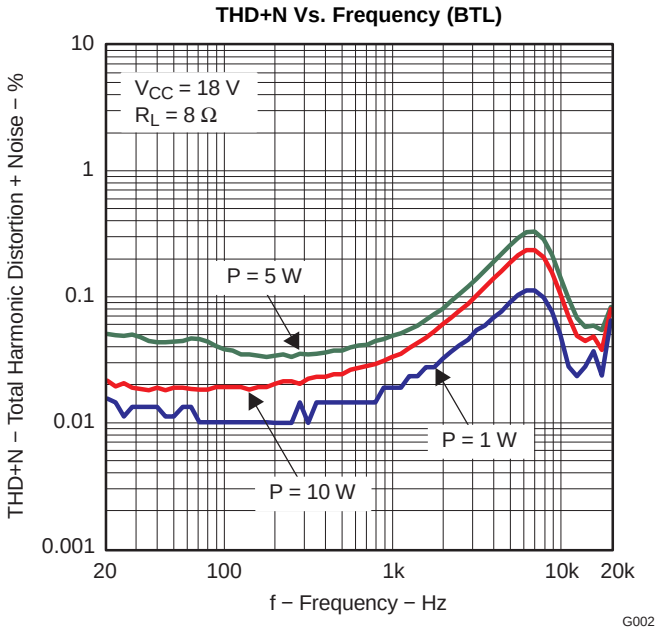


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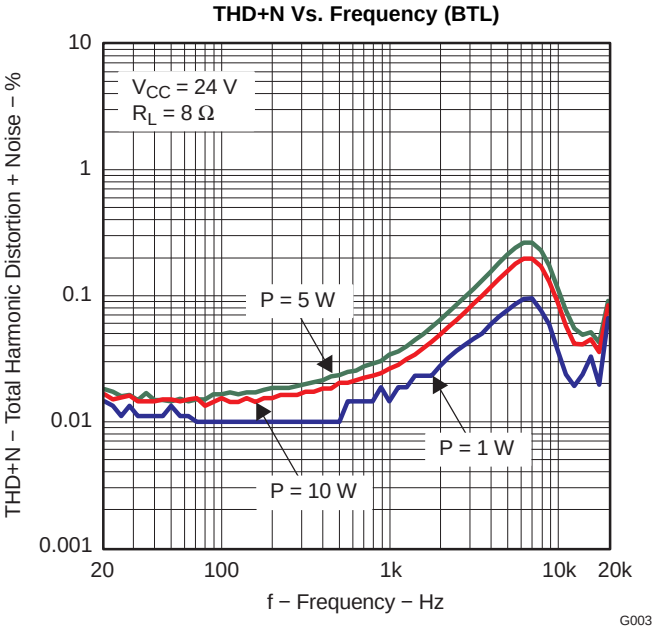


Figure 5.

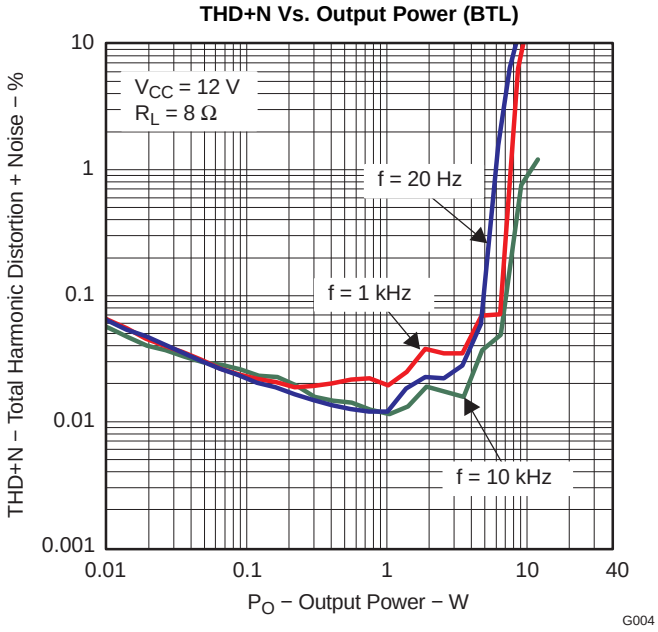


Figure 6.

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TYPICAL CHARACTERISTICS (continued)

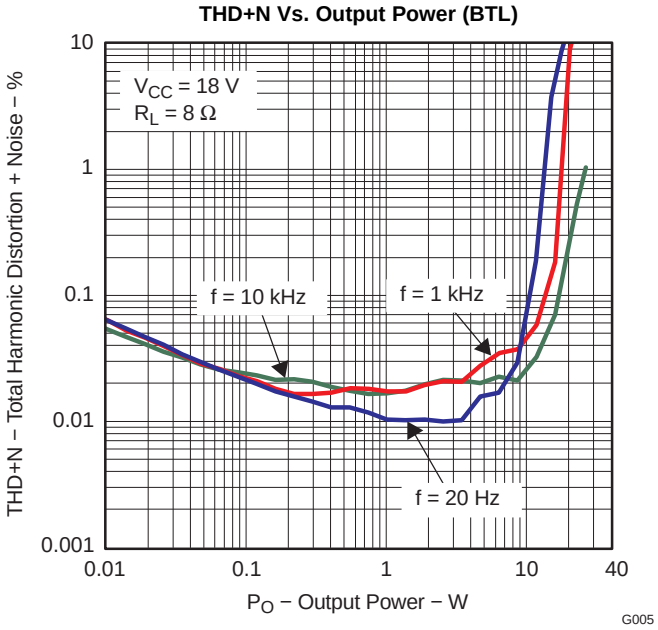


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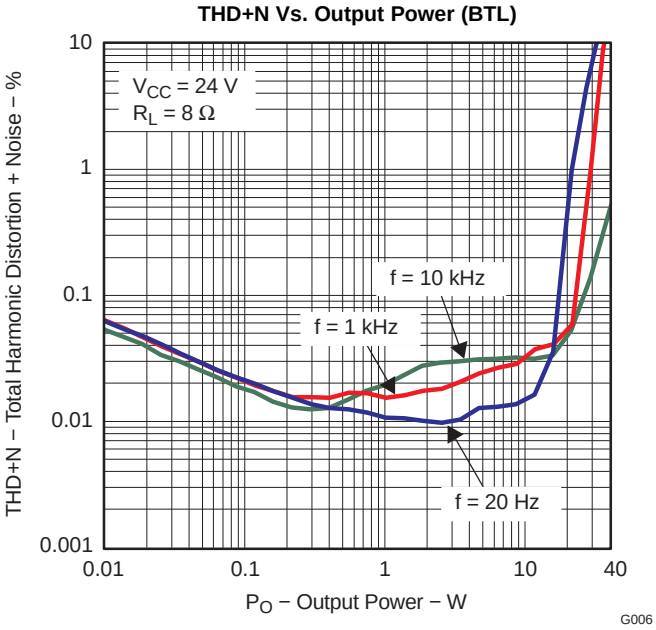


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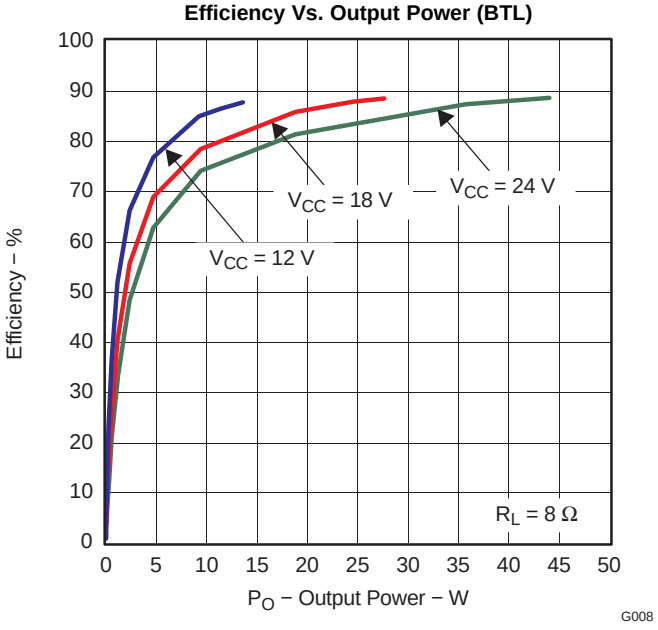


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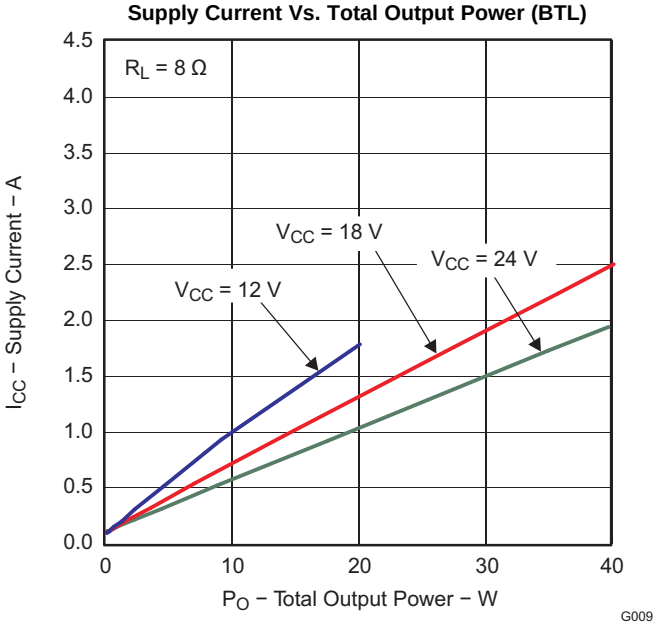


Figure 10.

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TYPICAL CHARACTERISTICS (continued)

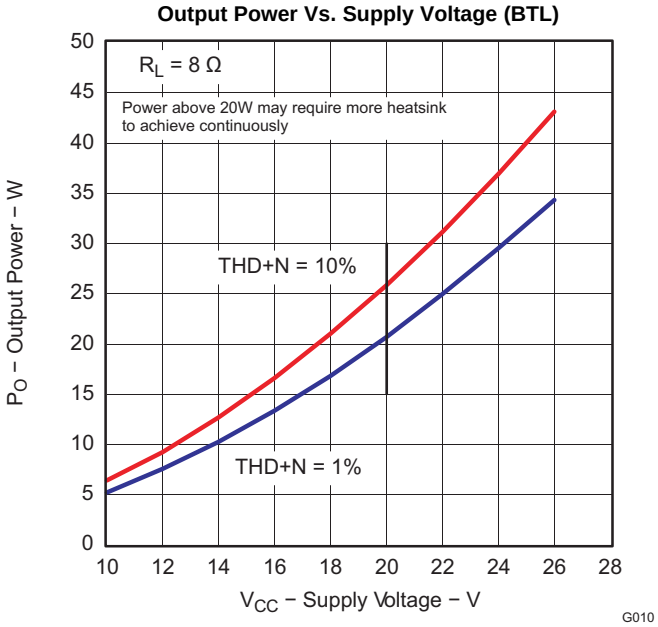


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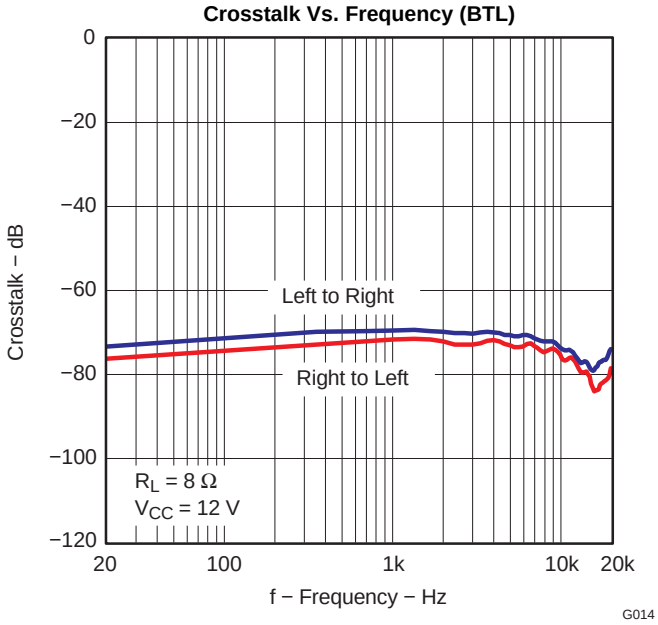


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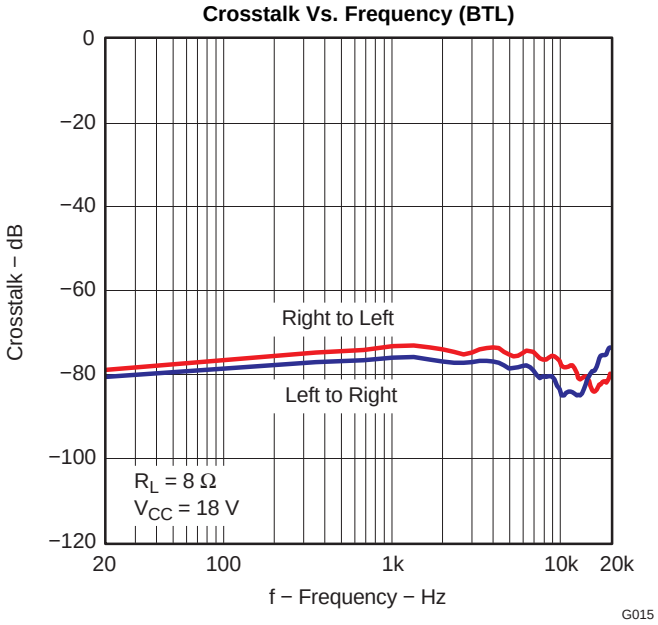


Figure 13.

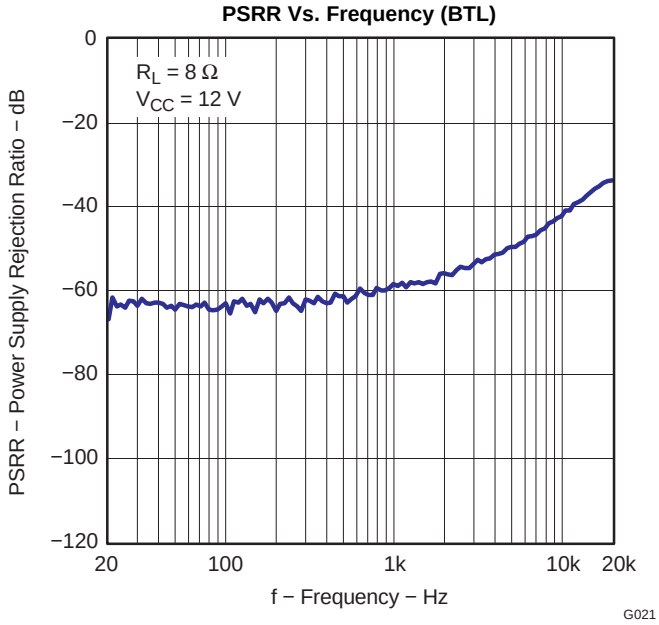


Figure 14.

TYPICAL CHARACTERISTICS (continued)

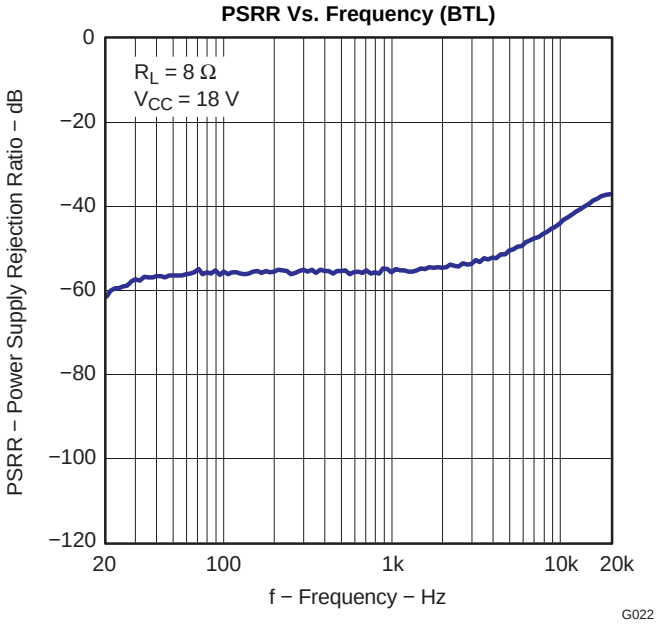


Figure 15.

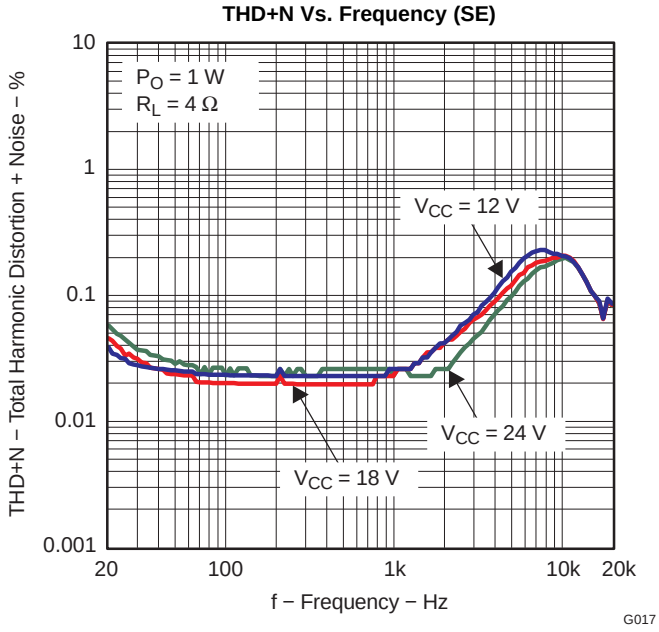


Figure 16.

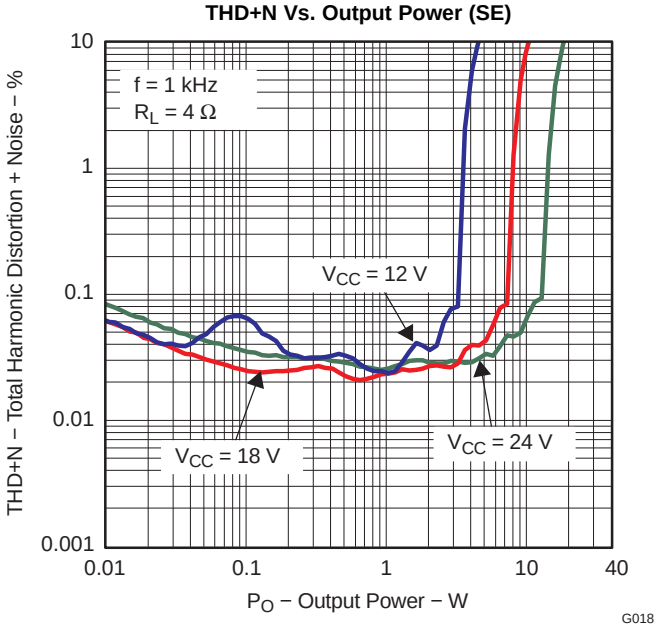


Figure 17.

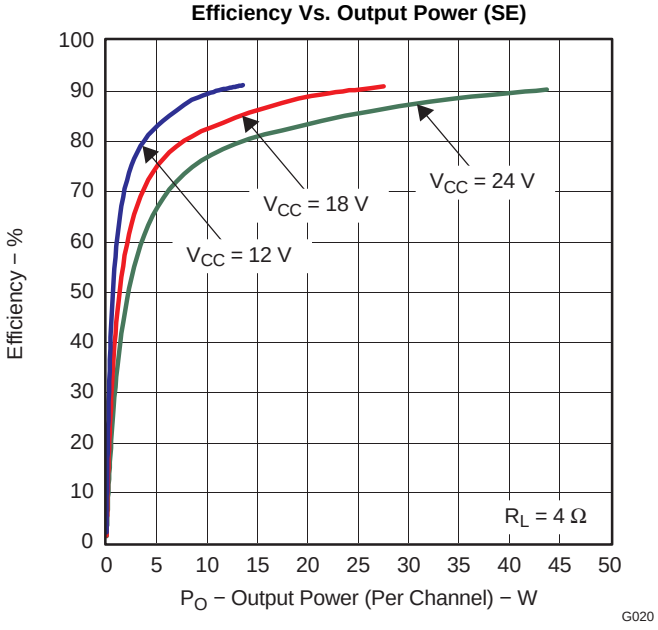


Figure 18.

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TYPICAL CHARACTERISTICS (continued)

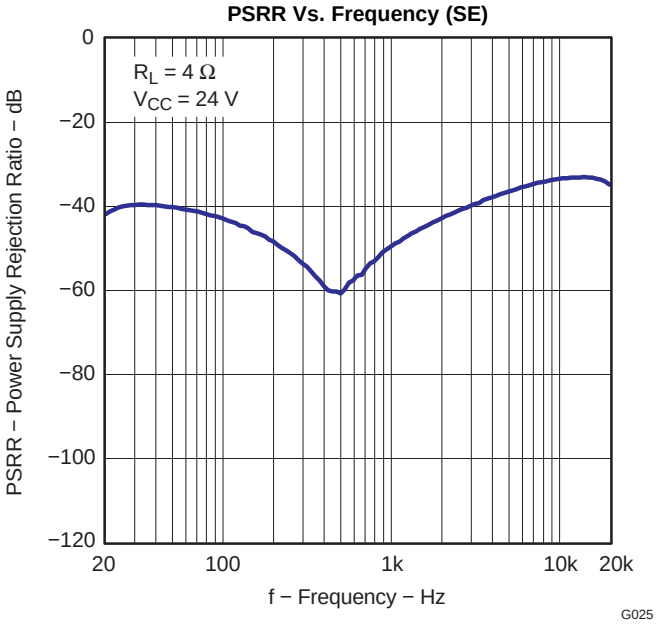


Figure 19.

APPLICATION INFORMATION

CLOSED-LOOP POWER STAGE CHARACTERISTICS

The TAS5602 is PWM input power stage with a closed loop architecture. A 2nd order feedback loop varies the PWM output duty cycle with changes in the supply voltage. This ensures that the output voltage (and output power) remain the same over transitions in the power supply.

Open-loop power stages have an output duty cycle that is equal to the input duty cycle. Since the duty cycle does NOT change to compensate for changes in the supply voltage, the output voltage (and power) change with supply voltage changes. This is undesirable effect that closed-loop architecture of the TAS5602 solves.

The single-ended (SE) gain of the TAS5602 is fixed, and specified below:

TAS5602 Gain = 0.13 / Modulation Level (Vrms/%)

Modulation level = fraction of full-scale modulation of the PWM signal at the input of the power stage.

TAS5602 (SE) Voltage Level (in Vrms) = 0.13 x Modulation Level

The bridge-tied (BTL) gain of the TAS5602 is equal to 2x the SE gain:

TAS5602 (BTL) Voltage Level (in Vrms) = 0.26 x Modulation Level

For a digital modulator like the TAS5706, the default maximum modulation limit is 97.7%. For a full scale input, the PWM output switches between 2.3% and 97.7%. This equates to a modulation level of 95.4% for a full scale input (0 dBFS).

For example, calculate the output voltage in RMS volts given a –20 dBFS signal to a digital modulator with a maximum modulation limit of 97.7% in a BTL output configuration:

TAS5602 Output Voltage = 0.1 (–20dB) x 0.26 (Gain) x 95.4 (Modulation Level)

= 2.48 Vrms

It is also important to maintain a switching signal at the PWM inputs of the TAS5602 while the $\overline{\text{RESET}}$ terminal is held HIGH (>1.9V). If a switching signal is not maintained on the inputs under the previous condition, a loud “pop” can occur in the speaker. The TAS5602 is not compatible with modulators that hard mute the outputs (output go to LOW-LOW state). For MUTE case, the modulator needs to hold outputs switching at 50% duty cycle.

For power-up, ensure that the PWM inputs are switching before $\overline{\text{RESET}}$ is transitioned HIGH (>1.9V). For shutdown and power-down, the PWM inputs should remain switching for the “turn-off” time specified in the DC Electrical Characteristics table. This ensures the best “pop” performance in the system.

POWER SUPPLIES

To allow simplified system design, the TAS5602 requires only a single supply (PVCC) for the power blocks and a 3.3 V (DVDD) supply for PWM input blocks. In addition, the high-side gate drive is provided by built-in bootstrap circuits requiring only an external capacitor for each half-bridge.

In order for the bootstrap circuit to function properly, it is necessary to connect a small ceramic capacitor from each bootstrap pin (BS_) to the corresponding output pin (OUT_). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate drive.

DEVICE PROTECTION SYSTEM

The TAS5602 contains a complete set of protection circuits carefully designed to make system design efficient as well as to protect the device against any kind of permanent failures due to short circuits, overload, overtemperature, and undervoltage.

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TAS5602 Fault timing chart

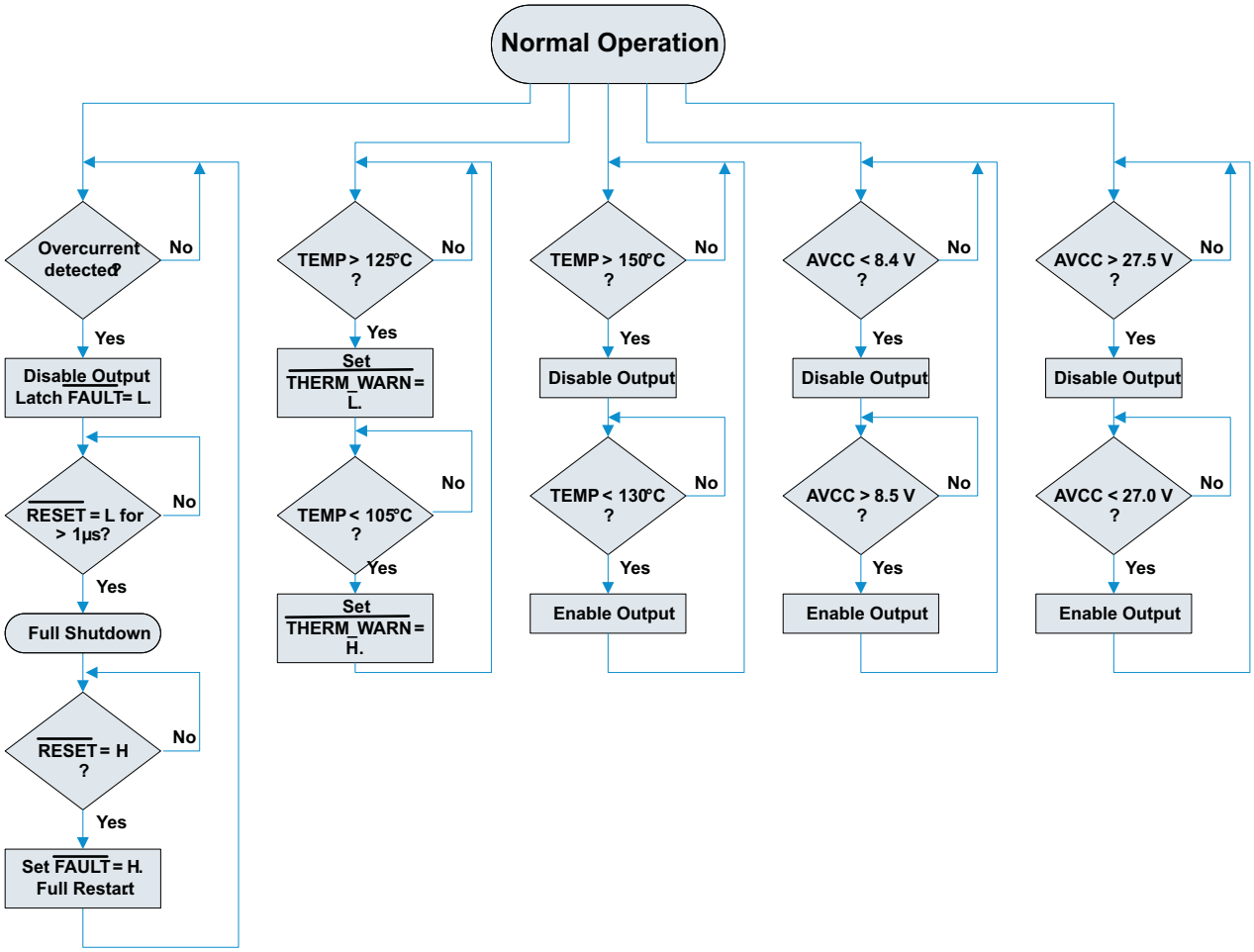


Figure 20. Device Protection Flow Chart

Protection Mechanisms in the TAS5602

- SCP (short-circuit protection, OCP) protects against shorts across the load, to GND, and to PVCC.
- OTP turns off the device if T_{die} (typical) > 150°C.
- UVP turns off the device if PVCC (typical) < 8.4 V
- OVP turns off the device if PVCC (typical) > 27.5 V

Single-Ended Output Capacitor, C_O

In single-ended (SE) applications, the dc blocking capacitor forms a high-pass filter with the speaker impedance. The frequency response rolls of with decreasing frequency at a rate of 20 dB/decade. The cutoff frequency is determined by:

$$f_c = = \pi C_O Z_L$$

Table 1 shows some common component values and the associated cutoff frequencies:

Table 1. Common Filter Responses

Speaker Impedance (Ω)	C_{SE} – DC Blocking Capacitor (μF)		
	f_c = 60 Hz (–3 dB)	f_c = 40 Hz (–3 dB)	f_c = 20 Hz (–3 dB)
4	680	1000	2200
8	330	470	1000

Output Filter and Frequency Response

For the best frequency response, a flat-passband output filter (second-order Butterworth) may be used. The output filter components consist of the series inductor and capacitor to ground at the output pins. There are several possible configurations, depending on the speaker impedance and whether the output configuration is single-ended (SE) or bridge-tied load (BTL). Table 2 lists the recommended values for the filter components. It is important to use a high-quality capacitor in this application. A rating of at least X7R is required.

Table 2. Recommended Filter Output Components

Output Configuration	Speaker Impedance (Ω)	Filter Inductor (μH)	Filter Capacitor (nF)
Single Ended (SE)	4	22	680
	8	47	390
Bridge Tied Load (BTL)	4	10	1500
	8	22	680

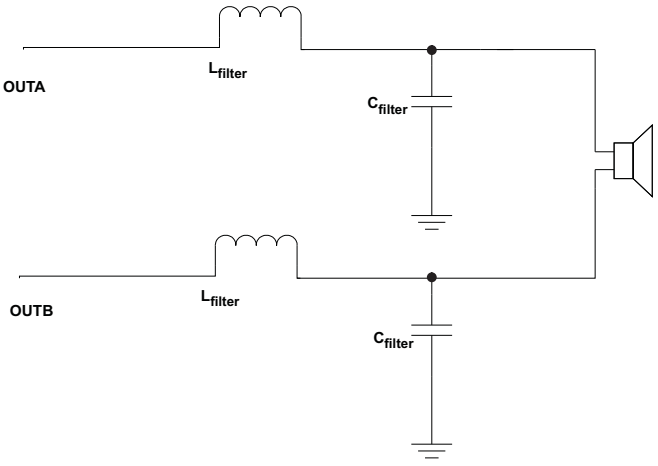


Figure 21. BTL Filter Configuration

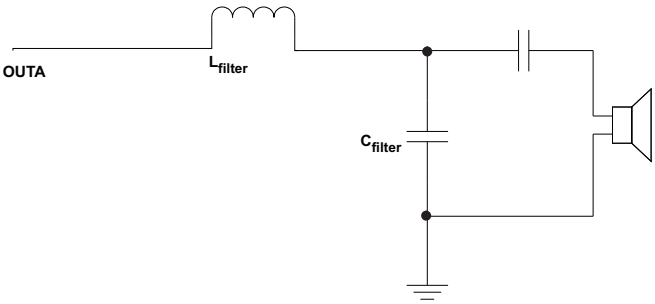


Figure 22. SE Filter Configuration

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Common Mode Resonance

The BTL filter shown above is an excellent, low-cost way to attenuate the high frequency energy from the Class D output stage while passing the audio signal cleanly to the speakers. However, at the resonant frequency of the LC combination, ringing can occur as a common mode output from the amplifier. This ringing can result in resonant frequency energy appearing on the speaker leads and can also cause the power dissipation in the filter L and C to increase.

To keep the common mode ringing to a reasonable level, some series resistance should be designed into the circuit. Testing and simulations have shown that 75 mΩ of series resistance in the path which includes the filter L and C is enough to control the common mode ringing. The series resistance of the filter coil and the ESR of the cap can be used to form the resistance. The copper traces in series with the filter capacitor are another good place to add some series resistance to the circuit.

Another way to improve the common mode ringing is to add an RC network to ground on each output. Testing has shown that a series network consisting of 100Ω and 47 nF is enough to damp the ringing for most speaker systems.

Power-Supply Decoupling, C_S

The TAS5602 is a high-performance CMOS audio amplifier that requires adequate power-supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power-supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power-supply leads. For higher-frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF to 1 μF, placed as close as possible to the device V_{CC} lead works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220 μF or greater placed near the audio power amplifier is recommended. The 220-μF capacitor also serves as local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 220-μF or larger capacitor should be placed on each PVCC terminal. A 10-μF capacitor on the AVCC terminal is adequate. These capacitors must be properly derated for voltage and ripple-current rating to ensure reliability.

BSN and BSP Capacitors

The half H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220-nF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input.

The bootstrap capacitors connected between the BSx pins and their corresponding outputs function as a floating power supply for the high-side N-channel power MOSFET gate-drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

VCLAMP Capacitor

To ensure that the maximum gate-to-source voltage for the NMOS output transistors is not exceeded, one internal regulator clamps the gate voltage. One 1-μF capacitor must be connected from each VCLAMP (terminal) to ground and must be rated for at least 16 V. The voltages at the VCLAMP terminal vary with V_{CC} and may not be used for powering any other circuitry.

VBYP Capacitor Selection

The scaled supply reference (BYPASS) nominally provides an AVCC/8 internal bias for the preamplifier stages. The external capacitor for this reference (C_{BYP}) is a critical component and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts. The start up time is proportional to 0.5 s per microfarad in single-ended mode (SE/$\overline{\text{BTL}}$ = DVDD). Thus, the recommended 1-μF capacitor results in a start-up time of approximately 500 ms (SE/$\overline{\text{BTL}}$ = DVDD). The second function is to reduce noise produced by the power supply caused by coupling with the output drive signal. This noise could result in degraded power-supply rejection and THD+N.

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The circuit is designed for a C_{BYP} value of 1 µF for best pop performance. The input capacitors should have the same value. A ceramic or tantalum low-ESR capacitor is recommended.

SE/$\overline{\text{BTL}}$ CONTROL PIN

If the SE/$\overline{\text{BTL}}$ CONTROL pin is pulled low (tied to ground), the start-up time is typically 420 msec which is optimized for the bridge tied load (BTL) output configuration. If the SE/$\overline{\text{BTL}}$ pin is pulled high, the start-up time is controlled by the V_{BYP} Capacitor as described in the previous section. For a value of C_{BYP} = 1µF, the start-up time is typically 800 msec. This gives a smooth, pop-free startup for single-ended (SE) output stages.

$\overline{\text{HIZ}}$ PIN

The $\overline{\text{HIZ}}$ pin can be used to immediately take the Class D output H Bridges to a Hi-Z state in the case of an unexpected power down situation. This allows the user to control the amplifier turn-off quickly if needed. Use a power supply which drops relatively quickly to pull the $\overline{\text{HIZ}}$ pin low before the PVCC reaches the UVLO voltage of 8.4 V (typ.) to avoid popping at power down.

$\overline{\text{RESET}}$ OPERATION

The TAS5602 employs a RESET mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of nonuse for power conservation. The $\overline{\text{RESET}}$ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling $\overline{\text{RESET}}$ low causes the outputs to ramp to GND and the amplifier to enter a low-current state. Never leave $\overline{\text{RESET}}$ unconnected, because amplifier operation would be unpredictable.

For the best power-up *pop* performance, place the amplifier in the RESET mode prior to applying the power-supply voltage.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

SHORT-CIRCUIT PROTECTION

The TAS5602 has short-circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts and output-to-GND shorts after the filter and output capacitor (at the speaker terminal.) Directly at the device terminals, the protection circuitry prevents damage to device during output-to-output, output-to-ground, and output-to-supply. When a short circuit is detected on the outputs, the part immediately disables the output drive. Normal operation is restored once the fault is cleared by cycling the RESET pin.

The $\overline{\text{FAULT}}$ will transition low when a short is detected. The $\overline{\text{FAULT}}$ pin will be cleared on the rising edge of $\overline{\text{RESET}}$ after $\overline{\text{RESET}}$ is cycled low to high.

THERMAL PROTECTION

Thermal protection on the TAS5602 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 20°C. The device begins normal operation at this point with no external system interaction.

Thermal protection fault is **NOT** reported on the $\overline{\text{FAULT}}$ terminal.

A $\overline{\text{THERM_WARN}}$ terminal can be used to monitor when the internal device temperature reaches 125°C. The terminal will transition low at this point and transition back high after the device cools approximately 20°C. It is not necessary to cycle $\overline{\text{RESET}}$ to clear this warning flag.

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THERMAL AND PACKAGE INFORMATION

The TAS5602DCA package is the DCA 56-pin TSSOP package. To estimate the junction temperature using measurable parameters, a thermal metric θ_{JT} is modeled, which relates the temperature at the top of the package to the junction temperature, T_J. For TAS5602DCA, θ_{JT} = 0.212 °C/W. If the temperature of the top of the case, T_C , and the Power in and out of the device are known, the junction temperature can be calculated by:

$$T_J = T_C + (\theta_{JT} \times (P_{IN} - P_O))$$

See the Texas Instruments application report *PowerPad™ Thermally Enhanced Package* (literature number SLMA002B) for more information regarding the proper use of the PowerPAD package. Also, see the Texas Instruments application report *IC Package Thermal Metrics* (literature number SPRA953A) for information regarding thermal metrics such as θ_{JT}.

PRINTED-CIRCUIT BOARD (PCB) LAYOUT

Because the TAS5602 is a class-D amplifier that switches at a high frequency, the layout of the printed-circuit board (PCB) should be optimized according to the following guidelines for the best possible performance.

- Decoupling capacitors—The high-frequency 0.1-µF decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. The BYPASS capacitor and VCLAMP_XX capacitors should also be placed as close to the device as possible. Large (220-µF or greater) bulk power-supply decoupling capacitors should be placed near the TAS5602 on the PVCCx terminals. For single-ended operation, a 220 µF capacitor should be placed on each PVCC pin. For Bridge-tied operation, a single 220 µF, capacitor can be shared between A and B or C and D.
- Grounding—The AVCC decoupling capacitor and BYPASS capacitor should each be grounded to analog ground (AGND). The PVCCx decoupling capacitors and VCLAMP_xx capacitors should each be grounded to power ground (PGND). Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the TAS5602.
- Output filter—The reconstruction LC filter should be placed as close to the output terminals as possible for the best EMI performance. The capacitors should be grounded to power ground.
- Thermal pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land are described in the mechanical section at the back of the data sheet. See TI Technical Briefs SLMA002 and SLOA120 for more information about using the thermal pad. For recommended PCB footprints, see figures at the end of this data sheet.

For an example layout, see the TAS5602 Evaluation Module (TAS5602EVM) User Manual, (SLOU189). Both the EVM user manual and the thermal pad application note are available on the TI Web site at http://www.ti.com.

BASIC MEASUREMENT SYSTEM

This section focuses on methods that use the basic equipment listed below:

- Audio analyzer or spectrum analyzer
- Digital multimeter (DMM)
- Oscilloscope
- Twisted-pair wires
- Signal generator
- Power resistor(s)
- Linear regulated power supply
- Filter components
- EVM or other complete audio circuit

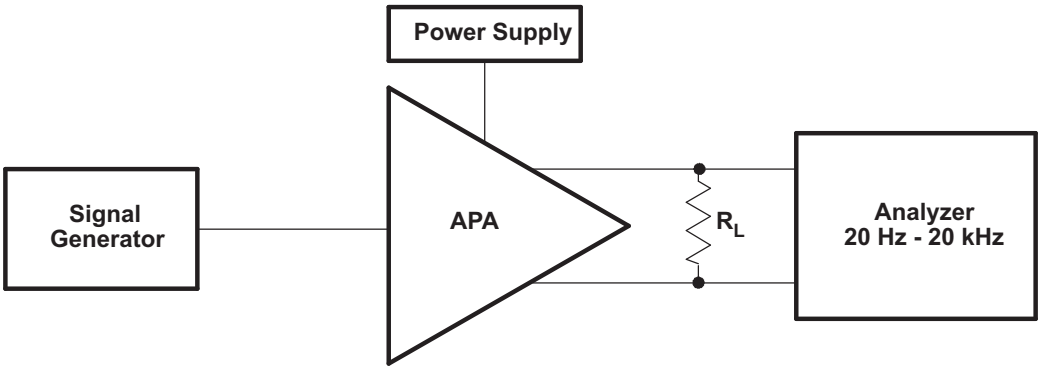
Figure 23 shows the block diagrams of basic measurement systems for class-AB and class-D amplifiers. A sine wave is normally used as the input signal because it consists of the fundamental frequency only (no other harmonics are present). An analyzer is then connected to the audio power amplifier (APA) output to measure the voltage output. The analyzer must be capable of measuring the entire audio bandwidth. A regulated dc power supply is used to reduce the noise and distortion injected into the APA through the power pins. A System Two™ audio measurement system (AP-II) by Audio Precision™ includes the signal generator and analyzer in one package.

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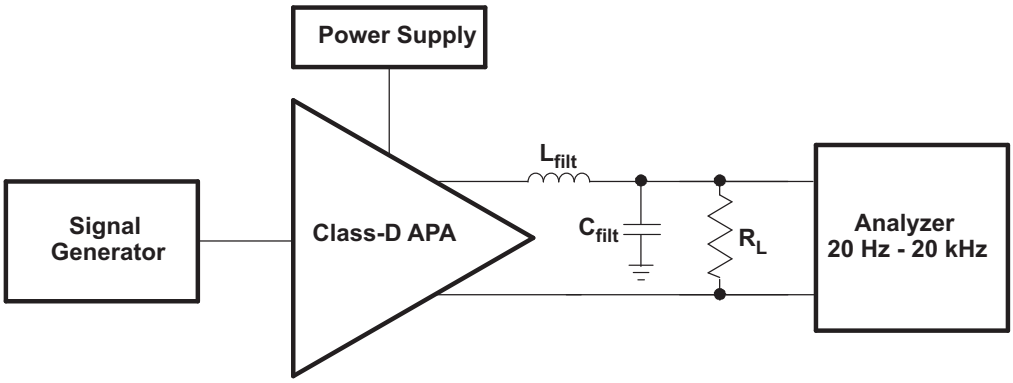
The generator output and amplifier input must be ac-coupled. However, the EVMs already have the ac-coupling capacitors, (C_{IN}), so no additional coupling is required. The generator output impedance should be low to avoid attenuating the test signal, and is important because the input resistance of APAs is not high. Conversely, the analyzer input impedance should be high. The output resistance, R_{OUT}, of the APA is normally in the hundreds of milliohms and can be ignored for all but the power-related calculations.

Figure 23(a) shows a class-AB amplifier system. It takes an analog signal input and produces an analog signal output. This amplifier circuit can be directly connected to the AP-II or other analyzer input.

This is not true of the class-D amplifier system shown in Figure 23(b), which requires low-pass filters in most cases in order to measure the audio output waveforms. This is because it takes an analog input signal and converts it into a pulse-width modulated (PWM) output signal that is not accurately processed by some analyzers.



(a) Basic Class-AB



(b) Traditional Class-D

Figure 23. Audio Measurement Systems

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SE Input and SE Output (TAS5602 SE Configuration)

The SE input and output configuration is used with class-AB amplifiers. A block diagram of a fully SE measurement circuit is shown in Figure 24. SE inputs normally have one input pin per channel. In some cases, two pins are present; one is the signal and the other is ground. SE outputs have one pin driving a load through an output ac-coupling capacitor and the other end of the load is tied to ground. SE inputs and outputs are considered to be unbalanced, meaning one end is tied to ground and the other to an amplifier input/output.

The generator should have unbalanced outputs, and the signal should be referenced to the generator ground for best results. Unbalanced or balanced outputs can be used when floating, but they may create a ground loop that affects the measurement accuracy. The analyzer should have balanced inputs to cancel out any common-mode noise in the measurement.

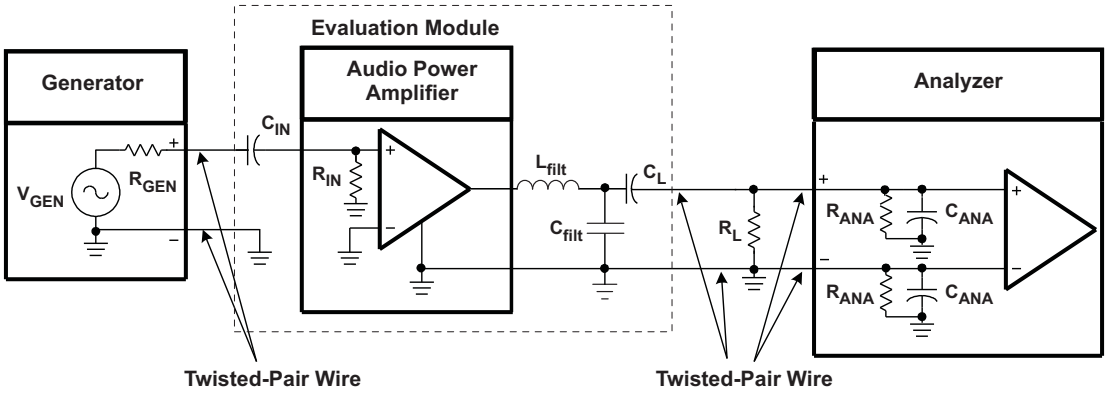


Figure 24. SE Input—SE Output Measurement Circuit

The following general rules should be followed when connecting to APAs with SE inputs and outputs:

- Use an unbalanced source to supply the input signal.
- Use an analyzer with balanced inputs.
- Use twisted-pair wire for all connections.
- Use shielding when the system environment is noisy.
- Ensure the cables from the power supply to the APA, and from the APA to the load, can handle the large currents (see Table 3).

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DIFFERENTIAL INPUT AND BTL OUTPUT (TAS5602 BTL Configuration)

Many of the class-D APAs and many class-AB APAs have differential inputs and bridge-tied-load (BTL) outputs. Differential inputs have two input pins per channel and amplify the difference in voltage between the pins. Differential inputs reduce the common-mode noise and distortion of the input circuit. BTL is a term commonly used in audio to describe differential outputs. BTL outputs have two output pins providing voltages that are 180° out of phase. The load is connected between these pins. This has the added benefits of quadrupling the output power to the load and eliminating a dc-blocking capacitor.

A block diagram of the measurement circuit is shown in Figure 25. The differential input is a balanced input, meaning the positive (+) and negative (–) pins have the same impedance to ground. Similarly, the BTL output equates to a balanced output.

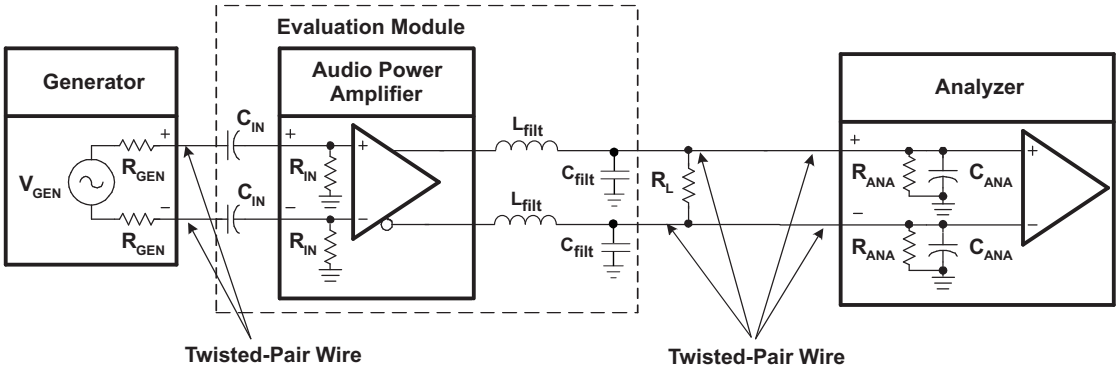


Figure 25. Differential Input, BTL Output Measurement Circuit

The generator should have balanced outputs, and the signal should be balanced for best results. An unbalanced output can be used, but it may create a ground loop that affects the measurement accuracy. The analyzer must also have balanced inputs for the system to be fully balanced, thereby cancelling out any common-mode noise in the circuit and providing the most accurate measurement.

The following general rules should be followed when connecting to APAs with differential inputs and BTL outputs:

- Use a balanced source to supply the input signal.
- Use an analyzer with balanced inputs.
- Use twisted-pair wire for all connections.
- Use shielding when the system environment is noisy.
- The cables from the power supply to the APA, and from the APA to the load, must be able to handle the large currents (see Table 3).

Table 3 shows the recommended wire size for the power supply and load cables of the APA system. The real concern is the dc or ac power loss that occurs as the current flows through the cable. These recommendations are based on 12-inch (30.5-cm)-long wire with a 20-kHz sine-wave signal at 25°C.

Table 3. Recommended Minimum Wire Size for Power Cables

P_{OUT} (W)	R_L(Ω)	AWG Size		DC POWER LOSS (mW)		AC POWER LOSS (mW)	
10	4	18	22	16	40	18	42
2	4	18	22	3.2	8	3.7	8.5
1	8	22	28	2	8	2.1	8.1
< 0.75	8	22	28	1.5	6.1	1.6	6.2

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5602DCA	ACTIVE	HTSSOP	DCA	56	35	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TAS5602	Samples
TAS5602DCAR	ACTIVE	HTSSOP	DCA	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TAS5602	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

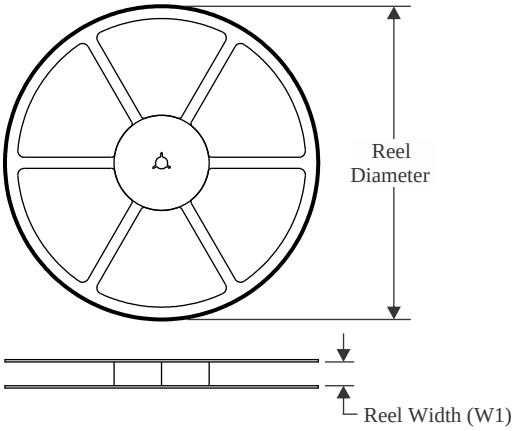
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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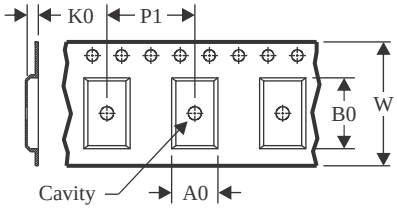
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

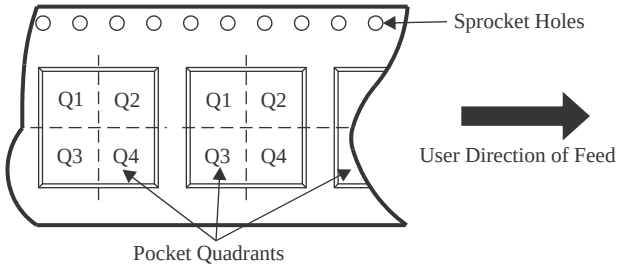


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

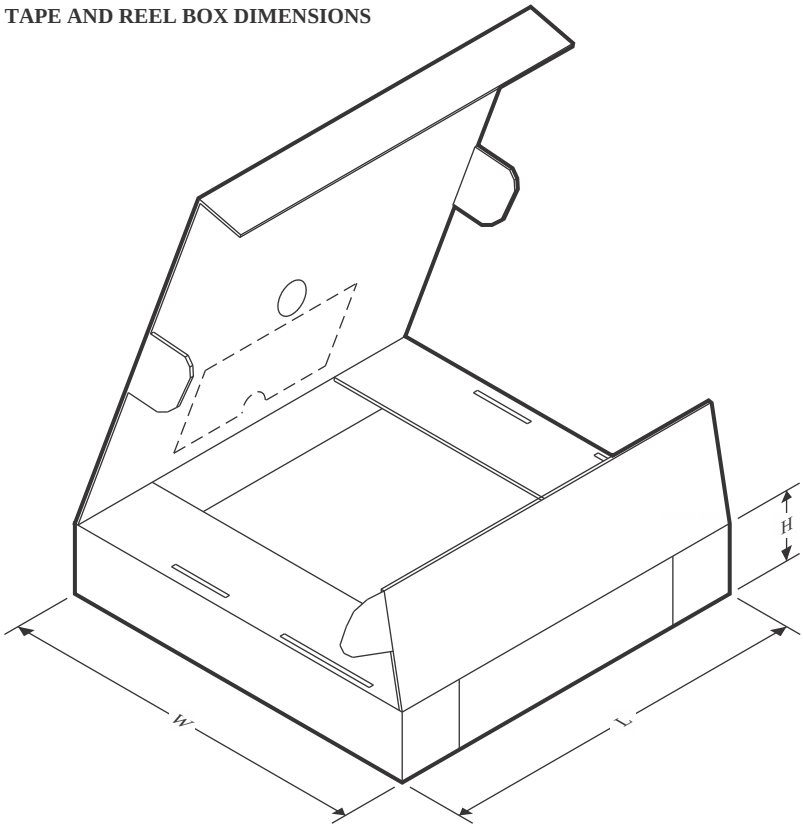
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5602DCAR	HTSSOP	DCA	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

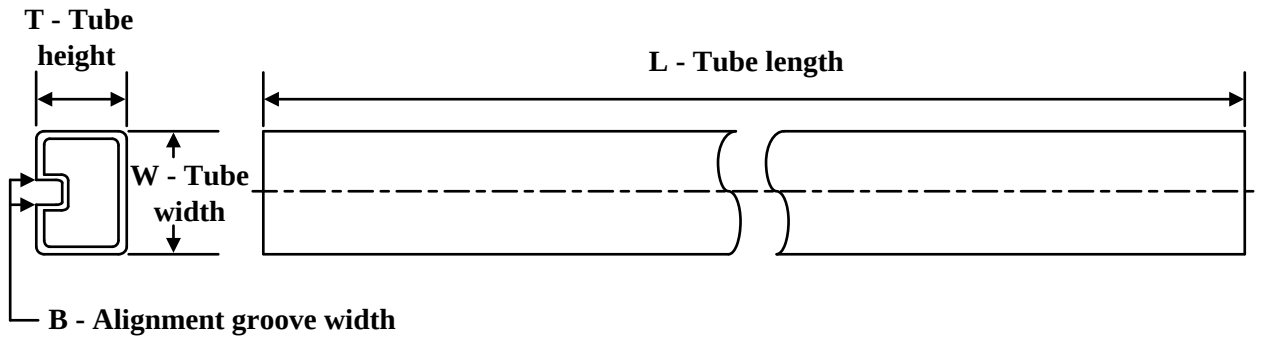
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5602DCAR	HTSSOP	DCA	56	2000	350.0	350.0	43.0

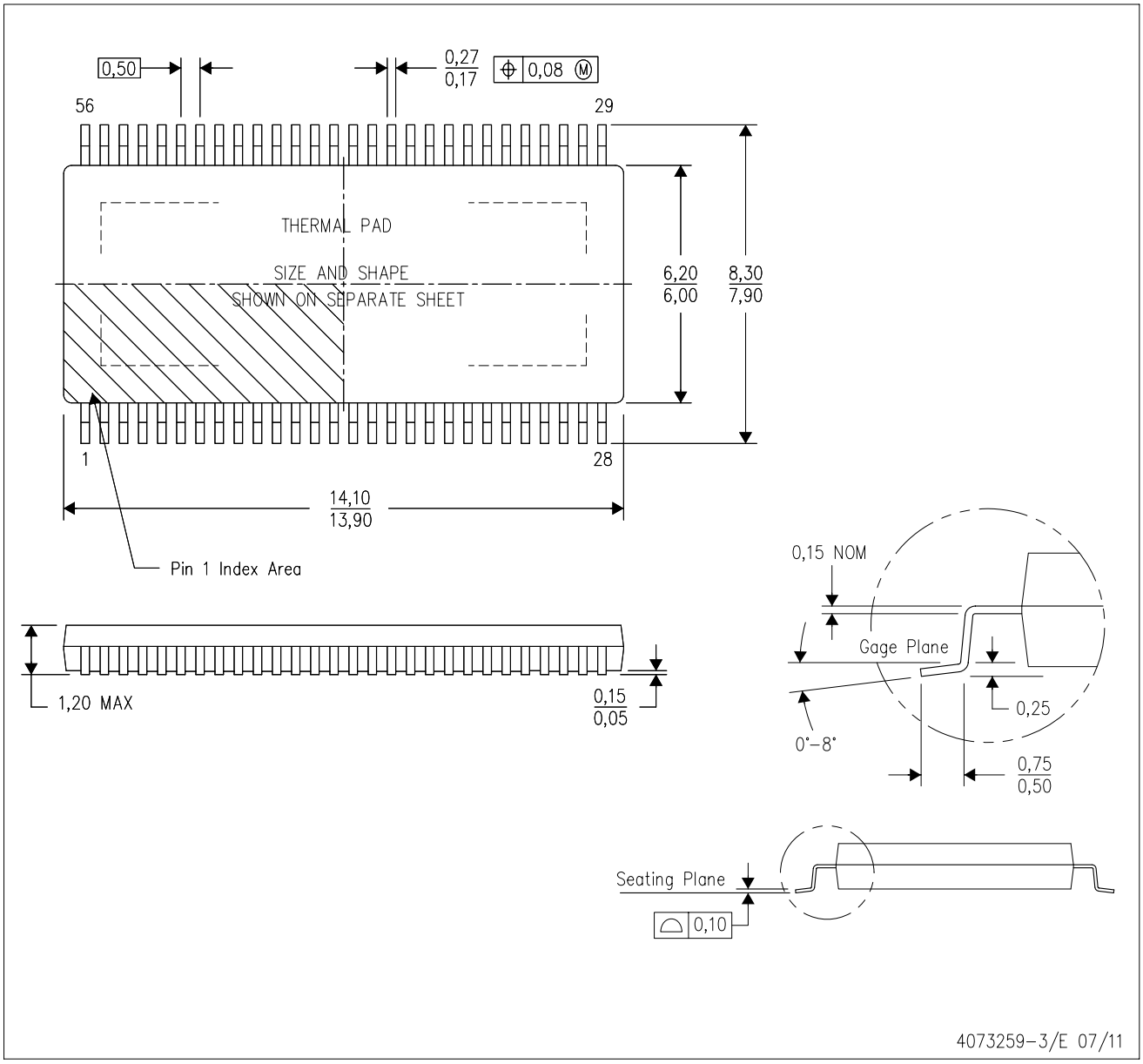
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TAS5602DCA	DCA	HTSSOP	56	35	530	11.89	3600	4.9

DCA (R–PDSO–G56) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

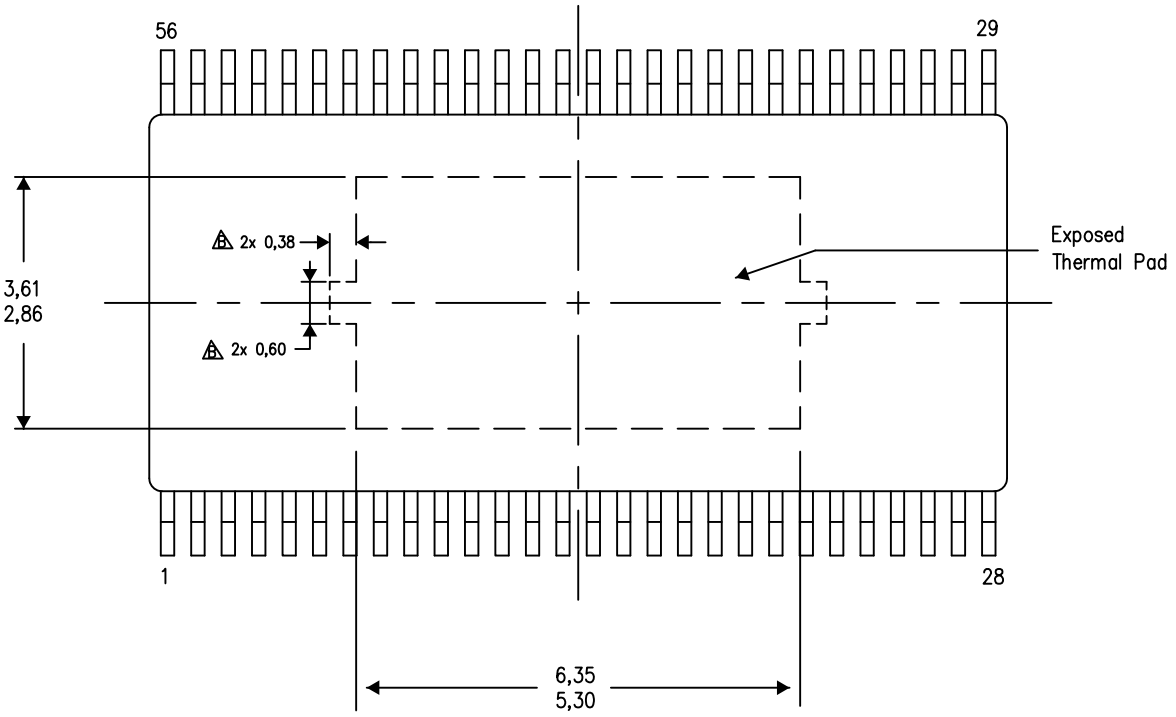
DCA (R–PDSO–G56) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

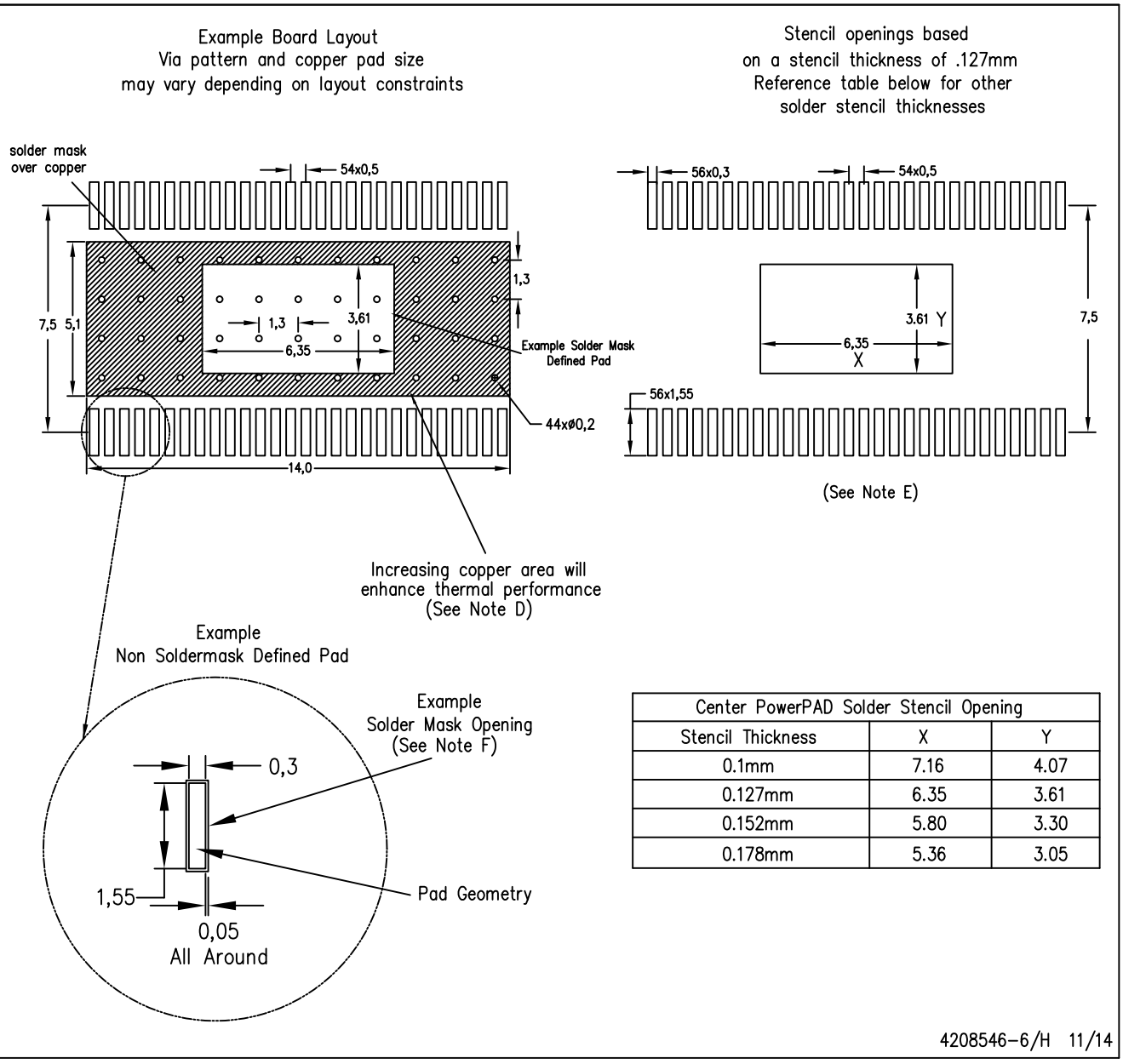
4206320–15/S 11/14

NOTES: A. All linear dimensions are in millimeters

B. Keep–out features are identified to prevent board routing interference.
These exposed metal features may vary within the identified area or completely absent on some devices.

PowerPAD is a trademark of Texas Instruments.

DCA (R–PDSO–G56) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	7.16	4.07
0.127mm	6.35	3.61
0.152mm	5.80	3.30
0.178mm	5.36	3.05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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