# 100 W STEREO DIGITAL AMPLIFIER POWER STAGE

## FEATURES

- **Total Power Output (Bridge Tied Load)**
  - **2 × 100 W at 10% THD+N Into 4 Ω**
  - **2 × 80 W at 10% THD+N Into 6 Ω**
  - **2 × 65 W at 10% THD+N Into 8 Ω**
- **Total Power Output (Single Ended)**
  - **4 × 40 W at 10% THD+N Into 3 Ω**
  - **4 × 30 W at 10% THD+N Into 4 Ω**
- **Total Power Output (Parallel Mode)**
  - **1 × 200 W at 10% THD+N Into 2 Ω**
  - **1 × 160 W at 10% THD+N Into 3 Ω**
- **>110 dB SNR (A-Weighted With TAS5518 Modulator)**
- **<0.1% THD+N (1 W, 1 kHz)**
- **Supports PWM Frame Rates of 192 kHz to 432 kHz**
- **Resistor-Programmable Current Limit**
- **Integrated Self-Protection Circuitry, Including:**
  - **Under Voltage Protection**
  - **Overtemperature Warning and Error**
  - **Overload Protection**
  - **Short-Circuit Protection**
  - **PWM Activity Detector**
- **Standalone Protection Recovery**
- **Power-On Reset (POR) to Eliminate System Power-Supply Sequencing**
- **High-Efficiency Power Stage (>90%) With 110-mΩ Output MOSFETs**
- **Thermally Enhanced Package 44-Pin HTSSOP (DDV)**
- **Error Reporting, 3.3-V and 5.0-V Compliant**
- **EMI Compliant When Used With Recommended System Design**

## APPLICATIONS

- **Mini/Micro Audio System**
- **DVD Receiver**
- **Home Theater**

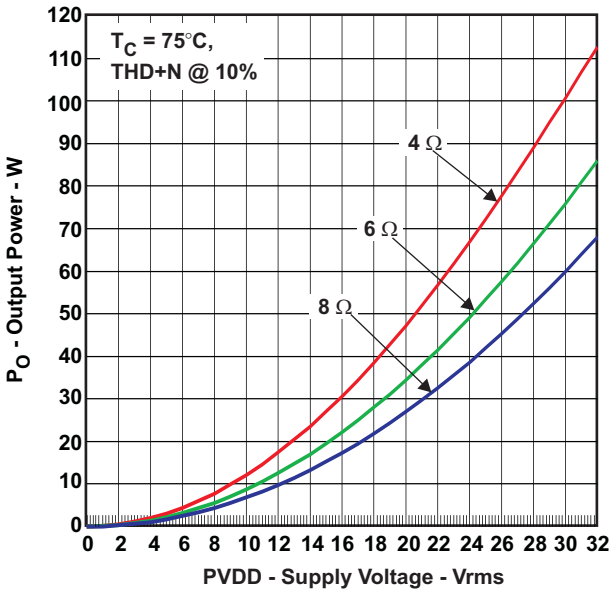
## DESCRIPTION

The TAS5342LA is a high-performance, integrated stereo digital amplifier power stage designed to drive a 4-Ω bridge-tied load (BTL) at up to 100 W per channel with low harmonic distortion, low integrated noise, and low idle current.

The TAS5342LA has a complete protection system integrated on-chip, safeguarding the device against a wide range of fault conditions that could damage the system. These protection features are short-circuit protection, over-current protection, under voltage protection, over temperature protection, and a loss of PWM signal (PWM activity detector).

A power-on-reset (POR) circuit is used to eliminate power-supply sequencing that is required for most power-stage designs.

**BTL OUTPUT POWER vs SUPPLY VOLTAGE**




Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PurePath Digital, PowerPAD are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2008, Texas Instruments Incorporated

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

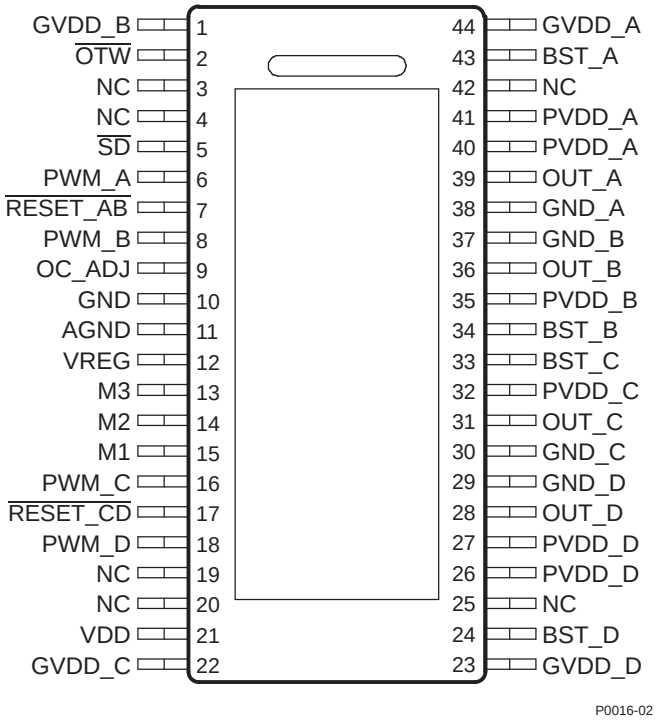
# GENERAL INFORMATION

## TERMINAL ASSIGNMENT

The TAS5342LA is available in a thermally enhanced package 44-pin HTSSOP PowerPAD™ package (DDV)

This package contains a thermal pad that is located on the top side of the device for convenient thermal coupling to the heatsink.

**DDV PACKAGE**
**(TOP VIEW)**




P0016-02


Copyright © 2008, Texas Instruments Incorporated

## PROTECTION MODE SELECTION PINS

Protection modes are selected by shorting M1, M2, and M3 to VREG or GND.

| MODE PINS | | | Mode Name | PWM Input(1) | Description |
|---|---|---|---|---|---|
| M3 | M2 | M1 | | | |
| 0 | 0 | 0 | BTL mode 1 | 2N | All protection systems enabled |
| 0 | 0 | 1 | BTL mode 2 | 2N | Latching shudown on, PWM activity detector and OLP disabled |
| 0 | 1 | 0 | BTL mode 3 | 1N | All protection systems enabled |
| 0 | 1 | 1 | PBTL mode | 1N / 2N(2) | All protection systems enabled |
| 1 | 0 | 0 | SE mode 1 | 1N | All protection systems enabled(3) |
| 1 | 0 | 1 | SE mode 2 | 1N | Latching shudown on, PWM activity detector and OLP disabled(3) |
| 1 | 1 | 0 | Reserved | | |
| 1 | 1 | 1 | | | |

(1) The 1N and 2N naming convention is used to indicate the number of PWM lines to the power stage per channel in a specific mode.
(2) PWM_D is used to select between the 1N and 2N interface in PBTL mode (Low = 1N; High = 2N). PWM_D is internally pulled low in PBTL mode. PWM_A is used as the PWM input in 1N mode and PWM_A and PWM_B are used as inputs for the 2N mode.
(3) PPSC detection system disabled.

## PACKAGE HEAT DISSIPATION RATINGS(1)

| PARAMETER | TAS5342LADDV |
|---|---|
| $R_{\theta JC}$ (°C/W)—2 BTL or 4 SE channels | 1.8 |
| $R_{\theta JC}$ (°C/W)—1 BTL or 2 SE channel(s) | 3.6 |
| $R_{\theta JC}$ (°C/W)—1 SE channel | 7.2 |
| Power Pad area(2) | 36 $mm^2$ |

(1) JC is junction-to-case, CH is case-to-heatsink.
(2) $R_{\theta CH}$ is an important consideration. Assume a 2-mil thickness of high performance grease with a thermal conductivity at 2.5W/m-K between the pad area and the heat sink. The $R_{\theta CH}$ with this condition is 0.6°C/W for the DDV package.

Copyright © 2008, Texas Instruments Incorporated

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted (1)

| TAS5342LA | |
|---|---|
| VDD to AGND | –0.3 V to 13.2 V |
| GVDD_X to AGND | –0.3 V to 13.2 V |
| PVDD_X to GND_X (2) | –0.3 V to 46V |
| OUT_X to GND_X (2) | –0.3 V to 46V |
| BST_X to GND_X (2) | –0.3 V to 59.2 V |
| BST_X to GVDD_X (2) | –0.3 V to 46V |
| VREG to AGND | –0.3 V to 4.2 V |
| GND_X to GND | –0.3 V to 0.3 V |
| GND_X to AGND | –0.3 V to 0.3 V |
| GND to AGND | –0.3 V to 0.3 V |
| PWM_X, OC_ADJ, M1, M2, M3 to AGND | –0.3 V to 4.2 V |
| $\overline{\text{RESET_X}}$, $\overline{\text{SD}}$, $\overline{\text{OTW}}$ to AGND | –0.3 V to 7 V |
| Maximum continuous sink current ($\overline{\text{SD}}$, $\overline{\text{OTW}}$) | 9 mA |
| Maximum operating junction temperature range, $T_J$ | 0°C to 125°C |
| Storage temperature | –40°C to 125°C |
| Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |
| Minimum pulse duration, low | 30 ns |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These voltages represent the dc voltage + peak ac waveform measured at the terminal of the device in all conditions.

## ORDERING INFORMATION(1)

| $T_A$ | PACKAGE | DESCRIPTION |
|---|---|---|
| 0°C to 70°C | TAS5342LADDV | 44-pin HTSSOP |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.


Copyright © 2008, Texas Instruments Incorporated

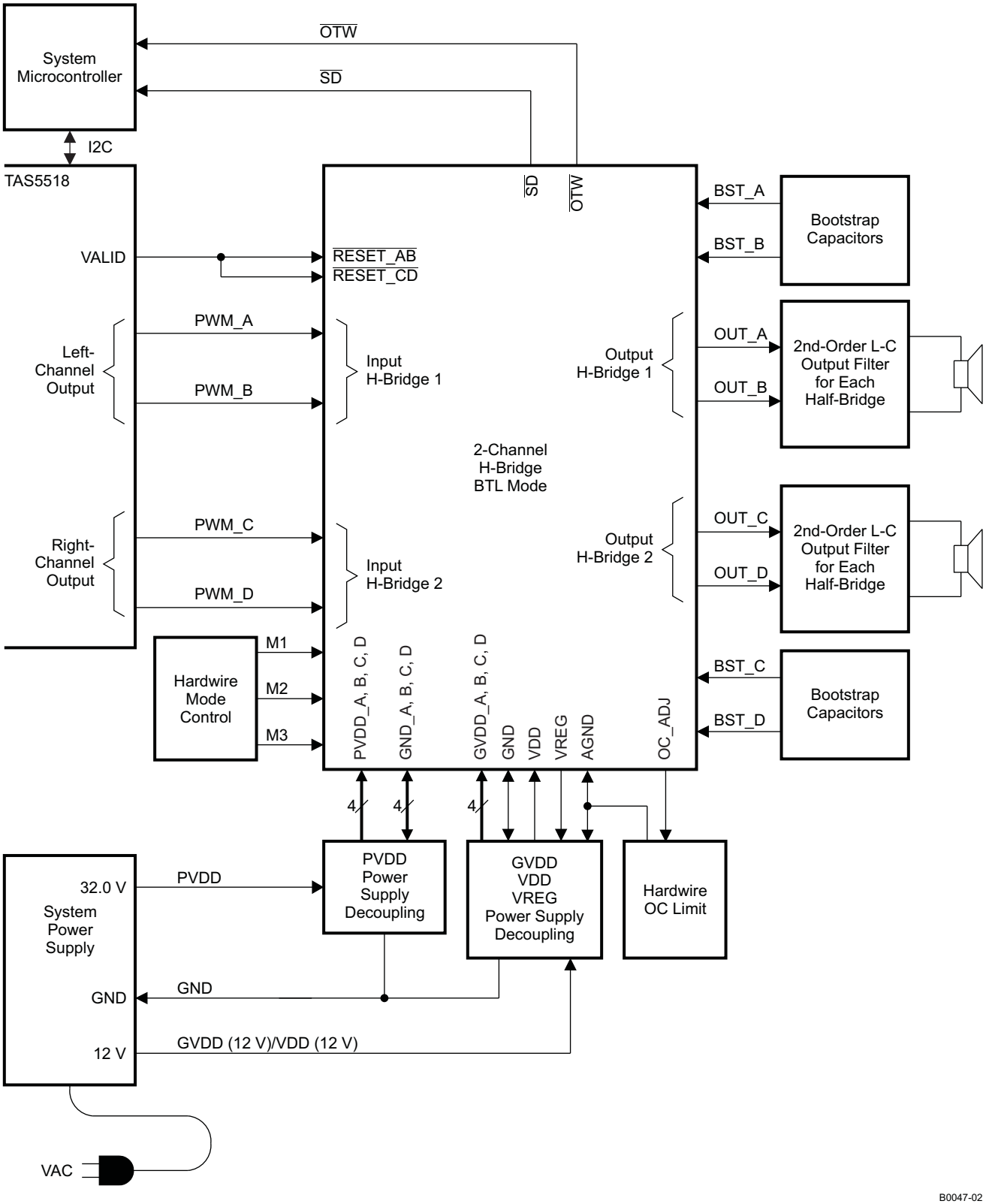
## TERMINAL FUNCTIONS

| TERMINAL | | FUNCTION (1) | DESCRIPTION |
|---|---|---|---|
| NAME | DDV NO. | | |
| AGND | 11 | P | Analog ground |
| BST_A | 43 | P | Bootstrap pin, A-Side |
| BST_B | 34 | P | Bootstrap pin, B-Side |
| BST_C | 33 | P | Bootstrap pin, C-Side |
| BST_D | 24 | P | Bootstrap pin, D-Side |
| GND | 10 | P | Ground |
| GND_A | 38 | P | Power ground for half-bridge A |
| GND_B | 37 | P | Power ground for half-bridge B |
| GND_C | 30 | P | Power ground for half-bridge C |
| GND_D | 29 | P | Power ground for half-bridge D |
| GVDD_A | 44 | P | Gate-drive voltage supply; A-Side |
| GVDD_B | 1 | P | Gate-drive voltage supply; B-Side |
| GVDD_C | 22 | P | Gate-drive voltage supply; C-Side |
| GVDD_D | 23 | P | Gate-drive voltage supply; D-Side |
| M1 | 15 | I | Mode selection pin (LSB) |
| M2 | 14 | I | Mode selection pin |
| M3 | 13 | I | Mode selection pin (MSB) |
| NC | 3, 4, 19, 20, 25, 42 | – | No connect. Pins may be grounded. |
| OC_ADJ | 9 | O | Analog overcurrent programming pin |
| $\overline{\text{OTW}}$ | 2 | O | Overtemperature warning signal, open-drain, active-low |
| OUT_A | 39 | O | Output, half-bridge A |
| OUT_B | 36 | O | Output, half-bridge B |
| OUT_C | 31 | O | Output, half-bridge C |
| OUT_D | 28 | O | Output, half-bridge D |
| PVDD_A | 40, 41 | P | Power supply input for half-bridge A |
| PVDD_B | 35 | P | Power supply input for half-bridge B |
| PVDD_C | 32 | P | Power supply input for half-bridge C |
| PVDD_D | 26, 27 | P | Power supply input for half-bridge D |
| PWM_A | 6 | I | PWM Input signal for half-bridge A |
| PWM_B | 8 | I | PWM Input signal for half-bridge B |
| PWM_C | 16 | I | PWM Input signal for half-bridge C |
| PWM_D | 18 | I | PWM Input signal for half-bridge D |
| $\overline{\text{RESET_AB}}$ | 7 | I | Reset signal for half-bridge A and half-bridge B, active-low |
| $\overline{\text{RESET_CD}}$ | 17 | I | Reset signal for half-bridge C and half-bridge D, active-low |
| $\overline{\text{SD}}$ | 5 | O | Shutdown signal, open-drain, active-low |
| VDD | 21 | P | Input power supply |
| VREG | 12 | P | Internal voltage regulator |

(1) I = input, O = output, P = power

Copyright © 2008, Texas Instruments Incorporated

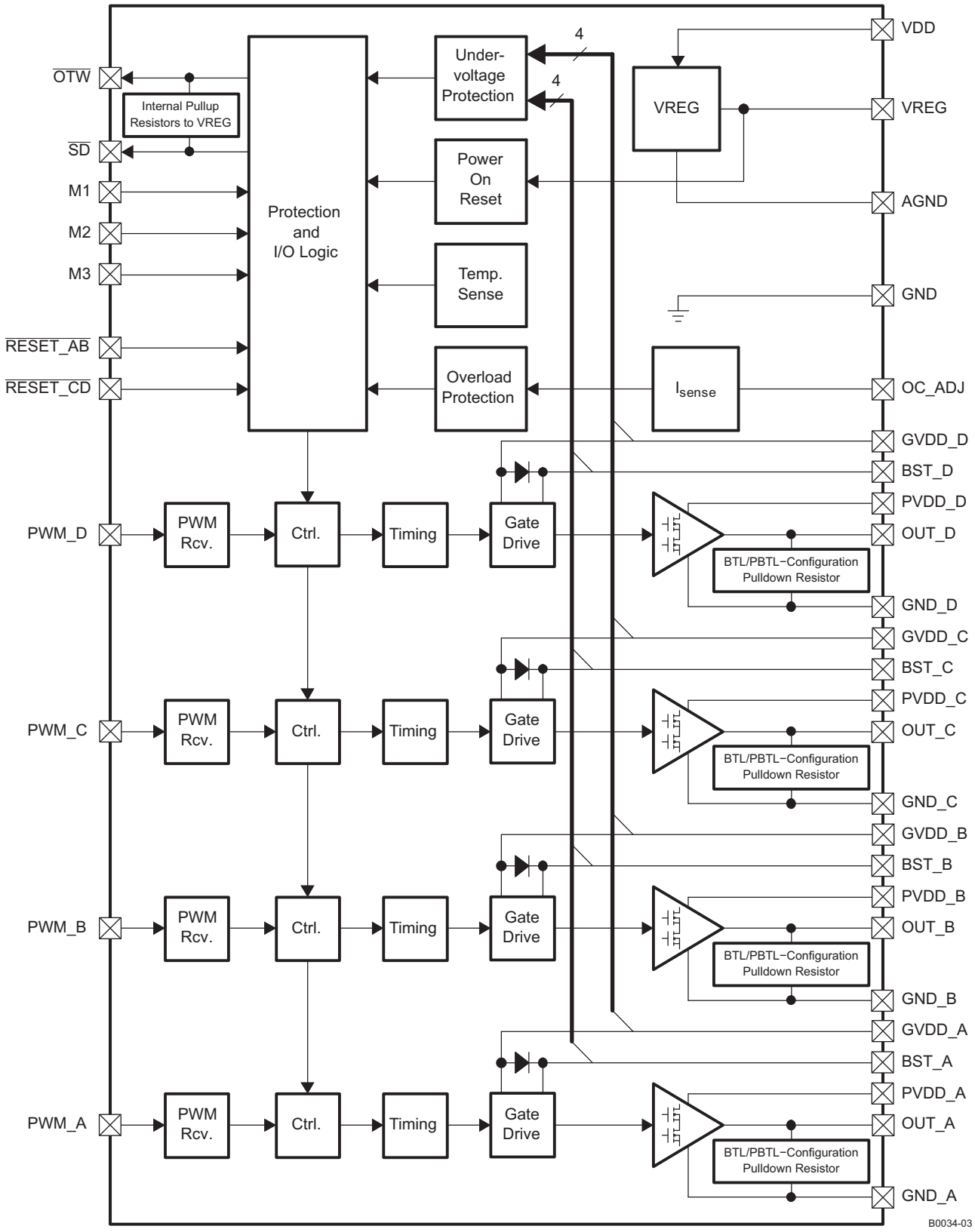
## TYPICAL SYSTEM BLOCK DIAGRAM





Copyright © 2008, Texas Instruments Incorporated

## FUNCTIONAL BLOCK DIAGRAM



## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| PVDD_X | Half-bridge supply voltage | | 0 | 32.0 | 34.0 | V |
| GVDD_X | Supply voltage for logic regulators and gate-drive circuitry | | 10.8 | 12 | 13.2 | V |
| VDD | Digital regulator supply voltage | | 10.8 | 12 | 13.2 | V |
| $R_L$ (BTL) | Resistive load impedance (no Cycle-by-Cycle current control), recommended demodulation filter | | 3 | 4 | | Ω |
| $R_L$ (SE) | | | 2.25 | 3 | | |
| $R_L$ (PBTL) | | | 1.5 | 2 | | |
| $L_{Output}$ (BTL) | Output-filter inductance | Minimum output inductance under short-circuit condition | 5 | 10 | | µH |
| $L_{Output}$ (SE) | | | 5 | 10 | | |
| $L_{Output}$ (PBTL) | | | 5 | 10 | | |
| $f_S$ | PWM frame rate | | 192 | 384 | 432 | kHz |
| $t_{LOW}$ | Minimum low-state pulse duration per PWM Frame, noise shaper enabled | | 30 | | | nS |
| $C_{PVDD}$ | PVDD close decoupling capacitors | | | 0.1 | | µF |
| $C_{BST}$ | Bootstrap capacitor, selected value supports PWM frame rates from 192 kHz to 432 kHz | | | 33 | | nF |
| $R_{OC}$ | Over-current programming resistor | Resistor tolerance = 5% | 22 | 22 | 47 | kΩ |
| $R_{EXT-PULLUP}$ | External pull-up resistor to +3.3V to +5.0V for $\overline{SD}$ or $\overline{OTW}$ | | 3.3 | 4.7 | | kΩ |
| $T_J$ | Junction temperature | | 0 | | 125 | °C |

## AUDIO SPECIFICATIONS (BTL)

Audio performance is recorded as a chipset consisting of a TAS5518 pwm processor (modulation index limited to 97.7%) and a TAS5342LA power stage. PCB and system configuraton are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_x = 32.0 V, GVDD_x = 12 V, $R_L$ = 4 Ω, $f_S$ = 384 kHz, $R_{OC}$ = 22 kΩ, $T_C$ = 75°C, Output Filter: $L_{DEM}$ = 10 µH, $C_{DEM}$ = 470 nF, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | TAS5342LA | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $P_{OMAX}$ | Maximum Power Output | $R_L$ = 4 Ω, 10% THD+N, clipped input signal | | 100 | | W |
| | | $R_L$ = 6 Ω, 10% THD+N, clipped input signal | | 80 | | |
| | | $R_L$ = 8 Ω, 10% THD+N, clipped input signal | | 65 | | |
| $P_O$ | Unclipped Power Output | $R_L$ = 4 Ω, 0 dBFS, unclipped input signal | | 80 | | W |
| | | $R_L$ = 6 Ω, 0 dBFS, unclipped input signal | | 64 | | |
| | | $R_L$ = 8 Ω, 0 dBFS, unclipped input signal | | 50 | | |
| THD+N | Total harmonic distortion + noise | 0 dBFS; AES17 filter | | 0.4% | | |
| | | 1 W; AES17 filter | | 0.09% | | |
| $V_n$ | Output integrated noise | A-weighted, AES17 filter, Auto mute disabled | | 55 | | µV |
| SNR | Signal-to-noise ratio (1) | A-weighted, AES17 filter, Auto mute disabled | | 110 | | dB |
| DNR | Dynamic range | A-weighted, input level = –60 dBFS, AES17 filter | | 110 | | dB |
| DC Offset | Output offset voltage | | | ±15 | | mV |
| $P_{idle}$ | Power dissipation due to idle losses (IPVDD_X) | $P_O$ = 0 W, all halfbridges switching (2) | | 3 | | W |

(1) SNR is calculated relative to 0-dBFS input level.
(2) Actual system idle losses are affected by core losses of output inductors.


Copyright © 2008, Texas Instruments Incorporated

## AUDIO SPECIFICATIONS (Single-Ended Output)

Audio performance is recorded as a chipset consisting of a TAS5086 pwm processor (modulation index limited to 97.7%) and a TAS5342LA power stage. PCB and system configuraton are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_x = 32.0 V, GVDD_x = 12 V, $R_L$ = 4 Ω, $f_S$ = 384 kHz, $R_{OC}$ = 22 kΩ, $T_C$ = 75°C, Output Filter: $L_{DEM}$ = 20 µH, $C_{DEM}$ = 1.0 µF, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | TAS5342LA | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $P_{OMAX}$ | Maximum Power Output | $R_L$ = 3 Ω, 10% THD+N, clipped input signal | | 40 | | W |
| | | $R_L$ = 4 Ω, 10% THD+N, clipped input signal | | 30 | | |
| $P_O$ | Unclipped Power Output | $R_L$ = 3 Ω, 0 dBFS, unclipped input signal | | 30 | | |
| | | $R_L$ = 4 Ω, 0 dBFS, unclipped input signal | | 20 | | |
| THD+N | Total harmonic distortion + noise | 0 dBFS; AES17 filter | | 0.4% | | |
| | | 1 W; AES17 filter | | 0.09% | | |
| $V_n$ | Output integrated noise | A-weighted, AES17 filter, Auto mute disabled | | 35 | | µV |
| SNR | Signal-to-noise ratio(1) | A-weighted, AES17 filter, Auto mute disabled | | 109 | | dB |
| DNR | Dynamic range | A-weighted, input level = –60 dBFS AES17 filter | | 109 | | dB |
| $P_{idle}$ | Power dissipation due to idle losses (IPVDD_X) | $P_O$ = 0 W, all half bridges switching(2) | | 3 | | W |

(1) SNR is calculated relative to 0-dBFS input level.
(2) Actual system idle losses are affected by core losses of output inductors.

## AUDIO SPECIFICATIONS (PBTL)

Audio performance is recorded as a chipset consisting of a TAS5518 pwm processor (modulation index limited to 97.7%) and a TAS5342LA power stage. PCB and system configuraton are in accordance with recommended guidelines. Audio frequency = 1kHz, PVDD_x = 32.0 V, GVDD_x = 12 V, $R_L$ = 3 Ω, $f_S$ = 384 kHz, $R_{OC}$ = 22 kΩ, $T_C$ = 75°C, Output Filter: $L_{DEM}$ = 10 µH, $C_{DEM}$ = 1.0 uF, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | TAS5342LA | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $P_{OMAX}$ | Maximum Power Output | $R_L$ = 2 Ω, 10% THD+N, clipped input signal | | 200 | | W |
| | | $R_L$ = 3 Ω, 10% THD+N, clipped input signal | | 160 | | |
| $P_O$ | Unclipped Power Output | $R_L$ = 2 Ω, 0 dBFS, unclipped input signal | | 150 | | W |
| | | $R_L$ = 3 Ω, 0 dBFS, unclipped input signal | | 120 | | |
| THD+N | Total harmonic distortion + noise | 0 dBFS; AES17 filter | | 0.4% | | |
| | | 1 W; AES17 filter | | 0.09% | | |
| $V_n$ | Output integrated noise | A-weighted, AES17 filter, Auto mute disabled | | 45 | | µV |
| SNR | Signal-to-noise ratio(1) | A-weighted, AES17 filter, Auto mute disabled | | 110 | | dB |
| DNR | Dynamic range | A-weighted, input level = –60 dBFS AES17 filter | | 110 | | dB |
| DC Offset | Outuput offset voltage | | | ±15 | | mV |
| $P_{idle}$ | Power dissipation due to idle losses (IPVDD_X) | $P_O$ = 0 W, all half bridges switching(2) | | 3 | | W |

(1) SNR is calculated relative to 0-dBFS input level.
(2) Actual system idle losses are affected by core losses of output inductors.

Copyright © 2008, Texas Instruments Incorporated

## ELECTRICAL CHARACTERISTICS

PVDD_x = 32.0 V, GVDD_X = 12 V, VDD = 12 V, $T_C$ (Case temperature) = 25°C, $f_S$ = 384 kHz, unless otherwise specified.

| PARAMETER | | TEST CONDITIONS | TAS5342LA | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **INTERNAL VOLTAGE REGULATOR AND CURRENT CONSUMPTION** | | | | | | |
| VREG | Voltage regulator, only used as a reference node | VDD = 12 V | 3 | 3.3 | 3.6 | V |
| IVDD | VDD supply current | Operating, 50% duty cycle | | 7.1 | 17 | mA |
| | | Idle, reset mode | | 5.6 | 11 | |
| IGVDD_X | Gate supply current per half-bridge | 50% duty cycle | | 5.9 | 12 | mA |
| | | Reset mode | | 1 | 1.8 | |
| IPVDD_X | Half-bridge idle current | 50% duty cycle, without output filter or load | | 10.5 | 20 | mA |
| | | Reset mode, no switching | | 594 | 713 | µA |
| **OUTPUT STAGE MOSFETs** | | | | | | |
| $R_{DSon,LS}$ | Drain-to-source resistance, Low Side | $T_J$ = 25°C, excludes metallization resistance | | 110 | 125 | mΩ |
| $R_{DSon,HS}$ | Drain-to-source resistance, High Side | | | 110 | 125 | mΩ |
| **I/O PROTECTION** | | | | | | |
| $V_{uvp,G}$ | Undervoltage protection limit, GVDD_X | | | 9.5 | | V |
| $V_{uvp,hyst}$ (1) | Undervoltage protection limit, GVDD_X | | | 250 | | mV |
| $BST_{uvpF}$ | Puts device into RESET when BST voltage falls below limit | | | 6.11 | | V |
| $BST_{uvpR}$ | Brings device out of RESET when BST voltage rises above limit | | | 7.25 | | V |
| OTW (1) | Overtemperature warning | | 115 | 125 | 135 | °C |
| $OTW_{HYST}$ (1) | Temperature drop needed below OTW temp. for $\overline{OTW}$ to be inactive after the $\overline{OTW}$ event | | | 25 | | °C |
| OTE (1) | Overtemperature error threshold | | 145 | 155 | 165 | °C |
| $OTE\text{-}OTW_{differential}$ (1) | $\overline{OTE}$ - $\overline{OTW}$ differential, temperature delta between $\overline{OTW}$ and $\overline{OTE}$ | | | 30 | | °C |
| OLPC | Overload protection counter | $f_S$ = 384 kHz | | 1.25 | | ms |
| $I_{OC}$ | Overcurrent limit protection | Resistor—programmable, high-end, $R_{OC}$ = 22 kΩ with 1 ms pulse, $T_C$= 75°C | 7.9 | 8.4 | | A |
| $I_{OCT}$ | Overcurrent response time | | | 150 | | ns |
| $t_{ACTIVITY\ DETECTOR}$ | Time for PWM activity detector to activate when no PWM is present | Lack of transistion of any PWM input | | 13.2 | | µS |
| $I_{PD}$ | Output pulldown current of each half-bridge | Connected when $\overline{RESET}$ is active to provide bootstrap capacitor charge. Not used in SE mode. | | 3 | | mA |
| **STATIC DIGITAL SPECIFICATIONS** | | | | | | |
| $V_{IH}$ | High-level input voltage | PWM_A, PWM_B, PWM_C, PWM_D, M1, M2, M3, RESET_AB, RESET_CD | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{Leakage}$ | Input leakage current | | | | 100 | µA |
| **OTW/SHUTDOWN (SD)** | | | | | | |
| $R_{INT_PU}$ | Internal pullup resistance, $\overline{OTW}$ to VREG, $\overline{SD}$ to VREG | | 20 | 26 | 32 | kΩ |
| $V_{OH}$ | High-level output voltage | Internal pullup resistor | 3 | 3.3 | 3.6 | V |
| | | External pullup of 4.7 kΩ to 5 V | 4.5 | | 5 | |
| $V_{OL}$ | Low-level output voltage | $I_O$ = 4 mA | | 0.2 | 0.4 | V |
| FANOUT | Device fanout $\overline{OTW}$, $\overline{SD}$ | No external pullup | | 30 | | Devices |

(1) Specified by design


Copyright © 2008, Texas Instruments Incorporated

## TYPICAL CHARACTERISTICS, BTL CONFIGURATION

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

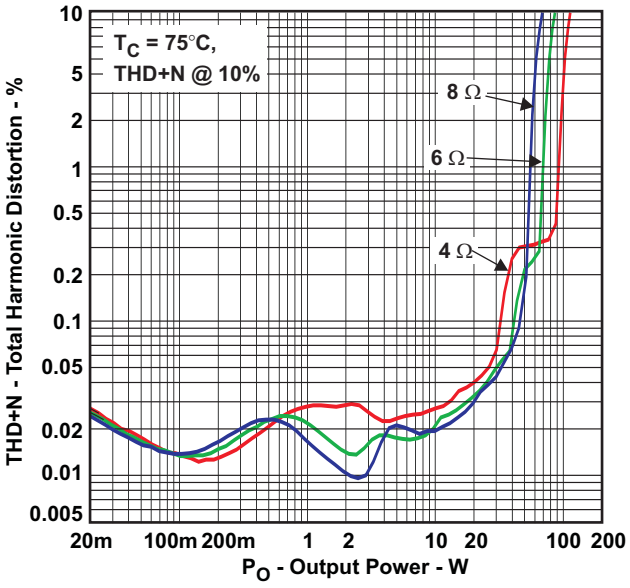



Figure 1.

OUTPUT POWER
vs
SUPPLY VOLTAGE

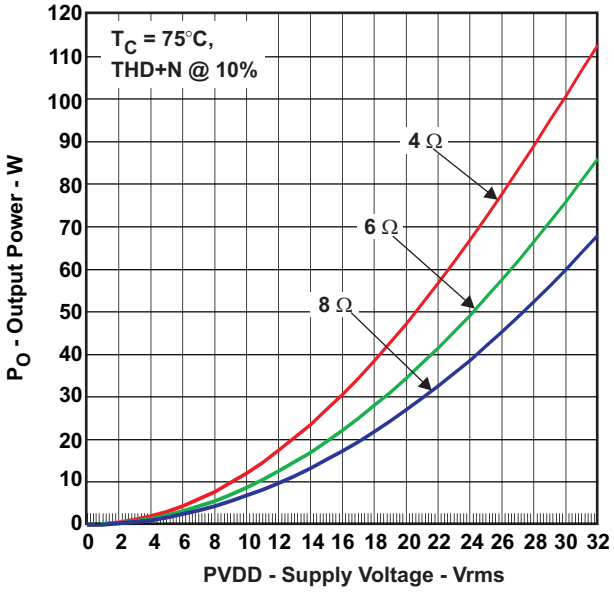



Figure 2.

UNCLIPPED OUTPUT POWER
vs
SUPPLY VOLTAGE

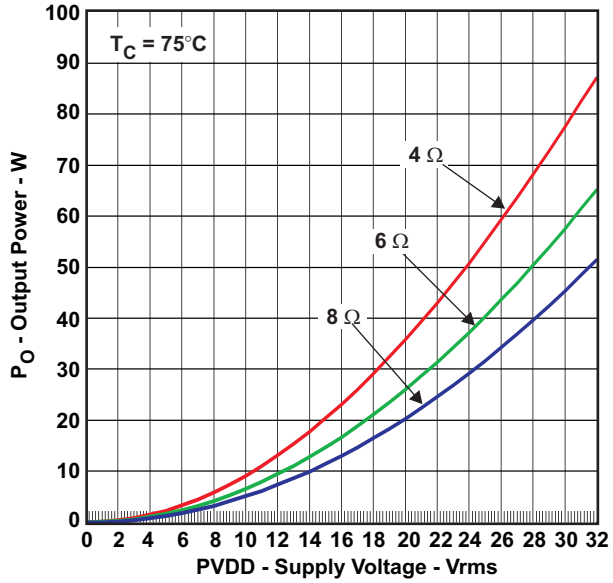



Figure 3.

SYSTEM EFFICIENCY
vs
OUTPUT POWER

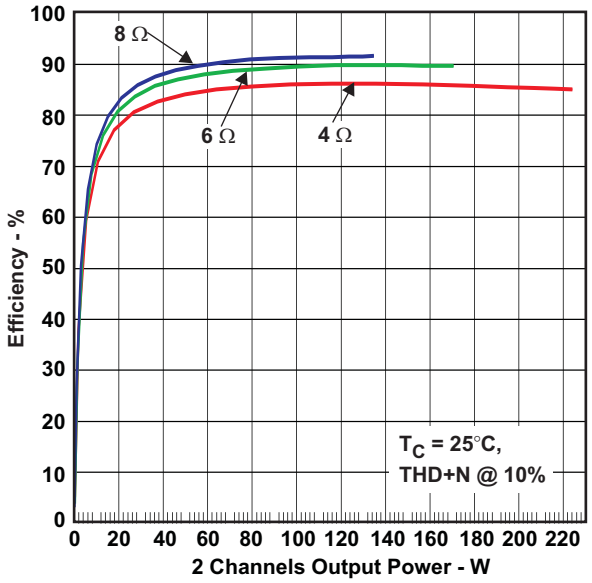



Figure 4.

Copyright © 2008, Texas Instruments Incorporated

## TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

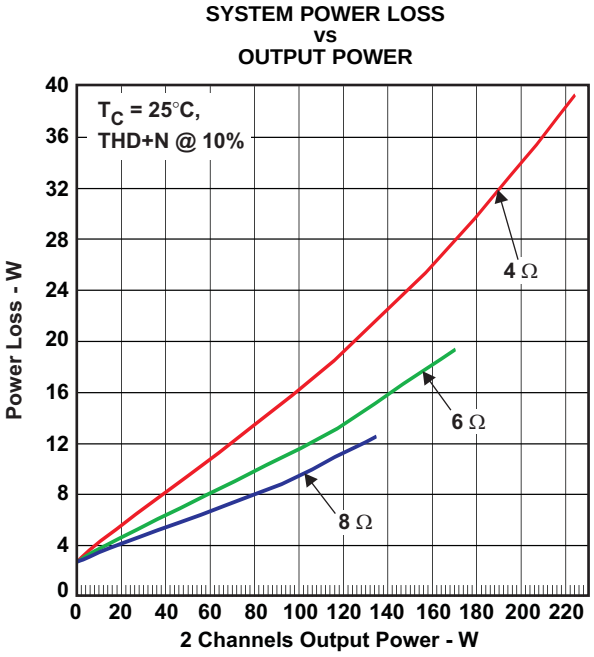



Figure 5.

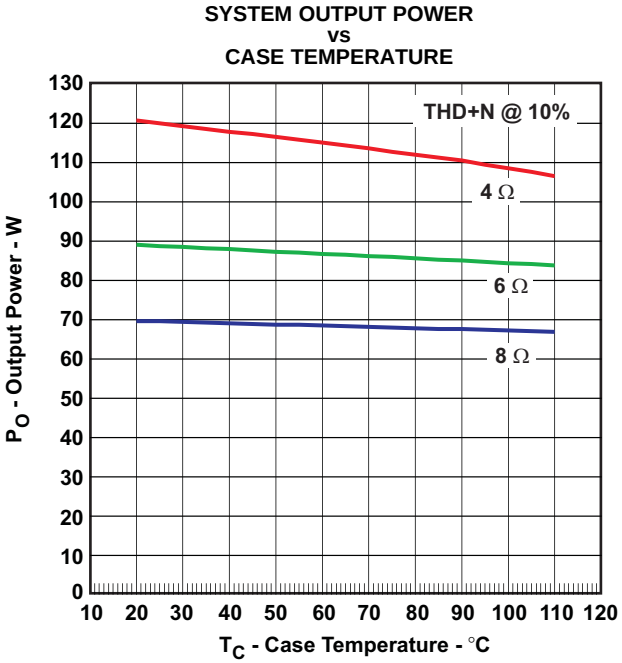



Figure 6.

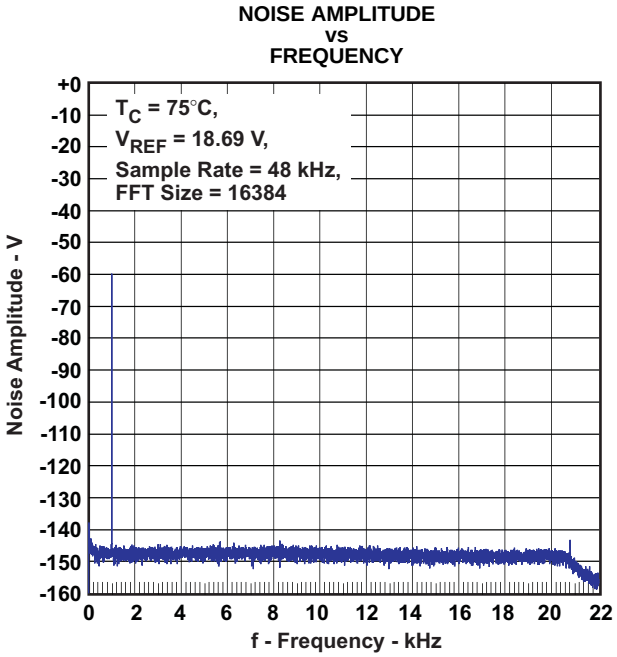



Figure 7.


Copyright © 2008, Texas Instruments Incorporated

## TYPICAL CHARACTERISTICS, SE CONFIGURATION

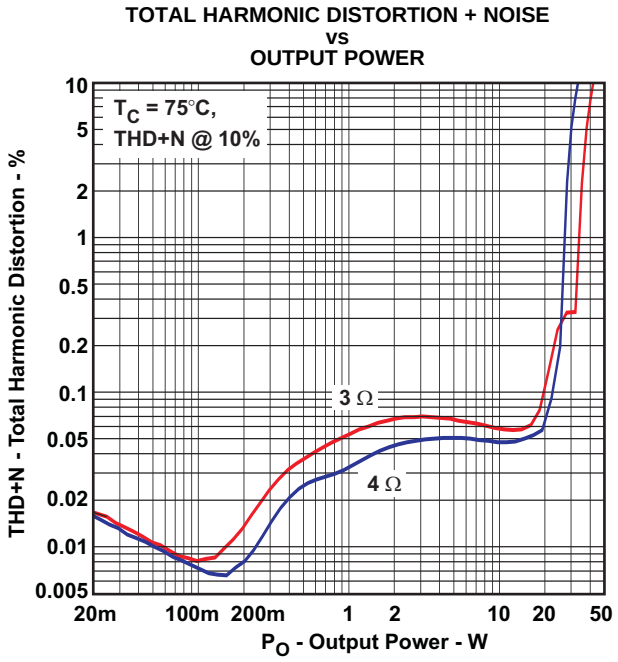



Figure 8.

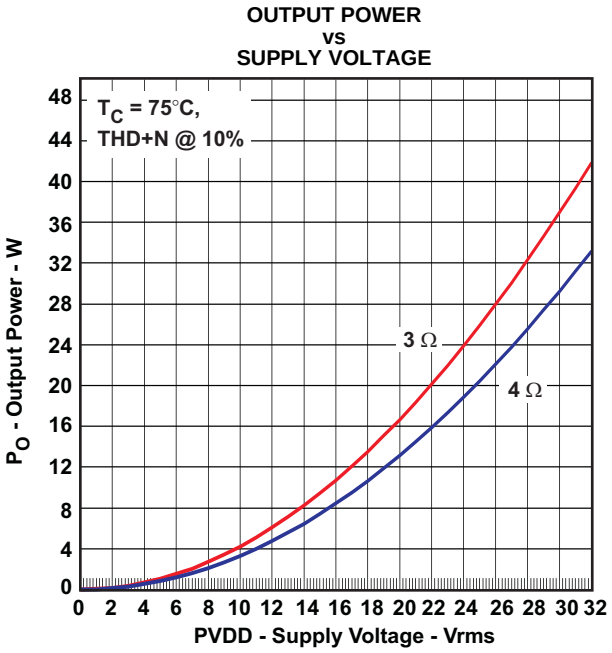



Figure 9.

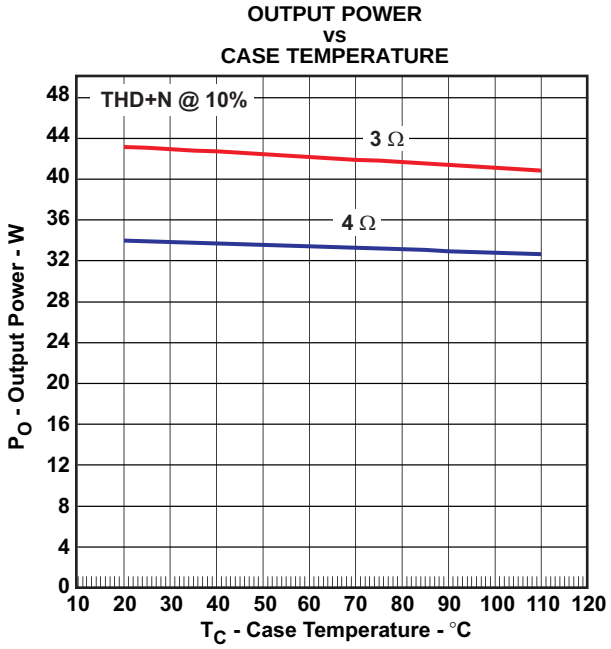



Figure 10.

Copyright © 2008, Texas Instruments Incorporated

## TYPICAL CHARACTERISTICS, PBTL CONFIGURATION

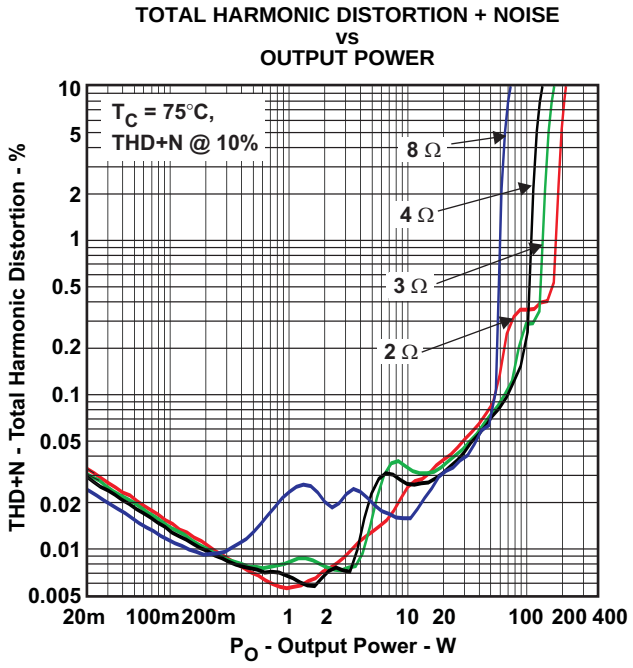



Figure 11.

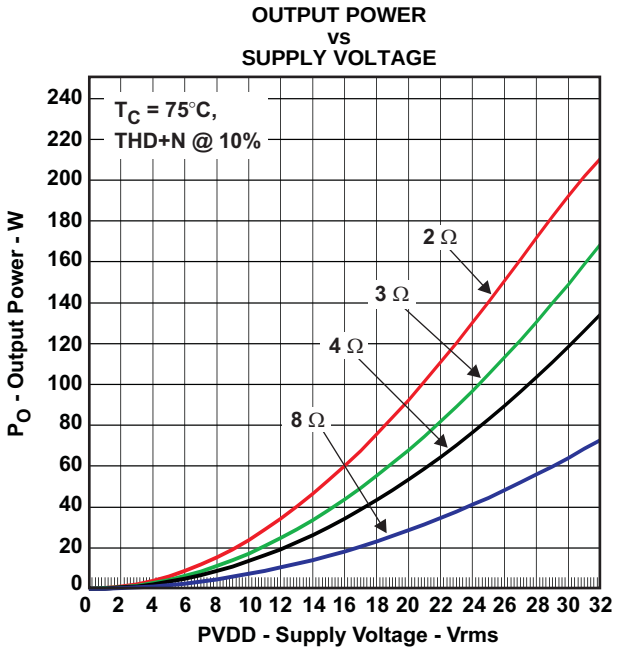



Figure 12.

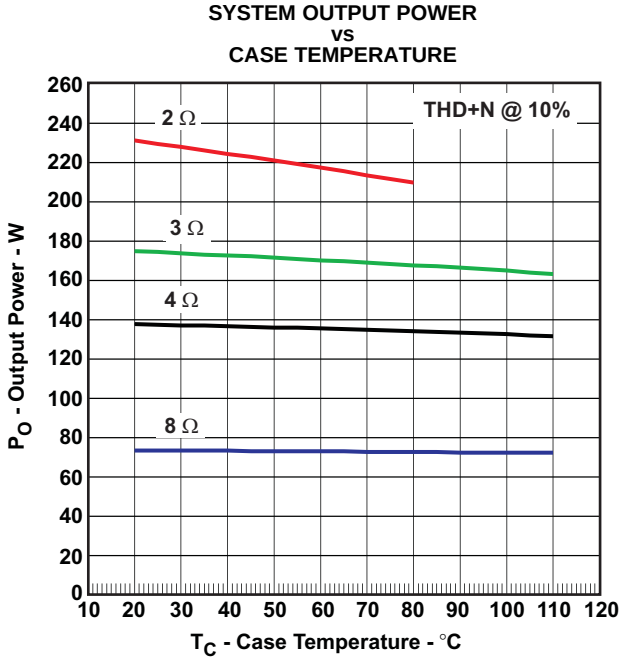



Figure 13.


Copyright © 2008, Texas Instruments Incorporated

# APPLICATION INFORMATION

## PCB MATERIAL RECOMMENDATION

FR-4 Glass Epoxy material with 2 oz. (70 µm) is recommended for use with the TAS5342LA. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin (due to lower PCB trace inductance.

## PVDD CAPACITOR RECOMMENDATION

The large capacitors used in conjunction with each full-birdge, are referred to as the PVDD Capacitors. These capacitors should be selected for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well designed system power supply, 1000 µF, 50-V will support more applications. The PVDD capacitors should be low ESR type because they are used in a circuit associtated with high-speed switching.

## DECOUPLING CAPACITOR RECOMMENDATIONS

In order to design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, good quality decoupling capacitors should be used. In practice, X7R should be used in this application.

The voltage of the decoupling capactors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. This fact is particularly true in the selection of the 0.1µF that is placed on the power supply to each half-bridge. It must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output, and the ripple current created by high power power output. A minimum voltage rating of **50-V** is required for use with a 32.0 V power supply.

## SYSTEM DESIGN RECOMMENDATIONS

The following schematics and PCB layouts illustrate "best practices" in the use of the TAS5342LA.

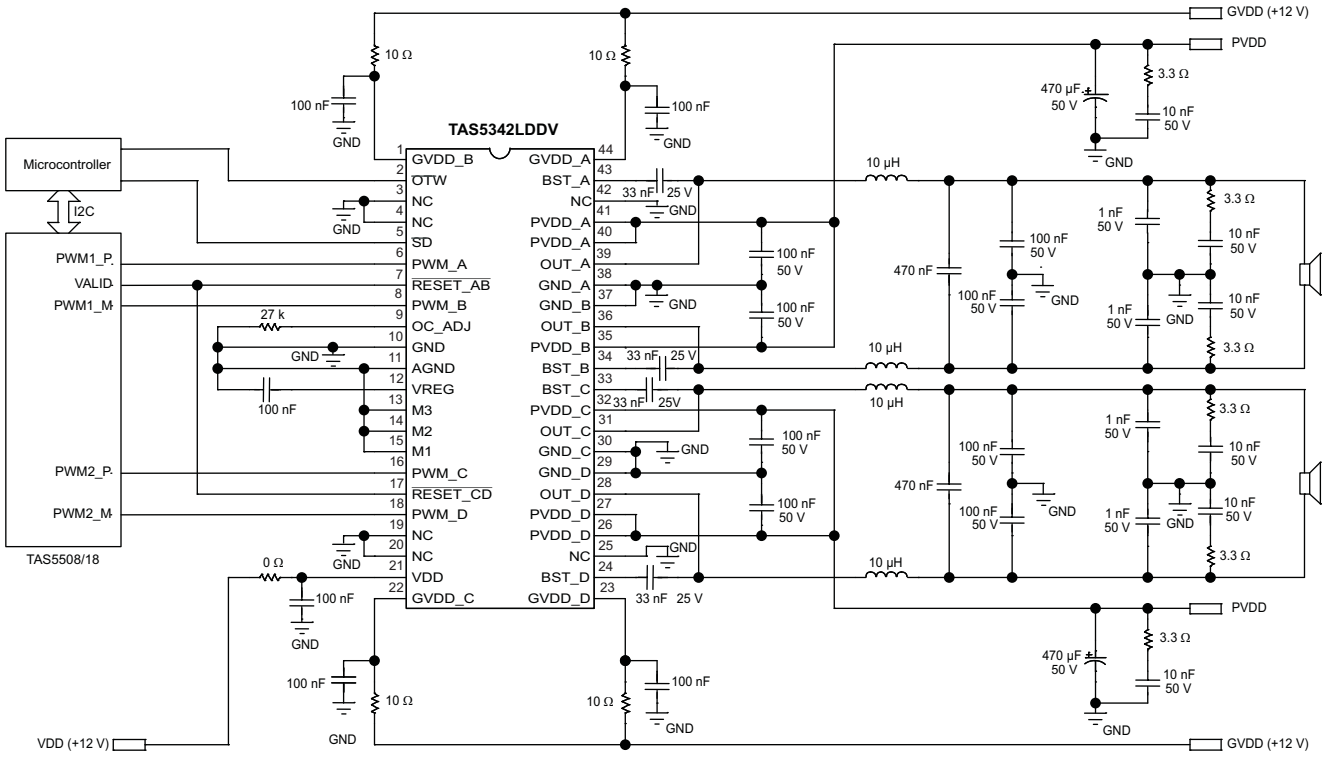



**Figure 14. Typical Differential (2N) BTL Application With AD Modulation Filters**

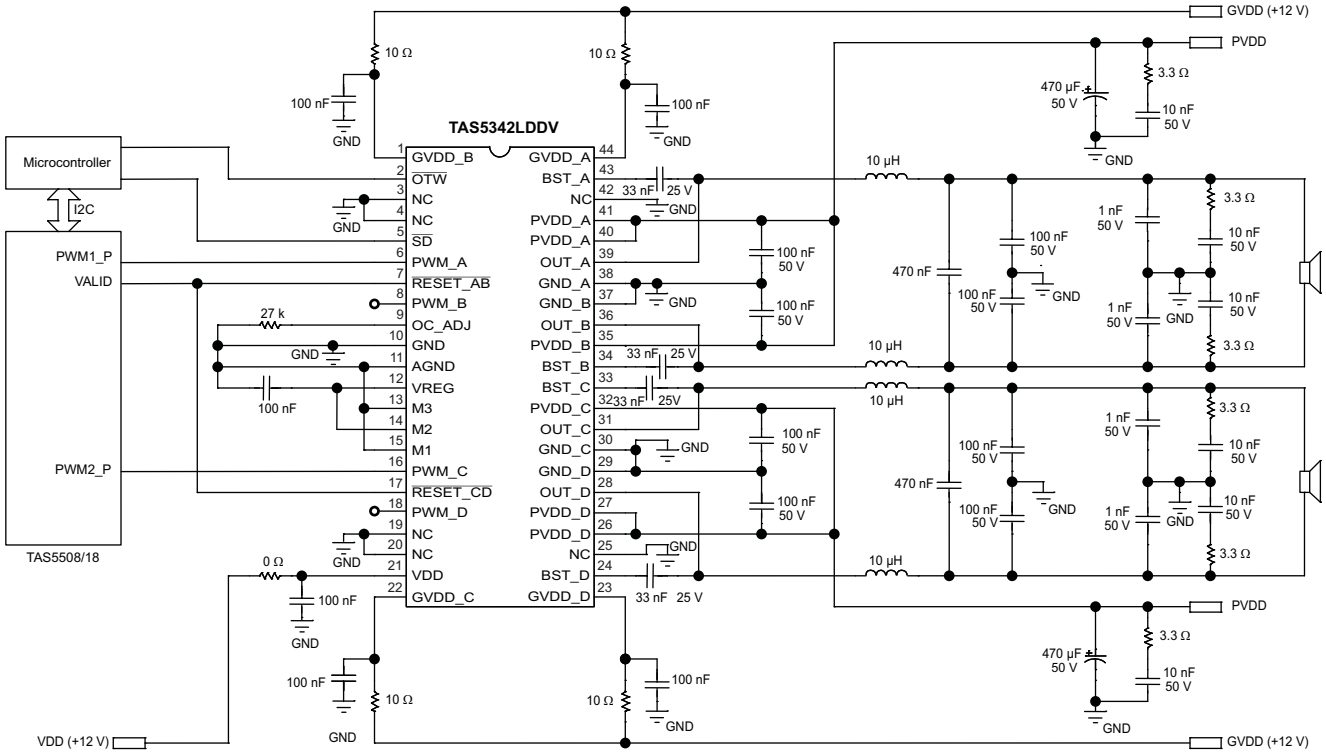
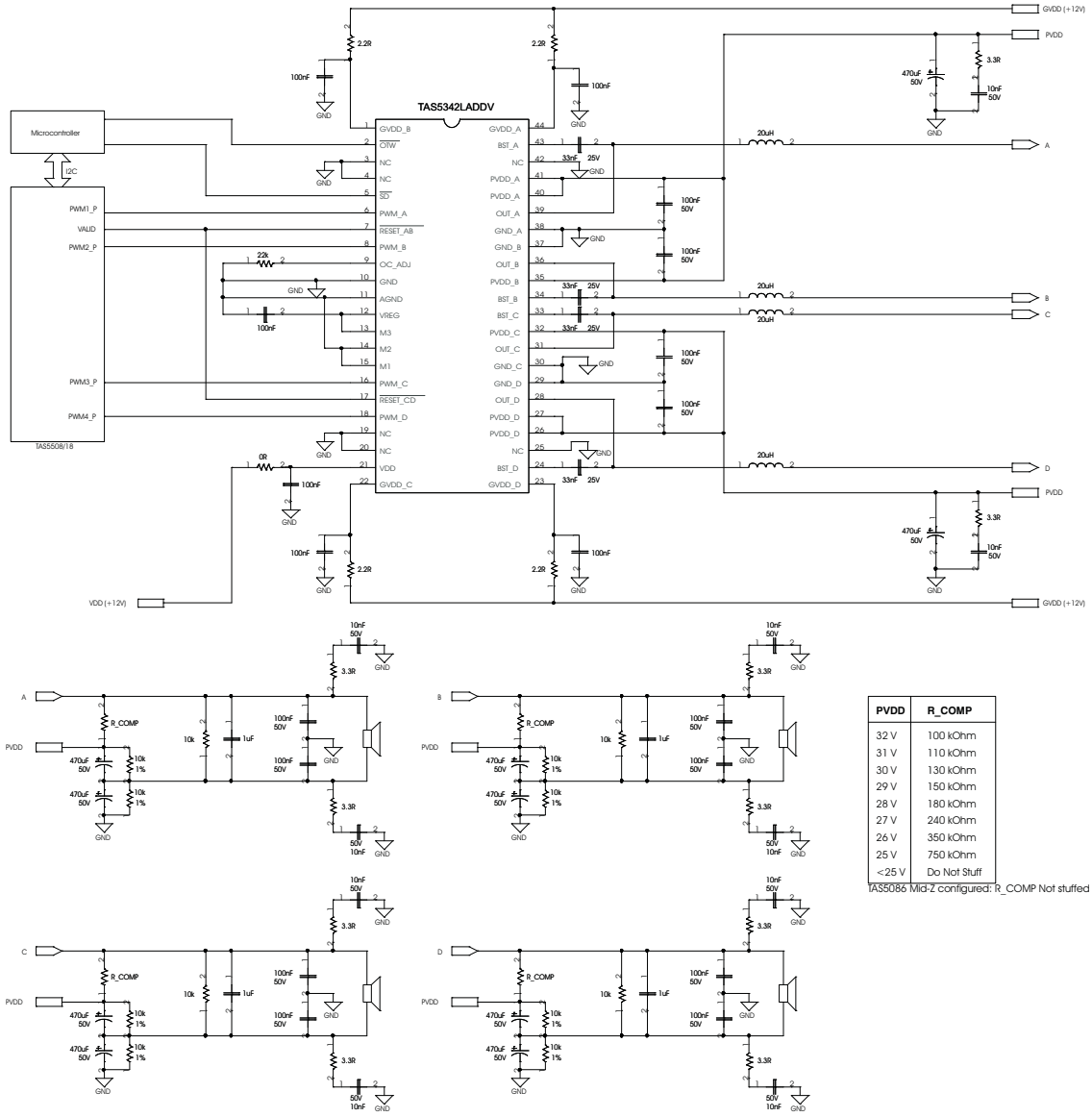



**Figure 15. Typical Non-Differential (1N) BTL Application With AD Modulation Filters**


Copyright © 2008, Texas Instruments Incorporated




| PVDD | R_COMP |
|---|---|
| 32 V | 100 kOhm |
| 31 V | 110 kOhm |
| 30 V | 130 kOhm |
| 29 V | 150 kOhm |
| 28 V | 180 kOhm |
| 27 V | 240 kOhm |
| 26 V | 350 kOhm |
| 25 V | 750 kOhm |
| <25 V | Do Not Stuff |

TAS5086 Mid-Z configured: R_COMP Not stuffed

**Figure 16. Typical SE Application**

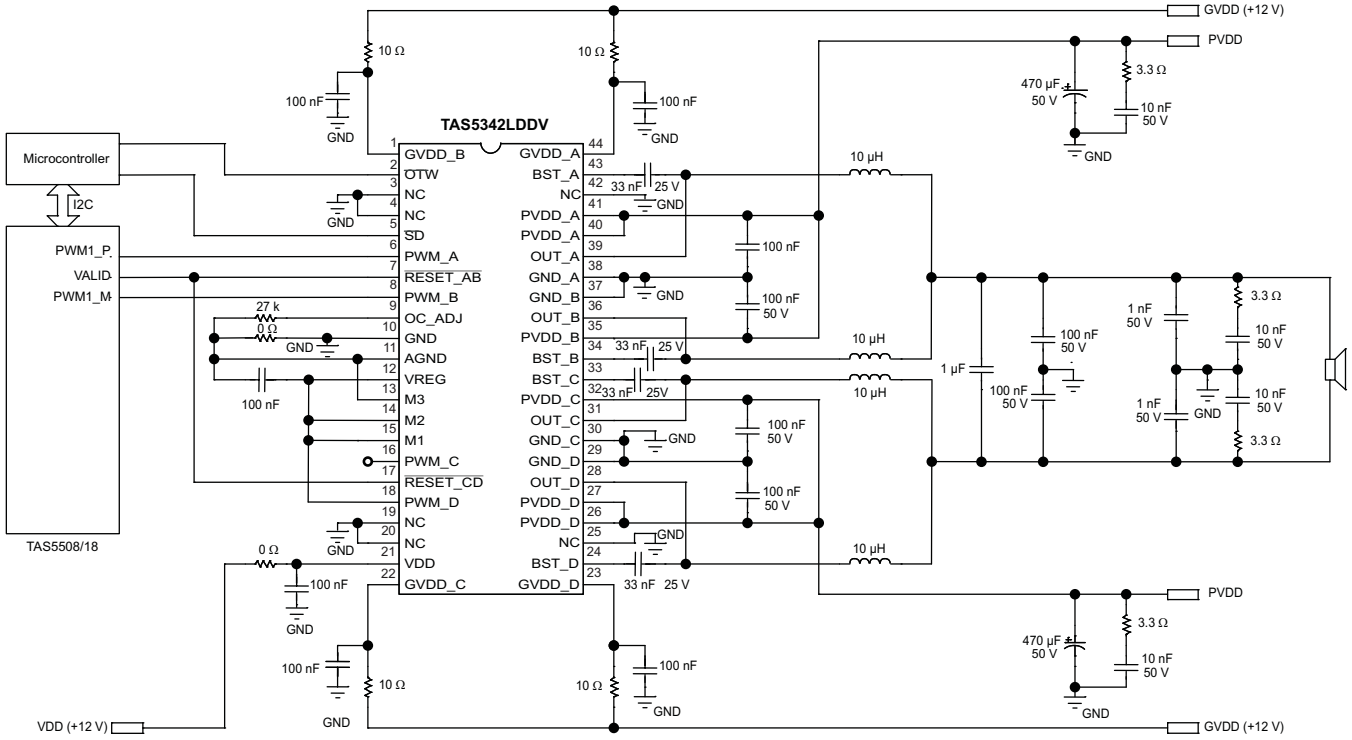



**Figure 17. Typical Differential (2N) PBTL Application With AD Modulation Filters**

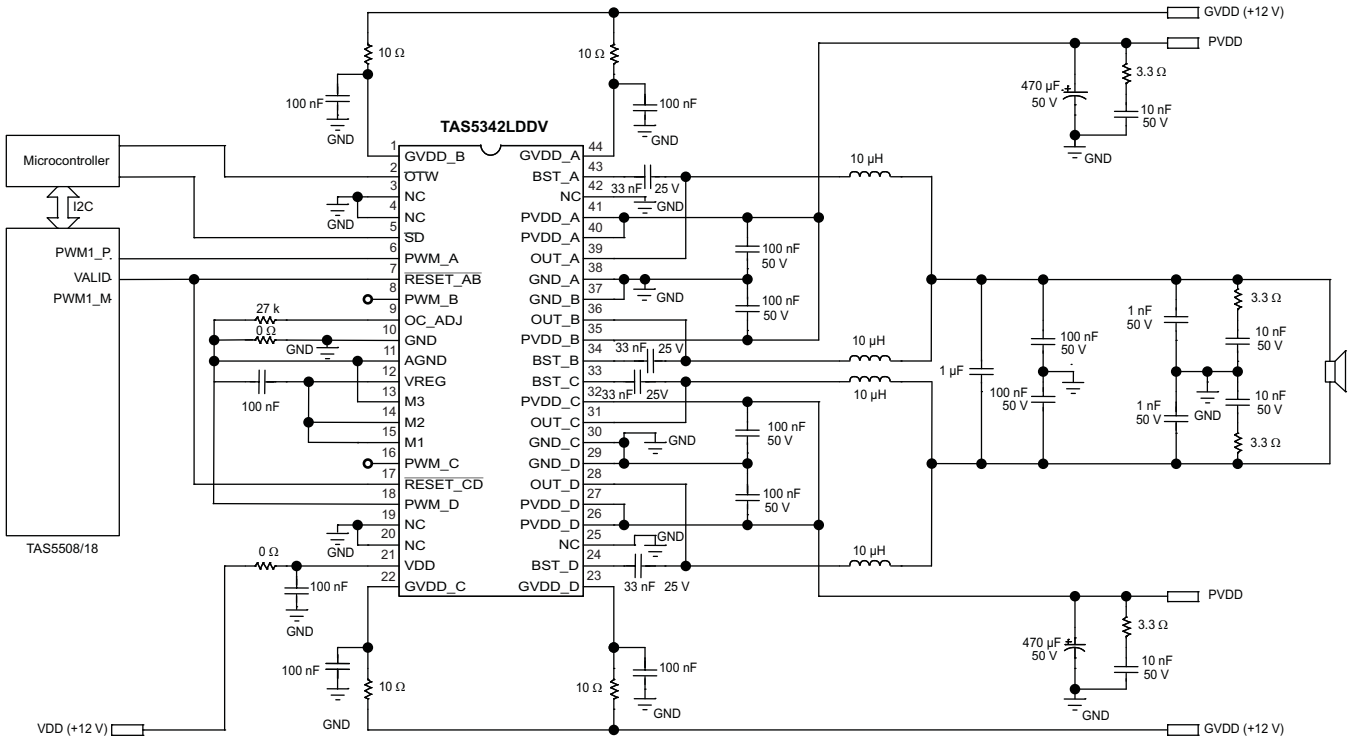



**Figure 18. Typical Non-Differential (1N) PBTL Application**


Copyright © 2008, Texas Instruments Incorporated

# THEORY OF OPERATION

## POWER SUPPLIES

To facilitate system design, the TAS5342LA needs only a 12-V supply in addition to the (typical) 32.0-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only an external capacitor for each half-bridge.

In order to provide outstanding electrical and acoustical characteristics, the PWM signal path including gate drive and output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate gate drive supply (GVDD_X), bootstrap pins (BST_X), and power-stage supply pins (PVDD_X). Furthermore, an additional pin (VDD) is provided as supply for all common circuits. Although supplied from the same 12-V source, it is highly recommended to separate GVDD_A, GVDD_B, GVDD_C, GVDD_D, and VDD on the printed-circuit board (PCB) by RC filters (see application diagram for details). These RC filters provide the recommended high-frequency isolation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided. (See reference board documentation for additional information.)

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 352 kHz to 384 kHz, it is recommended to use 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle. In an application running at a reduced switching frequency, generally 192 kHz, the bootstrap capacitor might need to be increased in value.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X pin is decoupled with a 100-nF ceramic capacitor placed as close as possible to each supply pin. It is recommended to follow the PCB layout of the TAS5342LA reference design. For additional information on recommended power supply and required components, see the application diagrams given previously in this data sheet.

The 12-V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 32.0 V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit. Moreover, the TAS5342LA is fully protected against erroneous power-stage turnon due to parasitic gate charging. Thus, voltage-supply ramp rates (dV/dt) are non-critical within the specified range (see the *Recommended Operating Conditions* section of this data sheet).

## SYSTEM POWER-UP/POWER-DOWN SEQUENCE

### Powering Up

The TAS5342LA does not require a power-up sequence. The outputs of the H-bridges remain in a high-impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, it is recommended to hold RESET_AB and RESET_CD in a low state while powering up the device. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output.

When the TAS5342LA is being used with TI PWM modulators such as the TAS5518, no special attention to the state of RESET_AB and RESET_CD is required, provided that the chipset is configured as recommended.

### Powering Down

The TAS5342LA does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical*

Copyright © 2008, Texas Instruments Incorporated

*Characteristics* section of this data sheet). Although not specifically required, it is a good practice to hold RESET_AB and RESET_CD low during power down, thus preventing audible artifacts including pops or clicks.

When the TAS5342LA is being used with TI PWM modulators such as the TAS5518, no special attention to the state of RESET_AB and RESET_CD is required, provided that the chipset is configured as recommended.

## MID Z SEQUENCE COMPATABILITY

The TAS5342LA is compatable with the Mid Z sequence of the TAS5086 Modulator. The Mid Z Sequence is a series of pulses that is generated by the modulator. This sequence causes the power stage to slowly enable its outputs as it begins to switch.

By slowly starting the PWM switching, the impulse response created by the onset of switching is reduced. This impulse response is the acoustic artifact that is heard in the output transducers (loudspeakers) and is commonly termed "click" or "pop".

The low acoustic artifact noise of the TAS5342LA will be further decreased when used in conjunction with the TAS5086 modulator with the Mid Z Sequence enabled.

The Mid Z sequence is primarily used for the single-ended output configuration. It facilitates a "softer" PWM output start after the split cap output configuration is charged.

## ERROR REPORTING

The $\overline{SD}$ and $\overline{OTW}$ pins are both active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown is signaled by the $\overline{SD}$ pin going low. Likewise, $\overline{OTW}$ goes low when the device junction temperature exceeds 125°C (see the following table).

| $\overline{SD}$ | $\overline{OTW}$ | DESCRIPTION |
|---|---|---|
| 0 | 0 | Overtemperature (OTE) or overload (OLP) or undervoltage (UVP) |
| 0 | 1 | Overload (OLP) or undervoltage (UVP) |
| 1 | 0 | Junction temperature higher than 125°C (overtemperature warning) |
| 1 | 1 | Junction temperature lower than 125°C and no OLP or UVP faults (normal operation) |

Note that asserting either $\overline{RESET_AB}$ or $\overline{RESET_CD}$ low forces the $\overline{SD}$ signal high, independent of faults being present. TI recommends monitoring the $\overline{OTW}$ signal using the system microcontroller and responding to an overtemperature warning signal by, e.g., turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3 V is provided on both $\overline{SD}$ and $\overline{OTW}$ outputs. Level compliance for 5-V logic can be obtained by adding external pullup resistors to 5 V (see the *Electrical Characteristics* section of this data sheet for further specifications).

## DEVICE PROTECTION SYSTEM

The TAS5342LA contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overload, overtemperature, and undervoltage. The TAS5342LA responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the $\overline{SD}$ pin low. In situations other than overload and over-temperature error ($\overline{OTE}$), the device automatically recovers when the fault condition has been removed, i.e., the supply voltage has increased.

The device will function on errors, as shown in the following table.

| BTL MODE | | PBTL MODE | | SE MODE | |
|---|---|---|---|---|---|
| Local Error In | Turns Off | Local Error In | Turns Off | Local Error In | Turns Off |
| A | A + B | A | A + B + C + D | A | A + B |
| B | | B | | B | |
| C | C + D | C | | C | C + D |
| D | | D | | D | |

Bootstrap UVP does not shutdown according to the table, it shutsdown the respective halfbridge.

### Use of TAS5342LA in High-Modulation-Index Capable Systems

This device requires at least 30 ns of low time on the output per 384-kHz PWM frame rate in order to keep the bootstrap capacitors charged. As an example, if the modulation index is set to 99.2% in the TAS5508, this setting allows PWM pulse durations down to 10 ns. This signal, which does not meet the 30-ns requirement, is sent to the PWM_X pin and this low-state pulse time does not allow the bootstrap capacitor to stay charged. The TAS5342LA device requires limiting the TAS5508 modulation index to 97.7% to keep the bootstrap capacitor charged under all signals and loads.

The TAS5342LA contains a bootstrap capacitor under voltage protection circuit (BST_UVP) that monitors


Copyright © 2008, Texas Instruments Incorporated

the voltage on the bootstrap capacitors. When the voltage on the bootstrap capacitors is less than required for proper control of the High-Side MOSFETs, the device will initiate bootstrap capacitor recharge sequences until the bootstrap capacitors are properly charged for robust operation. This function may be activated with PWM pulses less than 30 nS.

Therefore, TI strongly recommends using a TI PWM processor, such as TAS5518, TAS5086 or TAS5508, with the modulation index set at 97.7% to interface with TAS5342LA.

### Overcurrent (OC) Protection With Current Limiting and Overload Detection

The device has independent, fast-reacting current detectors with programmable trip threshold (OC threshold) on all high-side and low-side power-stage FETs. See the following table for OC-adjust resistor values. The detector outputs are closely monitored by two protection systems. The first protection system controls the power stage in order to prevent the output current from further increasing, i.e., it performs a current-limiting function rather than prematurely shutting down during combinations of high-level music transients and extreme speaker load impedance drops. If the high-current situation persists, i.e., the power stage is being overloaded, a second protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state. Current limiting and overload protection are independent for half-bridges A and B and, respectively, C and D. That is, if the bridge-tied load between half-bridges A and B causes an overload fault, only half-bridges A and B are shut down.

- For the lowest-cost bill of materials in terms of component selection, the OC threshold measure should be limited, considering the power output requirement and minimum load impedance. Higher-impedance loads require a lower OC threshold.
- The demodulation-filter inductor must retain at least 5 μH of inductance at twice the OC threshold setting.

Unfortunately, most inductors have decreasing inductance with increasing temperature and increasing current (saturation). To some degree, an increase in temperature naturally occurs when operating at high output currents, due to core losses and the dc resistance of the inductor's copper winding. A thorough analysis of inductor saturation and thermal properties is strongly recommended.

Setting the OC threshold too low might cause issues such as lack of enough output power and/or unexpected shutdowns due to too-sensitive overload detection.

In general, it is recommended to follow closely the external component selection and PCB layout as given in the *Application* section.

For added flexibility, the OC threshold is programmable within a limited range using a single external resistor connected between the OC_ADJ pin and AGND. (See the *Electrical Characteristics* section of this data sheet for information on the correlation between programming-resistor value and the OC threshold.) It should be noted that a properly functioning overcurrent detector assumes the presence of a properly designed demodulation filter at the power-stage output. Short-circuit protection is not provided directly at the output pins of the power stage but only on the speaker terminals (after the demodulation filter). It is required to follow certain guidelines when selecting the OC threshold and an appropriate demodulation inductor:

| OC-Adjust Resistor Values (kΩ) | Max. Current Before OC Occurs (A), $T_C$=75°C |
|---|---|
| 22 | 8.4 A |
| 33 | 6.8 A |
| 47 | 5.3 A |

The reported max peak current in the table above is measured with continuous current in 1 Ω, one channel active and the other one muted.

### Pin-To-Pin Short Circuit Protection System (PPSC)

The PPSC detection system protects the device from permanent damage in the case that a power output pin (OUT_X) is shorted to GND_X or PVDD_X. For comparison the OC protection system detects an over current after the demodulation filter where PPSC detects shorts directly at the pin before the filter. PPSC detection is performed at startup i.e. when VDD is supplied, consequently a short to either GND_X or PVDD_X after system startup will not activate the PPSC detection system. When PPSC detection is activated by a short on the output, all half bridges are kept in a Hi-Z state until the short is removed, the device then continues the startup sequence and starts switching. The detection is controlled globally by a two step sequence. The first step ensures that there are no shorts from OUT_X to GND_X, the second step tests that there are no shorts from OUT_X to PVDD_X. The total duration of this process is roughly proportional to the capacitance of the output LC filter. The typical duration is < 15 ms/μF. While the PPSC detection is in progress, $\overline{SD}$ is kept low, and the device will not react to changes applied to the $\overline{RESET}$ pins. If no shorts are present the PPSC detection passes, and $\overline{SD}$ is released. A device reset will not start a new PPSC detection.

Copyright © 2008, Texas Instruments Incorporated

PPSC detection is enabled in BTL and PBTL output configurations, the detection is not performed in SE mode. To make sure not to trip the PPSC detection system it is recommended not to insert resistive load to GND_X or PVDD_X.

### Overtemperature Protection

The TAS5342LA has a two-level temperature-protection system that asserts an active-low warning signal ($\overline{OTW}$) when the device junction temperature exceeds 125°C (nominal) and, if the device junction temperature exceeds 155°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{SD}$ being asserted low. OTE is latched in this case. To clear the OTE latch, either $\overline{RESET_AB}$ or $\overline{RESET_CD}$ must be asserted. Thereafter, the device resumes normal operation.

### Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the TAS5342LA fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach stated in the Electrical Characteristics Table. Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and $\overline{SD}$ being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

## DEVICE RESET

Two reset pins are provided for independent control of half-bridges A/B and C/D. When $\overline{RESET_AB}$ is asserted low, all four power-stage FETs in half-bridges A and B are forced into a high-impedance (Hi-Z) state. Likewise, asserting $\overline{RESET_CD}$ low forces all four power-stage FETs in half-bridges C and D into a high-impedance state. Thus, both reset pins are well suited for hard-muting the power stage if needed.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the reset inputs low enables weak pulldown of the half-bridge outputs. In the SE mode, the weak pulldowns are not enabled, and it is therefore recommended to ensure bootstrap capacitor charging by providing a low pulse on the PWM inputs when reset is asserted high.

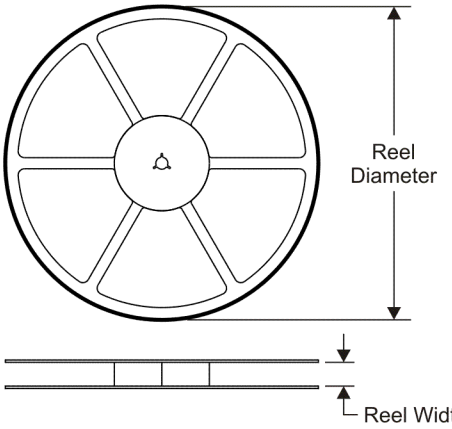
Asserting either reset input low removes any fault information to be signalled on the $\overline{SD}$ output, i.e., $\overline{SD}$ is forced high.

A rising-edge transition on either reset input allows the device to resume operation after an overload fault. To ensure thermal reliability, the rising edge of reset must occur no sooner than 4ms after the falling edge of $\overline{SD}$.

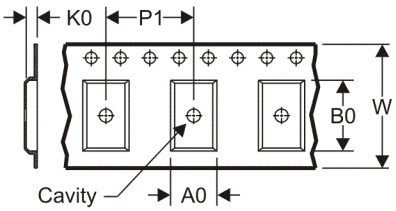

Copyright © 2008, Texas Instruments Incorporated

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

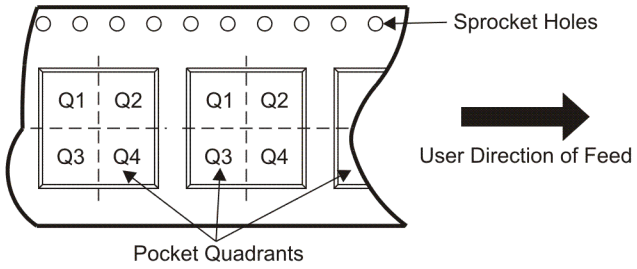



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

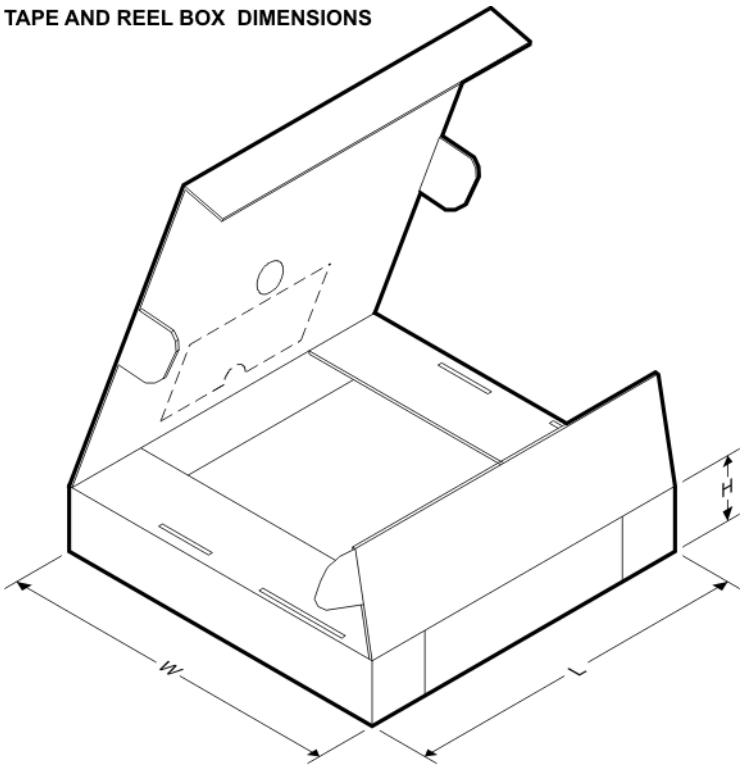
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TAS5342LADDVR | HTSSOP | DDV | 44 | 2000 | 330.0 | 24.4 | 8.6 | 15.6 | 1.8 | 12.0 | 24.0 | Q1 |

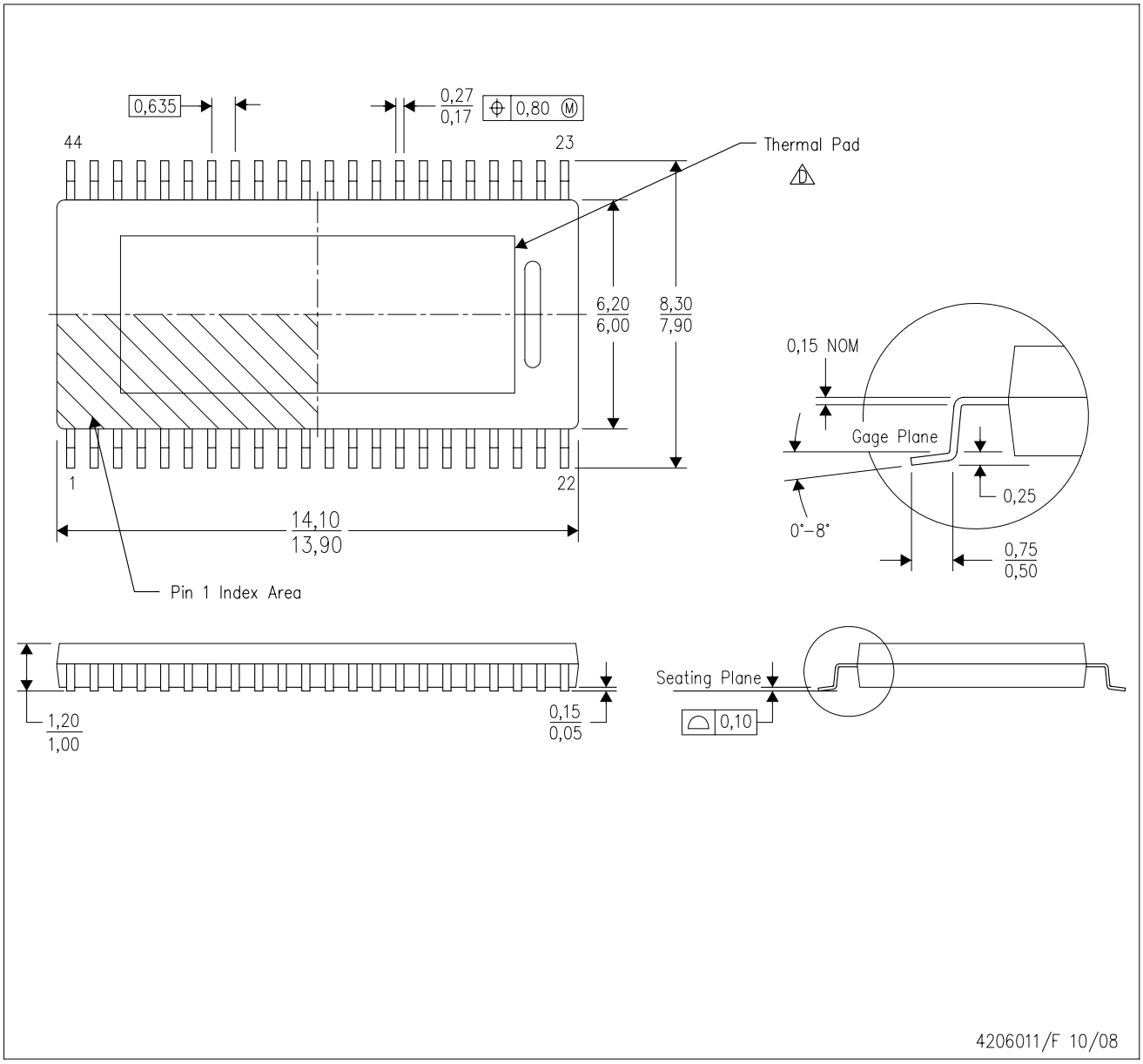
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TAS5342LADDVR | HTSSOP | DDV | 44 | 2000 | 346.0 | 346.0 | 41.0 |

DDV (R–PDSO–G44) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.

**PowerPAD is a trademark of Texas Instruments.**

# THERMAL PAD MECHANICAL DATA

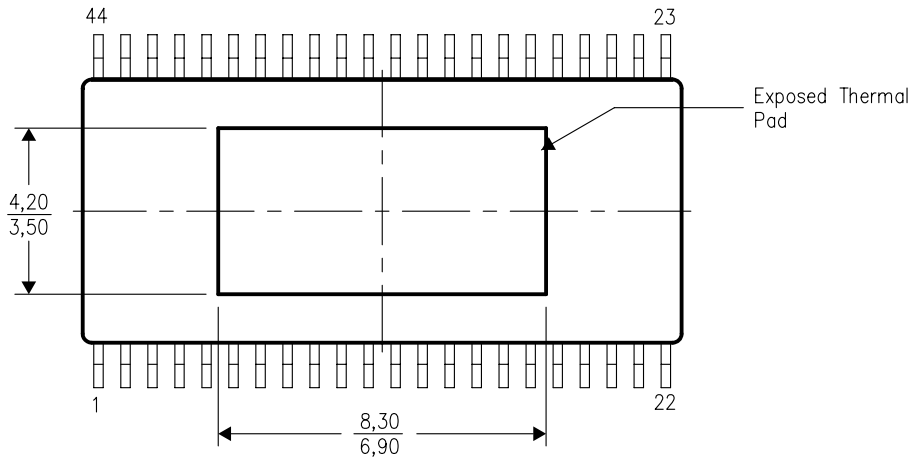
## DDV (R–PDSO–G44)

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| **Products** | | **Applications** | |
|---|---|---|---|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Clocks and Timers | www.ti.com/clocks | Digital Control | www.ti.com/digitalcontrol |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| RFID | www.ti-rfid.com | Telephony | www.ti.com/telephony |
| RF/IF and ZigBee® Solutions | www.ti.com/lprf | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated