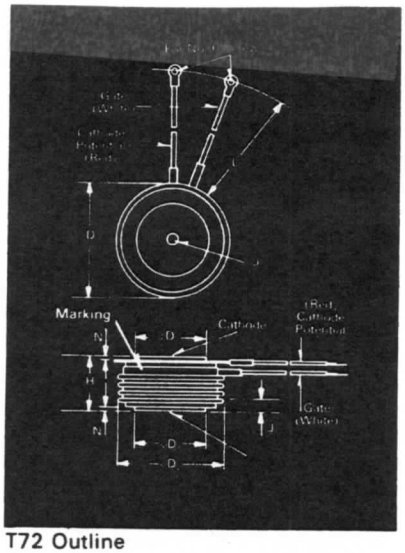
*New Jersey Semi-Conductor Products, Inc.*

20 STERN AVE.
SPRINGFIELD, NEW JERSEY 07081
U.S.A.

TELEPHONE: (973) 376-2922
(212) 227-6005
FAX: (973) 376-8960

# T72H SERIES

## SCR FAST SWITCHING
## 475A Avg.
## (750 RMS)
## UP TO 800 VOLTS




T72 Outline

| Symbol | Inches | | Millimeters | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| φD | 2.250 | 2.290 | 57.15 | 58.17 |
| φD₁ | 1.333 | 1.343 | 33.86 | 34.11 |
| φD₂ | 2.030 | 2.090 | 51.56 | 53.09 |
| H | 1.020 | 1.060 | 25.91 | 26.92 |
| φJ | .135 | .145 | 3.43 | 3.68 |
| J₁ | .075 | .090 | 1.91 | 2.29 |
| L | 7.75 | 8.50 | 196.85 | 215.90 |
| N | .040 | | 1.02 | |

**Creep Distance**—1.00 in. min. (25.40 mm).
**Strike Distance**—.69 in. min. (17.53 mm).
(In accordance with NEMA standards.)
Finish—Nickel Plate.
Approx. Weight—8 oz. (227 g).
1. Dimension "H" is a clamped dimension.

**Features:**
- Interdigitated, di/namic Gate structure
- Hard Commutation Turn-Off
- Forward Blocking Voltage Capabilities to 800 Volts
- Low Switching Losses at High Frequency
- Soft Commutation (Feedback Diode) Testing Available
- High di/dt with soft gate control

**Applications:**
- Induction Heating
- Transportation
- Inverters

### Ordering Information

| Type | Voltage | | Current | | Turn-off | | Gate current | | Leads | |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | $V_{DRM}$ and $V_{RRM}$ (V) | Code | $I_{T(av)}$ (A) | Code | tq usec | Code | $I_{GT}$ (ma) | Code | Case | Code |
| T72H | 100 | 01 | 475 | 48 | 20 | 6 | 150 | 4 | T72 | DN |
| | 200 | 02 | | | 25 | B | | | | |
| | 300 | 03 | | | 30 | 5 | | | | |
| | 400 | 04 | | | 40 | 4 | | | | |
| | 500 | 05 | | | | | | | | |
| | 600 | 06 | | | | | | | | |
| | 700 | 07 | | | | | | | | |
| | 800 | 08 | | | | | | | | |

### Example

Obtain optimum device performance for your application by selecting proper Order Code.

Type T72H rated at 475 A average with $V_{DRM}$ = 400V
$I_{GT}$ = 150 ma, $t_q$ = 30 μsec max. and leads—order as:

| Type | | | | Voltage | | Current | | Turn Off | Gate Current | Leads | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| T | 7 | 2 | H | 0 | 4 | 4 | 8 | 5 | 4 | D | N |

NJ Semi-Conductors reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by NJ Semi-Conductors is believed to be both accurate and reliable at the time of going to press. However, NJ Semi-Conductors assumes no responsibility for any errors or omissions discovered in its use. NJ Semi-Conductors encourages customers to verify that datasheets are current before placing orders.

**Quality Semi-Conductors**

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## Voltage ①

| Blocking State Maximums ($T_J$ = 125°C) | Symbol | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Repetitive peak forward blocking voltage, V | $V_{DRM}$ | 100 | 200 | 300 | 400 | 500 | 600 | 700 | 800 |
| Repetitive peak reverse voltage, V | $V_{RRM}$ | 100 | 200 | 300 | 400 | 500 | 600 | 700 | 800 |
| Non-repetitive transient peak reverse voltage, $t \leq 5.0$ msec, V | $V_{RSM}$ | 200 | 300 | 400 | 500 | 600 | 700 | 800 | 900 |
| Forward leakage current, mA peak | $I_{DRM}$ | ← 35 → | | | | | | | |
| Reverse leakage current, mA peak | $I_{RRM}$ | ← 35 → | | | | | | | |

## Current

| Conducting State Maximums ($T_J$ = 125°C) | Symbol | T72H__48 |
|---|---|---|
| RMS forward current, A | $I_{T(rms)}$ | 750 |
| Ave. forward current, A | $I_{T(av)}$ | 475 |
| One-half cycle surge current②, A | $I_{TSM}$ | 8000 |
| $I^2t$ for fusing (for times ≥ 8.3 ms) $A^2$ sec. | $I^2t$ | 265,000 |
| Forward voltage drop at ITM = 1500A and TJ = 25°C, V | $V_{TM}$ | 1.55 |
| Min. repetitive di/dt ①④⑥ A/μsec | di/dt | 600 |

## Switching

| ($T_J$ = 25°C) | Symbol | |
|---|---|---|
| Max. turn-off time, IT = 400A, TJ = 125°C tp = 100 μsec. dirR/dt = 25 A/μsec., reapplied dv/dt = 200V/μsec. linear to 0.8 VDRM, μsec. ③⑦ | tq | 20 to 40 |
| Typ. delay time, ITM = 1000A TD = .8 VDRM①, μsec | td | .5 |
| Typ turn-on-time $I_{TM}$ = 1000A, μsec | $t_{on}$ | 3.0 |
| Min. critical dv/dt exponential to .8 VDRM, TJ = 125°C, V/μsec ⑦⑤ | dv/dt | 300 |
| Min. di/dt, non-repetitive, A/μsec ①④⑥ | di/dt | 1200 |

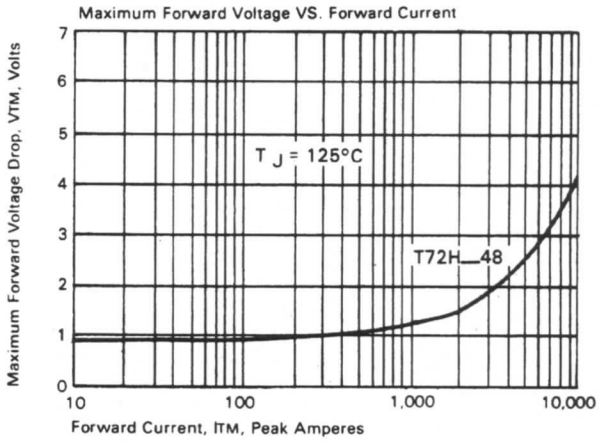
## Gate

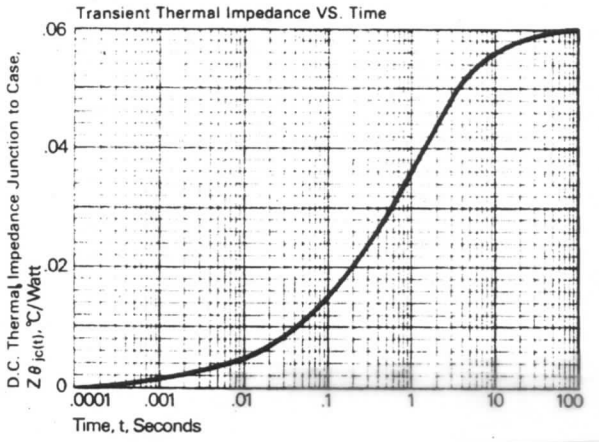
| Maximum Parameters ($T_J$ = 25°C) | Symbol | |
|---|---|---|
| Gate current to trigger at $V_D$ = 12V, mA | $I_{GT}$ | 150 |
| Gate voltage to trigger at $V_D$ = 12V, V | $V_{GT}$ | 3 |
| Non-triggering gate voltage, $T_J$ = 125°C, and rated $V_{DRM}$, V | $V_{GDM}$ | .25 |
| Peak forward gate current, A | $I_{GTM}$ | 4 |
| Peak reverse gate voltage, V | $V_{GRM}$ | 5 |
| Peak gate power, Watts | $P_{GM}$ | 16 |
| Average gate power, Watts | $P_{G(av)}$ | 3 |

## Thermal and Mechanical

| | Symbol | |
|---|---|---|
| Min., Max. oper. junction temp., °C | $T_J$ | −40 to +125 |
| Min., Max. storage temp., °C | Tstg | −40 to +150 |
| Max. mounting force, lb. ... ① | | 2000 to 2400 |
| Thermal resistance①, double-side cooling, junction to case, °C/Watt | $R_{\theta JC}$ | .06 |
| Case to sink, lubricated, °C/Watt | $R_{\theta CS}$ | .02 |

① Consult recommended mounting procedures.
② Applies for zero or negative gate bias.
③ Per JEDEC RS-397, 5.2.2.1.
④ With recommended gate drive.
⑤ Higher dv/dt ratings available, consult factory.
⑥ Per JEDEC standard RS-397, 5.2.2.6.
⑦ For operation with antiparallel diode, consult factory.




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