Data Sheet
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microelectronics group

Lucent Technologies
Bell Labs Innovations



T7290A DS1/T1/CEPT/E1 Line Interface

Features

- Fully integrated DS1/T1/CEPT/E1 line interface
- For use in systems that are compliant with CB119, AT&T PUB 43801, AT&T PUB 43802, AT&T PUB 62411, TR-TSY-000170, TR-TSY-000009, ITU-T G.703, G.735, G.823, and I.431 specifications
- Dual-rail system interface
- On-chip transmit equalization
- On-chip jitter attenuator
- Monolithic clock recovery with frequency-acquisition aide
- High jitter accommodation (>0.4 U.I.)
- No external crystal required
- Three clocking modes to accommodate multiple system clocking requirements
- Multiple link-status and alarm features
- Microprocessor interface option
- AIS (blue alarm) transmission
- Loopback modes for fault isolation
- Minimal external circuitry required

Description

The Lucent Technologies Microelectronics Group T7290A DS1/T1/CEPT/E1 Line Interface is a fully integrated line transceiver capable of operation at the domestic DS1/T1 carrier rate (1.544 Mbits/s) or the international CEPT/E1 rate (2.048 Mbits/s). The T7290A device combines features found in existing line-interface devices with additional desirable features.

The on-chip, low-impedance output drivers provide shaped waveforms to the transformer, guaranteeing template conformance. The T7290A device interfaces to the digital cross connect (DSX) at lengths up to 655 feet during DS1 operation and interfaces to line impedances of 75 Ω or 120 Ω during CEPT operation. The device line interface also can transmit waveforms compatible with T1 lines.

The T7290A line interface provides phase-locked loop clock recovery and data retiming on received data. Also, on-chip, selectable jitter attenuation is available. The jitter attenuator can be placed in the receive or transmit data path. No external crystals are required with the T7290A device.

Digital control circuitry allows for multiple loopbacks, testing, and alarm status monitoring. A microprocessor interface option allows for either control via a microprocessor or direct pin-selectable control (hardware mode).

The T7290A device is manufactured by using a low-power CMOS technology and is available in a 28-pin, plastic SOJ package or a 28-pin, plastic DIP package.

Note: Modification of an existing T7290 application may be required when migrating to a T7290A-based architecture. The functions of the TBS, TSC, LP1, DLOS, and LOS pins have been changed or modified. Please refer to the T7290A Migration from T7290 section of this data sheet.

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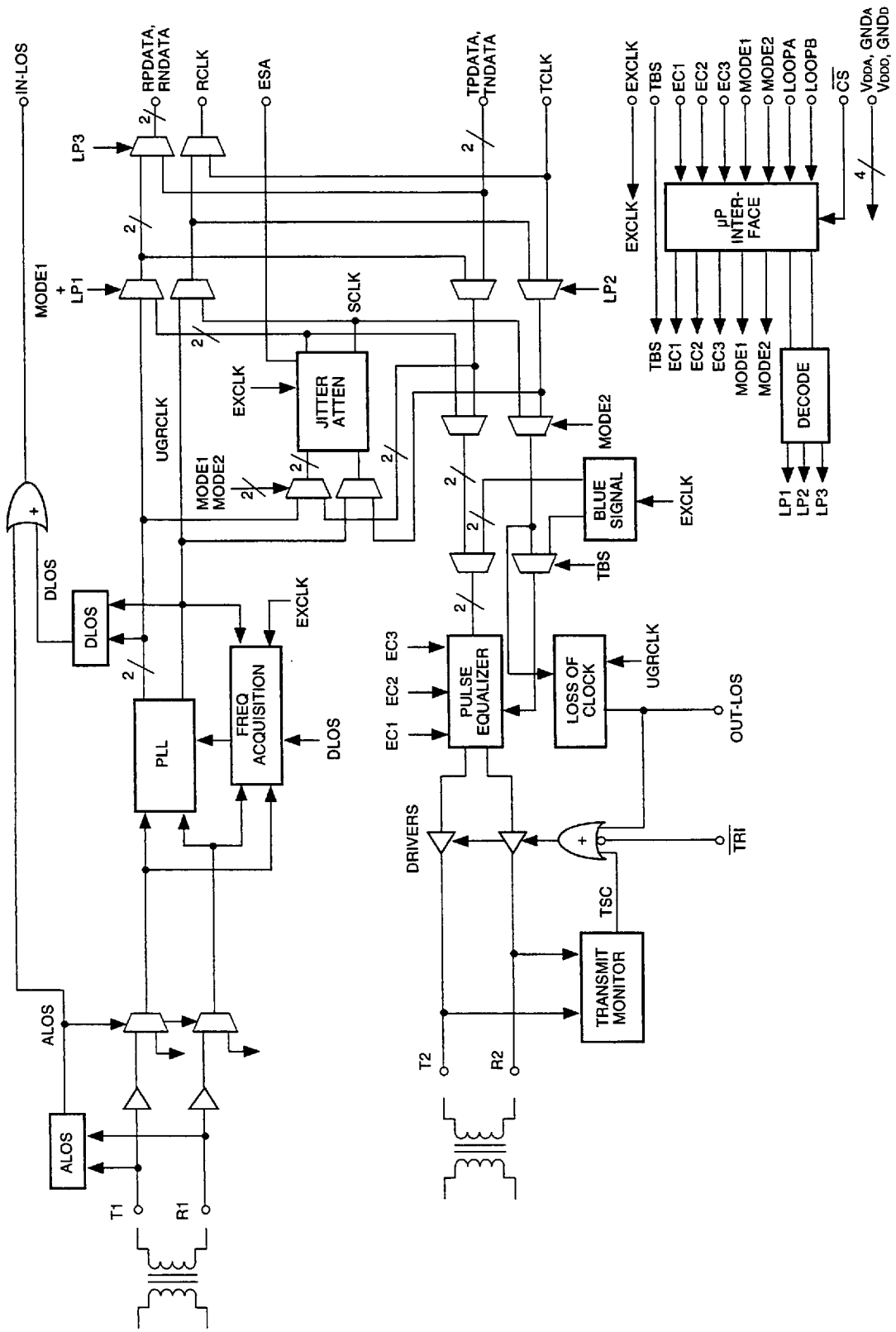
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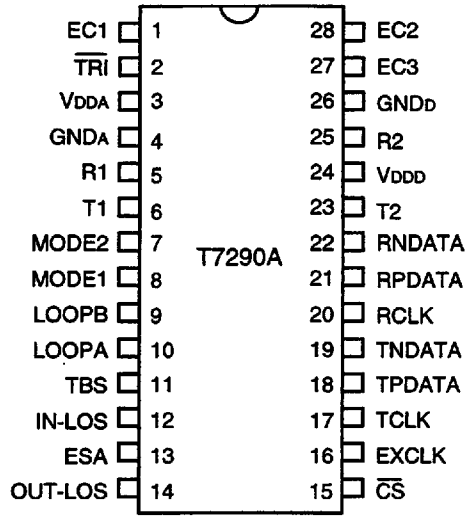
Description (continued)



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Figure 1. Block Diagram

Pin Information



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Figure 2. Pin Diagram

Table 1. Pin Descriptions

Pin	Symbol	Type*	Name/Function
1, 27, 28	EC1, EC3, EC2	I^d	**Equalizer/Rate Control 1—3.** Three control leads for selecting transmit equalization.
2	$\overline{TRI}$	I^u	**3-State (Active-Low).** This pin is set low to configure all output buffers into a high-impedance state during in-circuit testing.
3	V_{DDA}	—	**5 V ± 5% Analog Supply.** The powerup rise time (0 V to 4.75 V) must be less than 15 ms.
4	GND_A	—	**Analog Ground.**
5	R1	I	**Receive Bipolar Ring.** Negative bipolar receive data.
6	T1	I	**Receive Bipolar Tip.** Positive bipolar receive data.
7, 8	MODE2, MODE1	I^d	**Mode Select 2 and 1.** Two control leads for selecting clock and data paths through the jitter attenuator.
9, 10	LOOPB, LOOPA	I^d	**Loopback Control B and A.** Two control leads for selecting clock and data loopback paths.
11	TBS	I^d	**Transmit Blue Signal (AIS).** This pin is set high to transmit the blue signal (all 1s). A remote loopback (LP2) has priority over the transmit blue signal.
12	IN-LOS	O	**Input Loss of Signal.** This pin is set high if analog loss of signal at the receiver inputs is detected or if digital loss of signal of the recovered data is detected. IN-LOS can be tied directly to TBS to initiate a transmit blue signal upon loss of signal.

* I = input, O = output, I^u = input with pull-up, I^d = input with pull-down.

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Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type*	Name/Function
13	ESA	O	**Jitter Attenuator Alarm.** This pin is set high if the phase jitter of the incoming signal exceeds the tolerance of the jitter attenuator's buffer. This may result in a loss of receive data.
14	OUT-LOS	O	**Output Loss of Signal.** This pin is set high when either the transmit clock (TCLK) or the smoothing clock (SCLK) output of the jitter attenuator is absent.
15	$\overline{CS}$	I^d	**Chip Select for Microprocessor Interface (Active-Low).** $\overline{CS}$ loads data into the device on its falling edge and latches the data on its rising edge. $\overline{CS}$ is set low for hardware mode.
16	EXCLK	I	**External Clock.** DS1/T1 clock signal (1.544 MHz ± 130 ppm) or CEPT/E1 clock signal (2.048 MHz ± 80 ppm) for transmit blue signal, jitter attenuator calibration, and PLL acquisition aid. EXCLK must be an independent clock to guarantee device performance for all specifications. This clock should be continuously active (i.e., ungapped and unswitched) and void of jitter for the above features to operate.
17	TCLK	I	**Transmit Clock.** DS1/T1 clock signal (1.544 MHz ± 130 ppm) or CEPT/E1 clock signal (2.048 MHz ± 80 ppm).
18	TPDATA	I	**Transmit Positive Data.** DS1/T1 (1.544 Mbits/s) or CEPT/E1 (2.048 Mbits/s) positive bipolar data.
19	TNDATA	I	**Transmit Negative Data.** DS1/T1 (1.544 Mbits/s) or CEPT/E1 (2.048 Mbits/s) negative bipolar data.
20	RCLK	O	**Receive Clock.** Recovered receive clock signal for the terminal equipment.
21	RPDATA	O	**Receive Positive Data.** DS1/T1 (1.544 Mbits/s) or CEPT/E1 (2.048 Mbits/s) recovered positive data (NRZ).
22	RNDATA	O	**Receive Negative Data.** DS1/T1 (1.544 Mbits/s) or CEPT/E1 (2.048 Mbits/s) recovered negative data (NRZ).
23	T2	O	**Transmit Bipolar Tip.** Positive bipolar transmit data.
24	V_{DDD}	—	**5 V ± 5% Digital Supply.** The powerup rise time (0 V to 4.75 V) must be less than 15 ms.
25	R2	O	**Transmit Bipolar Ring.** Negative bipolar transmit data.
26	GND_D	—	**Digital Ground.**

* I = input, O = output, I^u = input with pull-up, I^d = input with pull-down.

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Receiver

Data Interface

The receive line-interface transmission format of the T7290A device is alternate mark inversion (AMI). The receive digital output format is dual-rail, nonreturn to zero (NRZ). Receiver specifications are shown in Table 2.

Clock Recovery and Data Retiming

The bipolar input signals from T1 and R1 are peak-detected and sliced by the receiver front end. Timing recovery is performed by a phase-locked loop (PLL) that locks an internal free-running, current-controlled oscillator (ICO) to the data-rate component. EC1, EC2, and EC3 rate control inputs must be set appropriately for DS1 or CEPT/E1 operation.

Frequency-Acquisition Aide

For robust operation, PLL is enhanced with a frequency-acquisition capability. The frequency-acquisition circuitry is intended to guarantee proper phase locking during start-up situations, such as powerup or data activation. Once the T7290A device is phase-locked to data, the frequency-acquisition mode is **not** activated unless a digital loss of signal occurs, in which case RCLK is frequency-locked/phase-locked to EXCLK. RCLK is always active and does not have any instantaneous phase hits or discontinuities.

A continuously active (i.e., ungapped and unswitched) reference clock must be present at EXCLK to enable the frequency-acquisition circuitry. EXCLK must be an independent reference such as an oscillator or system clock for proper operation. The EXCLK clock frequency must be 1.544 MHz ± 130 ppm for T1/DS1 operation or 2.048 MHz ± 80 ppm for CEPT/E1 operation.

Table 2. Receiver Specifications

Parameter	Min	Typ	Max	Unit
Receiver Sensitivity:*				
DS1	0.85	—	—	Vp
CEPT	0.7	—	—	Vp
Analog LOS Level:				
DS1	—	0.48	—	Vp
CEPT	—	0.28	—	Vp
PLL:†				
3 dB Bandwidth	—	33	—	kHz
Peaking	—	1.2	2	dB
ICO Free-run Frequency Error	—	—	±6	%
Input Density (1s)‡	12.5	—	—	%
Return Loss:§				
51 kHz—102 kHz	12	—	—	dB
102 kHz—2.048 MHz	18	—	—	dB
2.048 MHz—3.072 MHz	14	—	—	dB

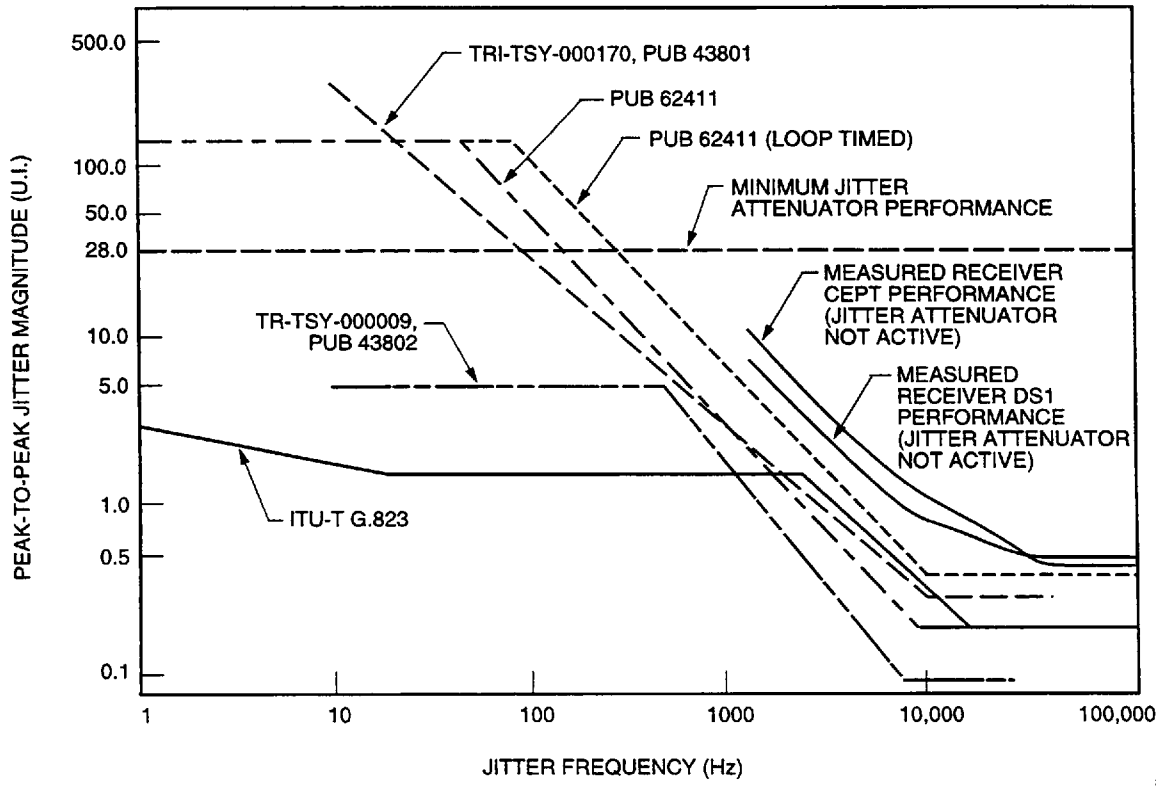
* Values shown are for flat loss only. Receiver also meets ITU-T G.703 interface immunity test (6 dB cable loss with −18 dB interference) for CEPT/E1 operation.
† Transfer characteristics (1/8 input).
‡ The maximum number of consecutive zeros = 15.
§ Return loss specifications according to ITU-T G.703/RC6367A (CEPT only).

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Receiver (continued)

Jitter

PLL is designed to accommodate large amounts of input jitter with high power supply rejection for operation in noisy environments. PLL has a minimum input jitter tolerance exceeding all requirements shown in Figure 3. The measured receiver jitter tolerance for DS1 and CEPT operation is also shown in Figure 3, with pseudorandom input data ($2^{15} - 1$) and with EXCLK synchronous with the data source. The receiver transfers incoming jitter to RCLK with no more than 2 dB of gain at any frequency, which can be further reduced with the jitter attenuator.



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Data Points (Hz, U.I.)

ITU-T G.823	TR-TSY-000170, AT&T PUB 43801	TR-TSY-000009, AT&T PUB 43802	AT&T PUB 62411	AT&T PUB 62411 Looped Timed	Measured Receiver DS1 Performance (BER = 10^{-6})	Measured Receiver CEPT Performance (BER = 10^{-6})
1, 2.9	10, 300	10, 5	1, 138	1, 138	2.0k, 6.51	2.0k, 9.43
20, 1.5	10k, 0.3	500, 5	48, 138	85, 138	5.0k, 2.03	5.0k, 2.84
2.4k, 1.5	50k, 0.3	8k, 0.1	10k, 0.2	10k, 0.4	8.0k, 1.12	8.0k, 1.70
18k, 0.2	—	40k, 0.1	100k, 0.2	100k, 0.4	10k, 0.97	10k, 1.38
100k, 0.2	—	—	—	—	15k, 0.84	15k, 1.00
—	—	—	—	—	20k, 0.66	20k, 0.84
—	—	—	—	—	30k, 0.52	30k, 0.57
—	—	—	—	—	40k, 0.49	40k, 0.48
—	—	—	—	—	70k, 0.48	70k, 0.47
—	—	—	—	—	100k, 0.48	100k, 0.47

Figure 3. PLL Jitter Tolerance Requirements

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Receiver (continued)

Data Patterns

Any data pattern with a minimum long-term 1s density of 12.5% with 15 or fewer consecutive 0s is allowed.

Loss of Signal

Both digital (DLOS) and analog (ALOS) loss-of-signal detection is used in the T7290A device. The digital signal detector is described later under the Alarms and Maintenance section. The analog signal detector uses the output of the receiver peak detector to determine if a signal is present at T1 and R1. If the input amplitude drops below approximately 0.48 Vp for DS1/T1 operation or 0.28 Vp for CEPT/E1 operation, the analog detector output becomes active. Hysteresis (250 mV) is provided in the analog detector to eliminate ALOS chattering. Either the analog or the digital detector sets IN-LOS high.

The time required to detect analog loss of signal (ALOS) depends on the incoming signal amplitude before it disappears. Typical ALOS detection times are given in Table 3.

Table 3. Typical ALOS Detection Times

Signal Amplitude (Vp)	Typical ALOS Detection Time (ms)
3.6	5.0
2.5	3.7
1.7	2.8
1.0	1.4

Transmitter

Output Pulse Shape

Transmitter specifications are shown in Table 4. The T1 pulse shape template is specified at the network interface as shown in Figure 4. The DS1 pulse shape template is specified at the DSX and is illustrated in Figure 5. CEPT transmit waveforms at the device output conform to the template shown in Figure 6.

Table 4. Transmitter Specifications

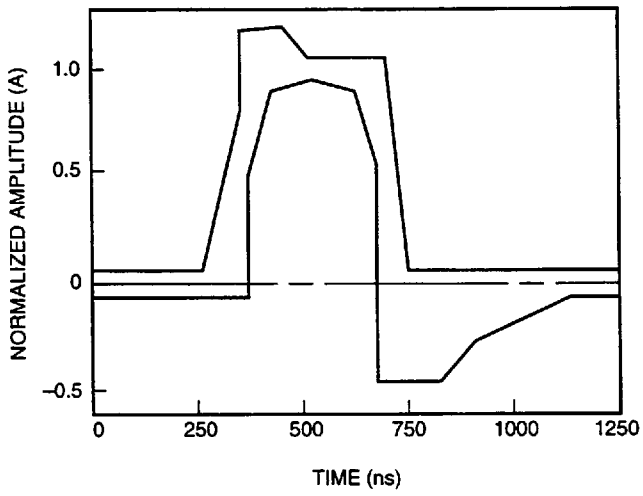
Parameter	Min	Typ	Max	Unit
Output Pulse Amplitude:*				
T1	2.7	3.0	3.3	V
DS1 (at DSX)	2.4	3.0	3.6	V
CEPT (into 75 Ω)	2.13	2.37	2.61	V
CEPT (into 120 Ω)	2.7	3.0	3.3	V
Output Pulse Width:				
T1	279	324	369	ns
DS1	330	350	370	ns
CEPT	219	244	269	ns
Output Power Levels:				
T1 (3 kHz band at 772 kHz)	12.0	16.5	19.0	dBm
T1 (3 kHz band at 1544 kHz)†	–25	–39	—	dB
DS1 (2 kHz band at 772 kHz)	12.6	16.5	17.9	dBm
DS1 (2 kHz band at 1544 kHz)†	–29	–39	—	dB
Positive/Negative Pulse Imbalance:				
DS1‡	—	0.1	0.5	dB
CEPT§	—	2	±5	%
CEPT Zero Level**	—	1	10	%
Return Loss:††				
51 kHz—102 kHz	8	—	—	dB
102 kHz—2.048 MHz	14	—	—	dB
2.048 MHz—3.072 MHz	10	—	—	dB

* In accordance with the interfaces described in the Line Termination section under Applications.
† Below the power at 772 kHz.
‡ Total power difference.
§ Percentage of the pulse amplitude and pulse width.
** Percentage of the pulse amplitude.
†† Meets CH-PTT return loss specifications (CEPT only).

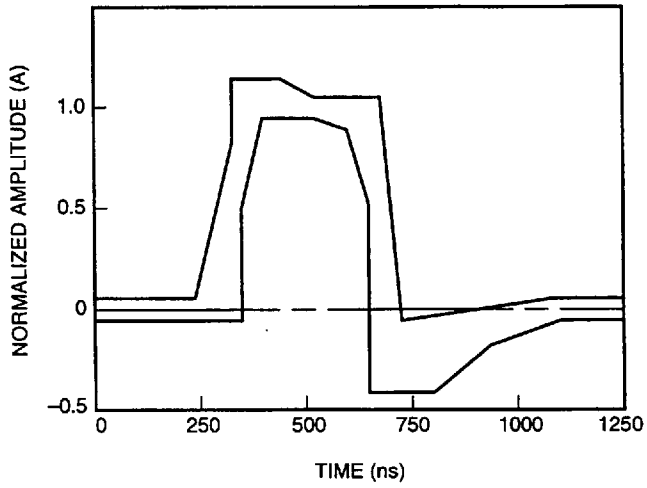
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Transmitter (continued)

Output Pulse Shape (continued)



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T1 Isolated-Pulse Corner Points According to FCC Part 68

Maximum Curve		Minimum Curve	
ns	Normalized Voltage	ns	Normalized Voltage
0	0.05	0	–0.05
242	0.05	350	–0.05
325	0.80	350	0.50
325	1.20	400	0.90
425	1.20	500	0.95
500	1.05	600	0.90
675	1.05	650	0.50
728	0.05	650	–0.45
1000	0.05	800	–0.45
1250	0.05	896	–0.26
—	—	1100	–0.05
—	—	1250	–0.05

Note: Successive corner points are joined by straight lines.

Figure 4. T1 Isolated-Pulse Template

DSX-1 Pulse Template Corner Points According to CB119

Maximum Curve		Minimum Curve	
ns	Normalized Voltage	ns	Normalized Voltage
0	0.05	0	–0.05
250	0.05	350	–0.05
325	0.80	350	0.50
325	1.15	400	0.95
425	1.15	500	0.95
500	1.05	600	0.90
675	1.05	650	0.50
725	–0.07	650	–0.45
1100	0.05	800	–0.45
1250	0.05	925	–0.20
—	—	1100	–0.05
—	—	1250	–0.05

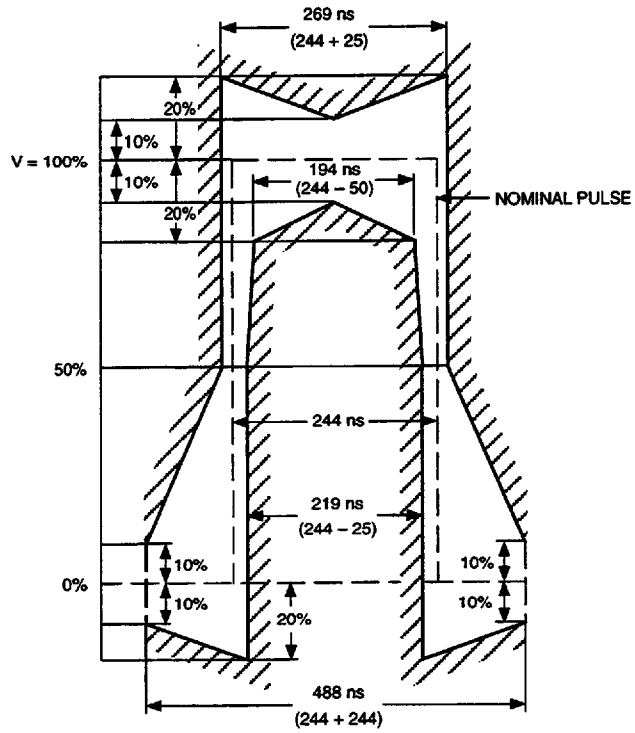
Note: Successive corner points are joined by straight lines.

Figure 5. DSX-1 Isolated-Pulse Template

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Transmitter (continued)

Output Pulse Shape (continued)



Note: V corresponds to the nominal peak value.

Figure 6. ITU-T G.703 Pulse Template

Output Pulse Generation

The transmitter accepts a clock with positive and negative data (dual-rail NRZ format) and converts the signal to a balanced bipolar data signal (AMI format). Positive 1s are produced by a positive pulse on device pin T2, and negative 1s are produced by a positive pulse on device pin R2. Binary 0s are converted to null pulses. All pulse shapes are controlled on-chip according to equalizer control inputs, as defined in Table 5. Transmitter specifications are shown in Table 4.

Table 5. Equalizer/Rate Control

Service	Clock Rate	Transmitter Equalization*	Maximum Cable Loss†	EC1	EC2	EC3
T1	1.544 MHz	—	22‡	0	0	0
DS1	1.544 MHz	0 ft.—131 ft.	0.6	0	0	1
		131 ft.—262 ft.	1.2	0	1	0
		262 ft.—393 ft.	1.8	0	1	1
		393 ft.—524 ft.	2.4	1	0	0
		524 ft.—655 ft.	3.0	1	0	1
CEPT	2.048 MHz	75 Ω	—	1	1	0
		120 Ω	—	1	1	1

* Distance to DSX in feet for 22-Ga. PIC (ABAM) cable (DS1 only). Use maximum loss figures for other cable types.
† dB at 772 kHz.
‡ According to *FCC Part 68, Subpart D, Option A* for 0 dB line build-out.

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Jitter Attenuator

Jitter transfer functions describe the amount of jitter that is transferred from the input to the output of the specified equipment. The jitter transfer functions are affected by the jitter attenuator circuitry, which can be placed in the receive data path, placed in the transmit data path, or bypassed. Placement of this circuit is controlled as described in Table 6. The external clock (EXCLK) must be present for the attenuation function to operate. When attenuation is selected, the T7290A device exhibits a jitter transfer function that has no peaking and a single 3.6 Hz pole frequency (DS1) or 4.8 Hz pole frequency (CEPT). Figure 7 displays a typical DS1 jitter transfer function for a constant input jitter amplitude of 2.0 U.I. peak-to-peak.

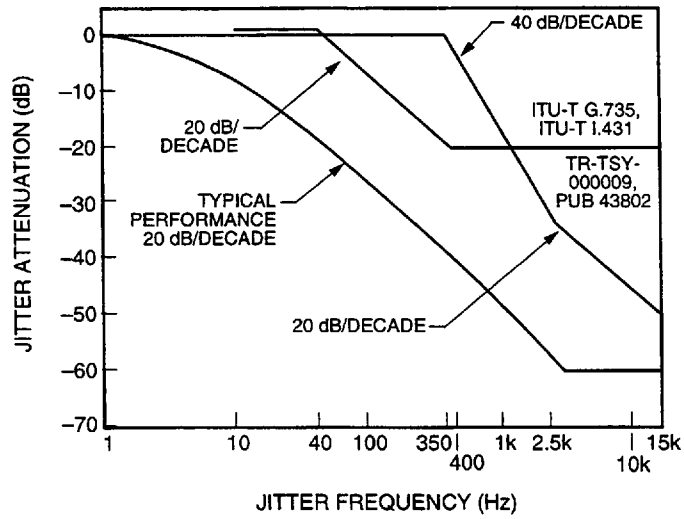
The amount of generated output jitter when no input jitter is present is measured by using the scheme shown in Figure 8. The jitter filters depicted represent the AT&T PUB 62411 specification for a 1.544 MHz data rate. The jitter produced at the labeled points does not exceed the following peak-to-peak levels: 0.05 U.I. at point 1, 0.025 U.I. at point 2, 0.025 U.I. at point 3, and 0.02 U.I. at point 4. A similar test can be performed for ITU-T I.431 qualification at the 2.048 MHz data rate, in which two jitter filters are 20 Hz—100 kHz (0.125 U.I.) and 700 Hz—100 kHz (0.02 U.I.).

The jitter tolerance of the attenuator meets the requirements of the TR-TSY-000009, AT&T PUB 43802, and ITU-T G.823 (see Figure 3). The attenuator also ensures that jitter accommodation is a minimum of 28 U.I. peak-to-peak (DS1) or 40 U.I. peak-to-peak (CEPT) (1 U.I. = 648 ns [T1/DS1] or 488 ns [CEPT]) during attenuation. The jitter attenuation function is identical when placed in either transmit or receive path.

Ideally, the tolerance of the attenuator is ±32 bits (64 U.I.). However, if Δf (Hz) = frequency (EXCLK) – frequency (input clock) and N = 23 (DS1) or 30.5 (CEPT), then the tolerance is degraded and equals:

$$64 - 2 \times \left(\text{RND_UP} \left(\frac{\text{ABS}(\Delta f)}{N} + 1 \right) \right) \text{ (U.I.)}$$

Figure 9 shows the phase step response (DS1) of the attenuator given Δf. The response is based on a phase offset (U.I.) generated by the read pointer of the buffer. It is this phase offset that degrades the attenuator's tolerance.



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Data Points (Hz, dB)

TR-TSY-000009, AT&T PUB 43802	ITU-T G.735, ITU-T I.431
1, 0.1	10, 0.5
350, 0.1	40, 0.5
2.5k, –33.6	400, –19.5
15k, –49.2	15k, –19.5

Figure 7. Jitter Transfer Function of the Jitter Attenuator

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Jitter Attenuator (continued)

When the T7290A device is used only as a jitter attenuator, loopback 1 (LP1) should be active and the attenuator must be placed in the transmit path (MODE1:2 = 01).

Table 6. Connectivity of Jitter Attenuator

Connectivity of Jitter Attenuator*	MODE1	MODE2
Bypass†	0	0
Transmit Path	0	1
Receive Path	1	0
Test Mode‡	1	1

* The jitter attenuator must be enabled after VDD exceeds 4.75 V during device powerup.
† Jitter attenuator is powered down during this mode (see Table 8 under the Electrical Characteristics section).
‡ Not used for normal operation.

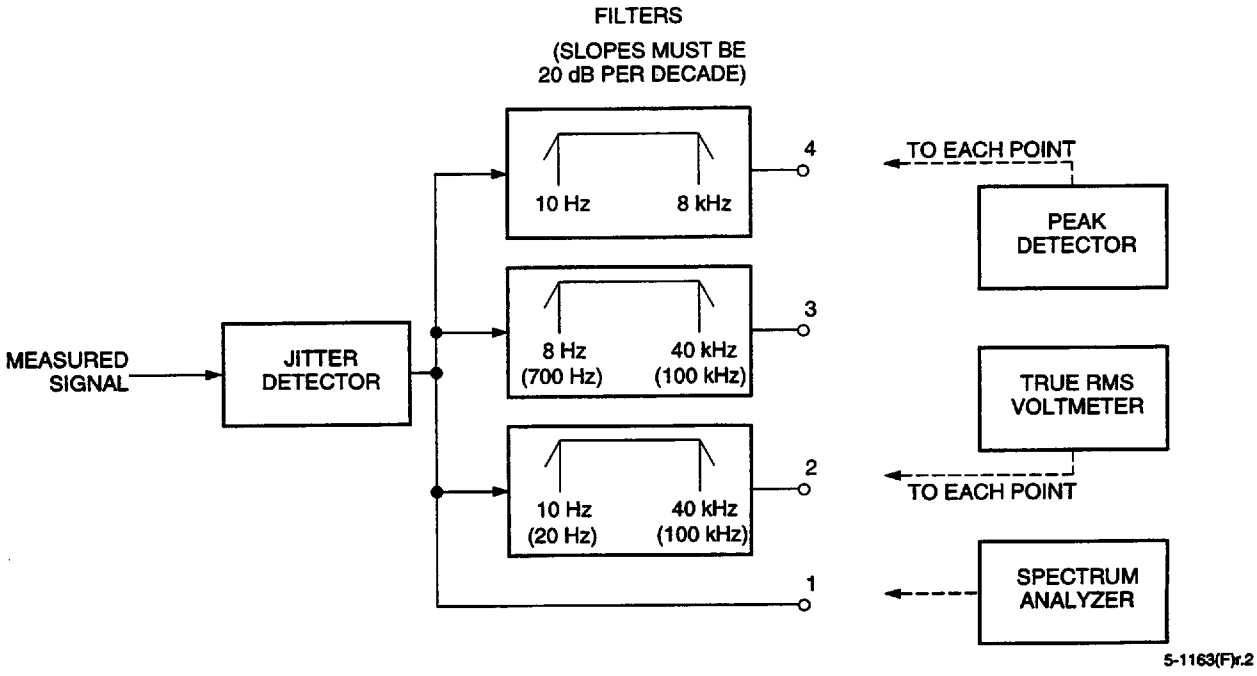


Figure 8. Measurement of Generated Jitter

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Jitter Attenuator (continued)

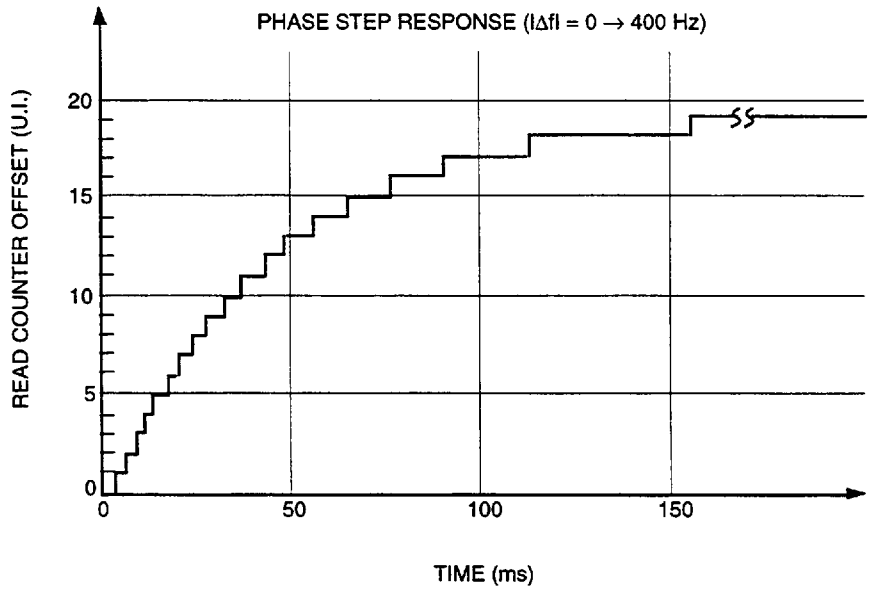


Figure 9. Jitter Attenuator Phase Response

Alarms and Maintenance

Digital Loss of Signal (DLOS)

A digital loss of signal (DLOS = 1) is indicated if 128 or more consecutive 0s occur in the receive data stream during DS1/T1 operation. During CEPT operation, a DLOS is indicated when 32 or more consecutive 0s occur in the receive data stream. DLOS is then deactivated when the ones density exceeds 12.5% and there are no more than 15 consecutive 0s (T1, DS1, and CEPT), signifying the return of good signal. DLOS deactivation monitors the data in fixed 32-bit windows. Each window must have at least four 1s with no more than 15 consecutive 0s. Consecutive 0s are also monitored across the window boundary. This condition must persist for two consecutive 32-bit windows, at which time DLOS is deactivated at the end of the window. Upon DLOS detection, RCLK is phase-locked to the external clock (EXCLK) so that other system devices slaved to the line clock continue to operate without instantaneous phase hits or discontinuities. Either an analog loss of signal (ALOS) or a digital loss of signal (DLOS) activates the IN-LOS output pin.

Output Loss of Signal (OUT-LOS)

An output loss of signal (OUT-LOS = 1) is indicated if either the transmit clock (TCLK) or the smoothing clock (SCLK) output of the jitter attenuator is absent. If the jitter attenuator is placed in the transmit path, SCLK is monitored. If the jitter attenuator is not used in the transmit path, TCLK is monitored. For every ten clock periods of the PLL oscillator clock, denoted as UGRCLK in Figure 1, a strobe is generated. If a single transmit clock period occurs between strobes, then OUT-LOS = 0. If no transmit clock period occurs between strobes, then OUT-LOS = 1, and the output drivers (T2 and R2) are placed into a high-impedance state and no data is transmitted. UGRCLK is always present, even in the absence of both EXCLK and T1/R1 input data; therefore, UGRCLK is the most suitable clock for monitoring OUT-LOS.

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Alarms and Maintenance (continued)

Jitter Attenuator Alarm (ESA)

A jitter attenuator alarm (ESA = 1) is indicated if the phase jitter exceeds the tolerance of the jitter attenuator. Bit errors occur when ESA is active. This signal is asserted until error-free operation resumes. See Figure 9 to determine the tolerance limits of the attenuator.

Transmitter Short Circuit

A transmitter monitor is provided to detect nonfunctioning links and protect the device from damage. If one of the transmitter's line drivers (T2 or R2) is shorted to the power supply or ground, or if T2 and R2 are shorted together, internal circuitry protects the device from damage. After 35 transmit clock cycles, the transmitter is powered up in its normal operating mode. The drivers attempt to correctly transmit the next data bit (+1, 0, or –1). If the short is still present, the transmitter is again internally protected for 35 transmit clock cycles. This process is continuously repeated until the short has disappeared. The TSC alarm is not available off-chip.

AIS (Blue Signal) Generator

When the transmit blue signal is set (TBS = 1), a continuous stream of bipolar 1s is transmitted onto the line synchronous with EXCLK. The TPDATA and TNDATA inputs are ignored during this mode. If the IN-LOS output is externally connected to the TBS input, an IN-LOS error initiates a transmit blue signal as long as IN-LOS = 1. Also, TBS input is ignored when a remote loopback is selected. There is no microprocessor interface for the TBS input, i.e., any change on the TBS pin is fed directly into the device and is not impeded by the $\overline{CS}$ function.

Loopbacks

The T7290A device has three independent loopback paths, which are activated as shown in Table 7.

A local loopback (LP1) connects the jitter attenuator's output clock and data to the receive clock and data output pins. MODE1:2 = 01 must be selected for this loopback to operate (jitter attenuator in the transmit path). Valid transmit output data continues to be sent to the network. However, if the transmit blue is initiated (TBS = 1), an all-1s signal is sent to the network and does not corrupt the looped data. The IN-LOS alarm still monitors the entire receive function.

A remote loopback (LP2) loops the recovered clock and retimed data into the transmitter and back onto the line. The receive front end, receive PLL, jitter attenuator (if engaged), and transmit driver circuitry are all exercised. The transmit clock, transmit data, and TBS inputs are ignored. Valid receive output data continues to be sent to RPDATA and RNDATA. This loop can be used to isolate failures between systems.

A digital local loopback (LP3) directly loops the transmit clock and data to the receive clock and data output pins. The blue signal can be transmitted when in this loopback. LP3 (rather than LP1) must be selected if MODE2 = 0.

Table 7. Loopback Control

Operation	Symbol	LOOPA	LOOPB
Normal	—	0	0
Digital Local Loopback	LP3	0	1
Remote Loopback	LP2*	1	0
Local Loopback	LP1	1	1

* TBS is ignored.

Microprocessor Interface

A chip-select input ($\overline{CS}$) configures the device in either hardware mode or microprocessor mode. The chip-select function applies to the following inputs: MODE1, MODE2, EC1, EC2, EC3, LOOPA, and LOOPB. In the hardware mode, any change on these asynchronous input pins is fed directly into the device. To maintain hardware mode, set $\overline{CS}$ = 0. In the microprocessor mode, new digital control inputs are loaded into the T7290A device on the falling edge of $\overline{CS}$ and are latched on the rising edge of $\overline{CS}$. Figure 11 shows a timing diagram of this function.

Note that there are special requirements only when using microprocessor mode. For example, the state of the input should not change while $\overline{CS}$ = 0. Also, the state of the internal latch is undefined (unknown to the user) until the first falling edge of $\overline{CS}$ is encountered.

In-Circuit Testing

The device has the ability to allow for in-circuit testing by activating the high-impedance mode ($\overline{TRI}$ = 0). During this mode, all output buffers (T2, R2, RCLK, RPDATA, RNDATA, IN-LOS, ESA, and OUT-LOS) are 3-stated. During the 3-stated condition, the absolute maximum voltage ratings must not be exceeded on any pin.

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Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent or latent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

External leads can be soldered safely at temperatures up to 300 °C.

Parameter	Symbol	Min	Max	Unit
dc Supply Voltage Range	V_{DD}	–0.5	6.5	V
Power Dissipation	P_D	—	500	mW
Storage Temperature	T_{stg}	–65	125	°C
Maximum Voltage (any pin) with Respect to V_{DD}	—	—	0.5	V
Minimum Voltage (any pin) with Respect to GND	—	–0.5	—	V
Maximum Allowable Voltages (T1, R1) with Respect to GND	—	–5.0	5.0	V

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 1000 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here is obtained by using these circuit parameters:

Human-Body Model ESD Threshold	
Device	**Voltage**
T7290A-EL	>1200 V
T7290A-PL	>1200 V

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Electrical Characteristics

Operating Conditions

–40 °C ≤ T_A ≤ +85 °C, V_{DD} = 5 V ± 5%, except as noted. V_{DD} rise time (0 V to 4.75 V) must be less than 15 ms.

Table 8. Power Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Power Dissipation:*	P_D				
Without Jitter Attenuator:					
T1		—	125	131	mW
DS1†		—	132	139	mW
CEPT (75 Ω)		—	126	132	mW
CEPT (120 Ω)		—	120	126	mW
With Jitter Attenuator:					
T1		—	165	173	mW
DS1†		—	172	181	mW
CEPT (75 Ω)		—	174	183	mW
CEPT (120 Ω)		—	168	176	mW

* Conditions with 50% 1s on the transmit side, T_A = 25 °C, V_{DD} = 5 V.
† Equalizer settings: EC1 = 0, EC2 = 1, EC3 = 1.

Table 9. Logic Interface Characteristics

An internal pull-up device is provided on the $\overline{TRI}$ lead. Internal pull-down devices are provided on the following leads: $\overline{CS}$, MODE1, MODE2, EC1, EC2, EC3, TBS, LOOPA, and LOOPB. The internal pull-up or pull-down devices require the input to source or sink no more than 20 µA.

Parameter	Symbol	Min	Max	Unit
Input Voltage:				
Low	V_{IL}	GND_D	0.8	V
High	V_{IH}	2.0	V_{DDD}	V
Output Voltage:				
Low	V_{OL}	GND_D	0.4	V
High	V_{OH}	2.4	V_{DDD}	V
Input Capacitance	C_I	—	20	pF
Load Capacitance	C_L	—	40	pF
Source Current	I_{source}	—	4.9	mA
Sink Current	I_{sink}	—	4.9	mA

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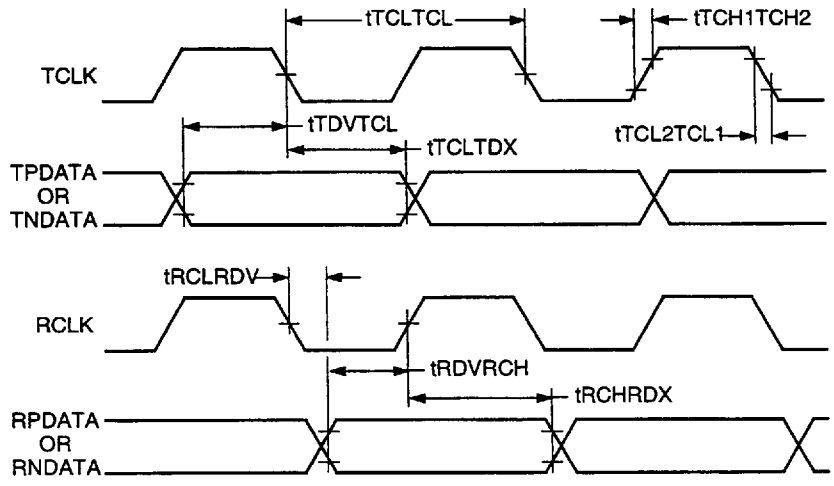
Timing Characteristics

All duty-cycle and timing relationships for receive and transmit data signals are referenced to a TTL, 1.4 V threshold level. Figure 10 shows this timing.

Table 10. Interface Data Timing (See Figure 10.)

Symbol	Parameter	Min	Typ	Max	Unit
—	TCLK Duty Cycle	40	50	60	%
tTCLTCL	TCLK Clock Period: DS1/T1 CEPT	 * †	 647.7 488	 * †	 ns ns
tTDVTCL	Transmit Data Setup Time	50	—	—	ns
tTCLTDX	Transmit Data Hold Time	40	—	—	ns
tTCH1TCH2	Clock Rise Time (10%—90%)	—	—	40	ns
tTCL2TCL1	Clock Fall Time (10%—90%)	—	—	40	ns
tRDVRCH	Receive Data Setup Time	140	—	—	ns
tRCHRDX	Receive Data Hold Time	180	—	—	ns
tRCLRDV	Receive Propagation Delay	—	—	40	ns

* A tolerance of ±130 ppm.
† A tolerance of ±80 ppm.



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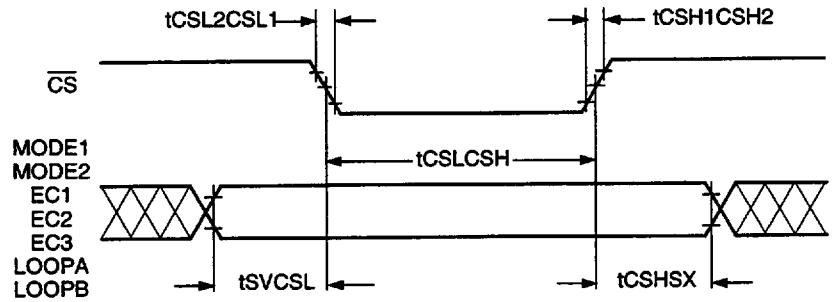
Figure 10. Interface Data Timing

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Timing Characteristics (continued)

Table 11. Microprocessor Interface Timing (See Figure 11.)

Symbol	Parameter	Min	Max	Unit
tSVCSL	Control Signal Setup Time	50	—	ns
tCSLCSH	Control Signal Pulse Width Time	40	—	ns
tCSHSX	Control Signal Hold Time	40	—	ns
tCSH1CSH2	Control Signal Rise Time (10%—90%)	—	40	ns
tCSL2CSL1	Control Signal Rise Time (10%—90%)	—	40	ns



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Figure 11. Microprocessor Interface Timing

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Applications

Line Termination

For the following applications (shown in Figures 12—15), the Lucent 2741 and 2745 Series transformers are recommended. The same transformers used for the T7290 device can be used for the T7290A device. The tolerance of all transformer turns ratios is a maximum of ±2%. The tolerance of all resistors in the transmit path (excluding the cable termination) is a maximum of ±1%.

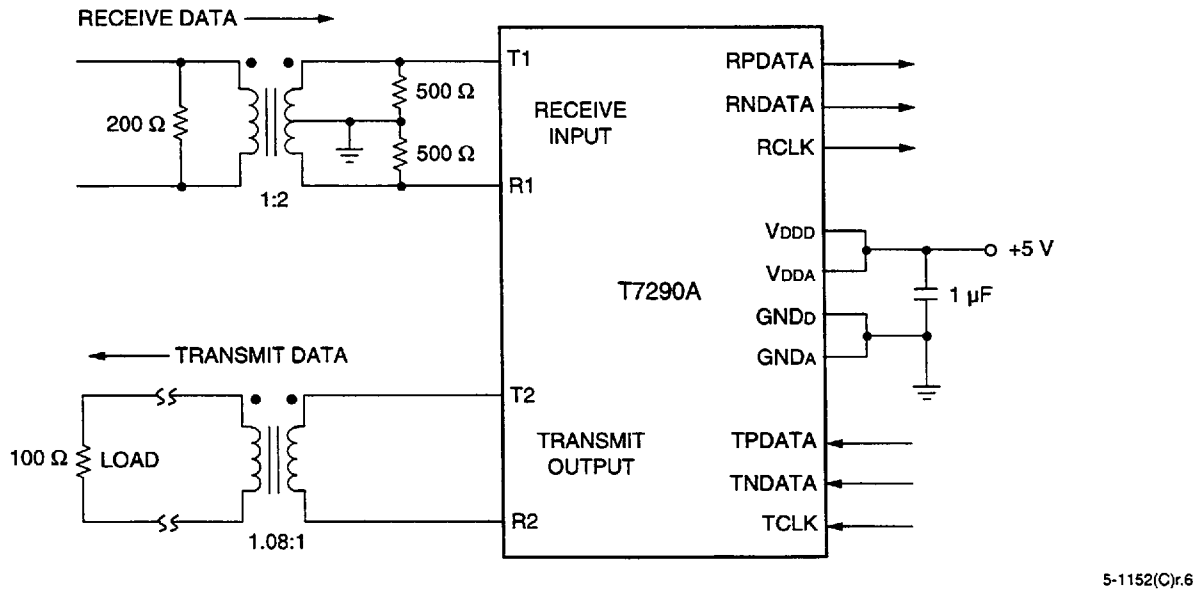


Figure 12. DS1 Application for Twisted-Pair Interface

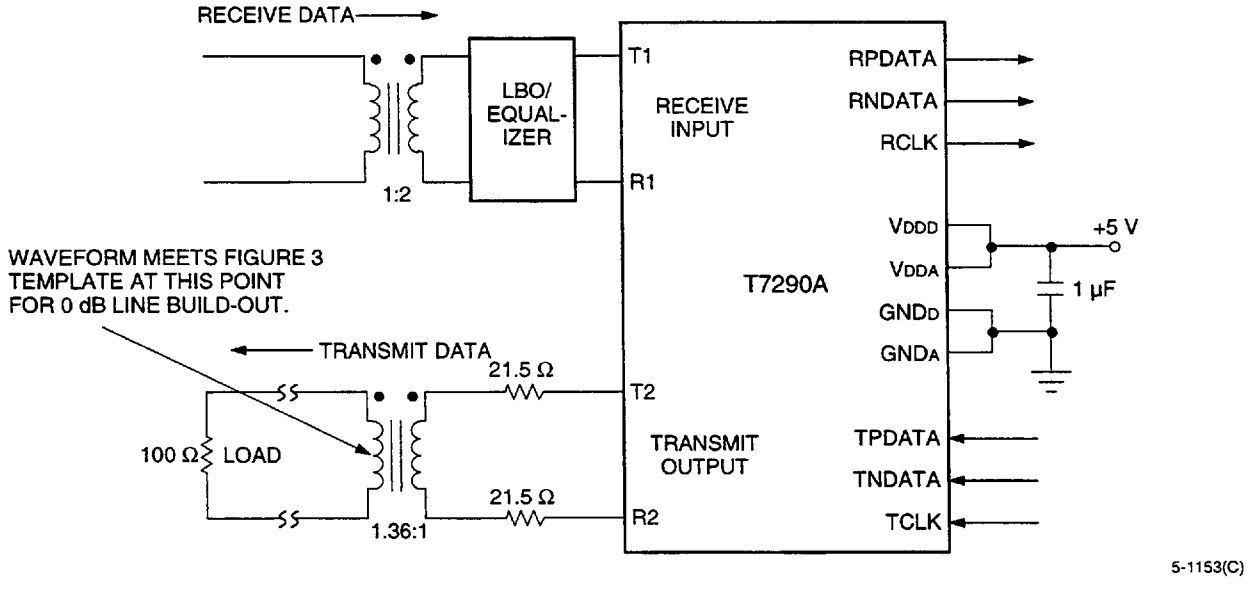


Figure 13. T1 Application Diagram

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Applications (continued)

Line Termination (continued)

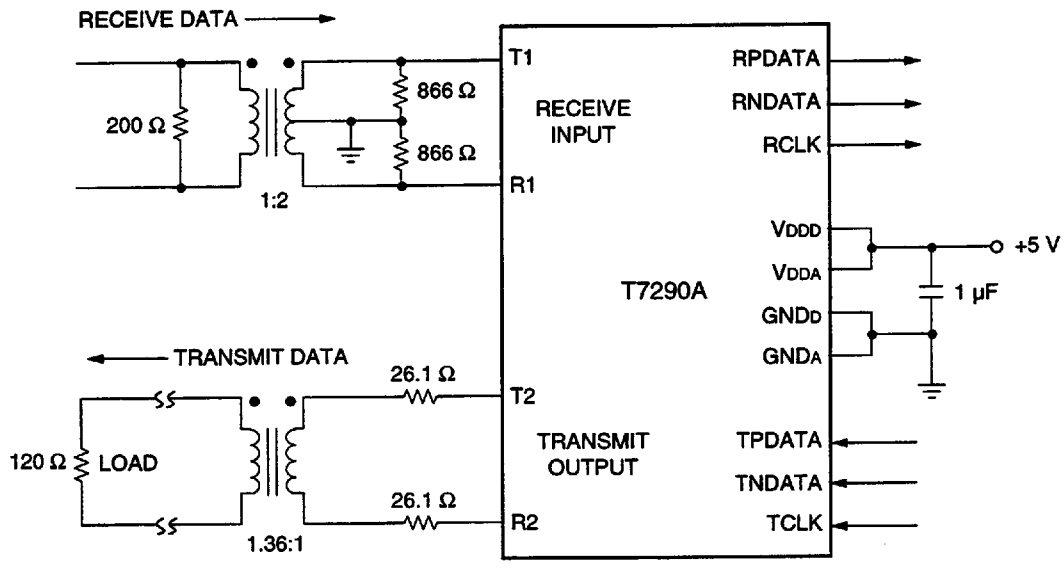


Figure 14. CEPT Application for Twisted-Pair Interface

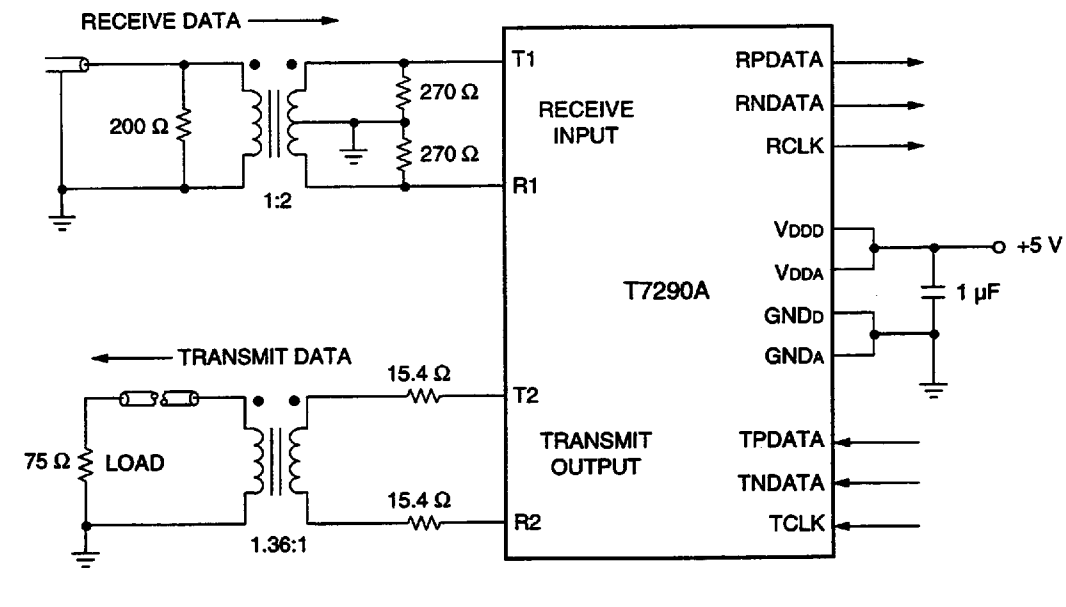


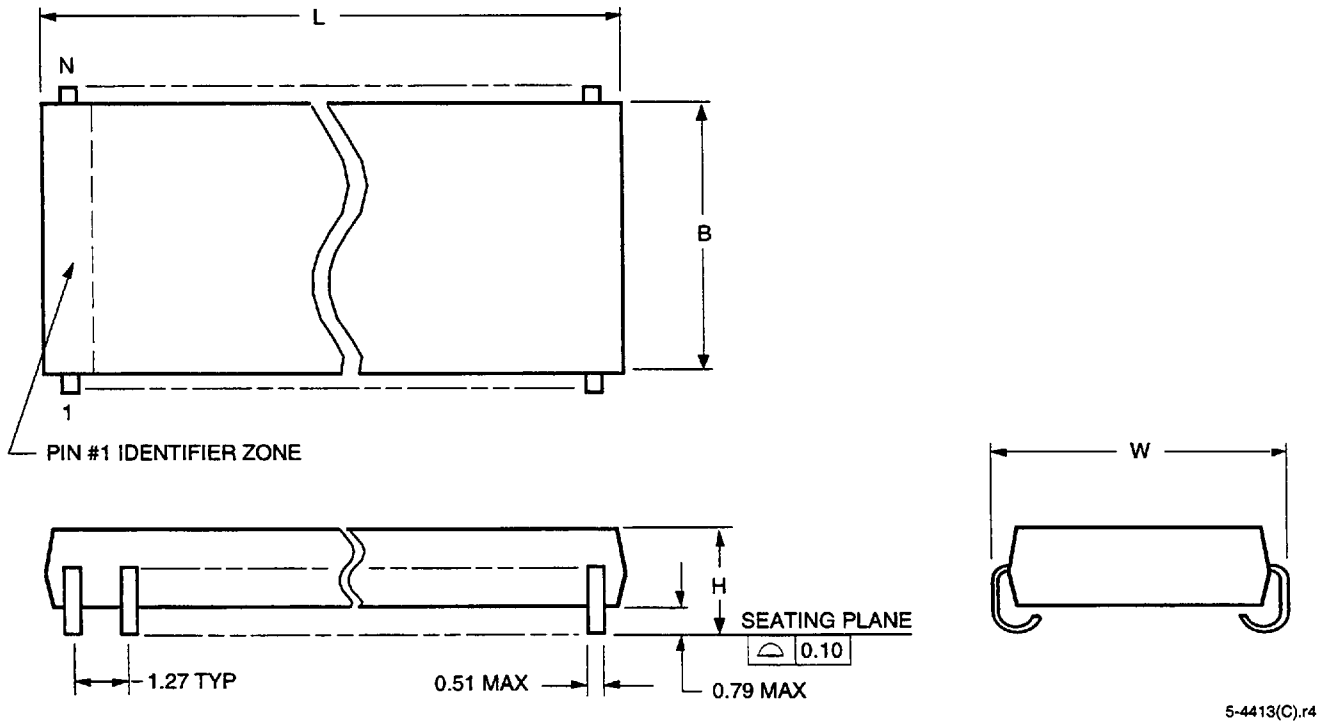
Figure 15. CEPT Application for Coaxial Interface

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Outline Diagrams

28-Pin, Plastic SOJ

Dimensions are in millimeters.



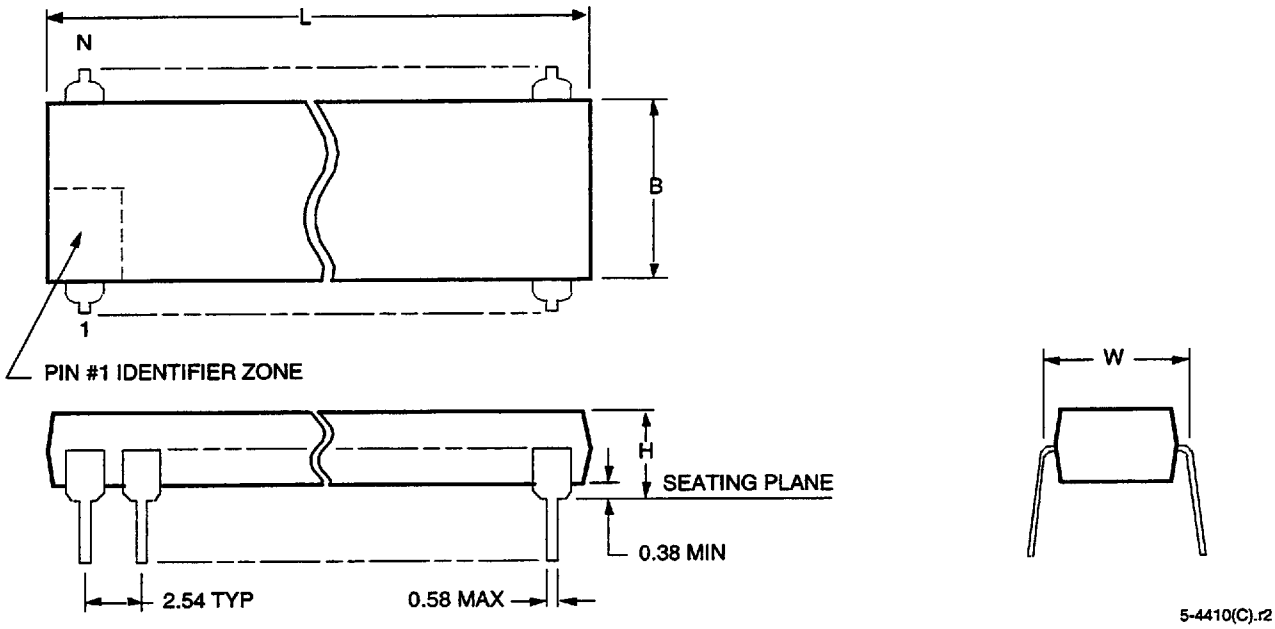
Number of Pins (N)	Package Dimensions (SOJ)			
	Maximum Length Including Leads (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
28	18.03	7.62	8.81	3.18

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Outline Diagrams (continued)

28-Pin, Plastic DIP

Dimensions are in millimeters.



Number of Pins (N)	Package Dimensions (DIP)			
	Maximum Length Including Leads (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
28	37.34	13.97	15.49	5.59

Ordering Information

Device Code	Package	Temperature	Comcode (Ordering Number)
T - 7290A - - PL	28-Pin DIP	–40 °C to +85 °C	106785645
T - 7290A - - EL	28-Pin SOJ	–40 °C to +85 °C	106785637

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T7290A Migration from T7290

The T7290A is a replacement for the T7290 family of devices that includes the T7290-EL, T7290-PL, T7290-EL2, and T7290-PL2. The following list describes the functional changes made to the T7290 to produce the T7290A. **Modification of an existing T7290 application may be required.**

- The TBS input of the T7290A directly controls the TBS function. The TBS function of the T7290 is gated by chip select ($\overline{CS}$).
- The transmitter short circuit (TSC) output alarm has been eliminated; however, the transmit drivers are still powered down under short-circuit conditions. The pin is renamed as output loss of signal (OUT-LOS) and indicates when either the transmit clock (TCLK) or the smoothing clock (SCLK) output of the jitter attenuator is absent.
- Loopback 1 (LP1) has been modified to route signals through the jitter attenuator only. The MODE2 pin must be set high for this loopback to operate (jitter attenuator on).
- The digital loss-of-signal (DLOS) functionality is now compatible for use in systems that must be compliant with Bellcore TR-TSY-000009.
- The loss-of-signal (LOS) output indication is renamed as input loss of signal (IN-LOS) and is now the ORed function of analog loss of signal (ALOS) and digital loss of signal (DLOS) regardless of the loopback setting.
- The frequency acquisition mode is enabled when a digital loss-of-signal (DLOS) condition occurs, in which case the receive clock (RCLK) is frequency-locked/phase-locked to the external clock (EXCLK).
- Improved ITU-T G.703 interference immunity for CEPT mode operation.

DS98-190TIC Replaces DS97-197TIC to Incorporate the Following Updates

1. Page 3, Figure 1, Block Diagram, updated.
2. Page 21, 28-Pin, Plastic SOJ, changed dimensions to millimeters.
3. Page 22, 28-Pin, Plastic DIP, changed dimensions to millimeters.
4. Page 22, corrected Device Code.

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