UG337: Si53208-EVB User's Guide

8-Output PCI-Express Gen1/2/3/4 and SRIS Clock Buffer Evaluation Board

This document describes operation of the Silicon Laboratories Si53208-EVB evaluation board. It's designed to evaluate the Si53208, 8-output PCI-Express Gen1/2/3/4 which is an SRIS Clock Buffer. Selector switches make it easy to select the voltage for both core and IO supplies. Jumpers allow for easy static configuration of the control inputs as well as provide a port for external test equipment access. Similarly, each regulated supply can be bypassed and driven externally for either precise voltage control or for measuring PSRR performance. Convenient probe pads and isolation resistors permit on-board single-ended or differential measurements. Finally, the PCB layout optimizes signal integrity and skew which rounds out the capabilities of this EVB.

KEY FEATURES

- Evaluation of Silicon Labs Si53208
- External power or USB powered
- DC-coupled differential output clocks
- DC-coupled differential input clock
- Switchable voltage settings
- Easy manual configuration via jumpers
- Easy current measurement

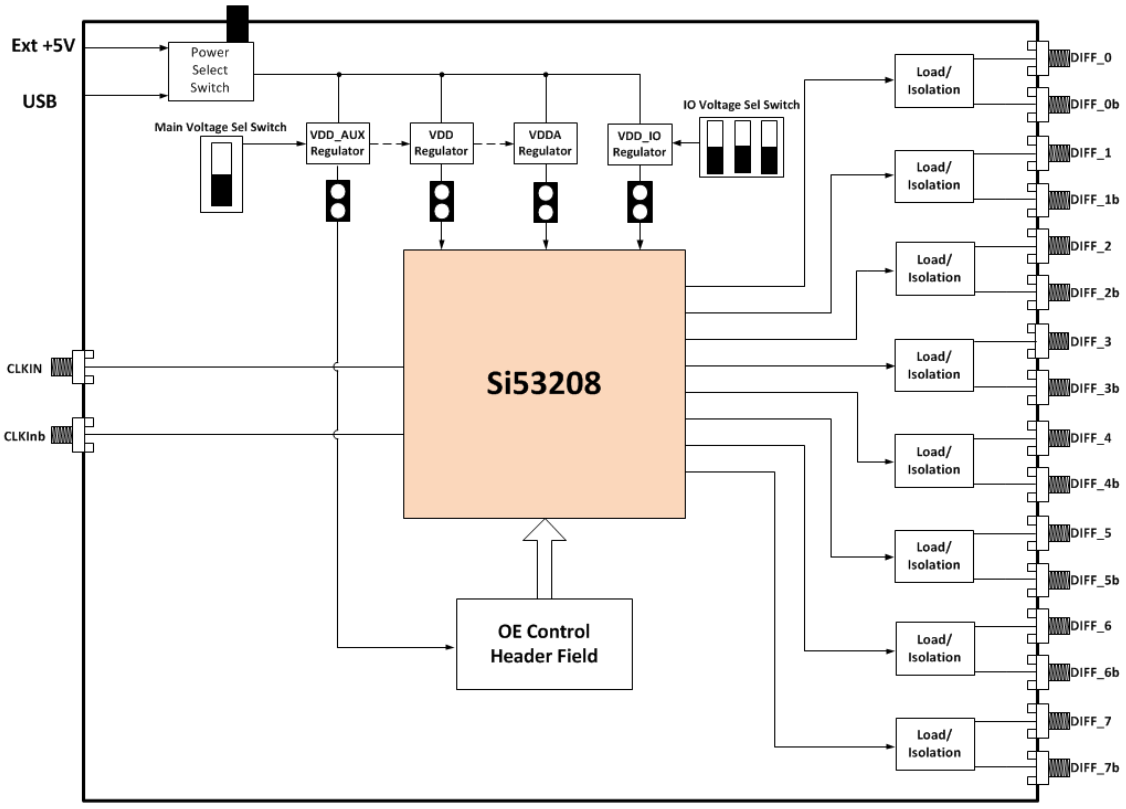


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1. Functional Description

The Si53208-EVB is an evaluation board designed to support the Si53208 device.

Control of device pins such as OE is done via on-board jumpers through the jumper header JP6. The DUT supply voltages (e.g., VDD, VDDA, VDD_AUX, and VDD_IO) can be set via on-board switches as shown in Section 2. Each supply can be sourced either by an on-board regulator for nominal values or via an external supply to test the device over a range of voltages (e.g., min/max supply testing).

2. Power Supply Switch Settings

The device supplies use a linear voltage regulator to drop the externally supplied +5 V (sourced either via USB or an external power supply using switch SW3) voltage to one of the supported nominal VDD voltages (+1.8 V or +1.5 V for VDD, VDDA, and VDD_AUX using switch SW1 and +1.8 V, +1.5 V, +1.2 V, or +1.0 V for VDD_IO using switch SW2).

2.1 +5 V Selection

The +5 V main supply is sourced by either an external power supply or by a USB-B connected to a computer. Use the +5V Source Select switch SW3 to change between them. See the figure below. Position the slide in the up position to select the USB port (J13) and in the down position to select the external supply (J11, J12).

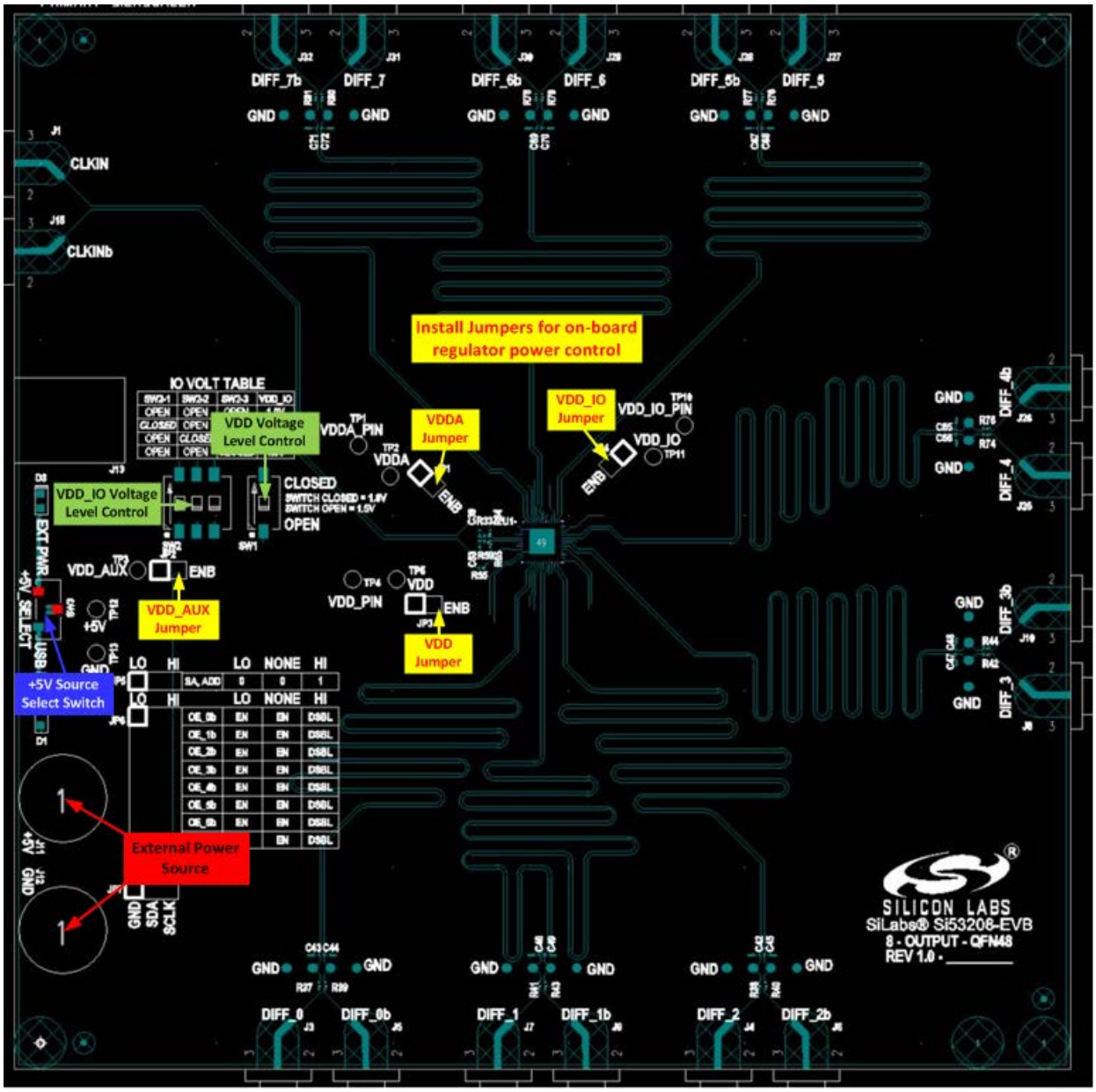


Figure 2.1. 2.1. Location of EVB Power and Voltage Switches and Jumpers

2.2 Voltage Selection for Non-Output Supplies (VDD, VDDA, and VDD_AUX)

The nominal voltage setting for all but VDD_IO is controlled by the VDD Voltage Level Control switch SW1 as shown in Figure 2.1 2.1. Location of EVB Power and Voltage Switches and Jumpers on page 4. Positioning the switch in the open position selects 1.5 V for all these supplies and positioning the switch in the closed position selects 1.8 V. Jumpers JP1-JP3 should be installed if the on-board regulator is desired. Alternatively, and external voltage source can be connected to an individual supply by removing the corresponding jumper and connecting the (+) voltage of the supply to pin 2 of the jumper and (-) voltage to GND (TP13). Note that pin 1 of the jumpers is identified by the highlighted square.

2.3 Voltage Selection for Output Supply (VDD_IO)

The nominal voltage setting for VDD_IO is controlled by the VDD_IO Voltage Level Control switch SW2 as shown in Figure 2.1. The table below shows the switch settings for nominal voltages: +1.8 V, +1.5 V, +1.2 V, and +1.0 V. Please note that only one switch should be in the "closed" position at any given time. Multiple closed switches at the same time could lead to part damage. Jumper JP4 should be installed if the on-board regulator is desired.

Alternatively, an external voltage source can be connected to this individual supply by removing JP4 and connecting the (+) voltage of the supply to pin 2 of the jumper and (-) voltage to GND (TP13). Note that this is an excellent way to test the PSRR performance of the part, as the dc supply can be modulated with a sinusoidal (noise) waveform and inserted on JP4, pin 2.

Table 2.1. Switch 2 Settings for Output Voltage Supply

SW2-1	SW2-2	SW2-3	VDD_IO
OPEN	OPEN	OPEN	1.0V
CLOSED	OPEN	OPEN	1.2V
OPEN	CLOSED	OPEN	1.5V
OPEN	OPEN	CLOSED	1.8V

2.4 Measuring Supply Currents (IDD, IDD_A, and IDD_{IO})

Measuring the current on any supply rail can be performed by measuring the voltage between test points VDD_X and VDD_X_PIN. There is a precision (±100 ppm) 1 ohm resistor between these two test points. Therefore, whatever voltage is measured maps to the equivalent current measurement (e.g., 30 mV -> 30 mA)

3. Control Signal Jumper Settings

Header JP6 is an 8x3, 100 mil header stake that provides access to the eight OE pins allowing easy enable or disable of individual outputs. Table below defines how to configure each input.

Table 3.1. Control Input Jumper Configuration Settings

Control Input Pin	LO	NONE	HI
OE_0b	Enable	Enable	Disable
OE_1b	Enable	Enable	Disable
OE_2b	Enable	Enable	Disable
OE_3b	Enable	Enable	Disable
OE_4b	Enable	Enable	Disable
OE_5b	Enable	Enable	Disable
OE_6b	Enable	Enable	Disable
OE_7b	Enable	Enable	Disable

Enable/disable times can be measured by connecting an external pulse generator to the middle pin of the header and GND to the "LO" pin and sending this signal to trigger a scope. By measuring the time differential between the rising (falling) edge of the trigger and last (first) output clock edge of the corresponding output, the user can determine the disable (enable) time for that output.

4. Output Clock Terminations

4.1 Differential Outputs (DIFF_0:7)

The figure below shows the output termination circuit for each of the 8 differential buffer outputs: Diff_0:7. To simplify on-board probing of the clock, exposed copper pads have been included and are spaced to accommodate a differential probe (e.g., Ag1132A). For example, the output of DIFF_1 can be measured using PCB13 for the signal with PCB6 for GND. The stock output clock termination is optimized for taking phase noise measurements. Note that most phase noise analyzers have a single-ended input, so a balun should be added to convert the differential output to single-ended.

To analyze signal integrity, instead of phase noise, change resistors R37:R44 and R74:R81 from 0 to 953 ohms. They are all 402 size. Also, add 2pF capacitors to C42:C49 and C65:C72, which are all 402 size. After implementing this change, remember that, if you are observing the outputs via the SMA connectors to a 50 ohm input scope, the scale should be set to 1:20.

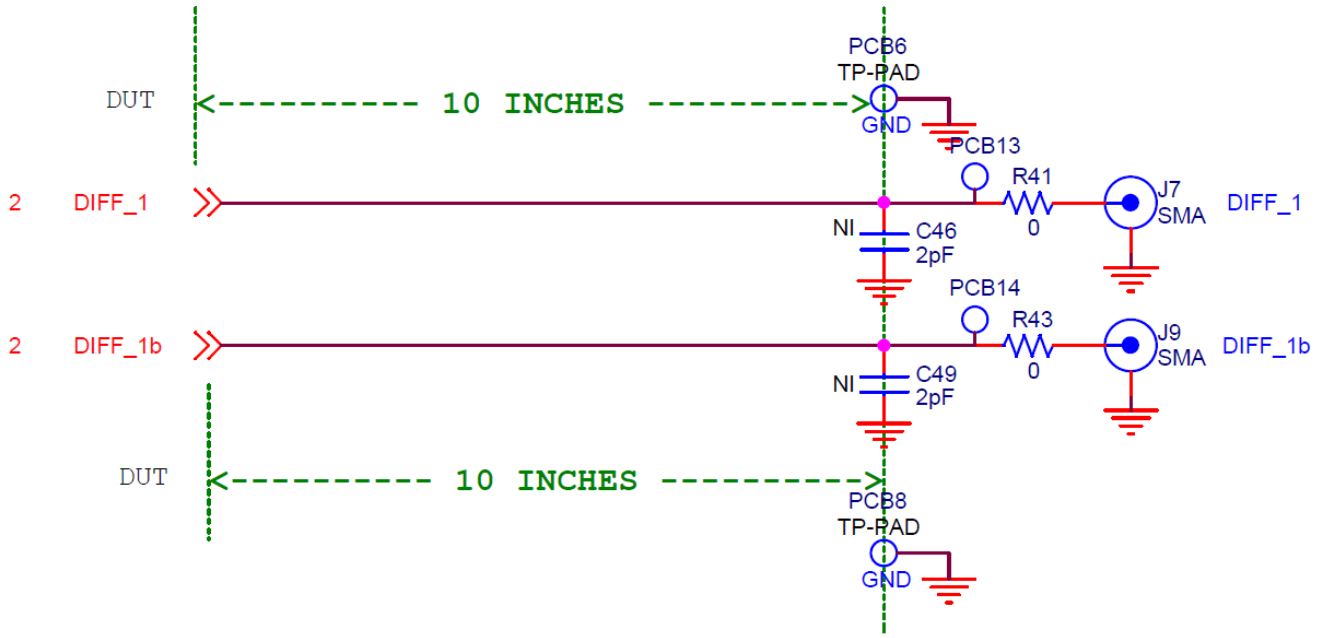


Figure 4.1. Differential Output Clock Termination

5. External Input Clock

The Si53208-EVB supports one HCSL external reference input (CLKIN). No additional termination is necessary for this input. For more details regarding the input clock's requirements, see the Si532xx datasheet.

6. LEDs

The Si53208-EVB has 2 status LEDs as shown in the table below. The board silkscreen identifies each LED.

Table 6.1. Status LEDs

LED name	Color	Location	Description
+5V_EXT	Green	D1	External +5 V source is present (independent of +5V_SELECT (SW3) switch setting)
+5V_USB	Blue	D3	USB port is present (independent of +5V_SELECT (SW3) switch setting)

7. Quick Start – Board Configuration Check List

1. Start with EVB powered down/off.
2. Set the voltage supply DIP switches (Described in Section 2.2 Section 2.3) according to the following:
   - Switch SW1 controls the voltage settings (either 1.5 V or 1.8 V) for the following supplies:
     - VDD
     - VDDA
     - VDD_AUX
   - Switch SW2 controls the voltage setting (either 1.0 V, 1.2 V, 1.5 V, or 1.8 V) for VDD_IO (voltage supply for output DIFF_0:7).
   - Ensure that jumpers JP1:4 are installed.
3. Connect external clock input.
4. Determine the type of measurement.
   - For phase noise measurements, no changes are required. Note that most phase noise analyzers have a single ended input, so a balun should be added to convert the differential output to single ended.
   - For signal integrity measurements, change resistors R37:R44 and R74:R81 from 0 to 953 ohms. They are all 402 size. Also, add 2pF capacitors to C42:C49 and C65:C72. These are also all 402 size. After implementing this change, remember that if you are observing the outputs via the SMA connectors to a 50 ohm input scope, the scale should be set to 1:20.
5. Configure the jumpers at JP5 and JP6 according to how you plan to test the part.
   - Outputs 0:7 enabled/disabled
6. Set +5 V Select switch (SW3) based on how you will power the EVB, either via USB or via external +5 V supply.
7. Connect power, either via USB port or external +5 V power supply as chosen in previous step.

8. Board Schematic, BOM, and Layout

The schematic, BOM, and layout files for the Si53208-EVB can be found at: Si53208-evaluation-kit.

9. Appendix: Typical Waveplots

The plots displayed in this section are provided as an example when measuring signals on this evaluation board with a good lab setup. These plots were taken using a Keysight Ag DSA90804A 8 GHz bandwidth oscilloscope. A Keysight 5 GHz Ag 1132A differential probe was used to measure the differential waveforms, and a Keysight N2796A 2 GHz high-impedance FET probe was used to measure the single-ended waveforms. The signals were measured on the test points located next to each output SMA. The outputs were set up in the stock configuration of no load capacitor and 0 ohm resistors.

9.1 Differential Clock (DIFF_0) Output (Differential Waveform)

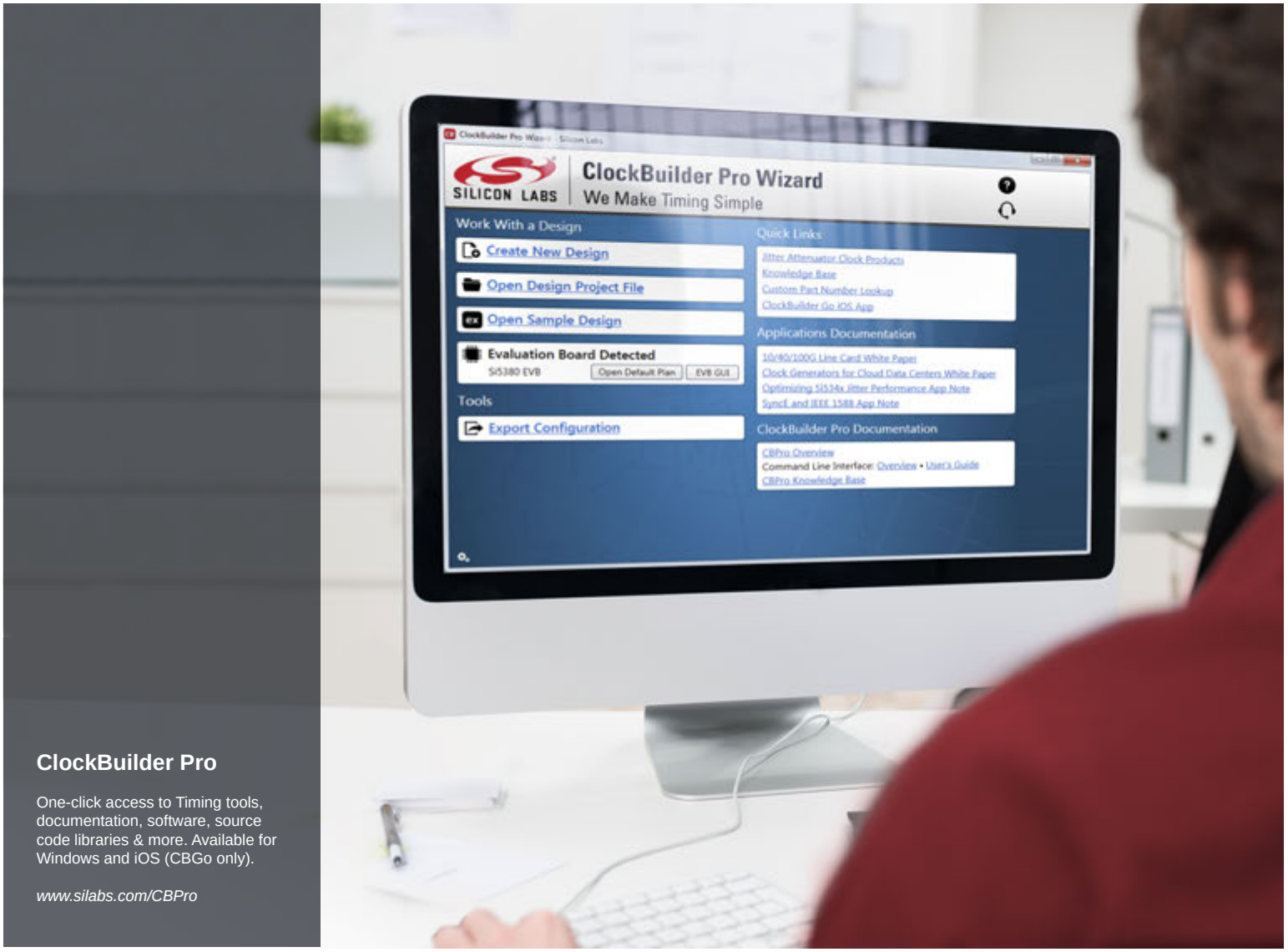


9.2 Differential Clock (DIFF_0) Crossing Voltage (100MHz) (Single-ended waveform)



9.3 Differential clock (DIFF_0) Crossing Voltage (200MHz) (Single-ended waveform)





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