

PCI-EXPRESS GEN 2 DUAL OUTPUT CLOCK GENERATOR

Features

- PCI-Express Gen 1 and Gen 2 compliant
- Low power HCSL differential output buffers
- Supports Serial-ATA (SATA) at 100 MHz
- No termination resistors required
- 25 MHz Crystal Input or Clock input
- Triangular spread spectrum profile for maximum EMI reduction (Si52112-B4)
- Extended Temperature: -40 to 85 °C
- 3.3 V Power supply
- Small package 10-pin TDFN (3x3 mm)
- Si52112-B3 does not support spread spectrum outputs
- Si52112-B4 supports 0.5% down spread outputs
- For PCIe Gen3 applications, see Si52112-B5/B6



Applications

- Network Attached Storage
- Multi-function Printer
- Wireless Access Point
- Routers

Description

Si52112-B3/B4 is a high-performance, PCIe clock generator that can source two PCIe clocks from a 25 MHz crystal or clock input. The clock outputs are compliant to PCIe Gen 1 and Gen 2 specifications. The ultra-small footprint (3x3 mm) and industry leading low power consumption make Si52112-B3/B4 the ideal clock solution for consumer and embedded applications.

Pin Assignments			
VDD	1	10	VDD
XOUT	2	9	DIFF2
XIN/CLKIN	3	8	DIFF2
VSS	4	7	DIFF1
VSS	5	6	DIFF1

Patents pending

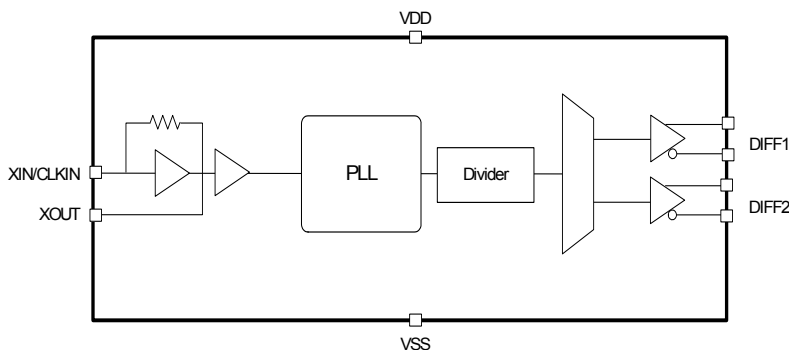


TABLE OF CONTENTS

<u>Section</u>	<u>Page</u>
1. Electrical Specifications	4
2. Crystal Recommendations	7
2.1. Crystal Loading	7
2.2. Calculating Load Capacitors	8
3. Test and Measurement Setup	9
4. Pin Descriptions	11
4.1. 10-Pin TDFN	11
4.2. 8-Pin TSSOP	12
5. Ordering Guide	13
6. Package Outlines	14
6.1. TDFN Package	14
6.2. TSSOP Package	16
7. Recommended Design Guideline	18
Document Change List	19
Contact Information	20

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage (extended)	$V_{DD(extended)}$	3.3 V $\pm$ 5%	3.13	3.3	3.46	V
Supply Voltage (commercial)	$V_{DD(commercial)}$	3.3 V $\pm$ 10%	2.97	3.3	3.63	V

Table 2. DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	3.3 V $\pm$ 10%	2.97	3.30	3.63	V
Operating Supply Current	I_{DD}	Full Active	—	—	17	mA
Input Pin Capacitance	C_{IN}	Input Pin Capacitance	—	3	5	pF
Output Pin Capacitance	C_{OUT}	Output Pin Capacitance	—	—	5	pF

Table 3. AC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal						
Long-term Accuracy	L_{ACC}	Measured at $V_{DD}/2$ differential	—	—	250	ppm
Clock Input						
CLKIN Duty Cycle	T_{DC}	Measured at $V_{DD}/2$	45	—	55	%
CLKIN Rise and Fall Times	T_R/T_F	Measured between 0.2 V_{DD} and 0.8 V_{DD}	0.5	—	4.0	V/ns
CLKIN Cycle-to-Cycle Jitter	T_{CCJ}	Measured at $V_{DD}/2$	—	—	250	ps
CLKIN Long Term Jitter	T_{LTJ}	Measured at $V_{DD}/2$	—	—	350	ps
Input High Voltage	V_{IH}	XIN/CLKIN pin	2	—	$V_{DD}+0.3$	V
Input Low Voltage	V_{IL}	XIN/CLKIN pin	—	—	0.8	V
Input High Current	I_{IH}	XIN/CLKIN pin, $V_{IN} = V_{DD}$	—	—	35	μA
Input Low Current	I_{IL}	XIN/CLKIN pin, $0 < V_{IN} < 0.8$	-35	—	—	μA
DIFF Clocks						
Duty Cycle	T_{DC}	Measured at 0 V differential	45	—	55	%
Skew	T_{SKEW}	Measured at 0 V differential	—	—	60	ps
Output Frequency	F_{OUT}	$V_{DD} = 3.3$ V	—	100	—	MHz
Frequency Accuracy	F_{ACC}	All output clocks	—	—	100	ppm
Slew Rate	$t_{r/f2}$	Measured differentially from ± 150 mV	0.6	—	4.0	V/ns
Cycle-to-Cycle Jitter	T_{CCJ}	Measured at 0 V differential	—	28	70	ps
PCIe Gen 1 Pk-Pk Jitter	$Pk-Pk_{GEN1}$	PCIe Gen 1	—	24	86	ps
PCIe Gen 2 Phase Jitter	RMS_{GEN2}	$10 \text{ kHz} < F < 1.5 \text{ MHz}$	—	1.35	3.0	ps
		$1.5 \text{ MHz} < F < \text{Nyquist}$	—	1.4	3.1	ps
Crossing Point Voltage at 0.7 V Swing	V_{OX}		300	—	550	mV
Voltage High	V_{HIGH}		—	—	1.15	V
Voltage Low	V_{LOW}		-0.3	—	—	V
Spread Range	S_{RNG}	Down Spread, -B4 only	—	-0.5	—	%
Modulation Frequency	F_{MOD}	-B4 only	30	31.5	33	kHz
Enable/Disable and Set-up						
Clock Stabilization from Power-up	T_{STABLE}		—	—	3	ms
Stopclock Set-up Time	T_{SS}		10.0	—	—	ns
Note: Visit www.pcsig.com for complete PCIe specifications.						

Table 4. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature, Storage	T_S	Non-functional	-65	—	150	°C
Temperature, Operating Ambient	T_A	Functional	-40	—	85	°C
Temperature, Junction	T_J	Functional	—	—	150	°C
Dissipation, Junction to Case (TDFN)	θ_{JC}	JEDEC (JESD 51)	—	—	38.3	°C/W
Dissipation, Junction to Case (TSSOP)	θ_{JC}	JEDEC (JESD 51)	—	—	37.0	°C/W
Dissipation, Junction to Ambient (TDFN)	θ_{JA}	JEDEC (JESD 51)	—	—	90.4	°C/W
Dissipation, Junction to Ambient (TSSOP)	θ_{JA}	JEDEC (JESD 51)	—	—	124.0	°C/W

Table 5. Absolute Maximum Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Main Supply Voltage	V _{DD_3.3V}		—	—	4.6	V
Input Voltage	V _{IN}	Relative to V _{SS}	−0.5	—	4.6	V _{DC}
ESD Protection (Human Body Model)	ESD _{HBM}	JEDEC (JESD 22 - A114)	2000	—	—	V
Flammability Rating	UL-94	UL (Class)	V−0			
Note: While using multiple power supplies, the voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.						

2. Crystal Recommendations

If using a crystal input, the device requires a parallel resonance crystal.

Table 6. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	ESR	Drive	Shunt Cap (max)	Motional (max)	Tolerance (max)	Stability (max)	Aging (max)
25 MHz	AT	Parallel	12–15 pF	<50 Ω	>150 μ W	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

2.1. Crystal Loading

Crystal loading is critical in achieving low ppm performance. To realize low ppm performance, use the total capacitance the crystal sees to calculate the appropriate capacitive loading (C_L).

Figure 1 shows a typical crystal configuration using two trim capacitors. It is important that the trim capacitors are in series with the crystal.

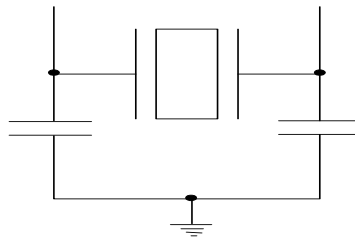


Figure 1. Crystal Capacitive Clarification

2.2. Calculating Load Capacitors

In addition to the standard external trim capacitors, consider the trace capacitance and pin capacitance to calculate the crystal loading correctly. Again, the capacitance on each side is in series with the crystal. The total capacitance on both sides is twice the specified crystal load capacitance (C_L). Trim capacitors are calculated to provide equal capacitive loading on both sides.

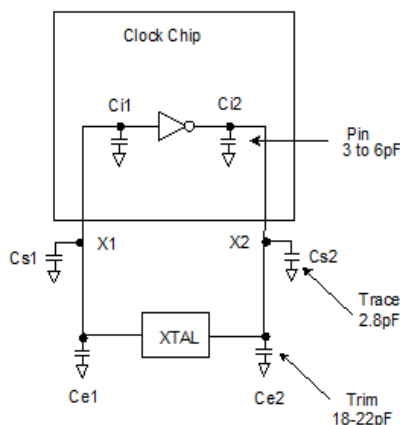


Figure 2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$C_e = 2 \times C_L - (C_s + C_i)$$

Total Capacitance (as seen by the crystal)

$$C_{Le} = \frac{1}{\left(\frac{1}{C_{e1} + C_{s1} + C_{i1}} + \frac{1}{C_{e2} + C_{s2} + C_{i2}} \right)}$$

- CL: Crystal load capacitance
- CLe: Actual loading seen by crystal using standard value trim capacitors
- Ce: External trim capacitors
- Cs: Stray capacitance (terraced)
- Ci: Internal capacitance (lead frame, bond wires, etc.)

3. Test and Measurement Setup

Figures 3 through 5 show the test load configuration for the differential clock signals.

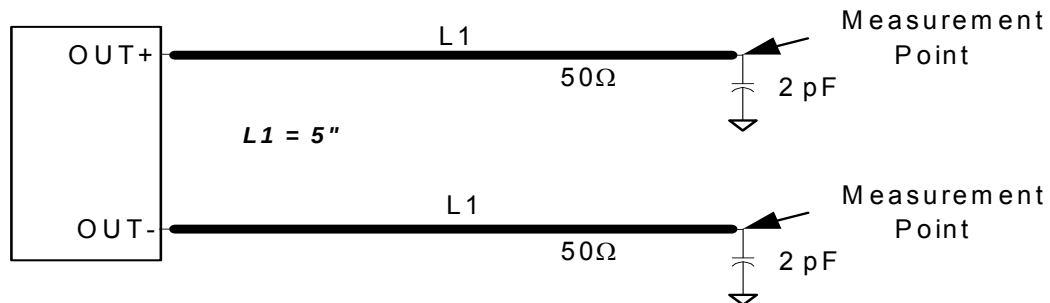
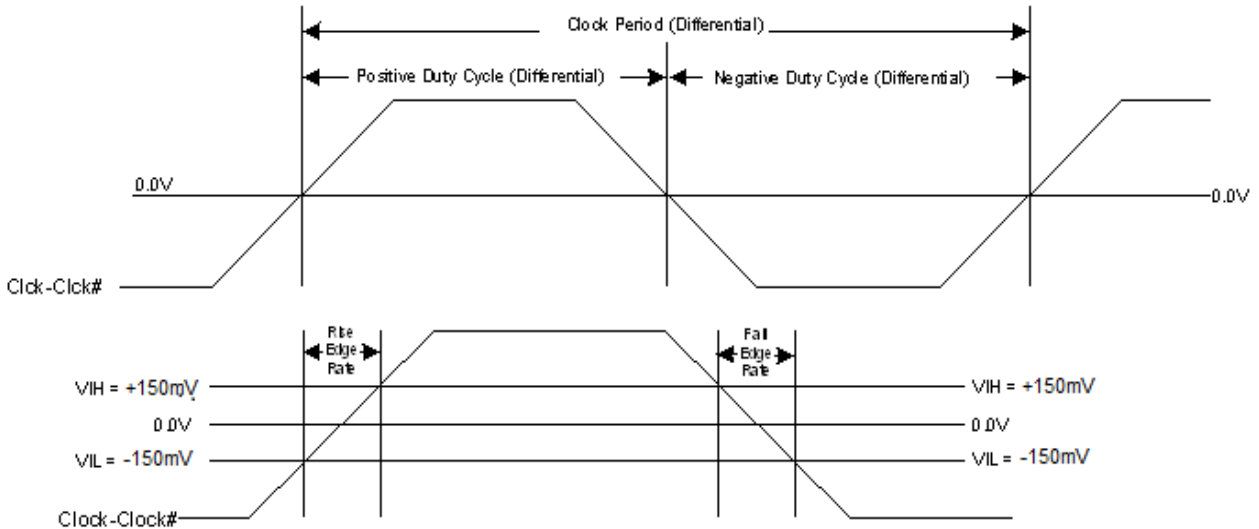
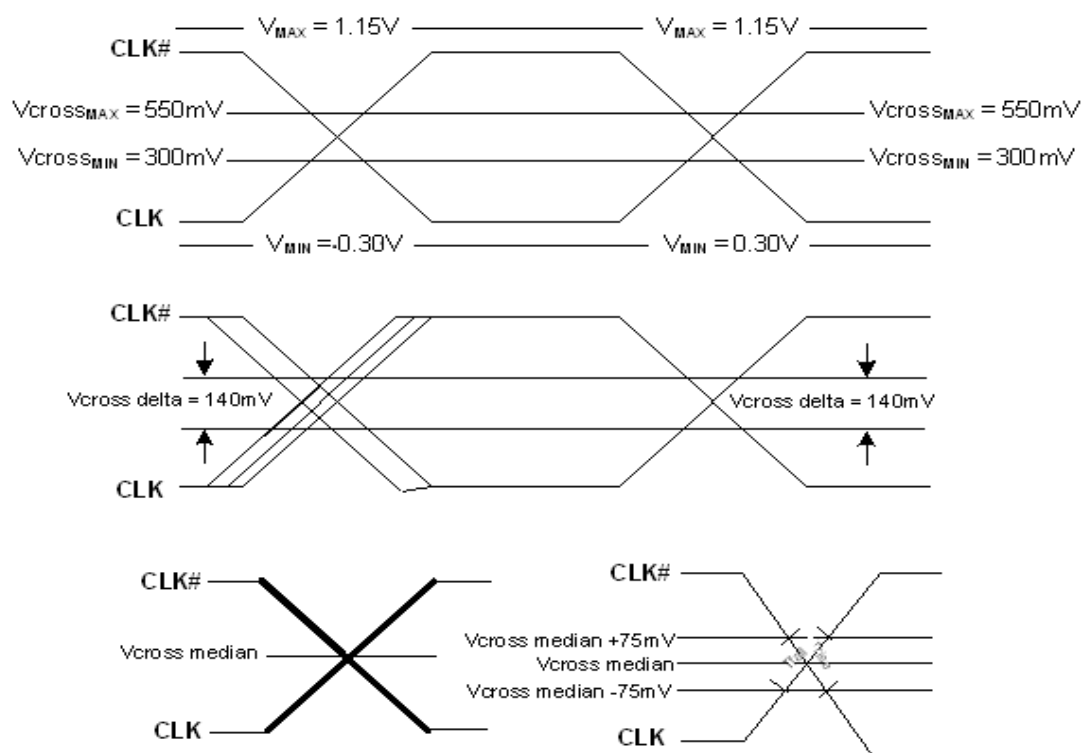


Figure 3. 0.7 V Differential Load Configuration



**Figure 4. Differential Measurement for Differential Output Signals
(for AC Parameters Measurement)**



**Figure 5. Single-ended Measurement for Differential Output Signals
(for AC Parameters Measurement)**

4. Pin Descriptions

4.1. 10-Pin TDFN

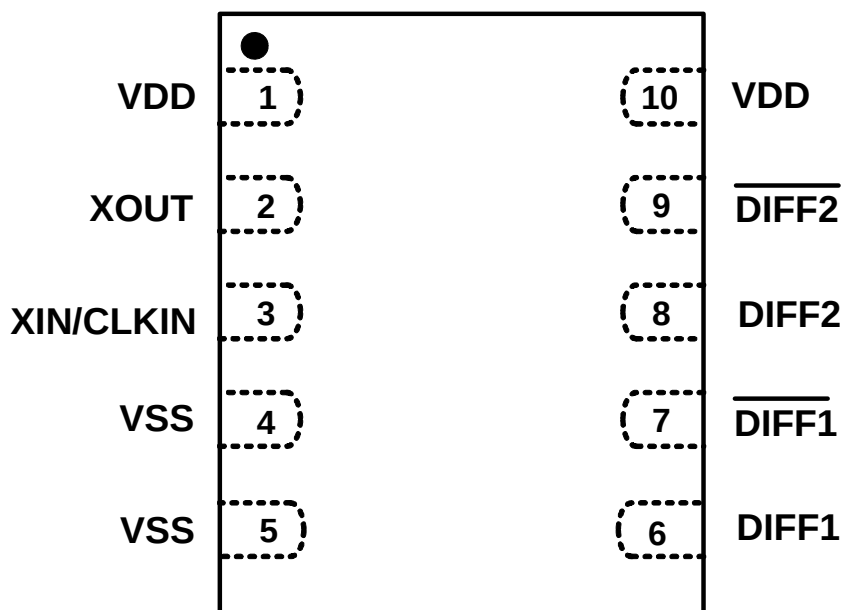


Figure 6. 10-Pin TDFN

Table 7. 10-Pin TDFN Descriptions

Pin #	Name	Type	Description
1	VDD	PWR	3.3 V power supply.
2	XOUT	O	25.00 MHz crystal output, Float XOUT if using only CLKIN (clock input).
3	XIN/CLKIN	I	25.00 MHz crystal input or 3.3 V, 25 MHz clock Input.
4	VSS	GND	Ground.
5	VSS	GND	Ground.
6	DIFF1	O, DIF	0.7 V, 100 MHz differential clock output.
7	$\overline{\text{DIFF1}}$	O, DIF	0.7 V, 100 MHz differential clock output.
8	DIFF2	O, DIF	0.7 V, 100 MHz differential clock output.
9	$\overline{\text{DIFF2}}$	O, DIF	0.7 V, 100 MHz differential clock output.
10	VDD	PWR	3.3 V power supply.

Si52112-B3/B4

4.2. 8-Pin TSSOP

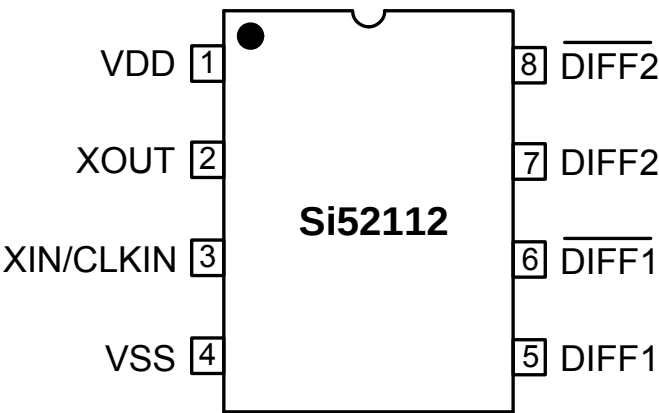


Figure 7. 8-Pin TSSOP

Table 8. 8-Pin TSSOP Descriptions

Pin #	Name	Type	Description
1	VDD	PWR	3.3 V Power supply.
2	XOUT	O	25.00 MHz crystal output, Float XOUT if using only CLKIN (clock input).
3	XIN/CLKIN	I	25.00 MHz crystal input or 3.3 V, 25 MHz clock Input.
4	VSS	GND	Ground.
5	DIFF1	O, DIF	0.7 V, 100 MHz differentials clock.
6	$\overline{\text{DIFF1}}$	O, DIF	0.7 V, 100 MHz differentials clock.
7	DIFF2	O, DIF	0.7 V, 100 MHz differentials clock.
8	$\overline{\text{DIFF2}}$	O, DIF	0.7 V, 100 MHz differentials clock.

5. Ordering Guide

Part Number	Spread Option	Package Type	Temperature
Si52112-B3-GM2	No Spread	10-pin TDFN	Extended, -40 to 85 °C
Si52112-B3-GM2R	No Spread	10-pin TDFN—Tape and Reel	Extended, -40 to 85 °C
Si52112-B3ZM21	No Spread	10-pin TDFN (UTAC only)	Extended, -40 to 85 °C
Si52112-B3ZM21R	No Spread	10-pin TDFN (UTAC only) — Tape and Reel	Extended, -40 to 85 °C
Si52112-B3-GT	No Spread	8-pin TSSOP	Extended, -40 to 85 °C
Si52112-B3-GTR	No Spread	8-pin TSSOP - Tape and Reel	Extended, -40 to 85 °C
Si52112-B4-GM2	-0.5% Spread	10-pin TDFN	Extended, -40 to 85 °C
Si52112-B4-GM2R	-0.5% Spread	10-pin TDFN—Tape and Reel	Extended, -40 to 85 °C
Si52112-B4ZM21	-0.5% Spread	10-pin TDFN (UTAC only)	Extended, -40 to 85 °C
Si52112-B4ZM21R	-0.5% Spread	10-pin TDFN (UTAC only) — Tape and Reel	Extended, -40 to 85 °C
Si52112-B4-GT	-0.5% Spread	8-pin TSSOP	Extended, -40 to 85 °C
Si52112-B4-GTR	-0.5% Spread	8-pin TSSOP - Tape and Reel	Extended, -40 to 85 °C

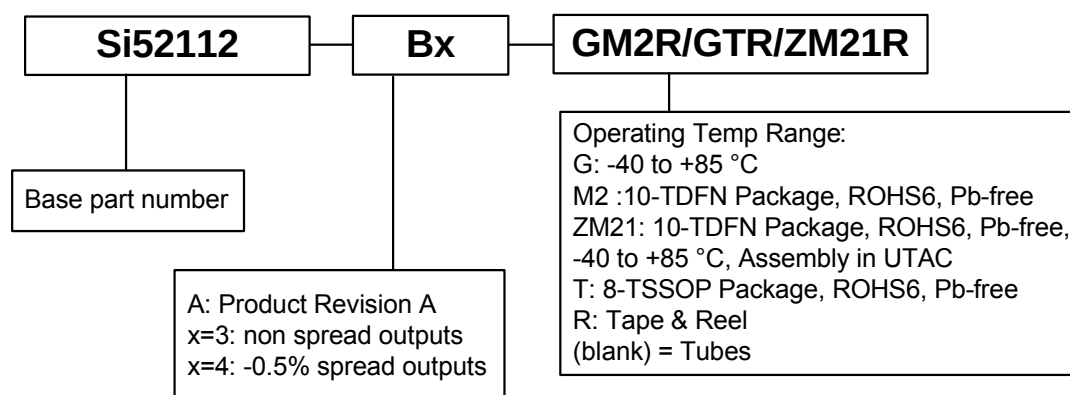


Figure 8. Ordering Information

6. Package Outlines

6.1. TDFN Package

Figure 9 illustrates the package details for the 10-pin TDFN. Table 9 lists the values for the dimensions shown in the illustration.

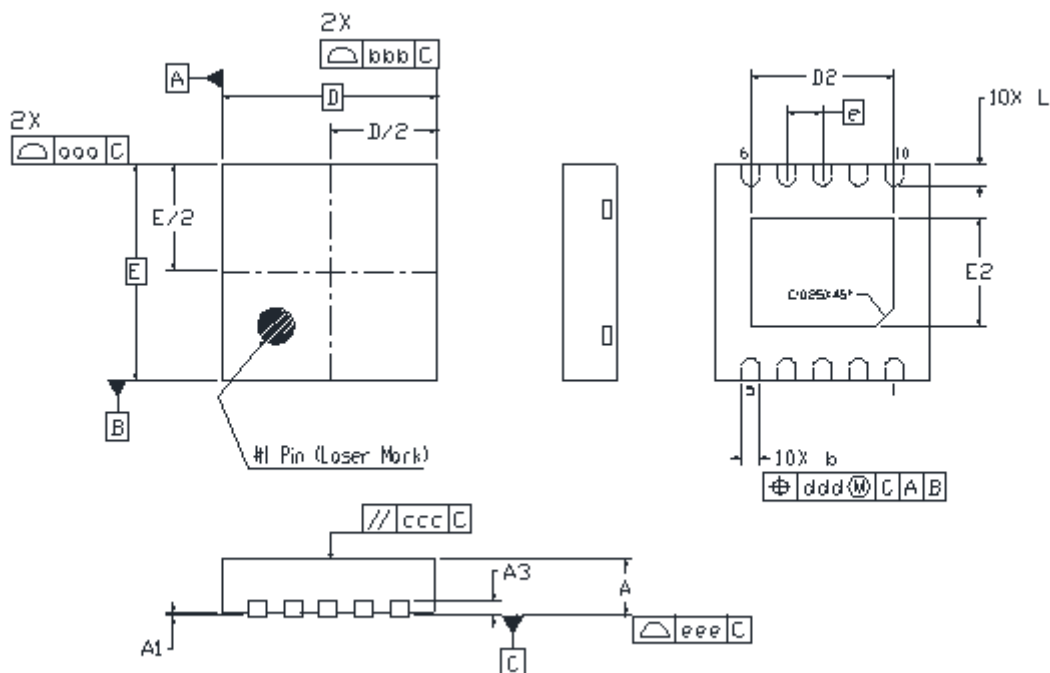


Figure 9. 10-Pin TDFN Package Drawing

Table 9. TDFN Package Diagram Dimensions

Symbol	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.18	0.25	0.30
D	3.00 BSC.		
D2	1.90	2.00	2.10
e	0.50 BSC		
E	3.00 BSC		
E2	1.40	1.50	1.60
L	0.25	0.30	0.35
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.10		
eee	0.08		
Notes:			
1. All dimensions shown are in millimeters (mm) unless otherwise noted.			
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.			
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.			
4. This drawing conforms to the JEDEC Solid State Outline MO-229.			

6.2. TSSOP Package

Figure 10 illustrates the package details for the 8-pin TSSOP. Table 10 lists the values for the dimensions shown in the illustration.

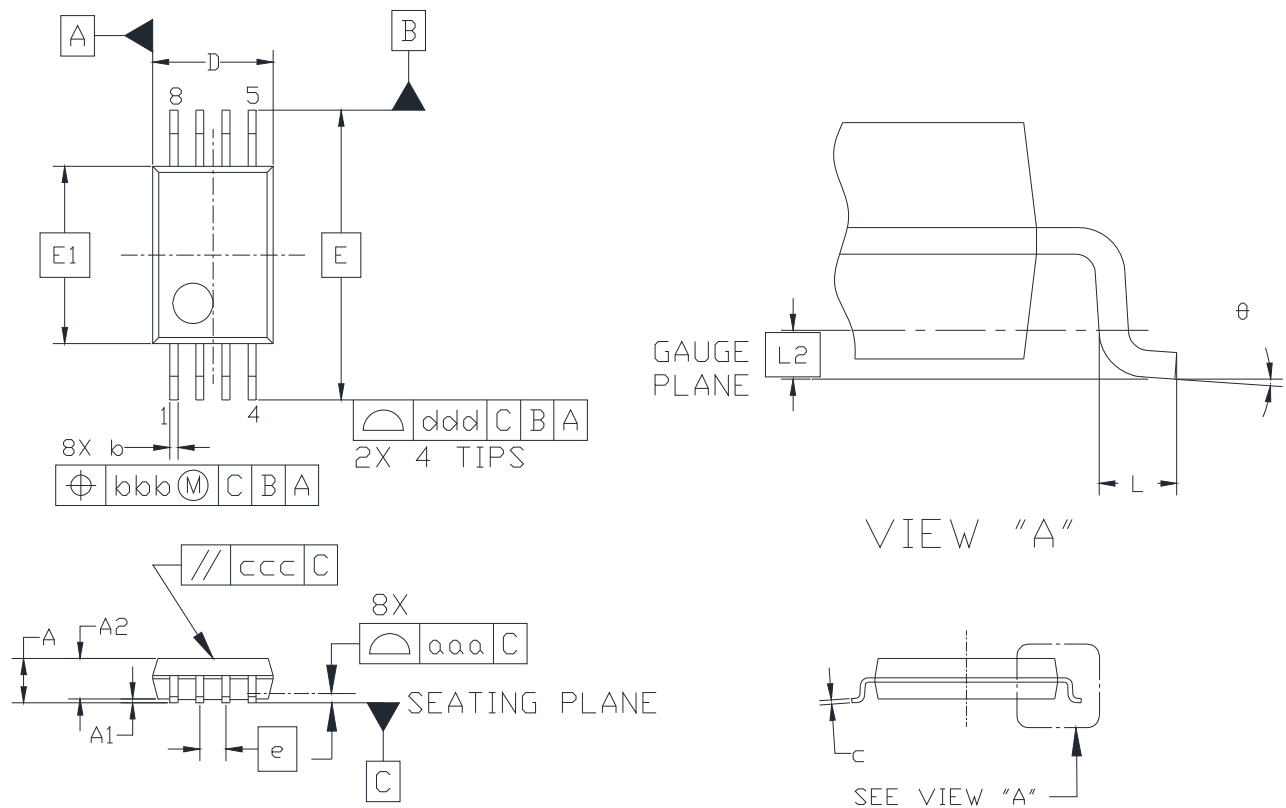
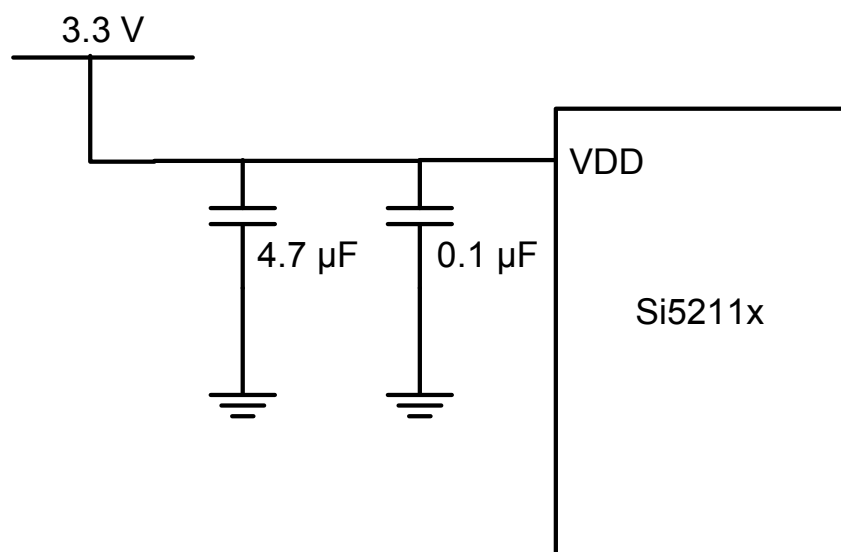


Figure 10. 8-Pin TSSOP Package Drawing

Table 10. TSSOP Package Diagram Dimensions

Symbol	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	0.90	1.05
b	0.19	—	0.30
c	0.09	—	0.20
D	2.90	3.00	3.10
E	6.40 BSC		
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L2	0.25 BSC		
θ	0°	—	8°
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.20		
Notes:			
1. All dimensions shown are in millimeters (mm) unless otherwise noted.			
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.			
3. This drawing conforms to the JEDEC Solid State Outline MO-153, Variation AA.			
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.			

7. Recommended Design Guideline



Note: FB Specifications:
DC resistance 0.1–0.3 Ω
Impedance at 100 MHz $\geq 1000 \Omega$

Figure 11. Recommended Application Schematic

DOCUMENT CHANGE LIST

Revision 1.0 to Revision 1.1

- Added “4.2. 8-Pin TSSOP” pin description on page 12.



ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

www.silabs.com/CBPro



Timing Portfolio
www.silabs.com/timing



SW/HW
www.silabs.com/CBPro



Quality
www.silabs.com/quality



Support and Community
community.silabs.com

Disclaimer

Silicon Laboratories intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Laboratories products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Laboratories reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Laboratories shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products must not be used within any Life Support System without the specific written consent of Silicon Laboratories. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Laboratories products are generally not intended for military applications. Silicon Laboratories products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.

Trademark Information

Silicon Laboratories Inc., Silicon Laboratories, Silicon Labs, SiLabs and the Silicon Labs logo, CMEMS®, EFM, EFM32, EFR, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZMac®, EZRadio®, EZRadioPRO®, DSPLL®, ISOModem®, Precision32®, ProSLIC®, SiPHY®, USBXpress® and others are trademarks or registered trademarks of Silicon Laboratories Inc. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.



Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

<http://www.silabs.com>