# SZA-5044
# SZA-5044Z

RoHS Compliant & GreenPackage

## 4.9 – 5.9 GHz 5V Power Amplifier

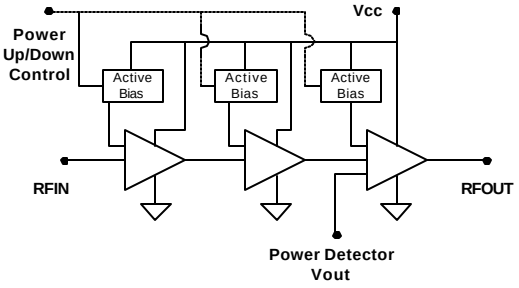


**4mm x 4mm QFN Package**

## Product Description

Sirenza Microdevices' SZA-5044 is a high efficiency class AB Heterojunction Bipolar Transistor (HBT) amplifier housed in a low-cost surface-mountable plastic package. This HBT amplifier is made with InGaP on GaAs device technology and fabricated with MOCVD for an ideal combination of low cost and high reliability. This product is specifically designed as a final or driver stage for 802.11a equipment in the 4.9 - 5.9 GHz band for a 5V supply. Optimized on-chip impedance matching circuitry provides a 50Ω nominal RF input impedance. A single external output matching circuit covers the entire 4.9-5.9GHz band simultaneously. The external output match allows for load line optimization for other applications or optimized performance over narrower bands. This product is available in a RoHS Compliant and Green package with matte tin finish, designated by the "Z" package suffix.

### Functional Block Diagram




## Product Features

- **802.11a 54Mb/s Class AB Performance**
  **Pout = 22dBm @ 3% EVM, 5V, 343mA**
- **High Gain = 33dB**
- **Output Return Loss < -11dB for Linear Tune**
- **On-chip Output Power Detector**
- **P1dB = 30dBm @ 5V**
- **Simultaneous 4.9- 5.9GHz Performance**
- **Robust - Survives RF Input Power = +15dBm**
- **Power up/down control < 1μs, Vpc 2.9V to 5V**

## Applications

- **802.11a WLAN, OFDM**
- **5.8GHz ISM Band, 802.16 WiMAX**

### Key Specifications

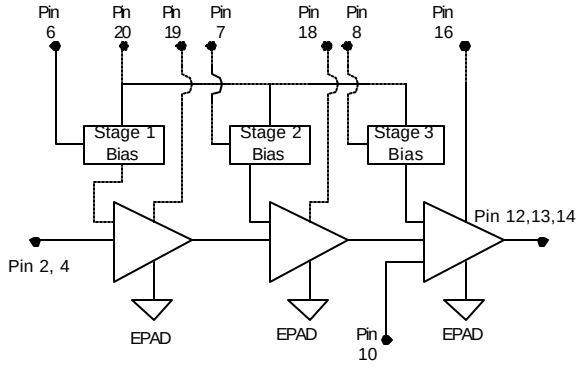
| Symbol | Parameters: Test Conditions, App circuit page 4<br>$Z_0$ = 50Ω, $V_{CC}$ = 5.0V, Icq = 270mA, $T_{BP}$ = 25°C | Unit | Min. | Typ. | Max. |
|---|---|---|---|---|---|
| $f_O$ | Frequency of Operation | MHz | 4900 | | 5900 |
| $P_{1dB}$ | Output Power at 1dB Compression – 5.15 GHz | dBm | | 30.2 | |
| | Output Power at 1dB Compression – 5.875 GHz | | 27.5 | 29 | |
| $S_{21}$ | Gain at 4.9 GHz | dB | 30.7 | 32.7 | 34.7 |
| | Gain at 5.15 GHz | dB | | 33.0 | |
| | Gain at 5.875 GHz | dB | 25.7 | 27.7 | 29.7 |
| Pout | Output power at 3% EVM 802.11a 54Mb/s - 5.15GHz | dBm | | 21 | |
| | Output Power at 3% EVM 802.11a 54Mb/s - 5.875GHz | | | 22 | |
| NF | Noise Figure at 5.875 GHz | dB | | 6.3 | |
| IM3 | Third Order Intermod at 18dBm per tone - 5.875GHz | dBc | | -39 | -35 |
| IRL | Worst Case Input Return Loss 4.9-5.875GHz | dB | 8.6 | 11.6 | |
| ORL | Worst Case Output Return Loss 4.9-5.875GHz | | 9.3 | 12.3 | |
| Vdet Range | Output Voltage Range for Pout=10dBm to 26dBm | V | | 0.8 to 1.9 | |
| Icq | Vcc Quiescent Current | mA | 230 | 270 | 310 |
| $I_{VPC}$ | Power Up Control Current, Vpc=5V ( $I_{VPC1} + I_{VPC2} + I_{VPC3}$ ) | mA | | 1.7 | |
| $I_{LEAK}$ | Off Vcc Leakage Current Vpc=0V | uA | | 8 | 100 |
| $R_{th, j-l}$ | Thermal Resistance (junction - lead) | °C/W | | 24 | |

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## Pin Out Description

| Pin # | Function | Description |
|---|---|---|
| 1,3,5,9, 11,15,17 | N/C | Pins are not used. May be grounded, left open, or connected to adjacent pin. |
| 6 | VPC1 | VPC1 is the bias control pin for the stage 1 active bias circuit and can be run from 2.9V to 5V control. An external series resistor is required for proper setting of bias levels depending on control voltage. Refer to the evaluation board schematic for resistor value. To prevent potential damage, do not apply voltage to this pin that is +1V greater than voltage applied to pin 20 (Vbias) unless Vpc supply current capability is less than 10 mA. |
| 7 | VPC2 | VPC2 is the bias control pin for the stage 2 active bias circuit and can be run from 2.9V to 5V control. An external series resistor is required for proper setting of bias levels depending on control voltage. Refer to the evaluation board schematic for resistor value. To prevent potential damage, do not apply voltage to this pin that is +1V greater than voltage applied to pin 20 (Vbias) unless Vpc supply current capability is less than 10 mA. |
| 8 | VPC3 | VPC3 is the bias control pin for the stage 3 active bias circuit and can be run from 2.9V to 5V control. An external series resistor is required for proper setting of bias levels depending on control voltage. Refer to the evaluation board schematic for resistor value. To prevent potential damage, do not apply voltage to this pin that is +1V greater than voltage applied to pin 20 (Vbias) unless Vpc supply current capability is less than 10 mA. |
| 10 | Vdet | Ouput power detector voltage. Load with 10K-100K ohms to ground for best performance. |
| 2,4 | RFIN | RF input pins. This is DC grounded internal to the IC. Do not apply voltage to this pin. All three pins must be used for proper operation. |
| 12,13,14 | RFOUT | RF output pin. This is also another connection to the 3rd stage collector |
| 16 | VC3 | 3rd stage collector bias pin. Apply 5V to this pin. |
| 18 | VC2 | 2nd stage collector bias pin. Apply 5V to this pin. |
| 19 | VC1 | 1st stage collector bias pin. Apply 5V to this pin. |
| 20 | Vbias | Active bias network VCC. Apply 5V to this pin. |
| EPAD | Gnd | Exposed area on the bottom side of the package needs to be soldered to the ground plane of the board for optimum thermal and RF performance. Several vias should be located under the EPAD as shown in the recommended land pattern (page 5). |

### Simplified Device Schematic




### Absolute Maximum Ratings

| Parameters | Value | Unit |
|---|---|---|
| VC3 Collector Bias Current (pin16) | 500 | mA |
| VC2 Collector Bias Current (pin18) | 225 | mA |
| VC1 Collector Bias Current (pin19) | 75 | mA |
| Device Voltage ($V_D$) | 7.0 | V |
| Power Dissipation | 3.4 | W |
| Operating Lead Temperature ($T_L$) | -40 to +85 | ºC |
| RF Input Power for 50 ohm RF out load | 15 | dBm |
| RF Input Power for 10:1 VSWR RF out load | 2 | dBm |
| Storage Temperature Range | -40 to +150 | ºC |
| Operating Junction Temperature ($T_J$) | +150 | ºC |
| ESD Human Body Model | >1000 | V |

**Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation the device voltage and current must not exceed the maximum operating values specified in the table on page one.**

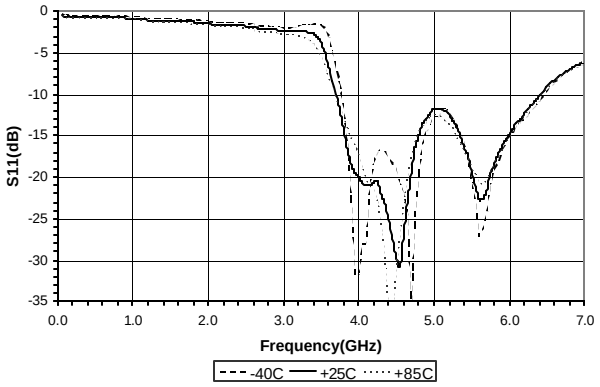
**Bias conditions should also satisfy the following expression: $I_D V_D < (T_J - T_L) / R_{TH, j-l}$**

### Caution: ESD Sensitive

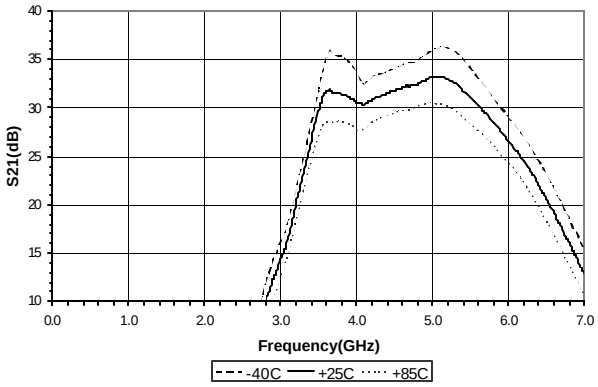
Appropriate precaution in handling, packaging and testing devices must be observed.

## 4.9 - 5.9 GHz Evaluation Board Data ($V_{BIAS}$ = 5.0V, $I_q$ = 270mA)

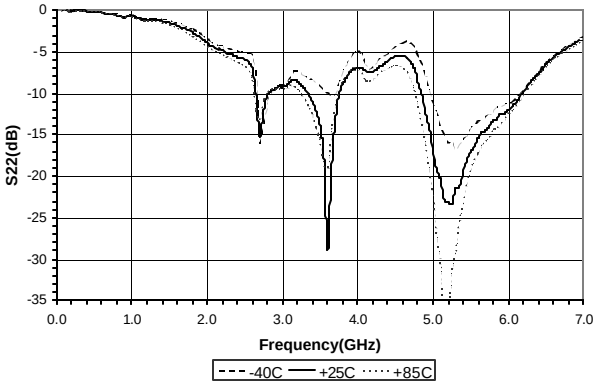
**Broadband S11 - Input Return Loss**



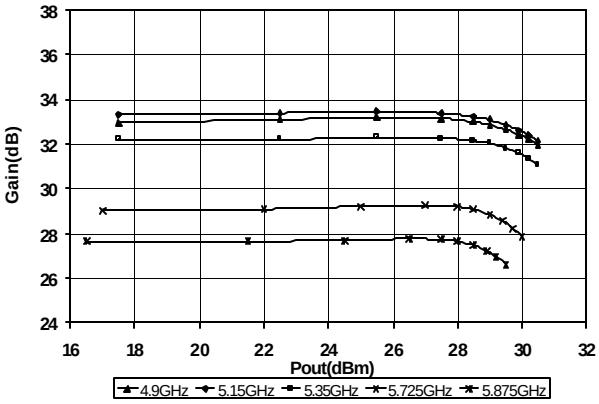

**Broadband S21 - Forward Gain**



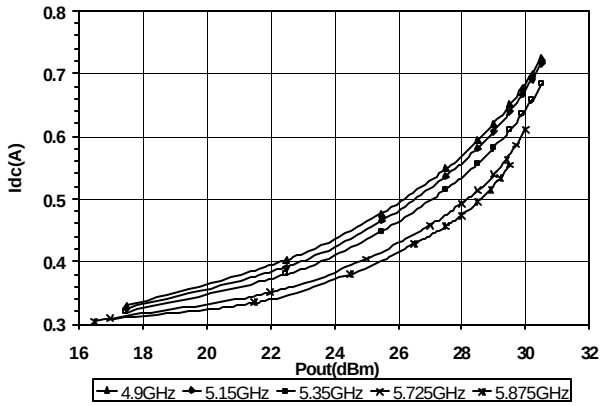

**Broadband S22 - Output Return Loss**



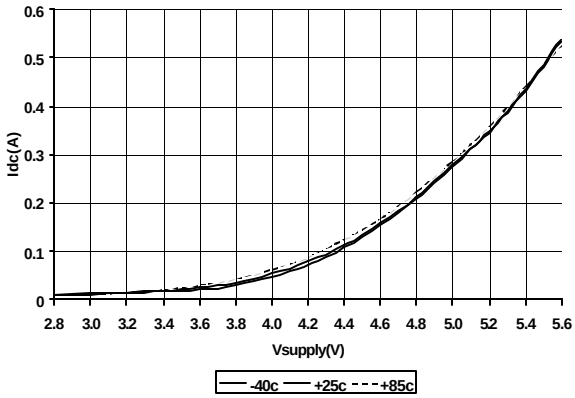

**Typical Gain vs Pout, T=+25C**




**DC Supply Current vs Pout, T=+25c**



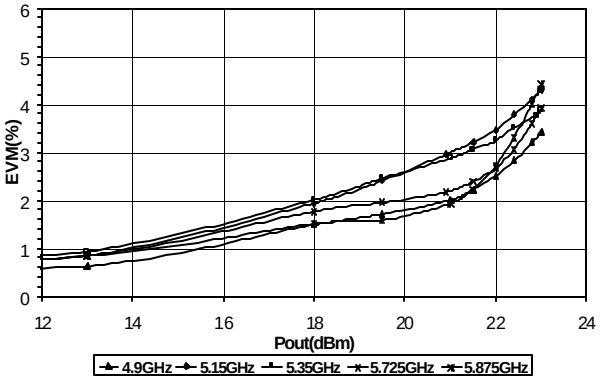

**Icq (DC bias point) vs Vsupply (V+ and Vpc)**



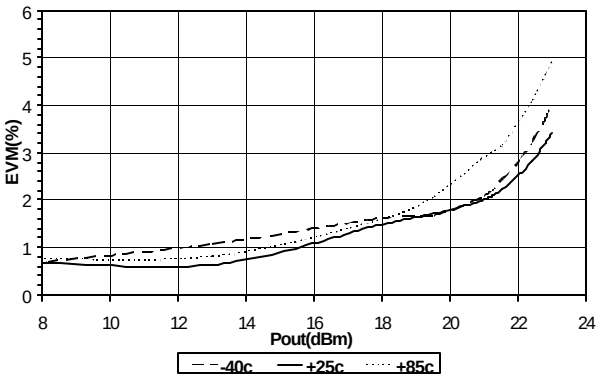
## 4.9 - 5.9 GHz Evaluation Board Data ($V_{BIAS}$ = 5.0V, $I_q$ = 270mA)

**802.11a EVM, OFDM, 54Mb/s, 64QAM**

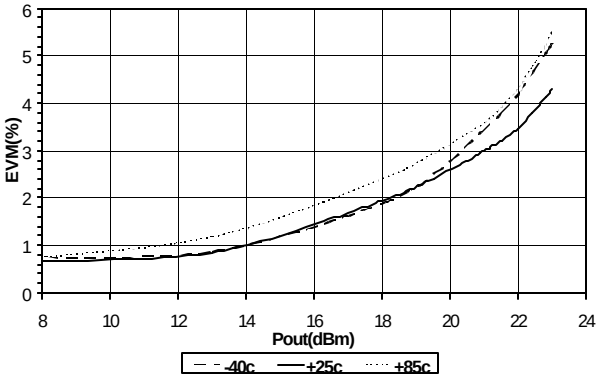
**EVM vs Pout T=+25c**
**802.11g, OFDM 54Mb/S, 64QAM**



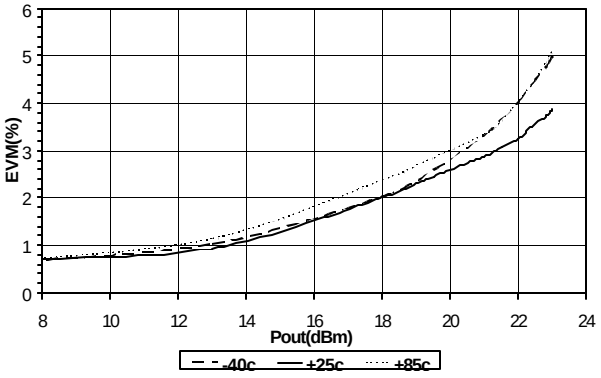

**EVM vs Pout F=4.9GHz**
**802.11g, OFDM 54Mb/S, 64QAM**



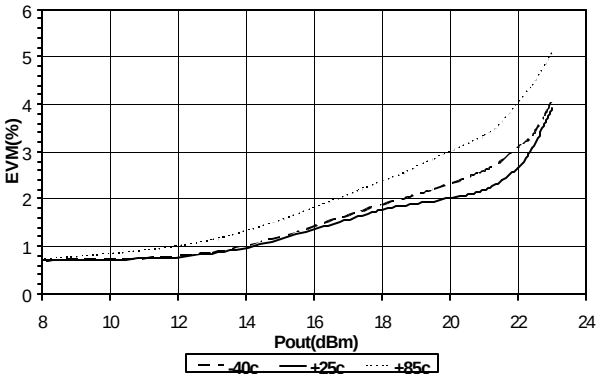

**EVM vs Pout F=5.15GHz**
**802.11g, OFDM 54Mb/S, 64QAM**



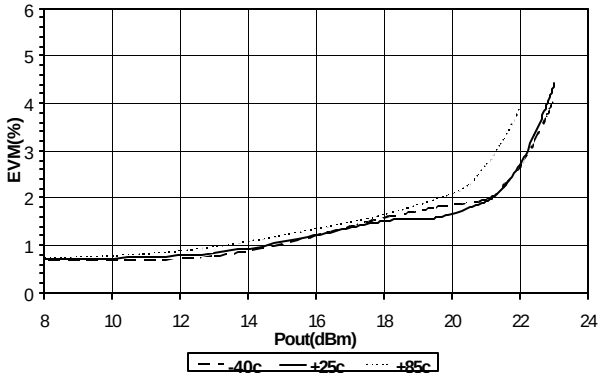

**EVM vs Pout F=5.35GHz**
**802.11g, OFDM 54Mb/S, 64QAM**



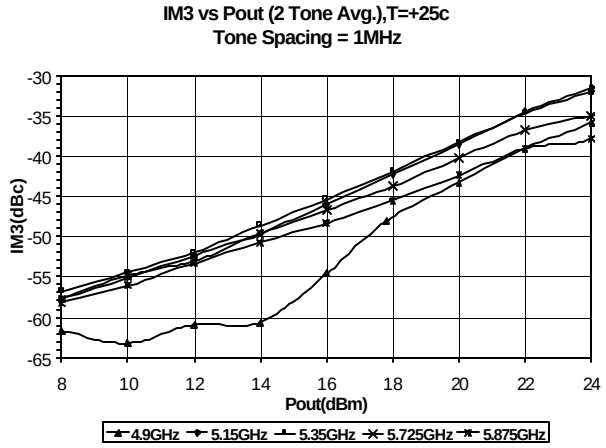

**EVM vs Pout F=5.725GHz**
**802.11g, OFDM 54Mb/S, 64QAM**

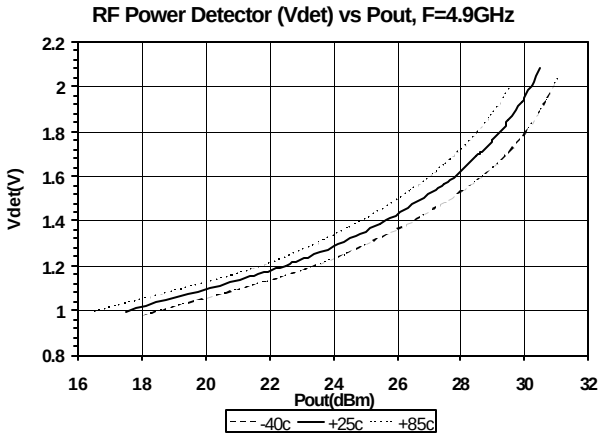


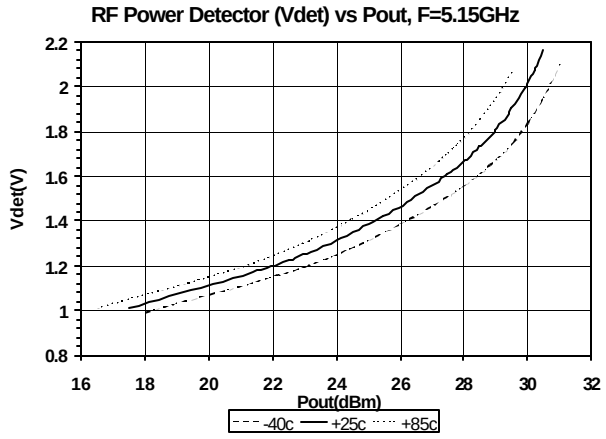

**EVM vs Pout F=5.875GHz**
**802.11g, OFDM 54Mb/S, 64QAM**

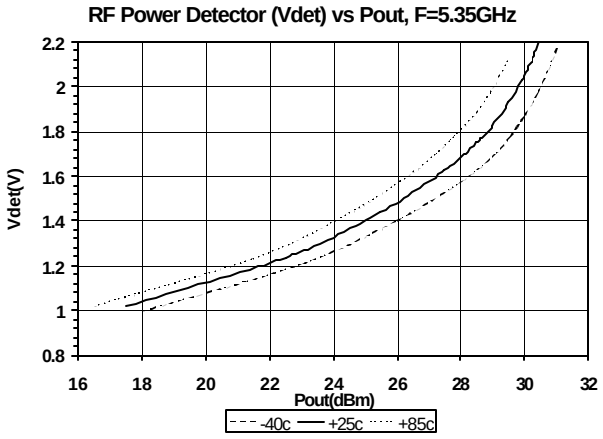


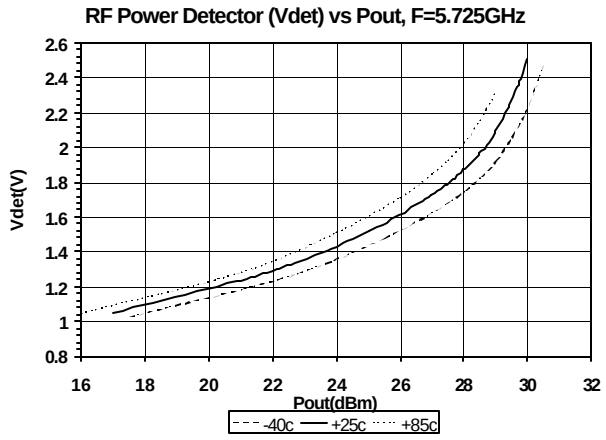
## 4.9 - 5.9 GHz Evaluation Board Data ($V_{BIAS}$ = 5.0V, $I_q$ = 270mA)

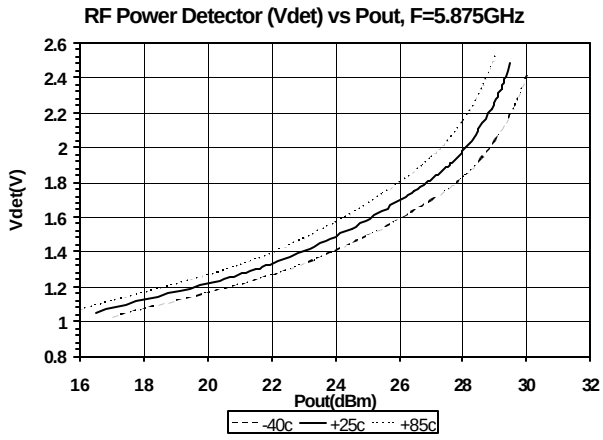


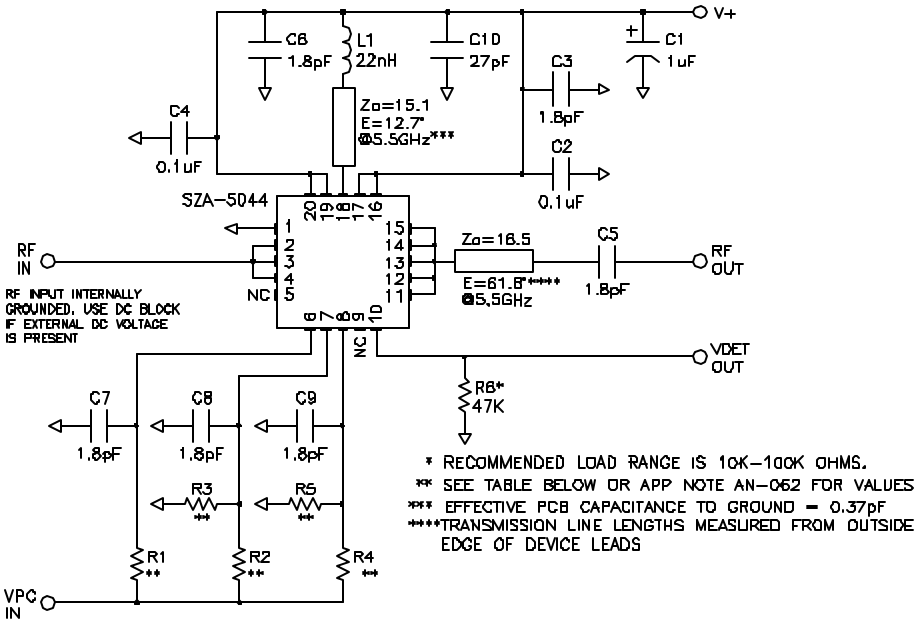



## 4.9 - 5.9 GHz Evaluation Board Schematic For V+ = Vcc = 5.0V

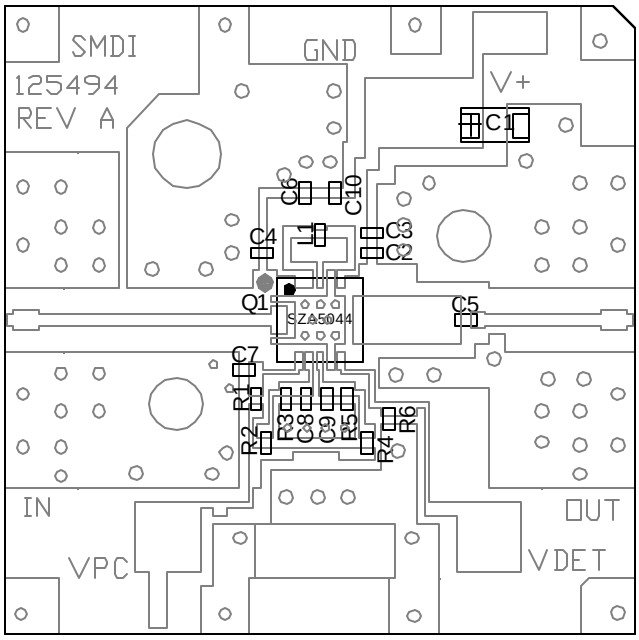



**Notes:**
Pins 1,3,5,9,11,15 and 17 are unwired (N/C) inside the package. Refer to page 2 for detailed pin descriptions. Some of these pins are wired to adjacent pins or grounded as shown in the application circuit. This is to maintain consistency with the evaluation board layout shown below. It is recommended to use this layout and wiring to achieve the specified performance.

To prevent potential damage, do not apply voltage to the Vpc pin that is +1V greater than voltage applied to pin 20 (Vbias/Vcc) unless Vpc supply current capability is less than 10 mA.

## 4.9 - 5.9 GHz Evaluation Board Layout For V+ = Vcc = 5.0V

- Board material GETEK, 10mil thick, Dk=3.9, 2 oz. copper finish




| DESG | DESCRIPTION |
|---|---|
| Q1 | SZA-5044 |
| R1,2,3,4,5,6 | 1%, 0402 |
| C1 | 1uF 16V TANTALUM CAP |
| C2,4 | 0.1uF CAP, 0402 |
| C3,5,6,7,8,9 | 1.8pF CAP, 0402 |
| C10 | 27pF CAP, 0402 |
| L1 | 22nH IND, 0402 |

Resistor values for Vpc=2.9V to 5V (Vcc=5V, Iq=270mA)

| VPC(V) | R1 | R2 | R4 | R3 | R5 |
|---|---|---|---|---|---|
| 2.9 | 0 | 698 | 10 | OUT | OUT |
| 3.0 | 174 | 1.1K | 261 | OUT | OUT |
| 3.1 | 348 | 1.37K | 499 | OUT | OUT |
| 3.2 | 511 | 1.78K | 750 | OUT | OUT |
| 3.3 | 698 | 2.15K | 1.00K | OUT | OUT |
| 5.0 | 3.74K | 2.49K | 2.61K | 7.5K | 7.5K |

Note: See app note AN-062 for other Vcc and Vpc combinations

PCB Notes:
Do not use less than recomended ground via holes
RF Layers thicker than .020 inches (0.5mm) not recomended.

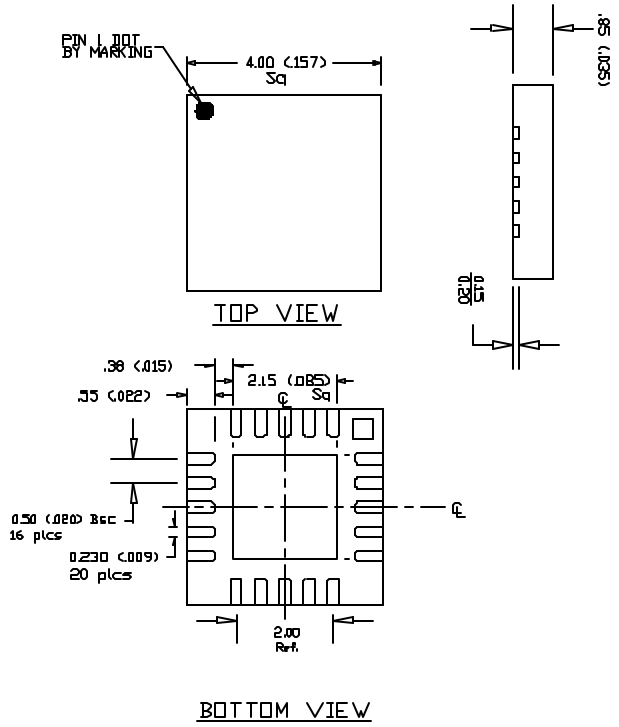
### Part Symbolization

The part will be symbolized with an "SZA-5044" for Sn/Pb plating or "SZA-5044Z" for RoHS green compliant product. Marking designator will be on the top surface of the package.

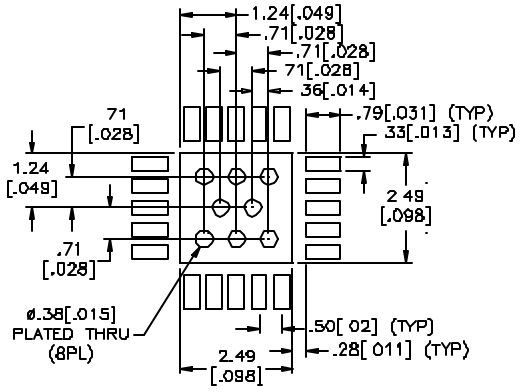
### Part Number Ordering Information

| Part Number | Reel Size | Devices/Reel |
|---|---|---|
| SZA-5044 | 13" | 3000 |
| SZA-5044Z | 13" | 3000 |

**Package Outline Drawing (dimensions in mm): Refer to package outlline drawing for more detail.**




**Recommended Land Pattern (dimensions in mm[in])**




**Recommended PCB Soldermask (SMBOC) for Land Pattern (dimensions in mm[in]):**

