SY89846U

1.5GHz Precision, LVPECL 1:5 Fanout with 2:1 MUX and Fail Safe Input with Internal Termination

Precision Edge®

General Description

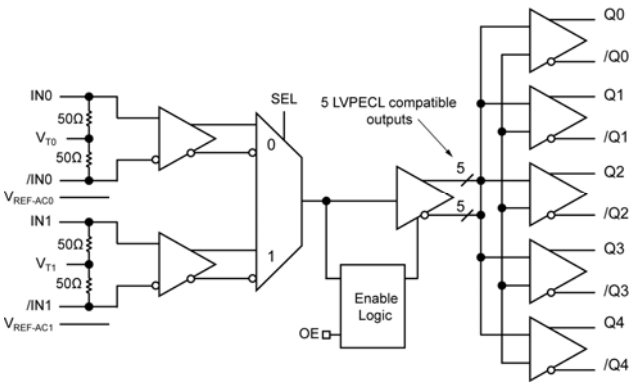
The SY89846U is a 2.5/3.3V, 1:5 LVPECL fanout buffer with a 2:1 differential input multiplexer (MUX). A unique Fail-Safe Input (FSI) protection prevents metastable output conditions when the selected input clock fails to a DC voltage (voltage between the pins of the differential input drops significantly below 100mV).

The differential input includes Micrel's unique, 3-pin internal termination architecture that can interface to any differential signal (AC- or DC-coupled) as small as 100mV ($200mV_{PP}$) without any level shifting or termination resistor networks in the signal path. The outputs are 800mV, LVPECL with fast rise/fall times guaranteed to be less than 250ps.

The SY89846U operates from a 2.5V ±5% or 3.3V ±10% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. The SY89846U is part of Micrel's high-speed, Precision Edge® product line.

All support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Block Diagram





Precision Edge®

Features

- Selects between two inputs, and provides 5 precision LVPECL copies
- Fail-Safe Input
  - Prevents outputs from oscillating when input is invalid
- Guaranteed AC performance over temperature and supply voltage:
  - DC-to >1.5GHz throughput
  - < 900ps Propagation Delay (IN-to-Q)
  - < 250ps Rise/Fall times
- Ultra-low jitter design:
  - <1ps$_{RMS}$ random jitter
  - <1ps$_{RMS}$ cycle-to-cycle jitter
  - <10ps$_{PP}$ total jitter (clock)
  - <0.7ps$_{RMS}$ MUX crosstalk induced jitter
- Unique, patented MUX input isolation design minimizes adjacent channel crosstalk
- Unique patented internal termination and VT pin accepts DC- and AC-coupled inputs (CML, PECL, LVDS)
- Wide input voltage range. VCC to GND
- 2.5V ±5% or 3.3 ±10% supply voltage
- -40°C to +85°C industrial temperature range
- Available in 32-pin (5mm x 5mm) MLF® package

Applications

- Fail-safe clock protection
- SONET clock distribution
- Backplane distribution

Markets

- LAN/WAN
- Enterprise servers
- ATE
- Test and measurement

Precision Edge is a registered trademark of Micrel, Inc.
MLF and *Micro*LeadFrame are registered trademarks of Amkor Technology

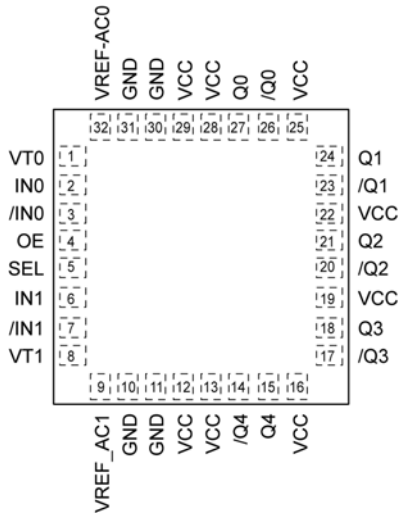
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89846UMG	MLF-32	Industrial	SY89846U with Pb-Free bar-line Indicator	NiPdAu Pb-Free
SY89846UMGTR[2]	MLF-32	Industrial	SY89846U with Pb-Free bar-line Indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals Only.
2. Tape and Reel.

Pin Configuration



32-Pin MLF® (MLF-32)

Pin Description

Pin Number	Pin Name	Pin Function
1,8	VT0, VT1	Input Termination Center-Tap: Each side of a differential input pair terminates to the VT pin. The VT pin provides a center-tap for each input (IN, /IN) to a termination network for maximum interface flexibility. See “Input Interface Applications” subsection.
2, 3 6, 7	IN0, /IN0 IN1, /IN1	Differential Inputs: These input pairs are the differential signal inputs to the device. These inputs accept AC- or DC-coupled signals as small as 100mV. The input pairs internally terminate to a VT pin through 50Ω. Each input has level shifting resistors of 3.72kΩ to VCC. This allows a wide input voltage range from VCC to GND. See Figure 3a, Simplified Differential Input Stage for details. Note that these inputs will default to a valid (either HIGH or LOW) state if left open. See “Input Interface Applications” subsection.
10, 11, 30, 31	GND, Exposed Pad	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pins.
4	OE	Single-Ended Input: This TTL/CMOS input disables and enables the Q0-Q4 outputs. It is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. When disabled, Q goes LOW and /Q goes HIGH. OE being synchronous, outputs will be enabled/disabled following a rising and a falling edge of the input clock. $V_{TH} = V_{CC}/2$.
5	SEL	Single-Ended Input: This single-ended TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if left open. $V_{TH} = V_{CC}/2$.
9, 32	VREF-AC1 VREF-AC0	Reference Voltage: These outputs bias to V_{CC}–1.2V. They are used for AC-coupling inputs IN and /IN. Connect VREF-AC directly to the corresponding VT pin. Bypass with 0.01µF low ESR capacitor to VCC. Due to limited drive capability, the VREF-AC pin is only intended to drive its respective VT pin. Maximum sink/source current is ±0.5mA. See “Input Interface Applications” subsection.
12, 13, 16, 19, 22, 25, 28, 29	VCC	Positive Power Supply: Bypass with 0.1µF||0.01µF low ESR capacitors as close to the V_{CC} pins as possible.
27, 26 24, 23 21, 20 18, 17 15, 14	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3 Q4, /Q4	LVPECL Differential Output Pairs: Differential buffered output copies of the selected input signal. The output swing is typically 800mV. Unused output pairs may be left floating with no impact on jitter. See “LVPECL Output Termination” subsection. Normally terminated with 50Ω to V_{CC}-2V. These differential LVPECL outputs are a logic function of the IN0, IN1, and SEL inputs. See “Truth Table” below.

Truth Table

Inputs					Outputs	
IN0	**/IN0**	**IN1**	**/IN1**	**SEL**	**Q**	**/Q**
0	1	X	X	0	0	1
1	0	X	X	0	1	0
X	X	0	1	1	0	1
X	X	1	0	1	1	0

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Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) .....–0.5V to +4.0V
Input Voltage (V_{IN}) .....–0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge..... 100mA
Current (V_T)
  Source or sink on VT pin..... ±100mA
Input Current
  Source or sink current on (IN, /IN) ..... ±50mA
Current (V_{REF})
  Source or sink current on V_{REF-AC}[4] ..... ±0.5mA
Maximum operating Junction Temperature .....125°C
Lead Temperature (soldering, 20sec.) .....260°C
Storage Temperature (T_s).....–65°C to +150°C

Operating Ratings [2]

Supply Voltage (V_{CC}) .....+2.375V to +2.625V
  .....+3.0V to +3.6V
Ambient Temperature (T_A)..... –40°C to +85°C
Package Thermal Resistance[3]
MLF® (θ_{JA})
  Still-Air ..... 50°C/W
MLF® (ψ_{JB})
  Junction-to-Board ..... 31°C/W

DC Electrical Characteristics [5]

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage		2.375 3.0	2.5 3.3	2.625 3.6	V V
I_{CC}	Power Supply Current	No load, max V_{CC}		60	75	mA
R_{IN}	Input Resistance (IN-to-V_T)		45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input HIGH Voltage (IN, /IN)		0.1		V_{CC}	V
V_{IL}	Input LOW Voltage (IN, /IN)		0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 2a. Note 6	0.1		1.0	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN-/IN|	See Figure 2b.	0.2		1.9	V
V_{IN_FSI}	Input Voltage Threshold that Triggers FSI			30	100	mV
V_{REF-AC}	Output Reference Voltage	$I_{VREF-AC}$ = ± 0.5mA	V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V
V_{T_IN}	Voltage from Input to V_T				1.28	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and ψ_{JB} values are determined for a 4-layer board in still air unless otherwise stated.
4. Due to the limited drive capability, use for input of the same package only.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. V_{IN} (max) is specified when V_T is floating.

LVPECL Outputs DC Electrical Characteristics [7]

V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L = 50Ω to V_{CC}-2V; T_A = –40°C to + 85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	Q, /Q	V_{CC}-1.145		V_{CC}-0.895	V
V_{OL}	Output LOW Voltage	Q, /Q	V_{CC}-1.945		V_{CC}-1.695	V
V_{OUT}	Output Voltage Swing	See Figure 2a.	550	800	950	mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 2b.	1100	1600		mV

LVTTL/CMOS DC Electrical Characteristics[7]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to + 85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		-125		30	µA
I_{IL}	Input LOW Current		-300			µA

Note:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics [8]

V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L = 50Ω to V_{CC}-2V; Input $t_r/t_f \leq$ 300ps; T_A = –40°C to + 85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	$V_{OUT} \geq$ 400mV, $V_{IN} \geq$ 200mV	1.5	2.0		GHz
		$V_{OUT} \geq$ 400mV, $V_{IN} \geq$ 100mV	1.0	1.5		GHz
t_{pd}	Differential Propagation Delay					
	IN-to-Q	100mV < $V_{IN} \leq$ 200mV, Note 9	600	850	1100	ps
	IN-to-Q	200mV < $V_{IN} \leq$ 800mV, Note 9	400	700	900	ps
	SEL-to-Q	V_{TH} = V_{CC}/2	350	600	800	ps
t_S OE	Set-up Time OE-to-IN	Note 10	300			ps
t_H OE	Hold Time IN-to-OE	Note 10	800			ps
t_{SKEW}	Output-to-Output Skew	Note 11		7	20	ps
	Input-to-Input Skew	Note 12		5	15	ps
	Part-to-Part Skew	Note 13			300	ps
t_{JITTER}	Clock					
	Random Jitter	Note 14			1	ps_{RMS}
	Cycle-to-Cycle Jitter	Note 15			1	ps_{RMS}
	Total Jitter	Note 16			10	ps_{PP}
	Crosstalk-Induced Jitter	Note 17			0.7	ps_{RMS}
t_r, t_f	Output Rise/Fall Time (20% to 80%)	At full output swing.	110	170	250	ps
	Duty Cycle	V_{IN} > 200mV	47		53	%
		100mV < $V_{IN} \leq$ 200mV	45		55	%

Notes:

8. High-frequency AC-parameters are guaranteed by design and characterization.
9. Propagation delay is measured with input t_r, $t_f \leq$ 300ps (20% to 80%). The propagation delay is a function of the rise and fall times at IN. See “Typical Operating Characteristics” for details.
10. Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold do not apply.
11. Output-to-Output skew is measured between two different outputs under identical transitions.
12. Input-to-Input skew is the time difference between the two inputs to one output, under identical input transitions.
13. Part-to-Part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
14. Random Jitter is measured with a K28.7 character pattern, measured at <f_{MAX}.
15. Cycle-to-Cycle Jitter definition: the variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.
16. Total Jitter definition: with an ideal clock input of frequency <f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
17. Crosstalk is measured at the output while applying two similar differential clock frequencies that are asynchronous with respect to each other at the inputs.

Functional Description

Clock Select (SEL)

SEL is an asynchronous TTL/CMOS compatible input that selects one of the two input signals. An internal 25kΩ pull-up resistor defaults the input to logic HIGH if left open. Input switching threshold is $V_{CC}/2$. Refer to Figure 1a.

Fail-Safe Input (FSI)

The input includes a special fail-safe circuit to sense the amplitude of the input signal and to latch the outputs when there is no input signal present, or when the amplitude of the input signal drops sufficiently below $100mV_{PK}$ ($200mV_{PP}$), typically $30mV_{PK}$. Maximum frequency of the SY89846U is limited by the FSI function. Refer to Figure 1b.

Input Clock Failure Case

If the input clock fails to a floating, static, or extremely low signal swing such that the voltage swing across the input pair is significantly less than 100mV, FSI function will eliminate a metastable condition and latch the outputs to the last valid state. No ringing and no undetermined state will occur at the output under these conditions. The output recovers to normal operation once the input signal returns to a valid state with a typical swing greater than 30mV.

Note that the FSI function will not prevent duty cycle distortion in case of a slowly deteriorating (but still toggling) input signal. Due to the FSI function, the propagation delay will depend on rise and fall time of the input signal and on its amplitude. Refer to “Typical Operating Characteristics” for detailed information.

Output Enable (OE)

OE is a synchronous TTL/CMOS compatible input that enables/disables the outputs based on the input to this pin. The enable function is synchronous so that the clock outputs will be enabled or disabled following a rising and a falling edge of the input clock. Refer to Figure 1c. Internal 25kΩ pull-up resistor defaults the input to logic HIGH if left open. Input switching threshold is $V_{CC}/2$.

Timing Diagrams

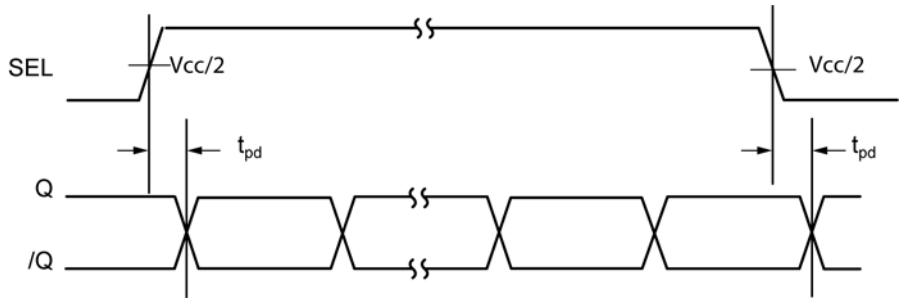


Figure 1a. SEL-to-Q Delay

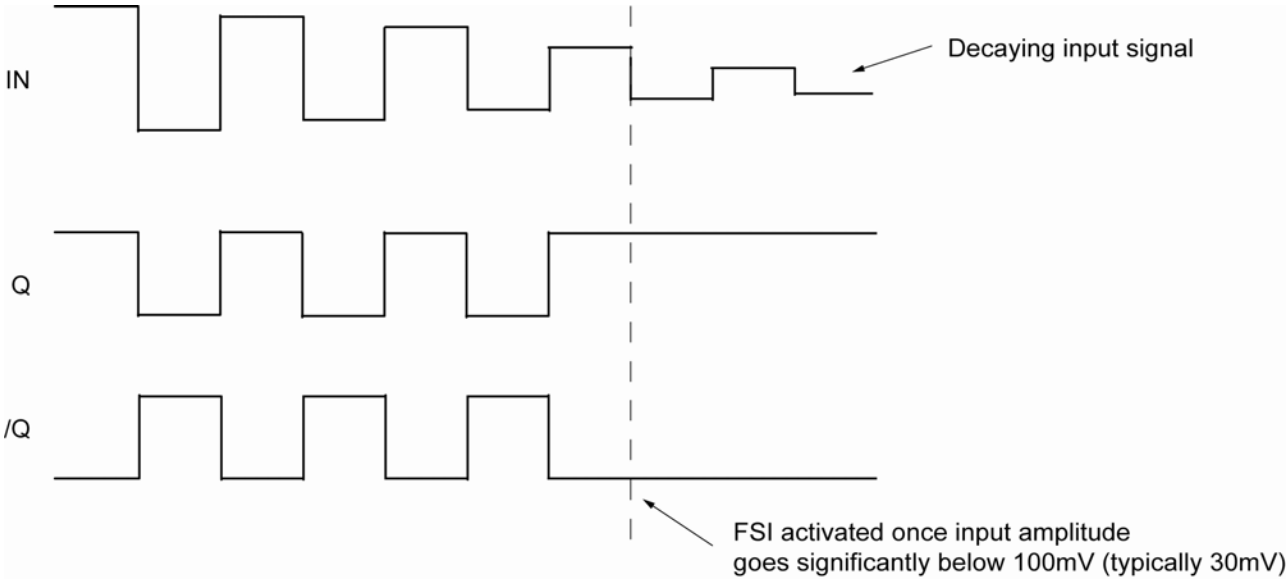


Figure 1b. Fail Safe Feature

Timing Diagrams (Continued)

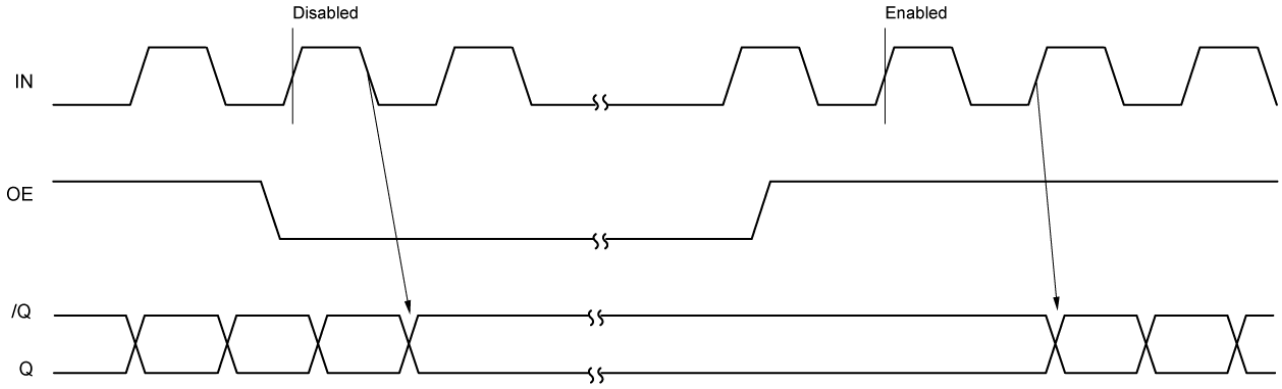


Figure 1c. Enable Output Timing Diagram

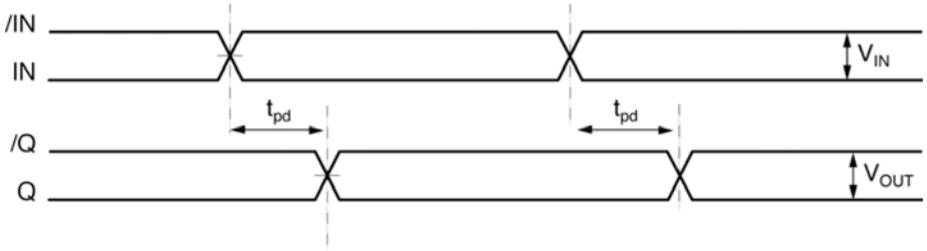


Figure 1d. Propagation Delay

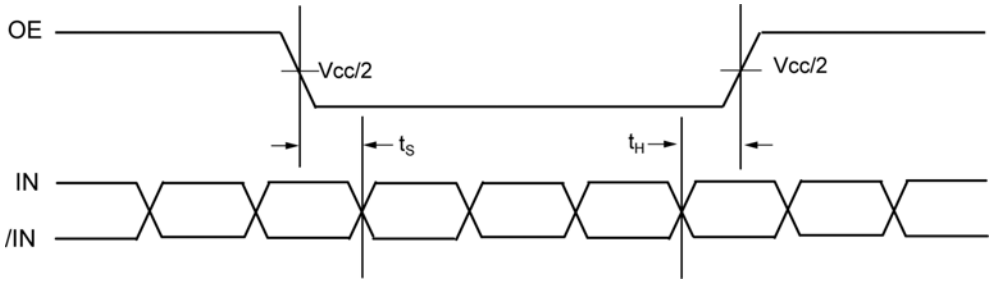
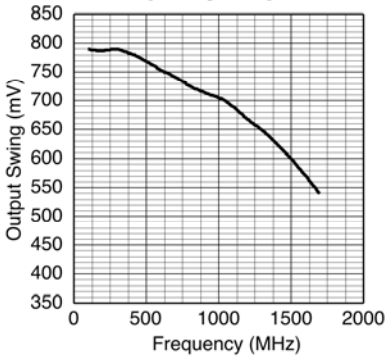


Figure 1e. Setup and Hold Time

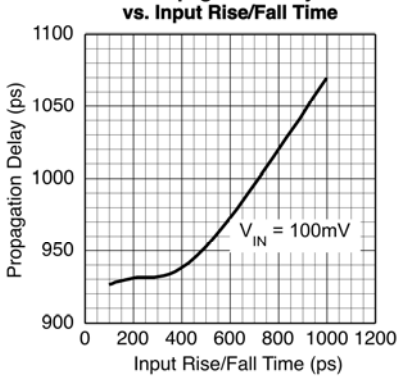
Typical Operating Characteristics

V_{CC} = 3.3V, GND = 0V, t_r / t_f ≤ 300ps, V_{IN} = 100mV, R_L = 50Ω to V_{CC}–2V; T_A = 25°C, unless otherwise stated.

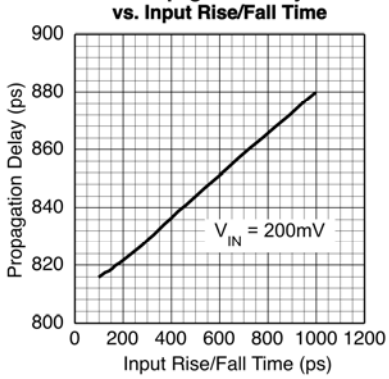
Frequency Response



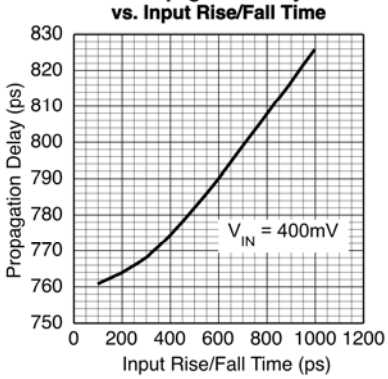
Propagation Delay vs. Input Rise/Fall Time



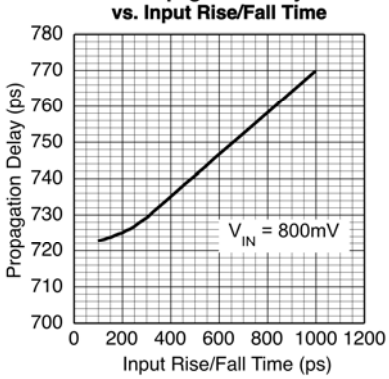
Propagation Delay vs. Input Rise/Fall Time



Propagation Delay vs. Input Rise/Fall Time



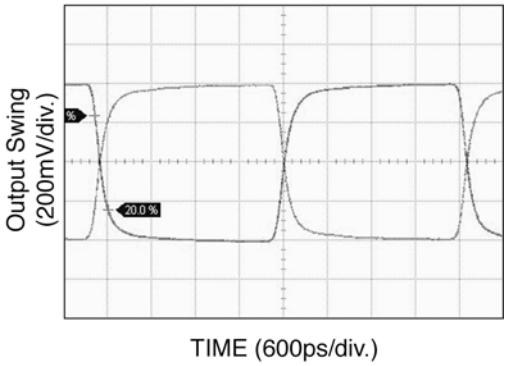
Propagation Delay vs. Input Rise/Fall Time



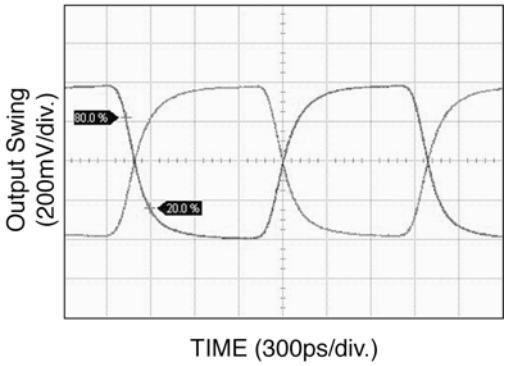
Functional Characteristics

V_{CC} = 3.3V, GND = 0V, $V_{IN} \geq 400mV$, $t_r/t_f \leq 300ps$, $R_L = 50\Omega$ to V_{CC}-2V; $T_A = 25°C$, unless otherwise stated.

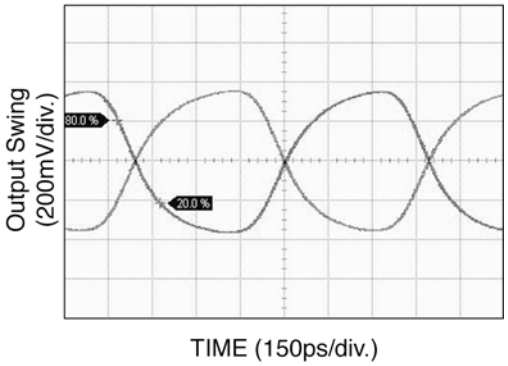
200MHz Clock



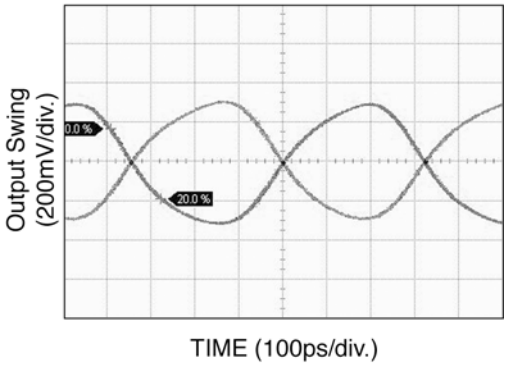
500MHz Clock



1GHz Clock



1.5GHz Clock



Single-Ended and Differential Swings

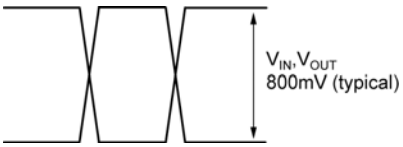


Figure 2a. Single-Ended Voltage Swing

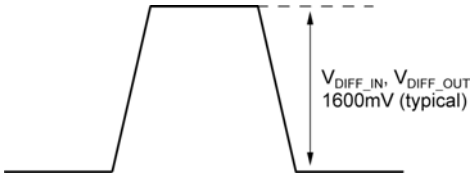


Figure 2b. Differential Voltage Swing

Input and Output Stages

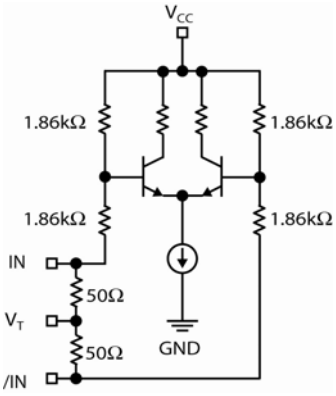


Figure 3a. Simplified Differential Input Stage

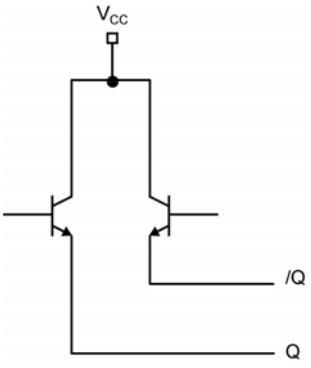


Figure 3b. Simplified Differential Output Stage

Input Interface Applications

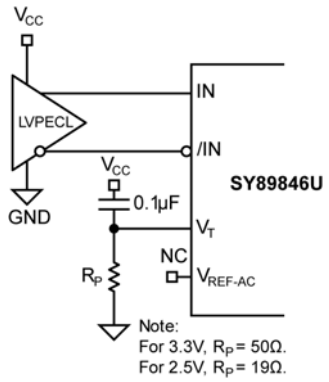


Figure 4a. LVPECL Interface (DC-Coupled)

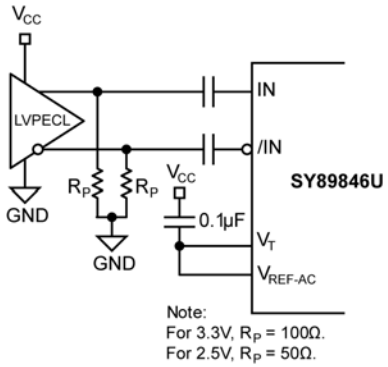
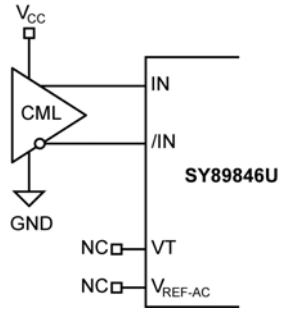


Figure 4b. LVPECL Interface (AC-Coupled)



Option: may connect V_T to V_{CC}

Figure 4c. CML Interface (DC-Coupled)

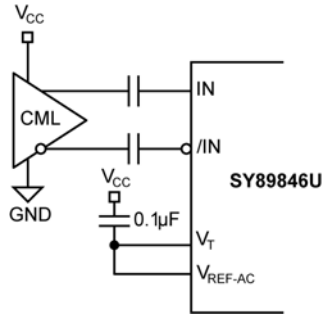


Figure 4d. CML Interface (AC-Coupled)

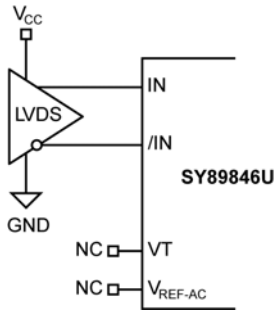


Figure 4e. LVDS Interface (DC-Coupled)

PECL Output Interface Applications

PECL has a high input impedance, a very low output impedance (open emitter), and a small signal swing which results in low EMI. PECL is ideal for driving 50Ω- and 100Ω-controlled impedance transmission lines. There are several techniques for terminating the PECL output: parallel termination-thevenin equivalent, parallel termination (3-resistor), and AC-coupled termination. Unused output pairs may be left floating. However, single-ended outputs must be terminated, or balanced.

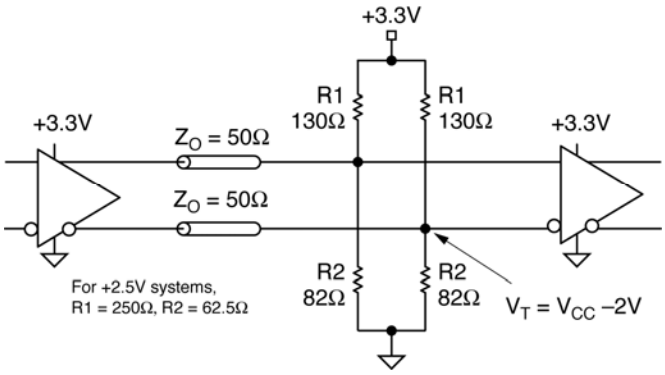
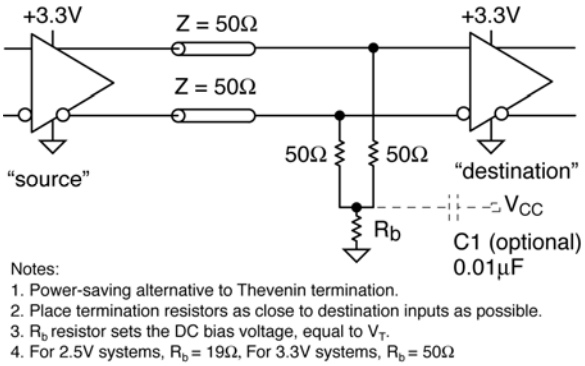


Figure 5a. Parallel Termination-Thevenin Equivalent



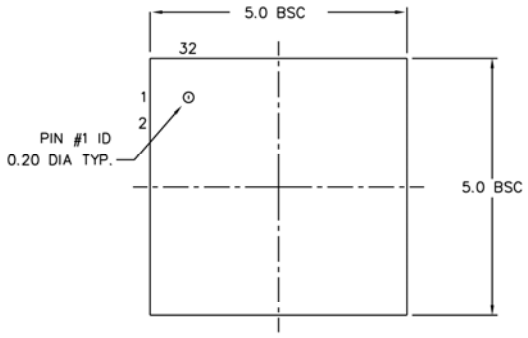
Notes:
1. Power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. R_b resistor sets the DC bias voltage, equal to V_T.
4. For 2.5V systems, R_b = 19Ω, For 3.3V systems, R_b = 50Ω

Figure 5b. Parallel Termination (3-Resistor)

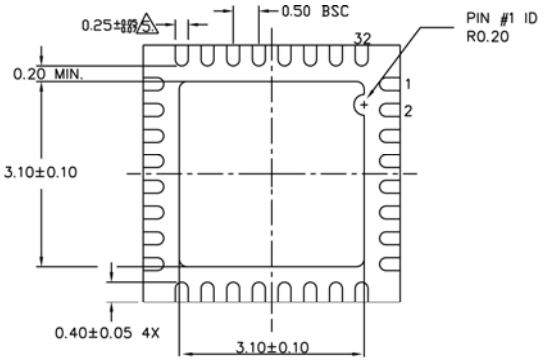
Related Product and Support Documentation

Part Number	Function	Data Sheet Link
SY89847U	Precision LVDS 1 :5 Fanout with 2 :1 MUX and Fail-Safe Input with Internal Termination	www.micrel.com/product-info/products/sy89847u.shtml.
	MLF® Application Note	www.amkor.com/products/notes_papers/MLFAppNote.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

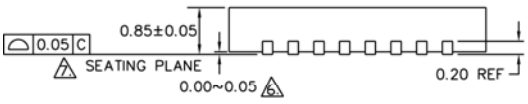
Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

32-Pin (5mm x 5mm) MLF®

Packages Notes:

1. Package meets Level 2 Moisture Sensitivity Classification.
2. All parts are dry-packed before shipment.
3. Exposed pad must be soldered to a ground for proper thermal management.

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