SY89833AL

3.3V Low-Noise, Ultra-Precision 1:4 LVDS Fanout Buffer/Translator with Internal Termination

Features

- Ultra-Low Jitter Design:
  - 80 fs_{RMS} Additive Phase Jitter (typical)
- Guaranteed AC Performance Over Temperature and Voltage:
  - DC-to > 2 GHz throughput
  - <470 ps Propagation Delay (IN-to-Q)
  - <20 ps Within-Device Skew
  - <190 ps Rise/Fall Times
- Unique Input Termination and V_T Pin Accepts DC- and AC-Coupled Inputs
- High-Speed LVDS Outputs
- 3.3V Power Supply Operation
- Industrial Temperature Range: –40°C to +85°C
- Available in 16-Pin (3 mm × 3 mm) QFN Package

Applications

- Processor Clock Distribution
- SONET Clock Distribution
- Fibre Channel Clock Distribution
- Gigabit Ethernet Clock Distribution

General Description

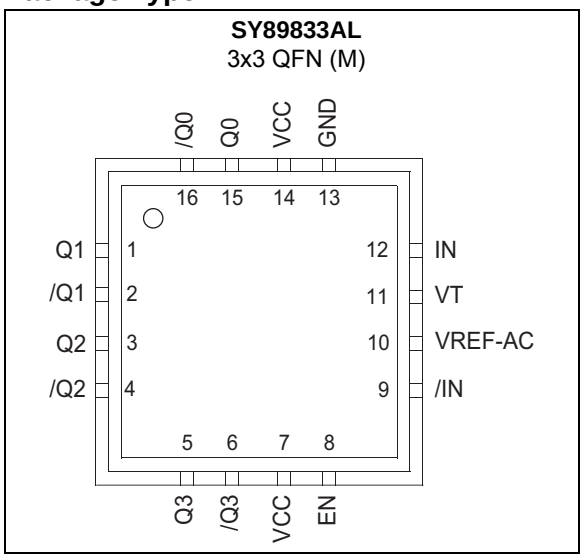
The SY89833AL is a lower noise version of the SY89833L 3.3V, high-speed 2 GHz differential, low voltage differential swing (LVDS) 1:4 fanout buffer optimized for ultra-low skew applications. Within device skew is guaranteed to be less than 20 ps over supply voltage and temperature.

The differential input buffer has a unique internal termination design that allows access to the termination network through a V_T pin. This feature allows the device to easily interface to different logic standards. A V_{REF-AC} reference is included for AC-coupled applications.

The SY89833AL is part of Microchip's high-speed clock synchronization family. For 2.5V applications, the SY89832U provides similar functionality while operating from a 2.5V ±5% supply. For applications that require a different I/O combination, consult the Microchip website and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators, and clock generators.

Package Type

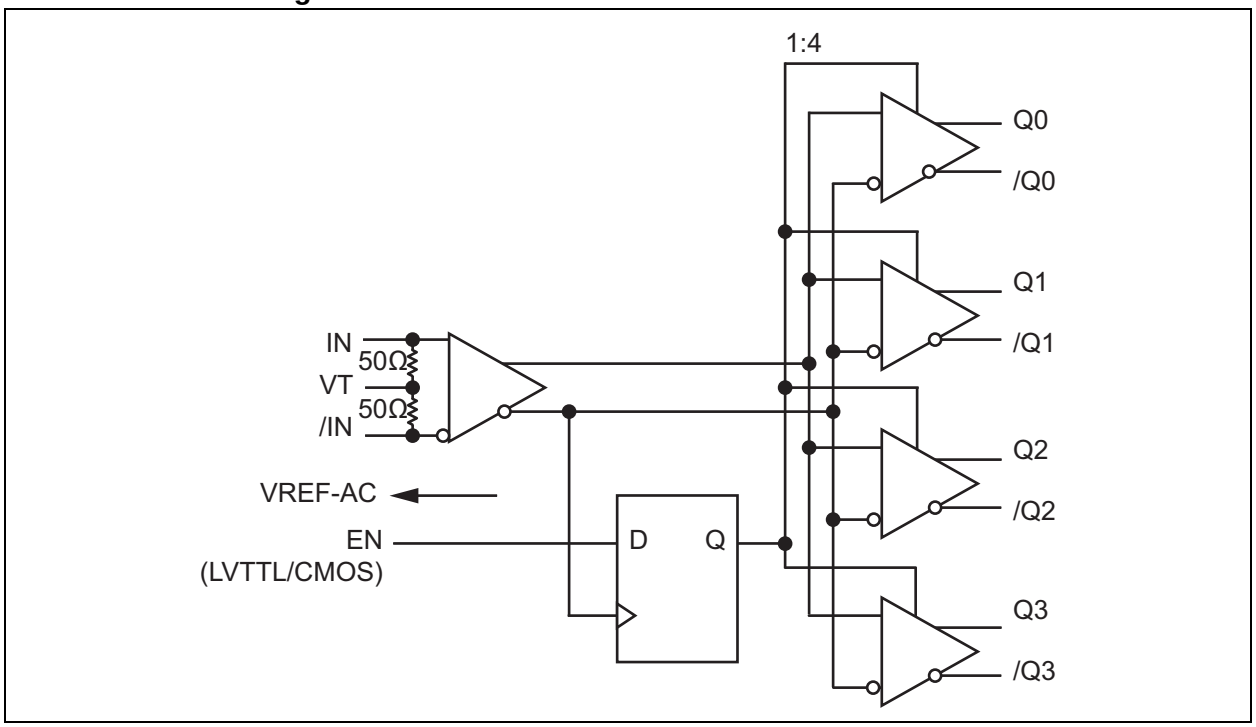
SY89833AL
3x3 QFN (M)



United States Patent No. RE44,134

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Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC} + 0.3V
LVDS Output Current (I_{OUT}) ..... +10 mA
Input Current Source or Sink Current on (IN, /IN) ..... ±50 mA
V_T Current Source or Sink Current on (V_T) ..... ±100 mA
V_{REF-AC} Current Source or Sink Current on (V_{REF-AC}) ..... ±2 mA

Operating Ratings ‡

Supply Voltage Range ..... +3.0V to +3.6V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Characteristics: T_A = –40°C to +85°C, unless otherwise stated. **(Note 1)**.						
Symbol	**Parameters**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
V_{CC}	Power Supply Voltage Range	3.0	3.3	3.6	V	—
I_{CC}	Power Supply Current	—	75	100	mA	No load; max. V_{CC}
R_{IN}	Input Resistance (IN-to-V_T)	45	50	55	Ω	—
$R_{DIFF-IN}$	Differential Input Resistance (IN-to-/IN)	90	100	110	Ω	—
V_{IH}	Input High Voltage (IN-to-/IN)	1.2	—	V_{CC}	V	—
V_{IL}	Input Low Voltage (IN-to-/IN)	0	—	V_{IH} - 0.1	V	—
V_{IN}	Input Voltage Swing (IN-to-/IN)	0.1	—	1.7	V	See Figure 5-3
V_{DIFF_IN}	Differential Input Voltage	0.2	—	—	V	See Figure 5-4
$\|I_{IN}\|$	Input Current (IN, /IN)	—	—	45	mA	Note 2
V_{REF-AC}	Reference Voltage	V_{CC} - 1.525	V_{CC} - 1.425	V_{CC} - 1.325	V	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

2: Due to the internal termination (see "Input Buffer Structure" section) the input current depends on the applied voltages at IN, /IN, and V_T inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit.

TABLE 1-2: LVDS OUTPUTS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 3.3V ±10%, R_L = 100Ω across the outputs; T_A = –40°C to +85°C. (Note 1)						
Symbol	**Parameters**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
V_{OUT}	Output Voltage Swing	250	325	—	mV	see Figure 5-3
V_{DIFF_OUT}	Differential Output Voltage Swing	500	650	—	mV	see Figure 5-4
V_{OCM}	Output Common-Mode Voltage	1.125	—	1.275	V	—
ΔV_{OCM}	Change in Common-Mode Voltage	–50	—	50	mV	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

TABLE 1-3: LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 3.3V ±10%, T_A = –40°C to +85°C. (Note 1)						
Symbol	**Parameters**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
V_{IH}	Input High Voltage	2.0	—	V_{CC}	V	—
V_{IL}	Input Low Voltage	0	—	0.8	V	—
I_{IH}	Input High Current	–125	—	30	µA	—
I_{IL}	Input Low Current	–300	—	—	µA	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

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TABLE 1-4: AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 3.3V ±10%, R_L = 100Ω across the outputs; T_A = –40°C to +85°C unless otherwise stated. (Note 1)						
Symbol	**Parameters**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
f_{MAX}	Maximum Frequency	2.0	—	—	GHz	V_{OUT} ≥ 200 mV
t_{pd}	Propagation Delay	250	—	470	ps	—
t_{SKEW}	Within-Device Skew	—	5	20	ps	Note 2
	Part-to-Part Skew	—	—	200	ps	Note 3
t_S	Set-Up Time	400	—	—	ps	Note 4
t_H	Hold Time	400	—	—	ps	Note 4
t_{JITTER}	Additive Phase Jitter, RMS	—	80	—	fs	622.08 MHz @ 3.3V, Integration range: 12 kHz to 20 MHz
t_r/t_f	Output Rise/Fall Times (20% to 80%)	60	110	190	ps	At Full Output Swing
—	Duty Cycle	47	—	53	%	Differential I/O

Note 1: High-frequency AC parameters are guaranteed by design and characterization.

2: Within device skew is measured between two different outputs under identical input transitions.

3: Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.

4: Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold times do not apply.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Operating Temperature	T_J	—	—	+125	°C	Note 1
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 20s
Ambient Temperature	T_A	–40	—	+85	°C	—
Package Thermal Resistances (Note 2)						
16-pin 3 mm x 3 mm QFN (Still-Air)	θ_{JA}	—	60	—	°C/W	—
16-pin 3 mm x 3 mm QFN	Ψ_{JB}	—	33	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2: Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. Ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

V_{CC} = 3.3V, GND = 0V, V_{IN} = 400 mV, R_L = 100Ω across the outputs; T_A = +25°C unless otherwise stated.

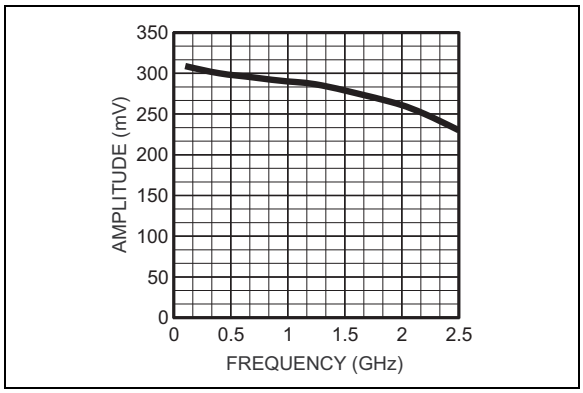


FIGURE 2-1: *Output Swing vs. Frequency.*

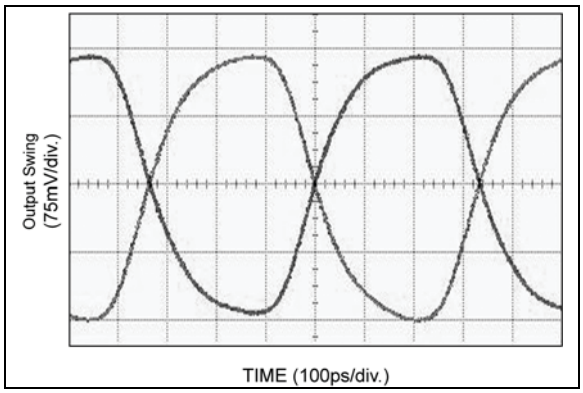


FIGURE 2-4: *1.5 GHz Output.*

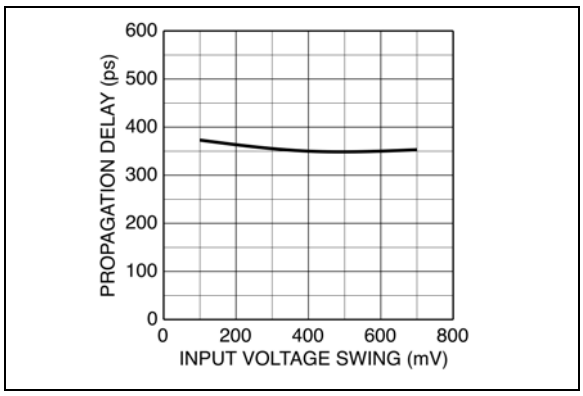


FIGURE 2-2: *Propagation Delay vs. Input Voltage Swing.*

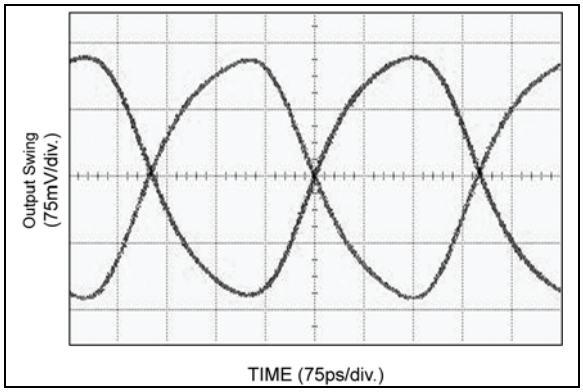


FIGURE 2-5: *2 GHz Output.*

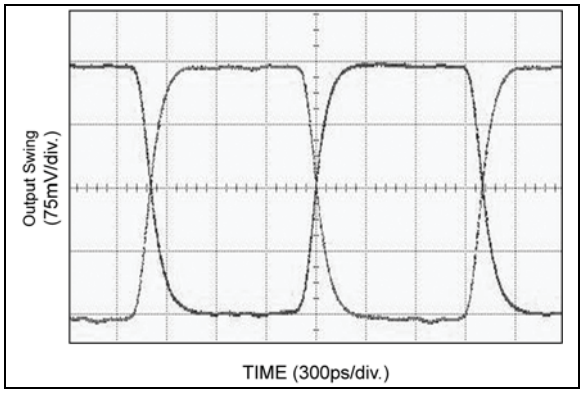


FIGURE 2-3: *500 MHz Output.*

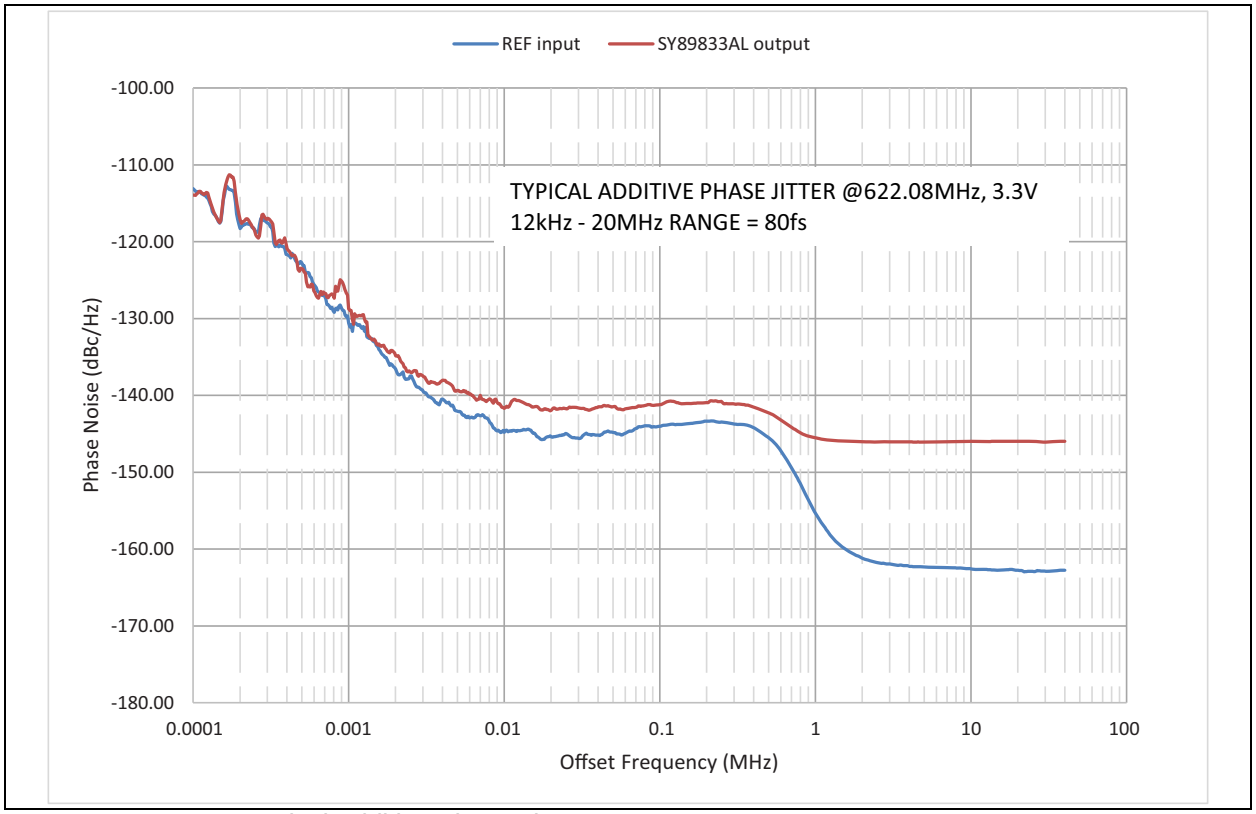


FIGURE 2-6: *Typical Additive Phase Jitter.*

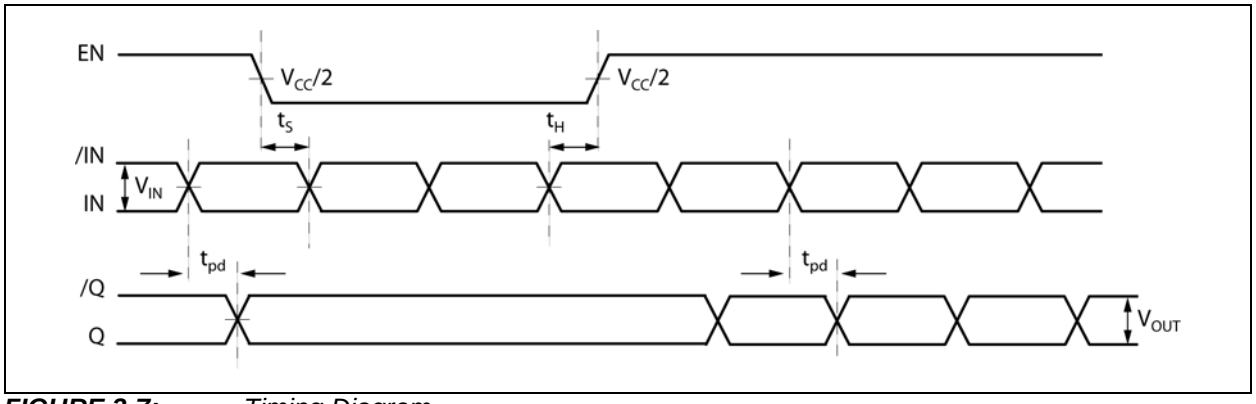


FIGURE 2-7: *Timing Diagram.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
15, 16 1, 2 3, 4 5, 6	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3	LVDS Differential Outputs: Normally terminated with 100Ω across the pair (Q, /Q). See the LVDS Outputs section, Figure 5-1. Unused outputs should be terminated with a 100Ω resistor across each pair.
8	EN	This single-ended TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable will only occur when the outputs are in a logic low state. Note that this input is internally connected to a 25 kΩ pull-up resistor and will default to logic high state (enabled) if left open.
9, 12	/IN, IN	Differential Input: This input pair is the differential signal input to the device. Input accepts AC- or DC-Coupled differential signals as small as 100 mV. Each pin of the pair internally terminates to a V_T pin through 50Ω. Note that this input will default to an intermediate state if left open. Please refer to the Input Interface Applications section for more details.
10	V_{REF-AC}	Reference Voltage: These outputs bias to V_{CC} – 1.425V.They are used when AC coupling the inputs (IN, /IN). For AC-coupled applications, connect V_{REF-AC} to V_T pin and bypass with 0.01 µF low-ESR capacitor to V_{CC}. See the Input Interface Applications section for more details. Maximum sink/source current is ±1.5 mA.
11	V_T	Input Termination Center-Tap: Each side of the differential input pair terminates to a V_T pin. The V_T pin provides a center-tap to a termination network for maximum interface flexibility. See the Input Interface Applications section for more details.
13	GND	Ground. GND pin and exposed pad must be connected to the most negative potential of the device ground.
7, 14	V_{CC}	Positive Power Supply: Bypass with 0.1 µF//0.01 µF low-ESR capacitors and place as close as possible to each V_{CC} pin.

TABLE 3-2: TRUTH TABLE

IN	/IN	EN	Q	/Q
0	1	1	0	1
1	0	1	1	0
X	X	0	0 (Note 1)	1 (Note 1)

Note 1: On next negative transition of the input signal (IN).

4.0 INPUT INFORMATION

4.1 Input Stage

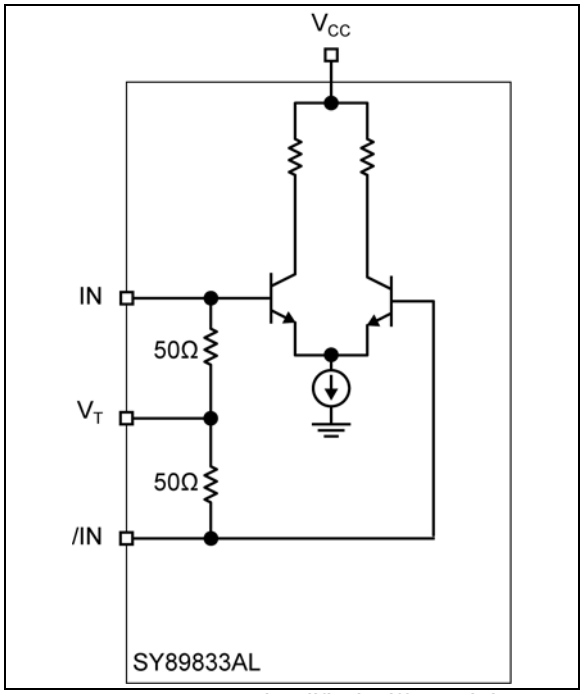


FIGURE 4-1: *Simplified Differential Input Buffer.*

4.2 Input Interface Applications

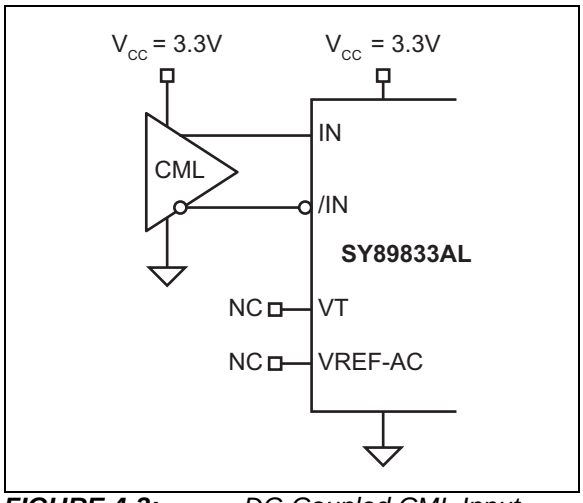


FIGURE 4-2: *DC-Coupled CML Input Interface (Option: May Connect V_T to V_{CC}).*

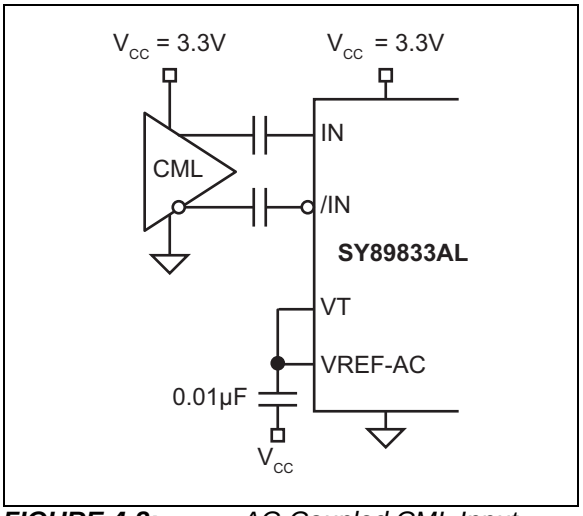


FIGURE 4-3: *AC-Coupled CML Input Interface.*

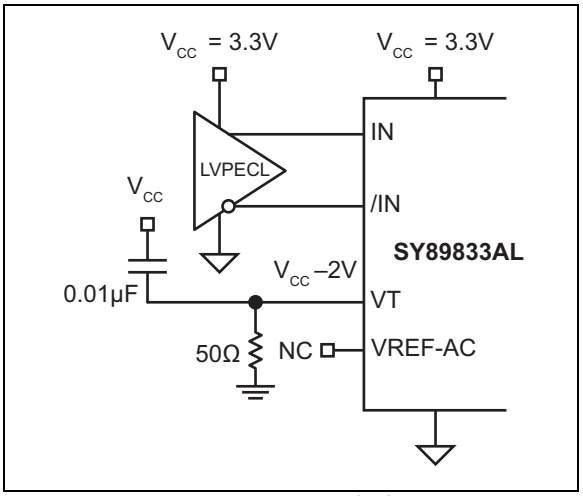


FIGURE 4-4: *DC-Coupled LVPECL Input Interface.*

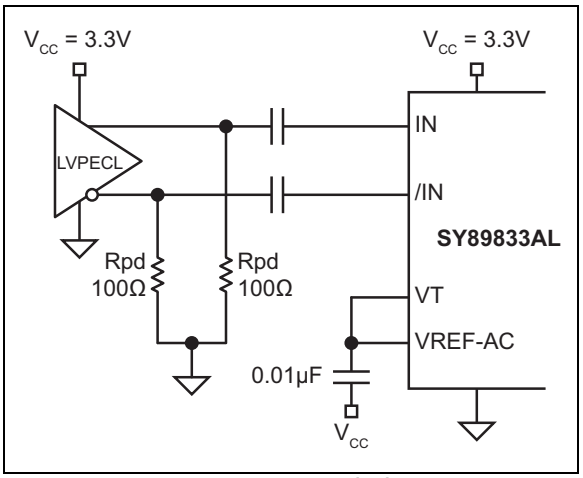


FIGURE 4-5: *AC-Coupled LVPECL Input Interface.*

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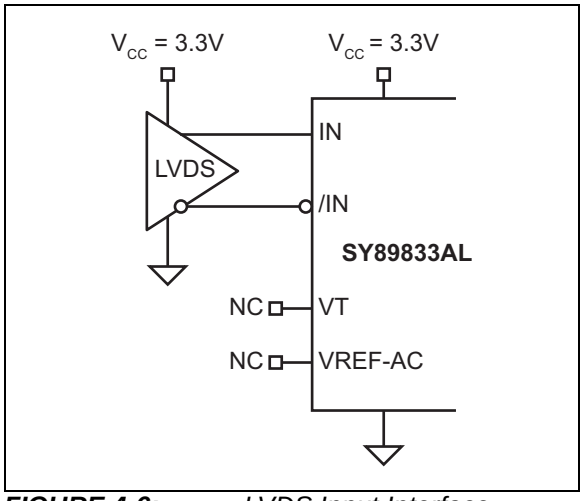


FIGURE 4-6: *LVDS Input Interface.*

5.0 LVDS OUTPUTS

LVDS specifies a small swing of 325 mV typical, on a nominal 1.20V common-mode above ground. The common-mode voltage has tight limits to permit large variations in ground noise between a LVDS driver and receiver.

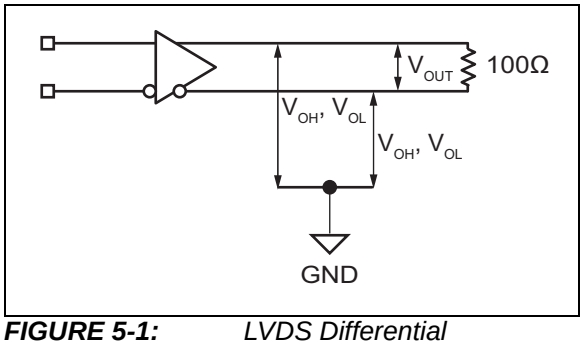


FIGURE 5-1: *LVDS Differential Measurement.*

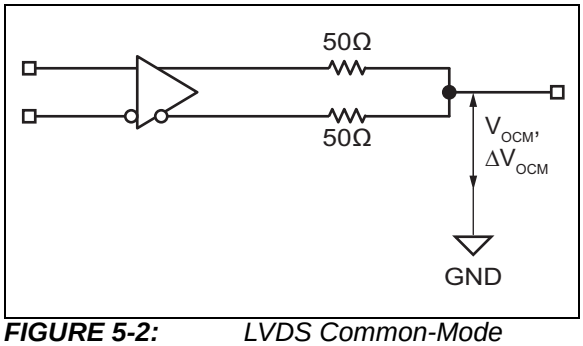


FIGURE 5-2: *LVDS Common-Mode Measurement.*

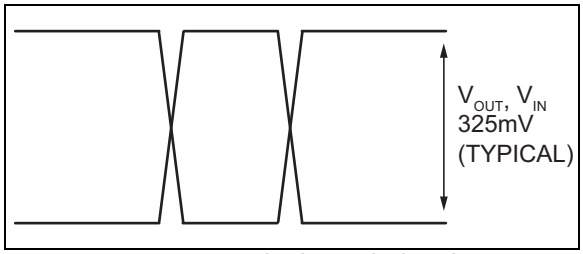


FIGURE 5-3: *Single-Ended Swing.*

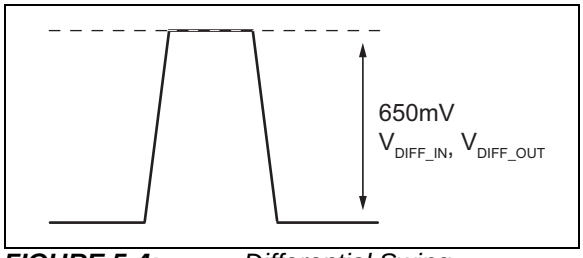


FIGURE 5-4: *Differential Swing.*

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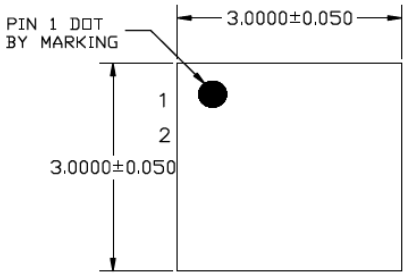
6.0 PACKAGING INFORMATION

16-Lead QFN 3 mm x 3 mm Package Outline

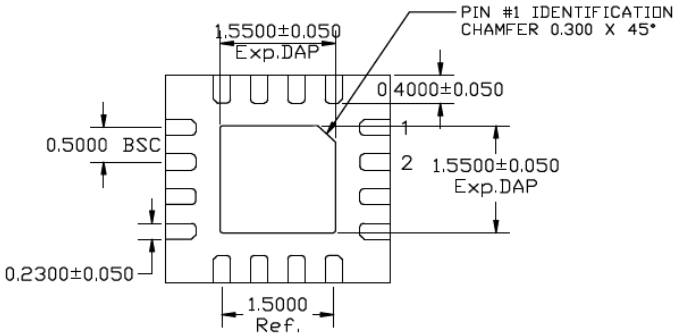
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TITLE
16 LEAD QFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

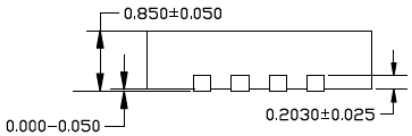
DRAWING #	QFN33-16LD-PL-1	UNIT	MM



TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



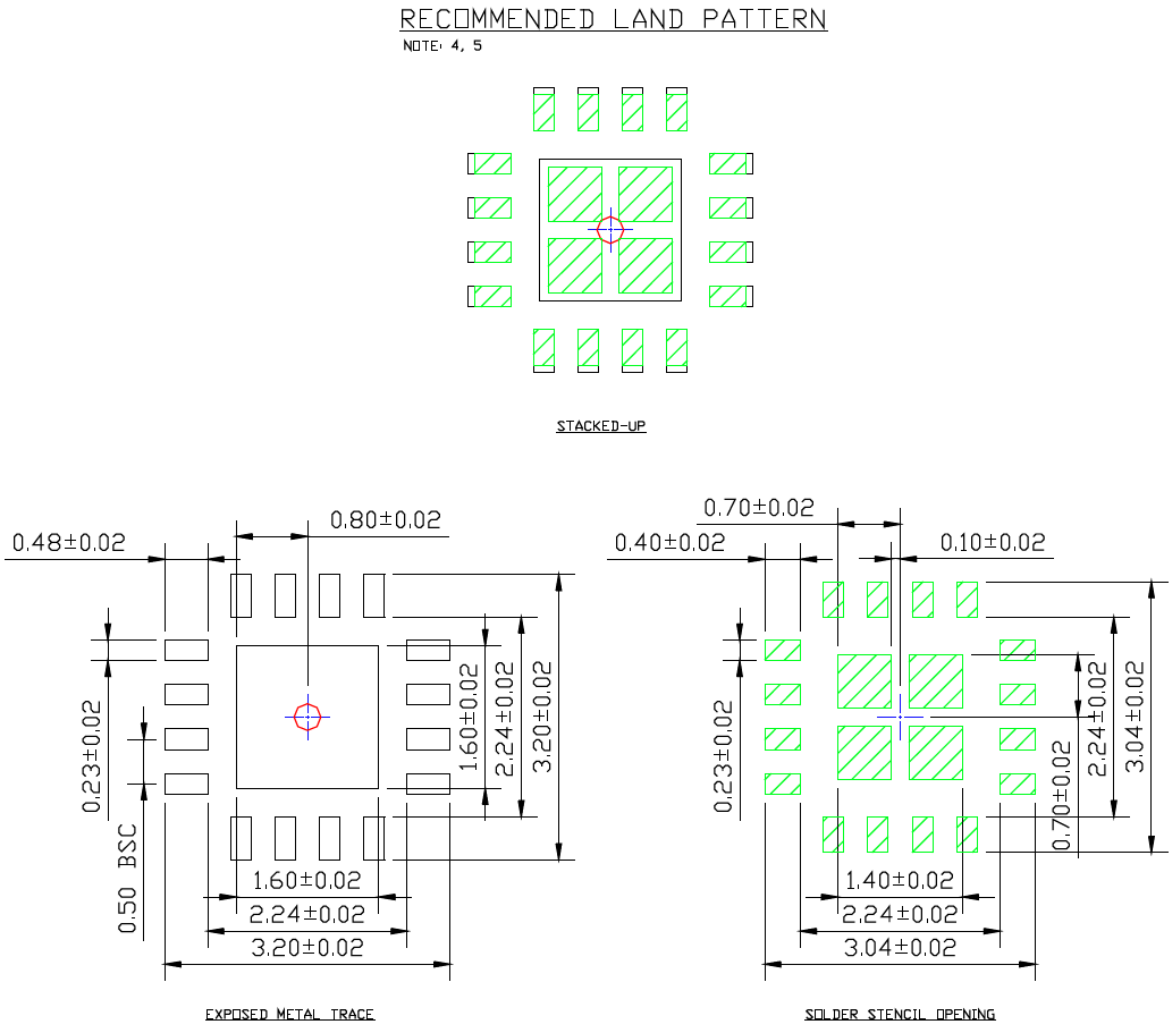
SIDE VIEW
NOTE: 1, 2, 3

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076 MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60 MM IN SIZE, 0.20 MM SPACING.

16-Lead QFN 3 mm x 3 mm Recommended Land Pattern

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

POD-Land Pattern drawing # QFN33-16LD-PL-1



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APPENDIX A: REVISION HISTORY

Revision A (January 2018)

- Converted Micrel document SY89833AL to Microchip data sheet DS20005608A.
- Minor text changes throughout.
- Updated Figure 2-6.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	—	XX
Device	Voltage Option	Package	Temperature		Special Processing

Device:	SY89833A:	3.3V Low-Noise, Ultra-Precision 1:4 LVDS Fanout Buffer/Translator with Internal Termination
Voltage Option:	L =	3.3V Only
Package:	M =	16-Pin 3 mm x 3 mm QFN
Temperature:	G =	–40°C to +85°C
Special Processing:	Blank =	Bulk, 100 pcs.
	TR =	Tape and Reel, 1000/Reel

Note 1: Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.

Examples:

a) SY89833ALMG: 3.3V Low-Noise, Ultra-Precision 1:4 LVDS Fanout Buffer/Translator with Internal Termination, 3.3V Voltage Option, –40°C to +85°C Temp. Range, 16-Pin QFN, 100 pcs.

b) SY89833ALMG-TR: 3.3V Low-Noise, Ultra-Precision 1:4 LVDS Fanout Buffer/Translator with Internal Termination, 3.3V Voltage Option, –40°C to +85°C Temp. Range, 16-Pin QFN, 1000/Reel

NOTES:

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Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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ISBN: 978-1-5224-2597-7

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