3.3V/5V DUAL LVTTL/LVCMOS-to-DIFFERENTIAL LVPECL TRANSLATOR

Precision Edge® SY89322V

FEATURES

- **3.3V and 5V power supply option**
- **300ps typical propagation delay**
- **Differential LVPECL outputs**
- **PNP LVTTL inputs for minimal loading**
- **Flow-through pinouts**
- **Q outputs will default HIGH with inputs open**
- **Max. frequency range 800MHz**
- **Available in ultra-small 8-pin MLF® (2mm x 2mm) package**

Precision Edge®

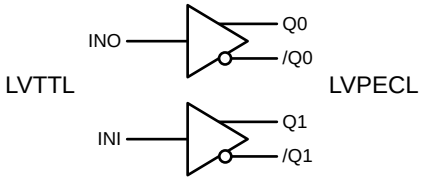
DESCRIPTION

The SY89322V is a dual TTL/CMOS-to-differential PECL translator capable of running from a 3.3V or 5V supply. This part can be used in either LVTTL/LVCMOS/LVPECL or TTL/CMOS/PECL systems.

It requires only a single positive supply of +3.3V or +5V, no negative supply is required.

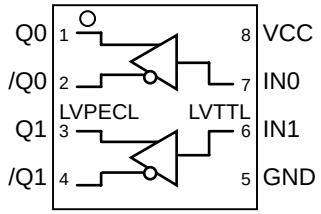
The SY89322V is functionally equivalent to the SY100EPT22V, but in an ultra-small 8-lead MLF® package that features a 70% smaller footprint. The ultra-small package and the low skew, dual gate design of the SY89322V makes it ideal for those applications where space, performance and low power are at a premium.

BLOCK DIAGRAM



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PACKAGE/ORDERING INFORMATION



8-Pin MLF®
Ultra-Small Outline (2mm × 2mm)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89322VMITR	MLF-8	Industrial	322	Sn-Pb
SY89322VMGTR(1)	MLF-8	Industrial	322 with Pb-Free bar-line indicator	Pb-Free NiPdAu

Note:

1. Pb-Free package is recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Type	Pin Function
1, 2, 3, 4	Q0, /Q0, Q1, /Q1	100k ECL Output	Differential LVPECL Outputs: Default to LOW if IN input left open. See *"Output Interface Applications"* section for recommendations on terminations.
5	GND, Exposed Pad	Ground	GND and exposed pad must be tied to ground plane.
6, 7	IN1, IN0	TTL/LVTTL Input	Single-ended TTL Inputs.
8	VCC	Power	Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitors.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +6.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Input Current
  Source or sink current on IN, /IN ..... ±50mA
Lead Temperature (soldering, 20 sec.) ..... +260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +3.0V to +3.6V
  ..... +4.5V to +5.5V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[3]
MLF® (θ_{JA})
  Still-Air ..... 93°C/W
  500lfpm ..... 87°C/W
MLF® (Ψ_{JB})
  Junction-to-Board ..... 60°C/W

DC ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage		3.0 4.5		3.6 5.5	V V
I_{CC}	Power Supply Current				25	mA

TTL DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±10% or +5.0V ±10%; T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7V V_{IN} = V_{CC}			20 100	µA µA
I_{IL}	Input LOW Current	V_{IN} = 0.5V			–0.2	mA
V_{IK}	Input Clamp Voltage	I_{IN} = –18mA			–1.2	V

PECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±10% or +5V ±10%; R_L = 50Ω to V_{CC}–2V; T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH		V_{CC}–1.080		V_{CC}–0.880	V
V_{OL}	Output LOW Voltage		V_{CC}–1.83		V_{CC}–1.550	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±10% or +5.0V ±10%; R_L = 50Ω to V_{CC} – 2V, T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Toggle Frequency				800	MHz
t_{PD}	Propagation Delay IN-to-Q		100		600	ps
t_{SKEW}	Within-Device Skew	**Note 4**			100	ps
	Part-to-Part Jitter	**Note 4**			500	ps
t_{Jitter}	Cycle-to-Cycle Jitter	**Note 5**			2	ps_{RMS}
	Total Jitter	**Note 6**			25	ps_{PP}
t_r, t_f	Output Rise/Fall Time (20% to 80%)		200		500	ps

Notes:

4. Same transition at common V_{CC} levels.

5. Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles, $T_n - T_{n-1}$,where T is the time between rising edges of the output signal.

6. Total jitter definition: with an ideal clock input of frequency ≤ f_{MAX}, no more than one output edge in 10^{12} output edge will deviate by more than the specified peak-to-peak jitter value.

LVPECL OUTPUT INTERFACE APPLICATIONS

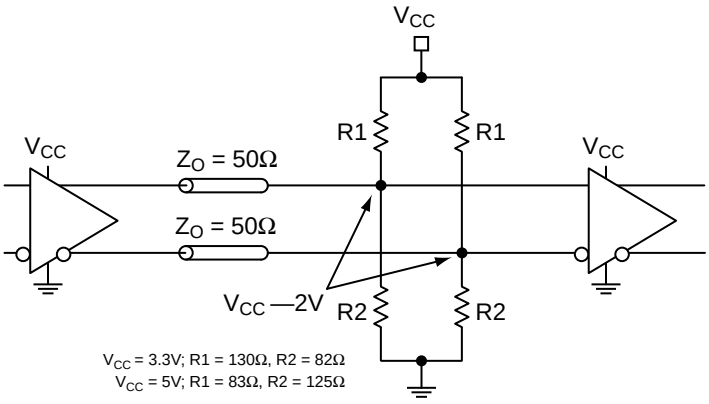


Figure 1a. Parallel Thevenin-Equivalent Termination

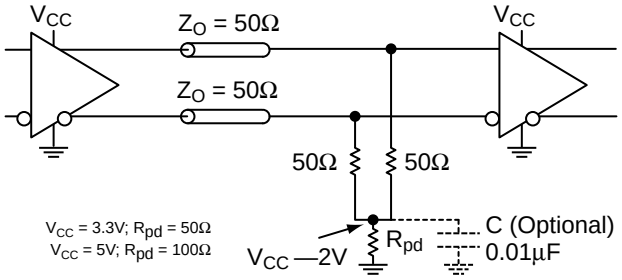


Figure 1b. Three Resistor "Y Termination"

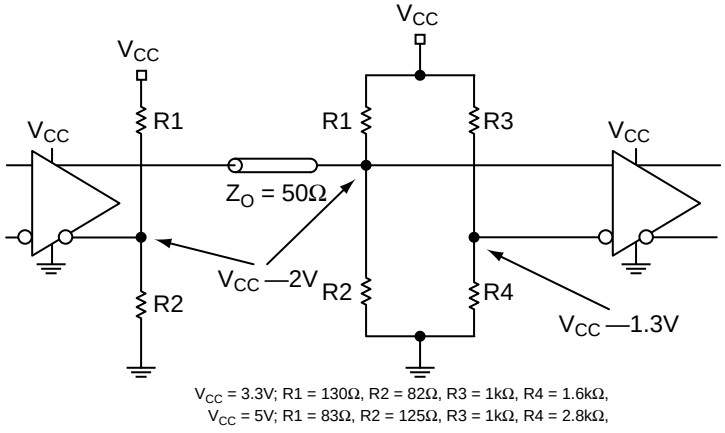
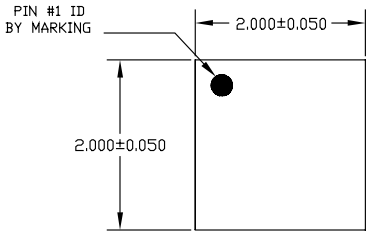
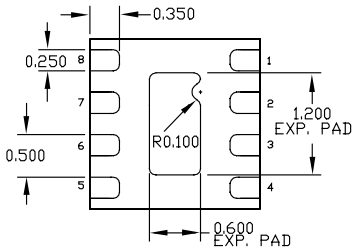


Figure 1c. Terminating Unused I/O

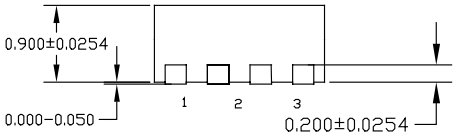
8-PIN ULTRA-SMALL EPAD-*Micro*LeadFrame® (MLF-8)



TOP VIEW

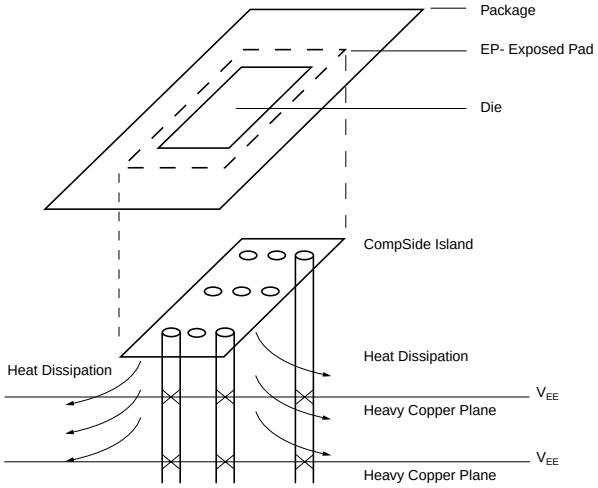


BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 8-Pin MLF® Package

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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