

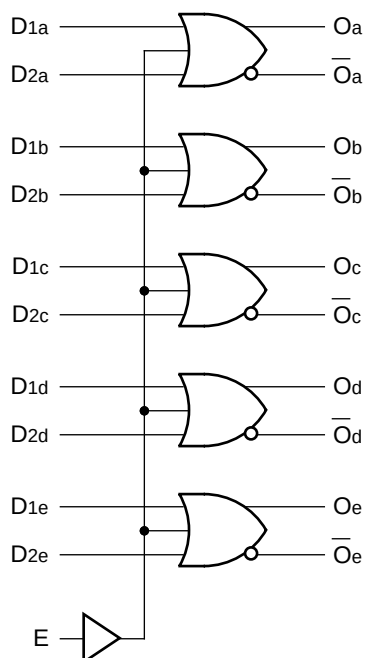
### FEATURES

- Max. propagation delay of 700ps
- IEE min. of -45mA
- Industry standard 100K ECL levels
- Extended supply voltage option:  
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75kΩ input pull-down resistors
- 50% faster than Fairchild 300K
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

### DESCRIPTION

The SY100S302 offers five 2-input OR/NOR gates designed for use in high-performance ECL systems. The five gates are controlled by a common Enable signal. All inputs have 75kΩ pull-down resistors and all outputs are buffered.

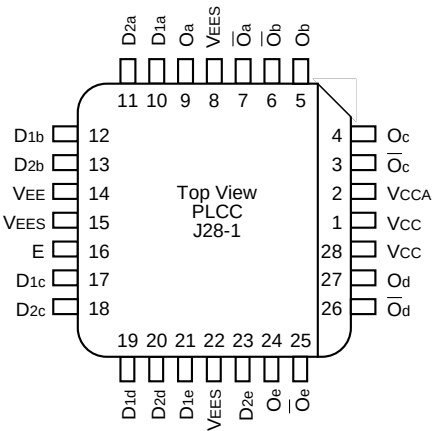
### BLOCK DIAGRAM



### PIN NAMES

| Pin                             | Function                   |
|---------------------------------|----------------------------|
| Dna – Dne                       | Data Inputs (n-1...5)      |
| E                               | Enable Input               |
| Oa – Oe                         | Data Outputs               |
| $\overline{Oa} - \overline{Oe}$ | Complementary Data Outputs |
| VEES                            | VEE Substrate              |
| VCCA                            | Vcco for ECL Outputs       |

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information

| Part Number                     | Package Type | Operating Range | Package Marking                             | Lead Finish |
|---------------------------------|--------------|-----------------|---------------------------------------------|-------------|
| SY100S302JC                     | J28-1        | Commercial      | SY100S302JC                                 | Sn-Pb       |
| SY100S302JCTR <sup>(1)</sup>    | J28-1        | Commercial      | SY100S302JC                                 | Sn-Pb       |
| SY100S302JZ <sup>(2)</sup>      | J28-1        | Commercial      | SY100S302JZ with Pb-Free bar-line indicator | Matte-Sn    |
| SY100S302JZTR <sup>(1, 2)</sup> | J28-1        | Commercial      | SY100S302JZ with Pb-Free bar-line indicator | Matte-Sn    |

- Notes:
1. Tape and Reel.
  2. Pb-Free package is recommended for new designs.

TRUTH TABLE<sup>(1)</sup>

| D1X | D2X | E | OX | $\overline{OX}$ |
|-----|-----|---|----|-----------------|
| L   | L   | L | L  | H               |
| L   | L   | H | H  | L               |
| L   | H   | L | H  | L               |
| L   | H   | H | H  | L               |
| H   | L   | L | H  | L               |
| H   | L   | H | H  | L               |
| H   | H   | L | H  | L               |
| H   | H   | H | H  | L               |

- Note:
1. H = High Voltage Level  
L = Low Voltage Level

## DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

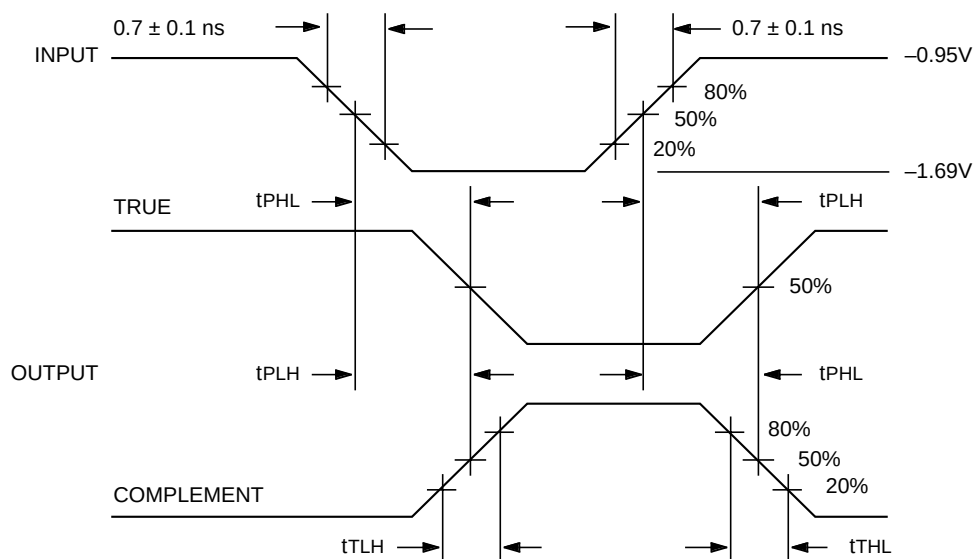
| Symbol   | Parameter                      | Min. | Typ. | Max. | Unit    | Condition                |
|----------|--------------------------------|------|------|------|---------|--------------------------|
| $I_{IH}$ | Input HIGH Current, All Inputs | —    | —    | 200  | $\mu A$ | $V_{IN} = V_{IH} (Max.)$ |
| $I_{EE}$ | Power Supply Current           | -45  | -28  | -21  | mA      | Inputs Open              |

## AC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

| Symbol                 | Parameter                                 | $T_A = 0^\circ C$ |      | $T_A = +25^\circ C$ |      | $T_A = +85^\circ C$ |      | Unit | Condition |
|------------------------|-------------------------------------------|-------------------|------|---------------------|------|---------------------|------|------|-----------|
|                        |                                           | Min.              | Max. | Min.                | Max. | Min.                | Max. |      |           |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>Data to Output       | 250               | 700  | 250                 | 700  | 250                 | 700  | ps   |           |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>Enable to Output     | 250               | 900  | 250                 | 900  | 250                 | 900  | ps   |           |
| $t_{TLH}$<br>$t_{THL}$ | Transition Time<br>20% to 80%, 80% to 20% | 300               | 900  | 300                 | 900  | 300                 | 900  | ps   |           |

## TIMING DIAGRAM

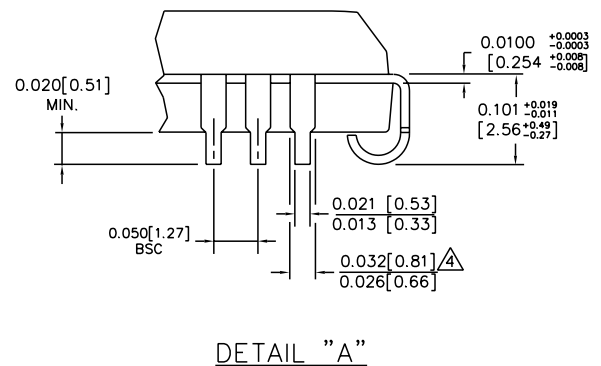
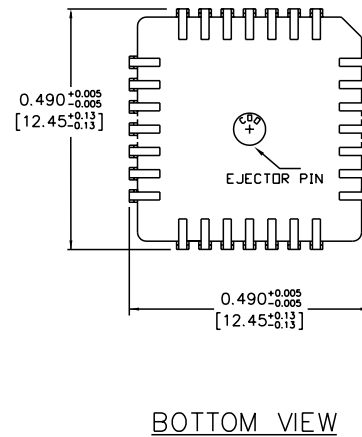
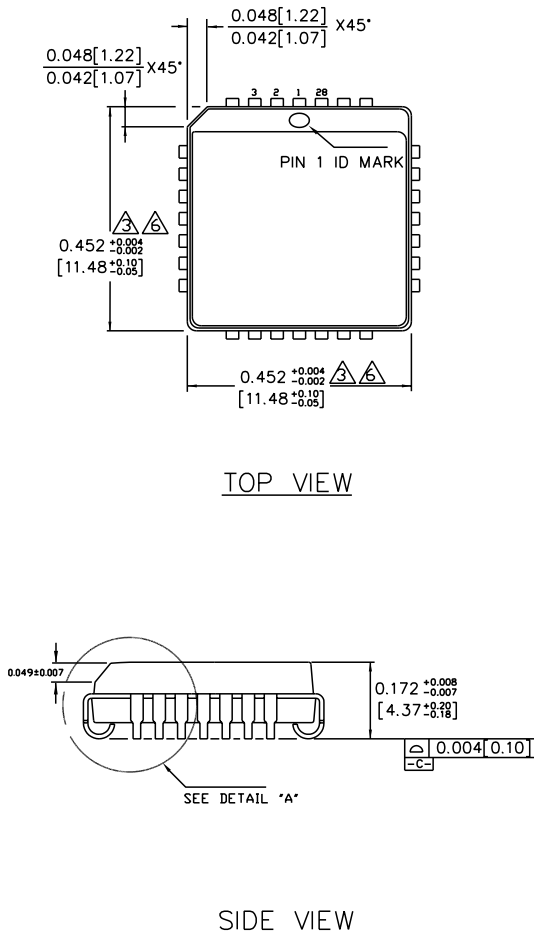


Propagation Delay and Transition Times

**Note:**

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

## 28-PIN PLCC (J28-1)



## NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. A

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