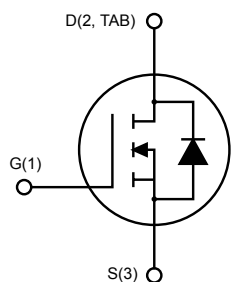
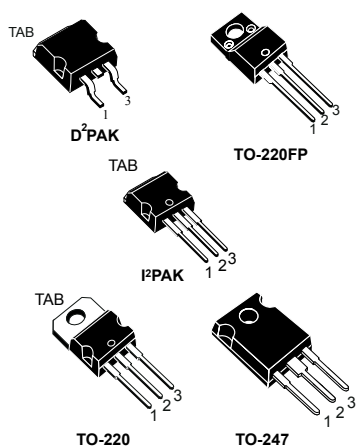


N-channel 650 V, 70 mΩ typ., 33 A, MDmesh M5 Power MOSFETs in D²PAK, TO-220FP, I²PAK, TO-220 and TO-247 packages



AM01475v1_noZen



Features

Order codes	V _{DS} @ T _{Jmax}	R _{DS(on)} max.	I _D	Package
STB42N65M5	710 V	79 mΩ	33 A	D ² PAK
STF42N65M5				TO-220FP
STI42N65M5				I ² PAK
STP42N65M5				TO-220
STW42N65M5				TO-247

- Extremely low R_{DS(on)}
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting products offer extremely low on-resistance, making them particularly suitable for applications requiring high power and superior efficiency.

Product status

STB42N65M5
STF42N65M5
STI42N65M5
STP42N65M5
STW42N65M5

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK, I ² PAK, TO-220, TO-247	TO-220FP	
V _{GS}	Gate-source voltage	±25		V
I _D	Drain current (continuous) at T _C = 25 °C	33	33 ⁽¹⁾	A
	Drain current (continuous) at T _C = 100 °C	20.8	20.8 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	132	132	A
P _{TOT}	Total power dissipation at T _C = 25 °C	190	40	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)		2500	V
T _J	Operating junction temperature range	-55 to 150		°C
T _{stg}	Storage temperature range			

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. I_{SD} ≤ 33 A, di/dt ≤ 400 A/μs, V_{DD} = 400 V, V_{DS(peak)} < V_{(BR)DSS}.

Table 2. Thermal data

Symbol	Parameter	Value					Unit
		D ² PAK	I ² PAK	TO-220	TO-247	TO-220FP	
R _{thj-case}	Thermal resistance junction-case	0.66				3.1	°C/W
R _{thj-amb}	Thermal resistance junction-ambient		62.5		50	62.5	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb	30					°C/W

1. When mounted on an 1 inch² FR-4, 2 Oz copper board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T _{Jmax})	11	A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	950	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	650			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 650 V			1	μA
		V _{GS} = 0 V, V _{DS} = 650 V, T _C = 125 °C ⁽¹⁾			100	μA
I _{GSS}	Gate body leakage current	V _{GS} = ±25 V, V _{DS} = 0 V			100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	3	4	5	V
R _{DS(on)}	Static drain-source on- resistance	V _{GS} = 10 V, I _D = 16.5 A		70	79	mΩ

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V	-	4650	-	pF
C _{oss}	Output capacitance			110		
C _{rss}	Reverse transfer capacitance			3.2		
C _{o(tr)} ⁽¹⁾	Equivalent capacitance time related	V _{DS} = 0 to 520 V, V _{GS} = 0 V	-	100	-	pF
C _{o(er)} ⁽²⁾	Equivalent capacitance energy related			285		
R _g	Gate input resistance	f = 1 MHz, I _D = 0 A	-	1.1	-	Ω
Q _g	Total gate charge	V _{DD} = 520 V, I _D = 33 A,	-	98	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 0 to 10 V		28		
Q _{gd}	Gate-drain charge	(see Figure 20. Test circuit for gate charge behavior)		39		

1. C_{o(tr)} is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

2. C_{o(er)} is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(v)}	Voltage delay time	V _{DD} = 400 V, I _D = 20 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 21. Test circuit for inductive load switching and diode recovery times and Figure 24. Switching time waveform)	-	52	-	ns
t _{r(v)}	Voltage rise time			8.4		
t _{f(i)}	Current fall time			8.7		
t _{c(off)}	Crossing time			14		

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		33	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				132	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 33\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 33\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see Figure 21. Test circuit for inductive load switching and diode recovery times)	-	400		ns
Q_{rr}	Reverse recovery charge			7		μC
I_{RRM}	Reverse recovery current			35		A
t_{rr}	Reverse recovery time	$I_{SD} = 33\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 21. Test circuit for inductive load switching and diode recovery times)	-	532		ns
Q_{rr}	Reverse recovery charge			10		μC
I_{RRM}	Reverse recovery current			38		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

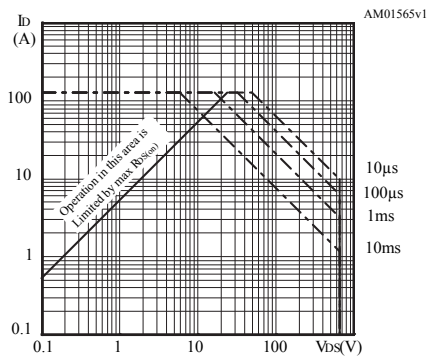
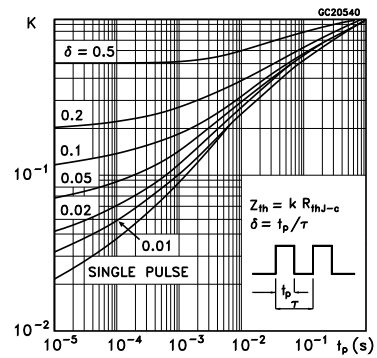
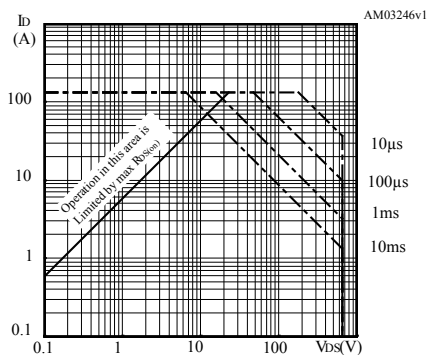
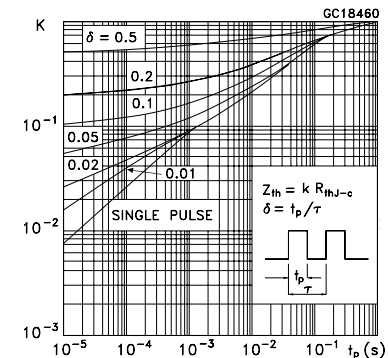
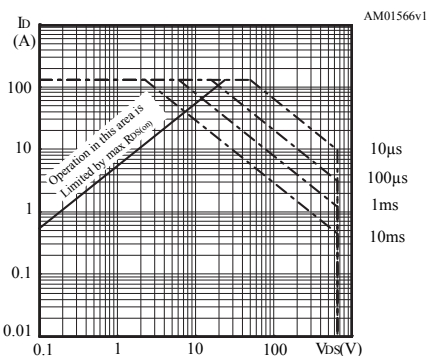
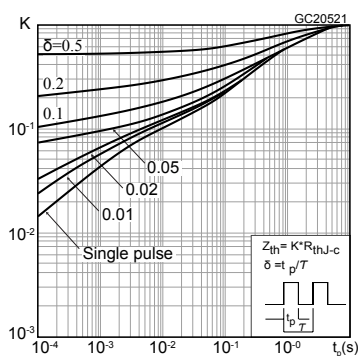
Figure 1. Safe operating area for D²PAK, I²PAK, TO-220

Figure 2. Thermal impedance for D²PAK, I²PAK, TO-220

Figure 3. Safe operating area for TO-247

Figure 4. Thermal impedance for TO-247

Figure 5. Safe operating area for TO-220FP

Figure 6. Thermal impedance for TO-220FP


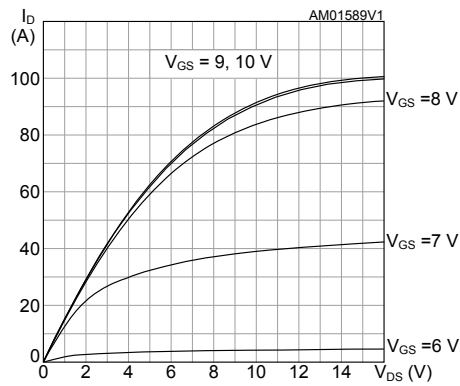
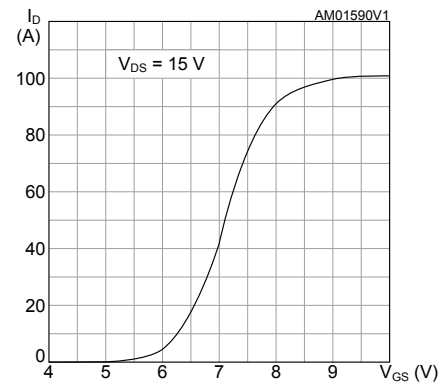
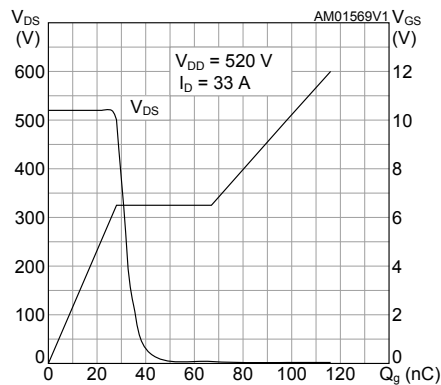
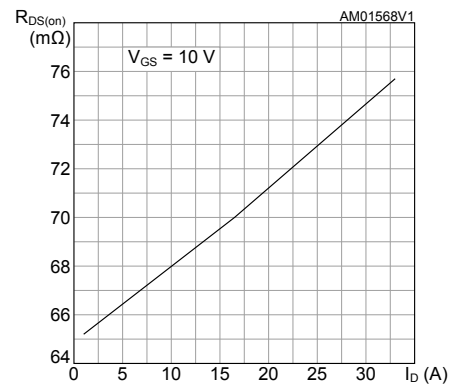
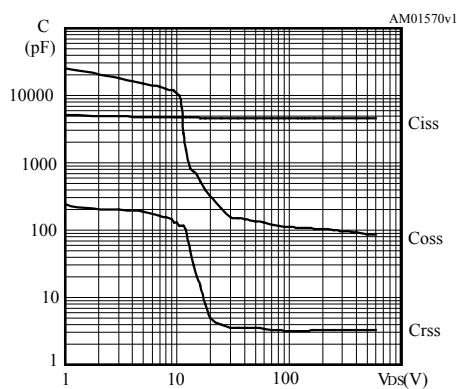
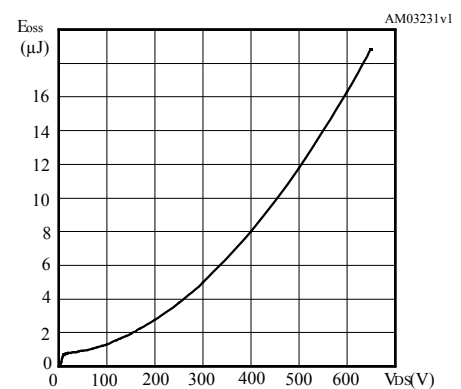
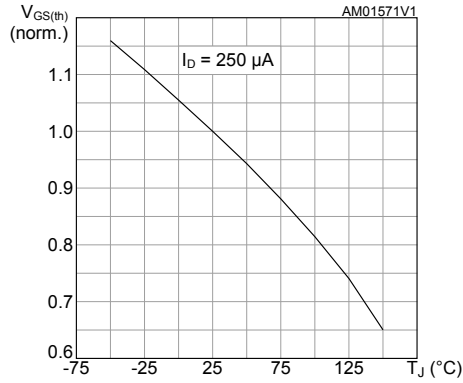
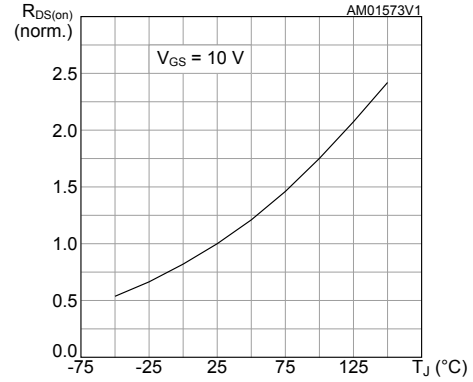
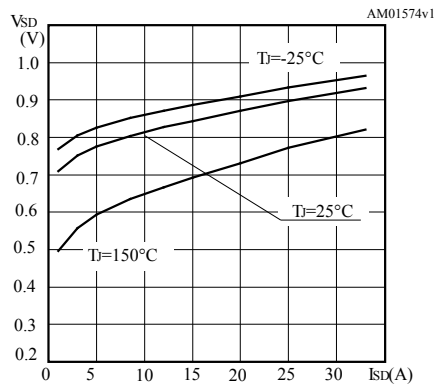
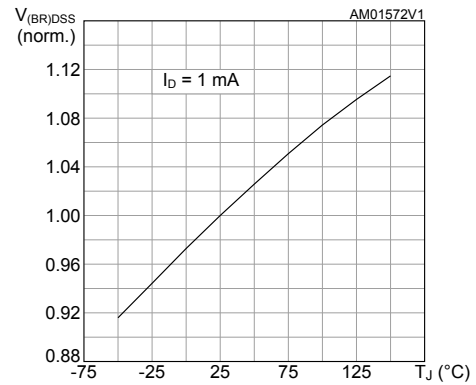
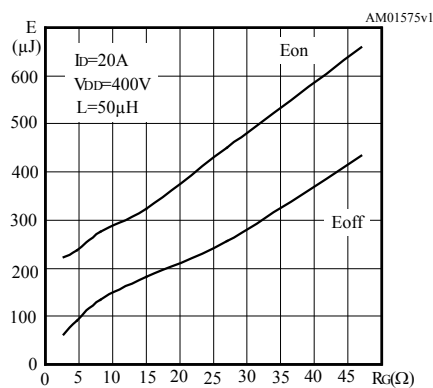
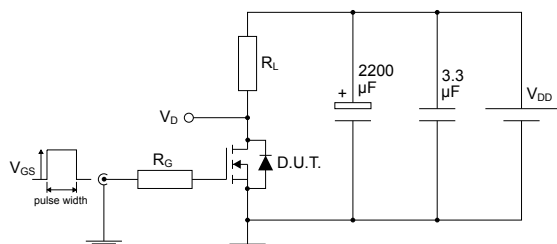
Figure 7. Output characteristics

Figure 8. Transfer characteristics

Figure 9. Gate charge vs gate-source voltage

Figure 10. Static drain-source on-resistance

Figure 11. Capacitance variations

Figure 12. Output capacitance stored energy


Figure 13. Normalized gate threshold voltage vs temperature

Figure 14. Normalized on-resistance vs temperature

Figure 15. Source-drain diode forward characteristics

Figure 16. Normalized $V_{(BR)DSS}$ vs temperature

Figure 17. Switching energy vs gate resistance


Note: E_{on} including reverse recovery of a SiC diode.

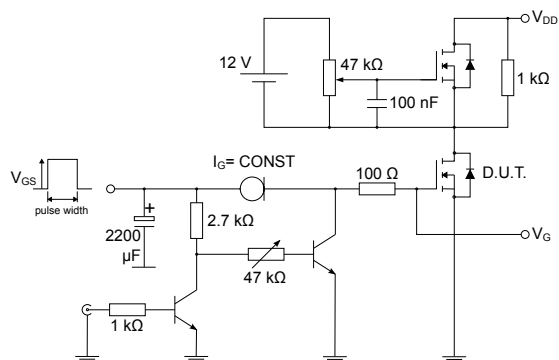
3 Test circuits

Figure 19. Test circuit for resistive load switching times



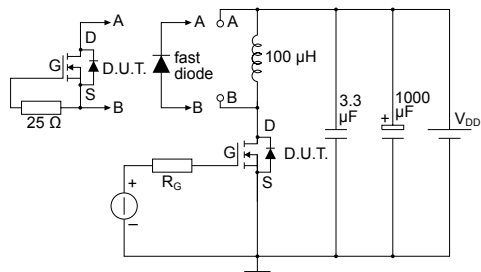
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Figure 20. Test circuit for gate charge behavior



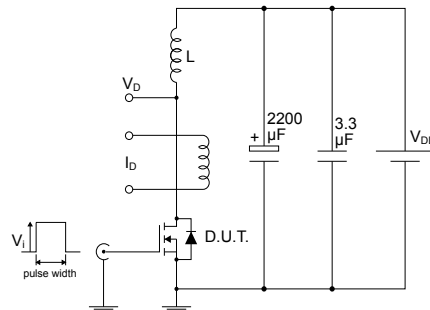
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Figure 21. Test circuit for inductive load switching and diode recovery times



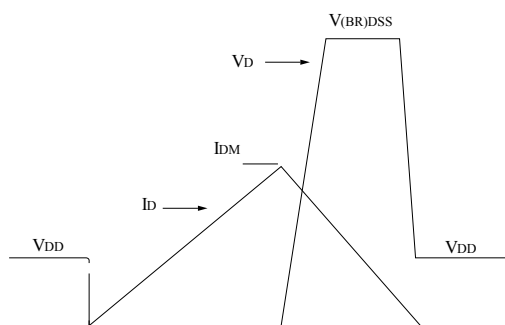
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Figure 22. Unclamped inductive load test circuit



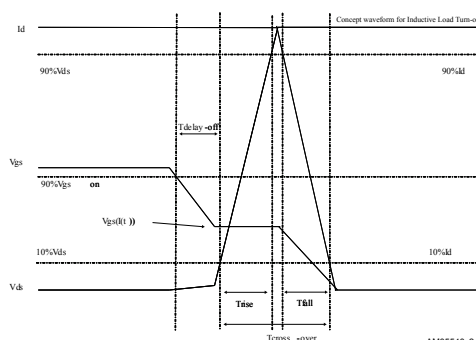
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Figure 23. Unclamped inductive waveform



AM01472v1

Figure 24. Switching time waveform



AM05540v2

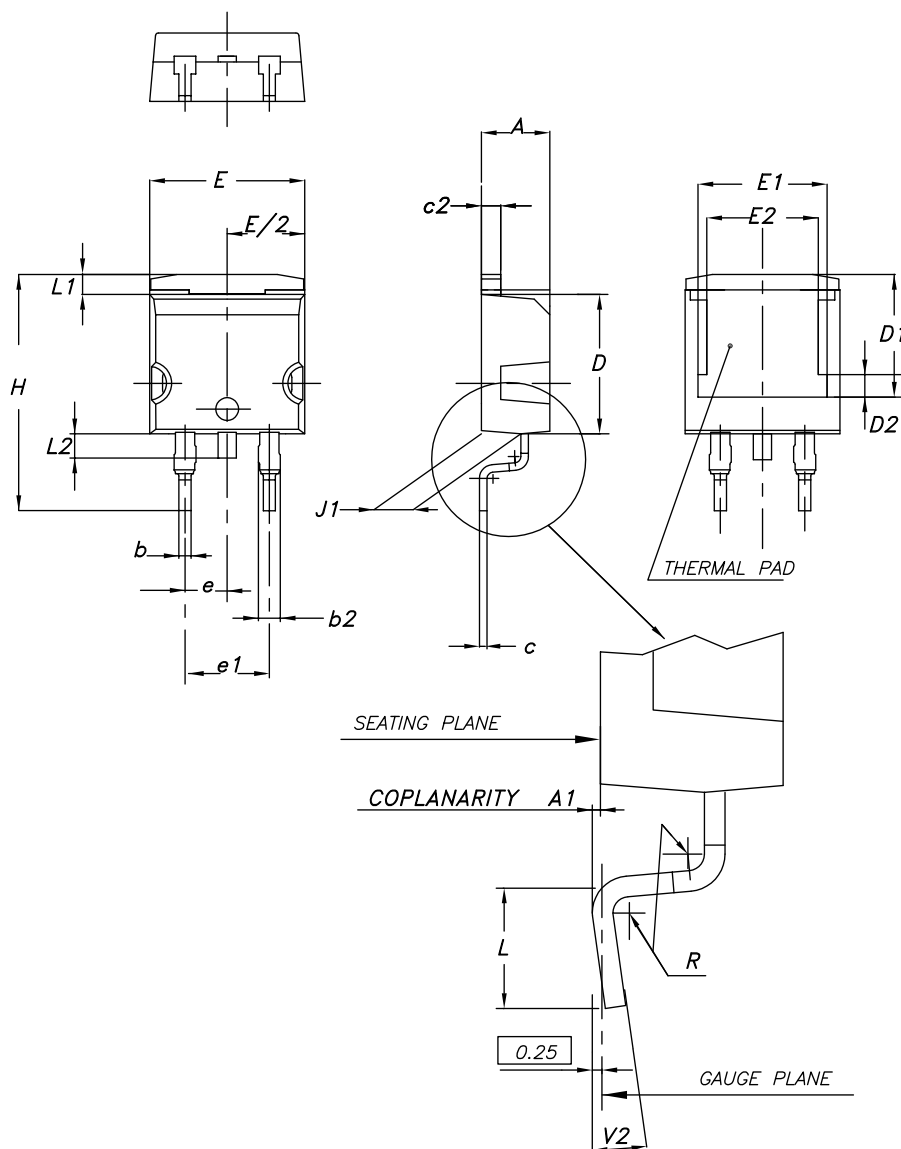


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A2 package information

Figure 25. D²PAK (TO-263) type A2 package outline

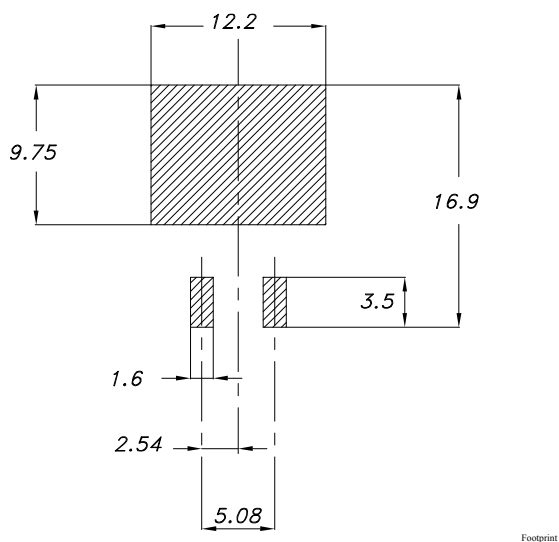


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Table 8. D²PAK (TO-263) type A2 package mechanical data

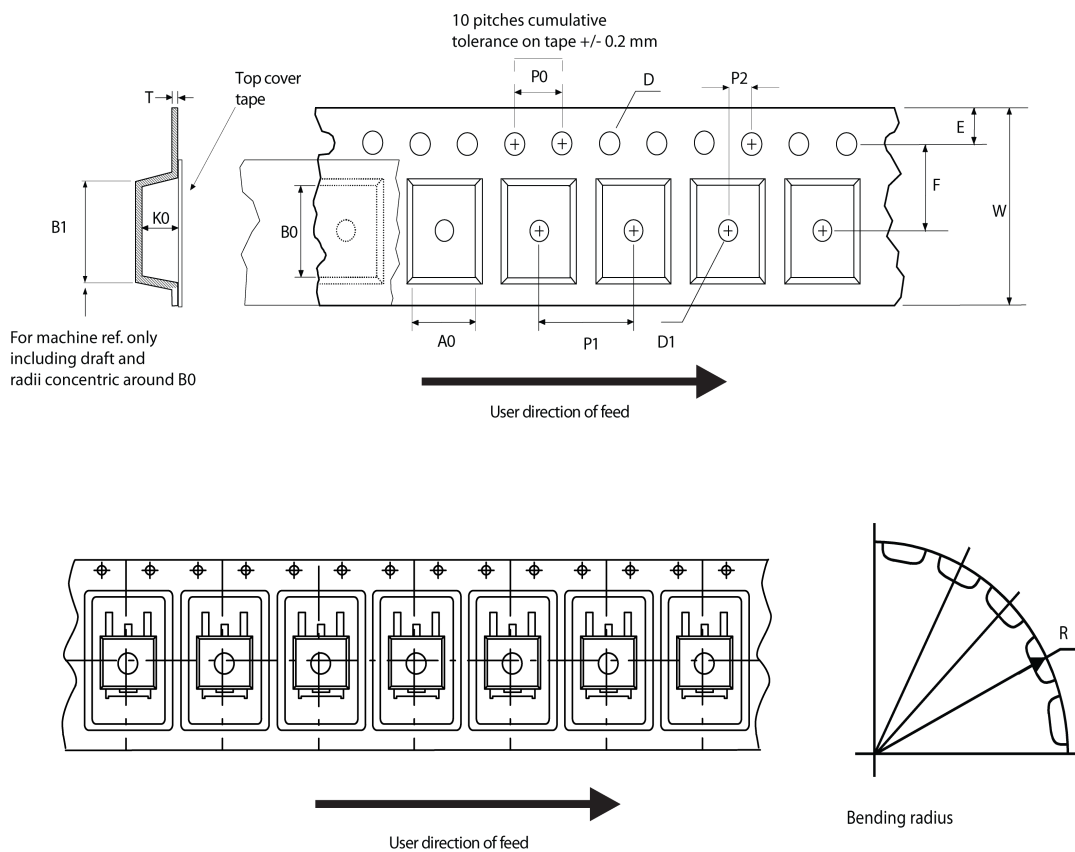
Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.70	8.90	9.10
E2	7.30	7.50	7.70
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 26. D²PAK (TO-263) recommended footprint (dimensions are in mm)

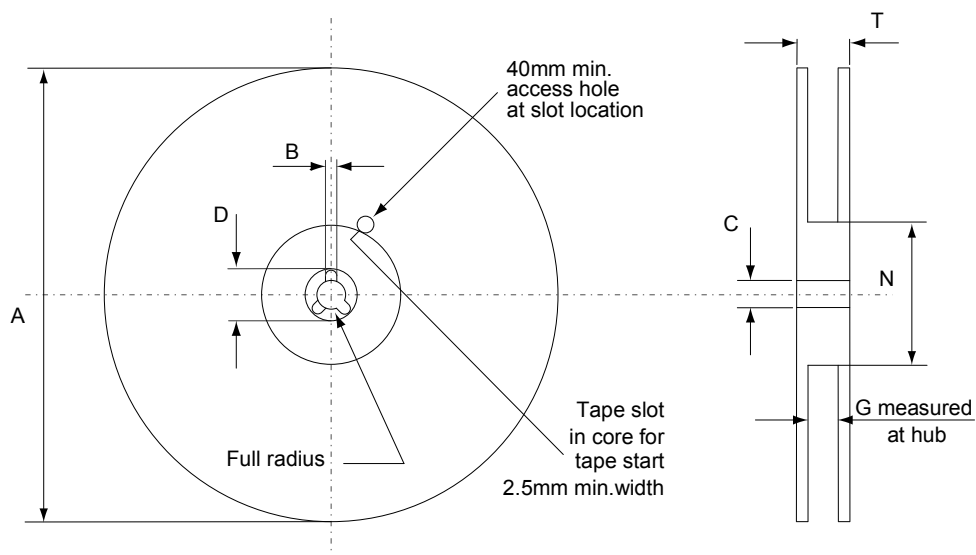


4.2 D²PAK packing information

Figure 27. D²PAK tape outline



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Figure 28. D²PAK reel outline


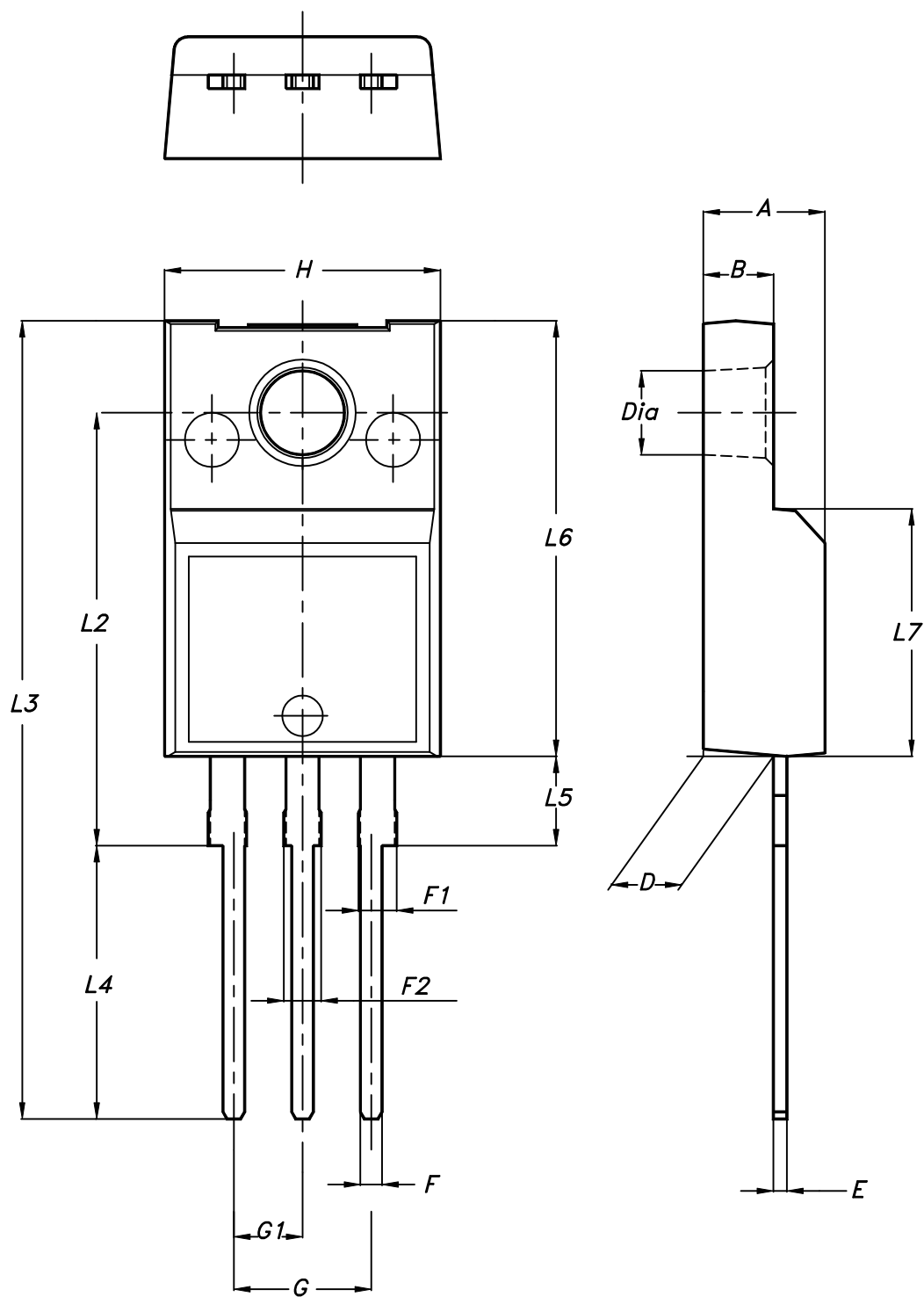
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Table 9. D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

4.3 TO-220FP package information

Figure 29. TO-220FP package outline



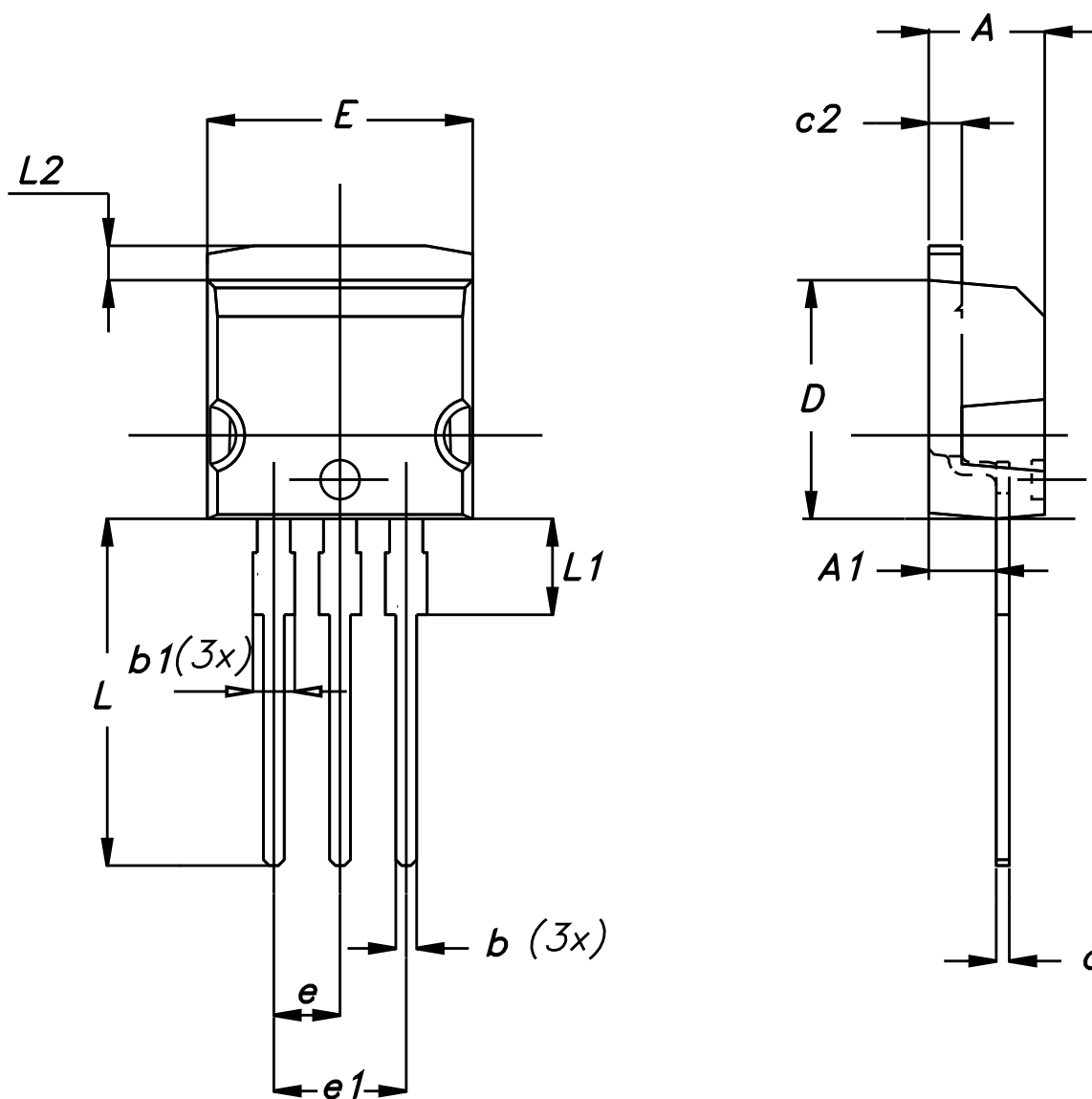
7012510_Rev_12_B

Table 10. TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.4 I²PAK package information

Figure 30. I²PAK package outline



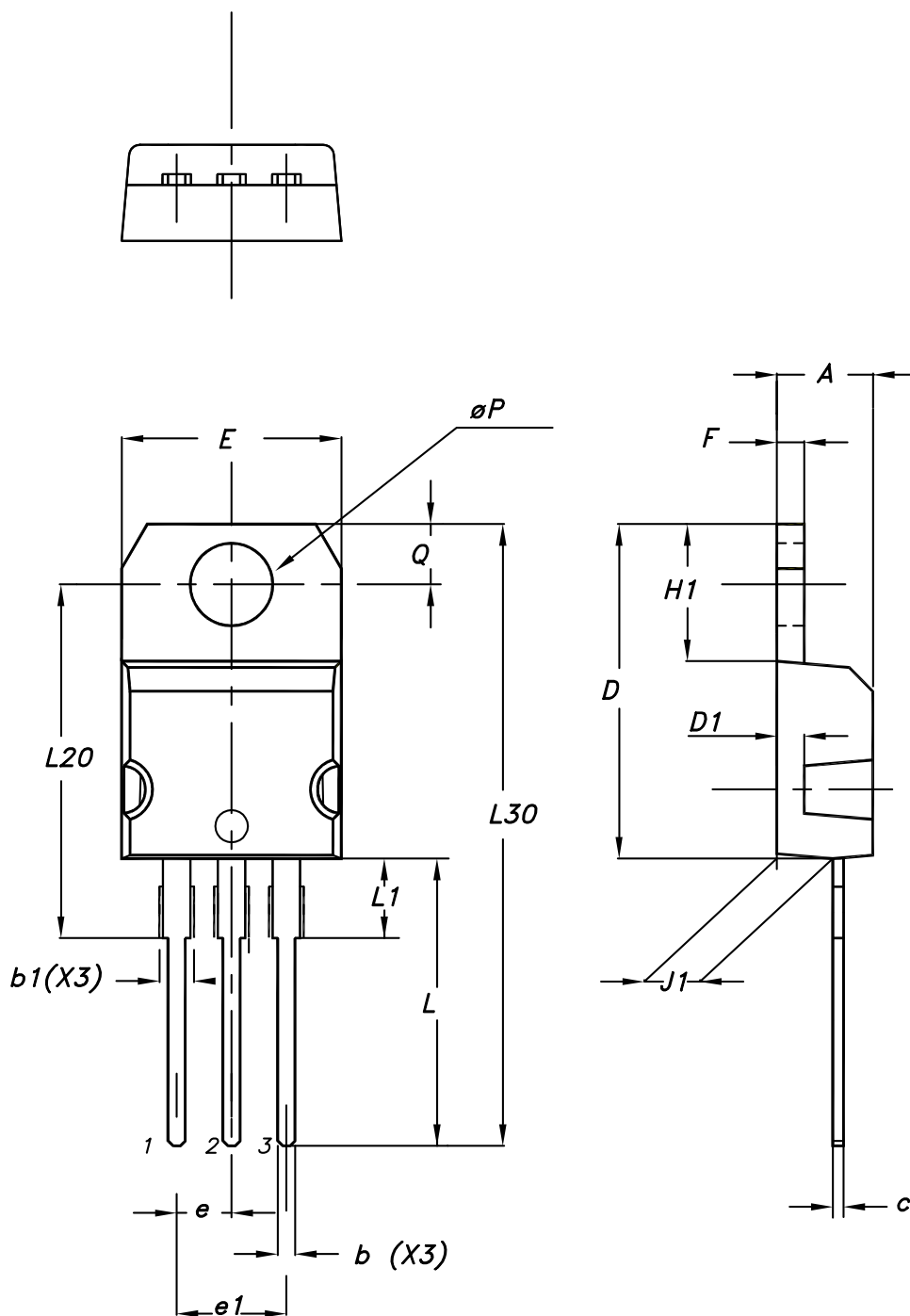
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Table 11. I²PAK package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
A1	2.40	-	2.72
b	0.61	-	0.88
b1	1.14	-	1.70
c	0.49	-	0.70
c2	1.23	-	1.32
D	8.95	-	9.35
e	2.40	-	2.70
e1	4.95	-	5.15
E	10	-	10.40
L	13	-	14
L1	3.50	-	3.93
L2	1.27	-	1.40

4.5 TO-220 type A package information

Figure 31. TO-220 type A package outline



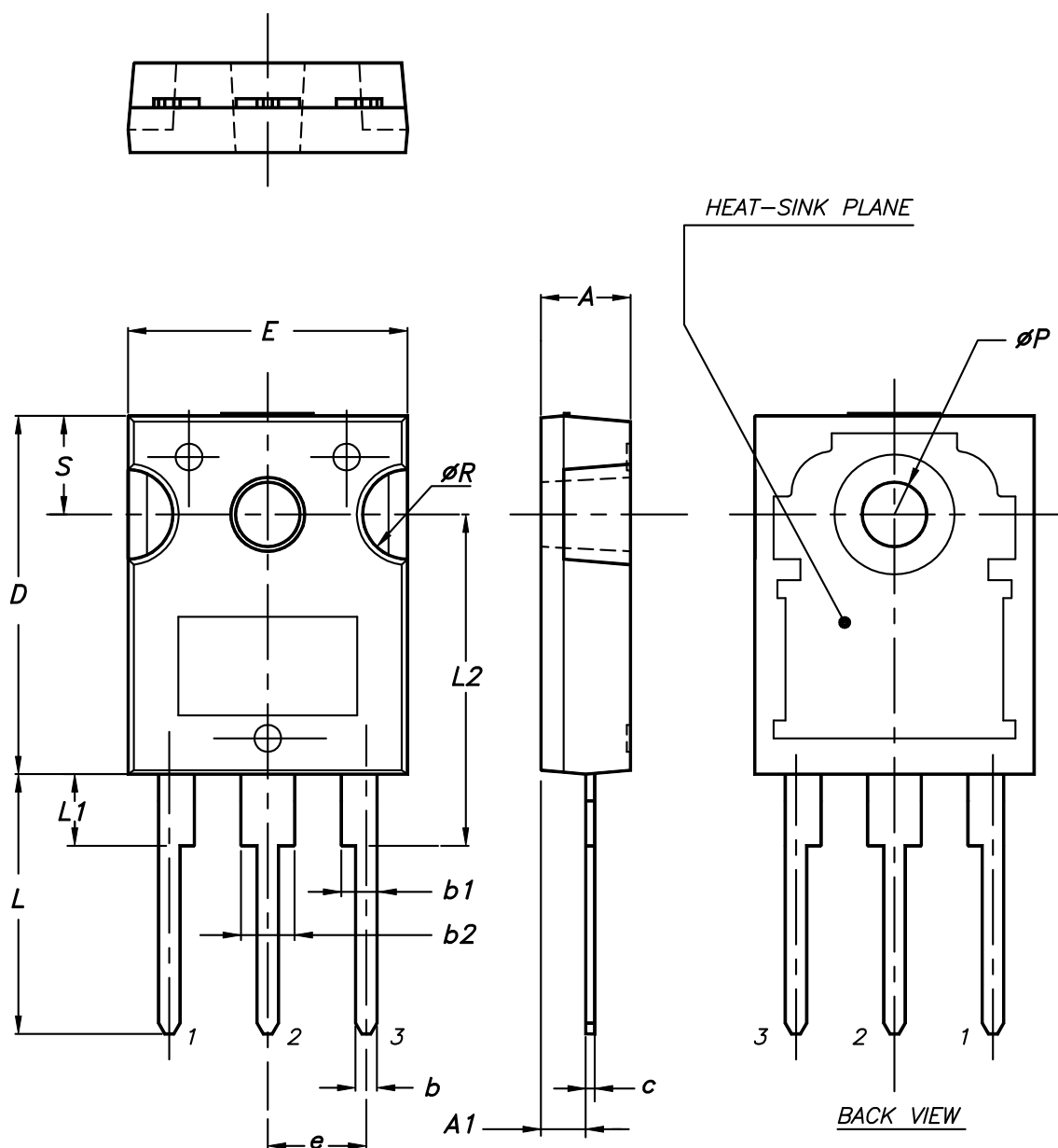
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Table 12. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.6 TO-247 package information

Figure 32. TO-247 package outline



0075325_9

Table 13. TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70



5 Ordering information

Table 14. Order codes

Order code	Marking	Package	Packing
STB42N65M5	42N65M5	D ² PAK	Tape and reel
STF42N65M5		TO-220FP	Tube
STI42N65M5		I ² PAK	
STP42N65M5		TO-220	
STW42N65M5		TO-247	

Revision history

Table 15. Document revision history

Date	Version	Changes
16-Jan-2009	1	First release.
15-May-2009	2	Updated <i>figures 9, 10, 11</i> and <i>17</i>
12-Jun-2009	3	<i>Figure 15</i> has been updated
02-May-2019	4	Modified features and description on cover page. Updated Section 4 Package information . Minor text changes.

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