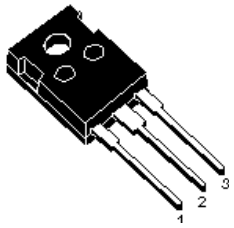
# STW8NC80Z

## N-CHANNEL 800V - 1.3 Ω - 6.7A TO-247
## Zener-Protected PowerMESH™III MOSFET

| TYPE | $V_{DSS}$ | $R_{DS(on)}$ | $I_D$ |
|---|---|---|---|
| STW8NC80Z | 800 V | < 1.5 Ω | 6.7 A |

- TYPICAL $R_{DS}(on)$ = 1.3 Ω
- EXTREMELY HIGH dv/dt CAPABILITY GATE-TO-SOURCE ZENER DIODES
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED




**TO-247**

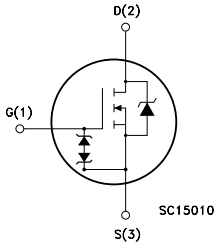
### DESCRIPTION

The third generation of MESH OVERLAY™ Power MOSFETs for very high voltage exhibits unsurpassed on-resistance per unit area while integrating back-to-back Zener diodes between gate and source. Such arrangement gives extra ESD capability with higher ruggedness performance as requested by a large variety of single-switch applications.

### APPLICATIONS

- SINGLE-ENDED SMPS IN MONITORS, COMPUTER AND INDUSTRIAL APPLICATION
- WELDING EQUIPMENT

**INTERNAL SCHEMATIC DIAGRAM**




### ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source Voltage ($V_{GS}$ = 0) | 800 | V |
| $V_{DGR}$ | Drain-gate Voltage ($R_{GS}$ = 20 kΩ) | 800 | V |
| $V_{GS}$ | Gate- source Voltage | ±25 | V |
| $I_D$ | Drain Current (continuos) at $T_C$ = 25°C | 6.7 | A |
| $I_D$ | Drain Current (continuos) at $T_C$ = 100°C | 4.2 | A |
| $I_{DM}$ (•) | Drain Current (pulsed) | 27 | A |
| $P_{TOT}$ | Total Dissipation at $T_C$ = 25°C | 160 | W |
| | Derating Factor | 1.28 | W/°C |
| $I_{GS}$ | Gate-source Current | ±50 | mA |
| $V_{ESD(G-S)}$ | Gate source ESD(HBM-C=100pF, R=15KΩ) | 3 | KV |
| dv/dt (1) | Peak Diode Recovery voltage slope | 3 | V/ns |
| $T_{stg}$ | Storage Temperature | –65 to 150 | °C |
| $T_j$ | Max. Operating Junction Temperature | 150 | °C |

(•)Pulse width limited by safe operating area

(1)$I_{SD}$ ≤6.7A, di/dt ≤100A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX.}$

## THERMAL DATA

| | | | |
|---|---|---|---|
| Rthj-case | Thermal Resistance Junction-case Max | 0.78 | °C/W |
| Rthj-amb | Thermal Resistance Junction-ambient Max | 30 | °C/W |
| $T_l$ | Maximum Lead Temperature For Soldering Purpose | 300 | °C |

## AVALANCHE CHARACTERISTICS

| Symbol | Parameter | Max Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max) | 6.7 | A |
| $E_{AS}$ | Single Pulse Avalanche Energy (starting $T_j$ = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V) | 275 | mJ |

## ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source Breakdown Voltage | $I_D$ = 250 µA, $V_{GS}$ = 0 | 800 | | | V |
| $\Delta BV_{DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | $I_D$ = 1 mA, $V_{GS}$ = 0 | | 0.9 | | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current ($V_{GS}$ = 0) | $V_{DS}$ = Max Rating | | | 1 | µA |
| | | $V_{DS}$ = Max Rating, $T_C$ = 125 °C | | | 50 | µA |
| $I_{GSS}$ | Gate-body Leakage Current ($V_{DS}$ = 0) | $V_{GS}$ = ±20V | | | ±10 | µA |

ON (1)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static Drain-source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 3.3 A | | 1.3 | 1.5 | Ω |

DYNAMIC

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (1) | Forward Transconductance | $V_{DS}$ > $I_{D(on)}$ x $R_{DS(on)max}$, $I_D$ =3.3 A | | 6 | | S |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25V, f = 1 MHz, $V_{GS}$ = 0 | | 2350 | | pF |
| $C_{oss}$ | Output Capacitance | | | 164 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 17 | | pF |

**ELECTRICAL CHARACTERISTICS** (CONTINUED)

SWITCHING ON (RESISTIVE LOAD)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DD}$ = 400V, $I_D$ = 3A | | 33 | | ns |
| $t_r$ | Rise Time | $R_G$ = 4.7Ω $V_{GS}$ = 10V (see test circuit, Figure 3) | | 12 | | ns |
| $Q_g$ | Total Gate Charge | $V_{DD}$ = 640V, $I_D$ = 6 A, | | 43 | 58 | nC |
| $Q_{gs}$ | Gate-Source Charge | $V_{GS}$ = 10V | | 12 | | nC |
| $Q_{gd}$ | Gate-Drain Charge | | | 15 | | nC |

SWITCHING OFF (INDUCTIVE LOAD)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{r(Voff)}$ | Off-voltage Rise Time | $V_{DD}$ = 640V, $I_D$ = 6 A, | | 13 | | ns |
| $t_f$ | Fall Time | $R_G$ = 4.7Ω, $V_{GS}$ = 10V (see test circuit, Figure 5) | | 13 | | ns |
| $t_c$ | Cross-over Time | | | 20 | | ns |

SOURCE DRAIN DIODE

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain Current | | | | 6.7 | A |
| $I_{SDM}$ (2) | Source-drain Current (pulsed) | | | | 24 | A |
| $V_{SD}$ (1) | Forward On Voltage | $I_{SD}$ = 6 A, $V_{GS}$ = 0 | | | 1.6 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_{SD}$ = 6 A, di/dt = 100A/µs, | | 680 | | ns |
| $Q_{rr}$ | Reverse Recovery Charge | $V_{DD}$ = 100V, $T_j$ = 150°C (see test circuit, Figure 5) | | 6 | | µC |
| $I_{RRM}$ | Reverse Recovery Current | | | 18 | | A |

GATE-SOURCE ZENER DIODE

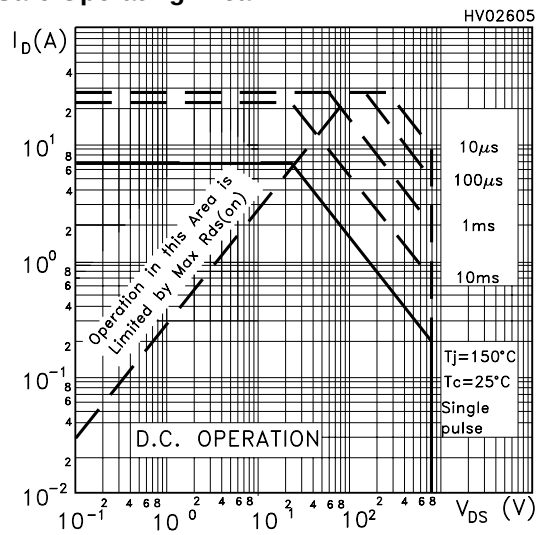
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $BV_{GSO}$ | Gate-Source Breakdown Voltage | Igs=± 1mA (Open Drain) | 25 | | | V |
| αT | Voltage Thermal Coefficient | T=25°C Note(3) | | 1.3 | | $10^{-4}$/°C |
| Rz | Dynamic Resistance | $I_D$ = 20 mA, $V_{GS}$ = 0 | | 90 | | Ω |

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.
3. $\Delta V_{BV} = \alpha T\ (25°\text{-}T)\ BV_{GSO}(25°)$

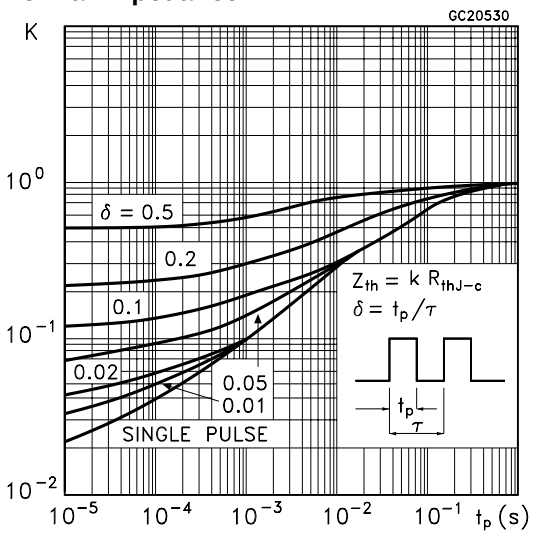
**PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES**

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to souce. In this respect the 25V Zener voltage is appropiate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

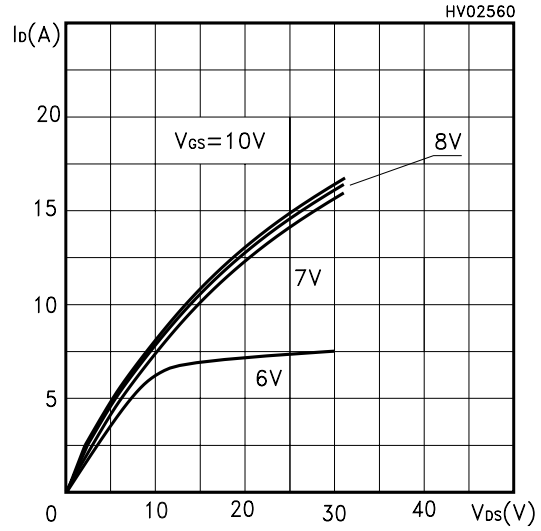
### Safe Operating Area



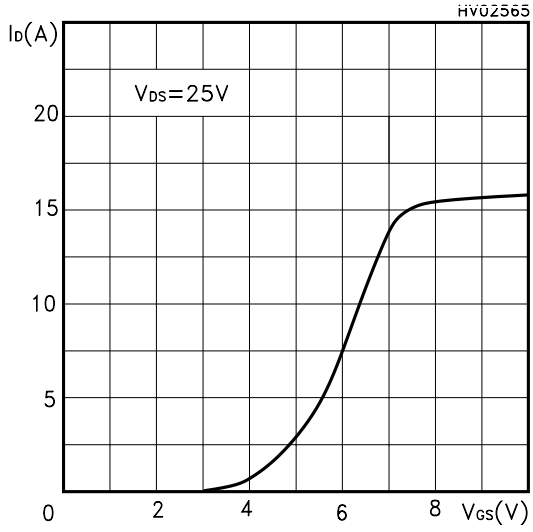

### Thermal Impedance



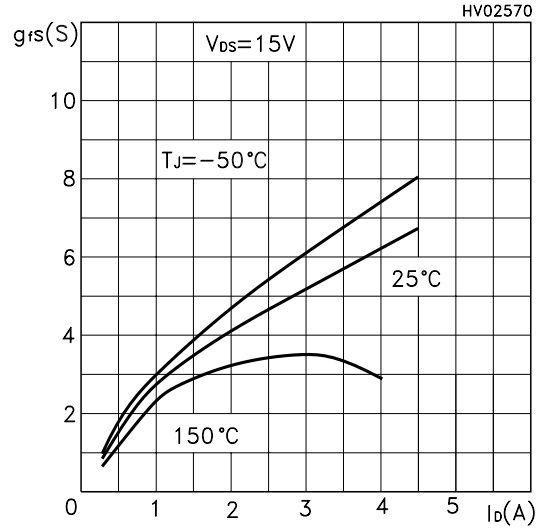

### Output Characteristics



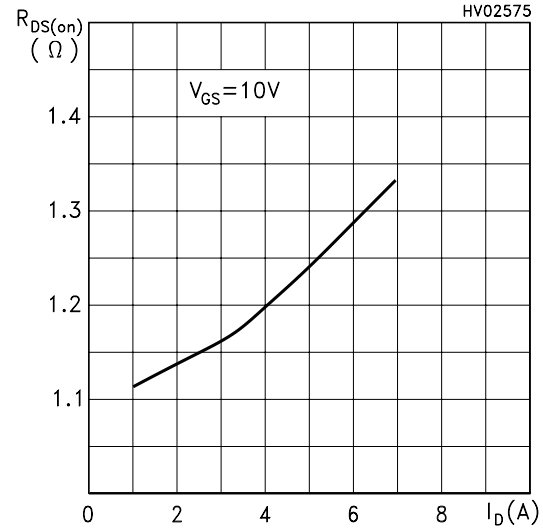

### Transfer Characteristics



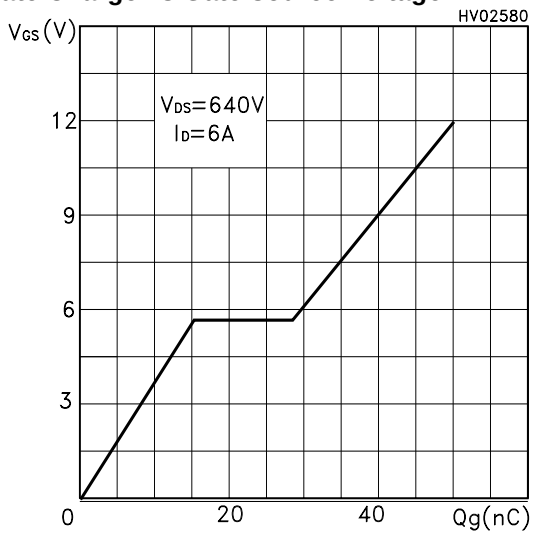

### Transconductance



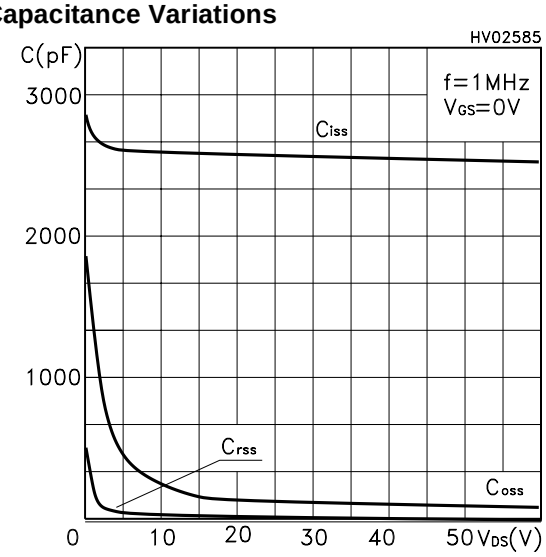

### Static Drain-source On Resistance



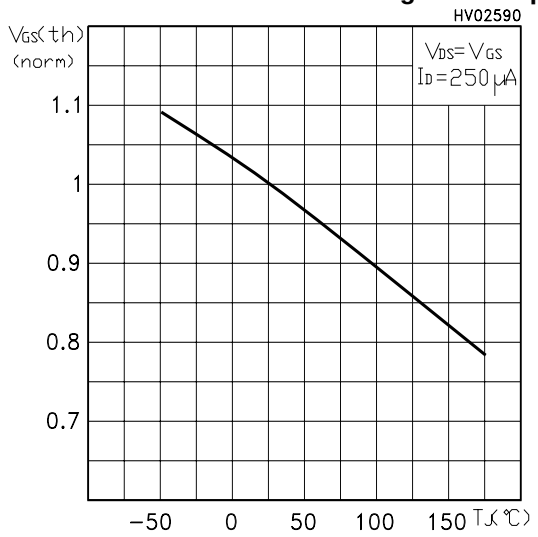
### Gate Charge vs Gate-source Voltage



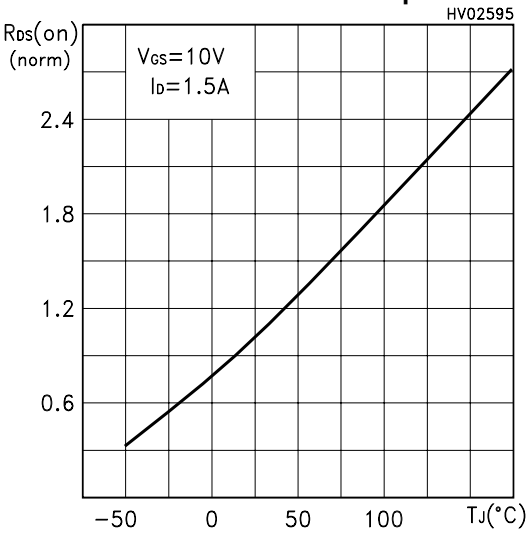

### Capacitance Variations




### Normalized Gate Threshold Voltage vs Temp.




### Normalized On Resistance vs Temperature




### Source-drain Diode Forward Characteristics

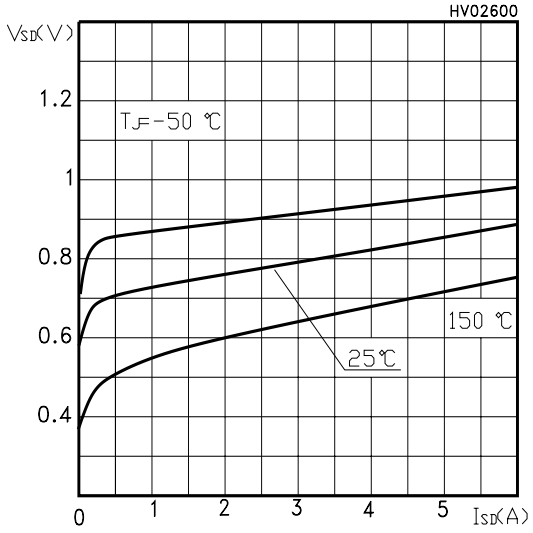


**Fig. 1:** Unclamped Inductive Load Test Circuit

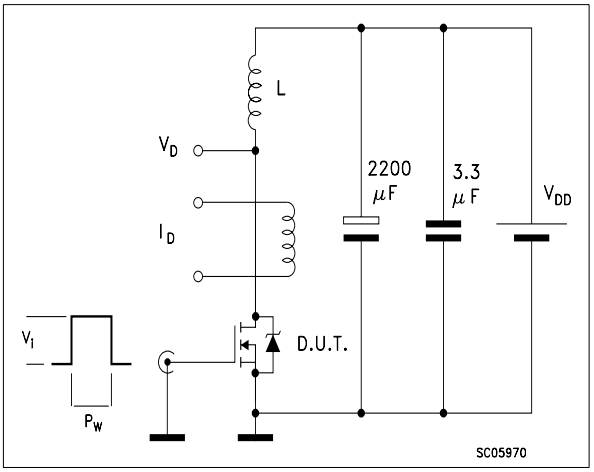



**Fig. 2:** Unclamped Inductive Waveform

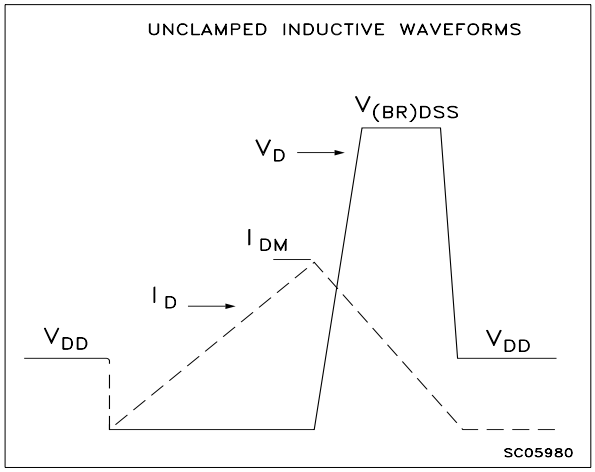



**Fig. 3:** Switching Times Test Circuits For Resistive Load

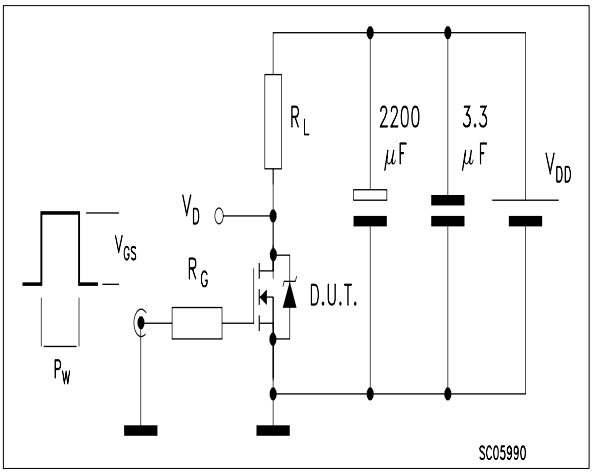



**Fig. 4:** Gate Charge test Circuit

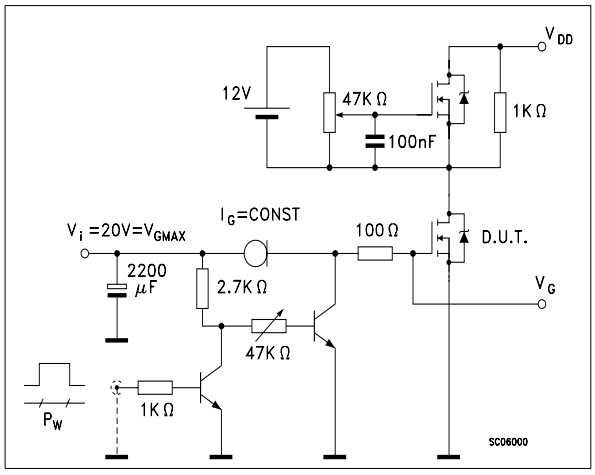
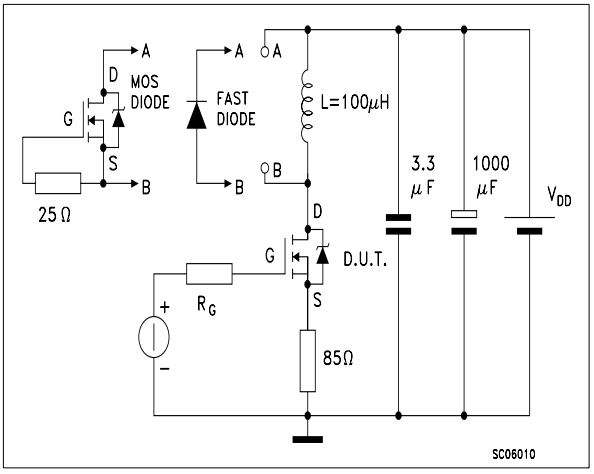
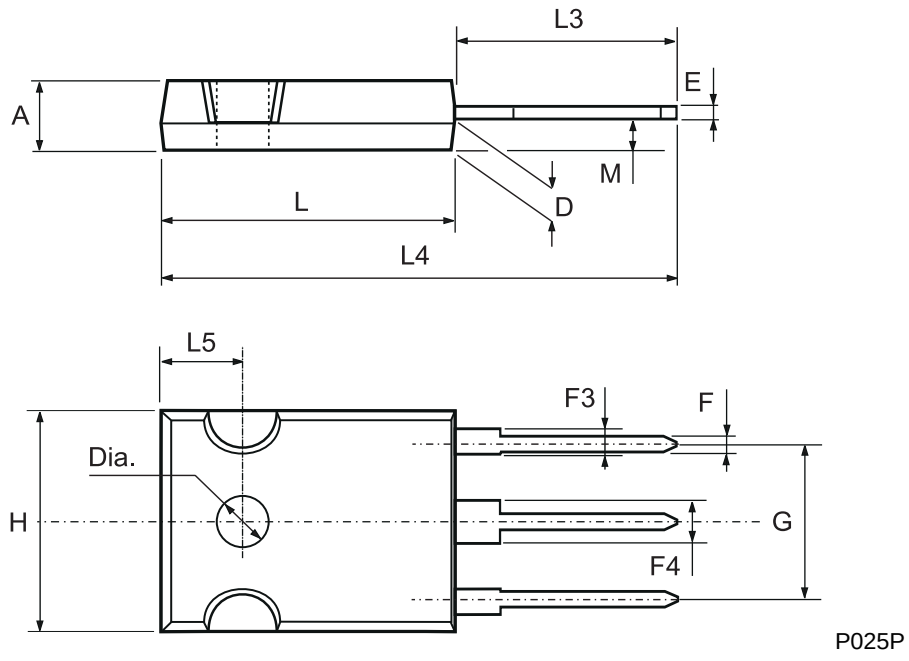



**Fig. 5:** Test Circuit For Inductive Load Switching And Diode Recovery Times



## TO-247 MECHANICAL DATA

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 4.7 | | 5.3 | 0.185 | | 0.209 |
| D | 2.2 | | 2.6 | 0.087 | | 0.102 |
| E | 0.4 | | 0.8 | 0.016 | | 0.031 |
| F | 1 | | 1.4 | 0.039 | | 0.055 |
| F3 | 2 | | 2.4 | 0.079 | | 0.094 |
| F4 | 3 | | 3.4 | 0.118 | | 0.134 |
| G | | 10.9 | | | 0.429 | |
| H | 15.3 | | 15.9 | 0.602 | | 0.626 |
| L | 19.7 | | 20.3 | 0.776 | | 0.779 |
| L3 | 14.2 | | 14.8 | 0.559 | | 0.582 |
| L4 | | 34.6 | | | 1.362 | |
| L5 | | 5.5 | | | 0.217 | |
| M | 2 | | 3 | 0.079 | | 0.118 |



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