# STw8009
# STw8019

## Mobile Video DENC

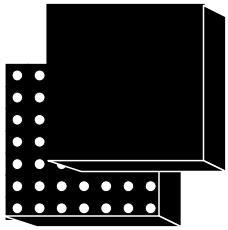
**Preliminary Data**

## Features

- Two analog outputs (10 bits DAC) with:
  - CVBS (Composite) output or Y/C (S-VHS)
  - NTSC-M & 4.43 & PAL-BDGHI, N, M support
  - 35 mA current driver
- 8-bit digital interface input supporting both embedded and external synchro
  - CCIR 601 / YCbCr 4:2:2 format
  - CCIR 656: 27 Mhz pixel input clock
- Latest Macrovision (7.1.L1) (STw8019 only)
- 2-wire serial MPU interface (I2C compatible)
- Master and slave modes
- TV / VCR plug insertion detection
- Supply voltages
  - 2.8V/3.3V analog
  - 1.8 V digital I/O
  - 1.2 V for core
- Power consumption
  - Sleep mode: 5 µW
  - Standby mode: 150 µW maximum
  - CVBS: 125 mW
  - Y/C: 245 mW
- Package
  - TFBGA 4x4x1.2 mm height, 0.5 mm pitch,
  - VFBGA 3x3x1 mm height, 0.4 mm pitch
  - TQFP64 also available
- Full matrix: 7 x 7

## Description

STw8009/STw8019 is aimed at mobile video Digital ENCoder (DENC). This device converts digital video signals into high quality analog signal compliant with TV standards, it is able to encode interlaced (in all standards) and non-interlaced (in PAL and NTSC).



TFBGA 4 mm x 4 mm x 1.2 mm
VFBGA 3 mm x 3 mm x 1.0 mm

Featuring ultra low power consumption, it suits perfectly mobile appliances that interface occasionally with TV sets or VCRs. It is also the ideal companion for digital application processors such as ST's Nomadik family.

To minimize PCB space usage, STw8009/STw8019 features a high level of integration. STw8009/STw8019 drives directly the video input, CVBS of a TV set or the Y/C video input of a VCR through optional ESD protection devices.

The 27 MHz clock and the device power management are controlled through the digital processor interface [PORn, Suspend and 2-wire I2C compatible serial MPU]. This digital processor interface also controls the STw8009/STw8019 operating modes (off, sleep, standby and active).

## Applications

- Mobile video Digital ENCoder (DENC)

## Order codes

| Part number | Package |
|---|---|
| STw8009A | TFBGA49 |
| STw8019A | TFBGA49 |
| STw8009BS3 | VFBGA49 |
| STw8019BS3 | VFBGA49 |



This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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# 1 Overview

STw8009/STw8019 is aimed at mobile video Digital ENCoder (DENC). This device converts digital video signals into high quality analog signal compliant with TV standards, it is able to encode interlaced (in all standards) and non-interlaced (in PAL and NTSC).

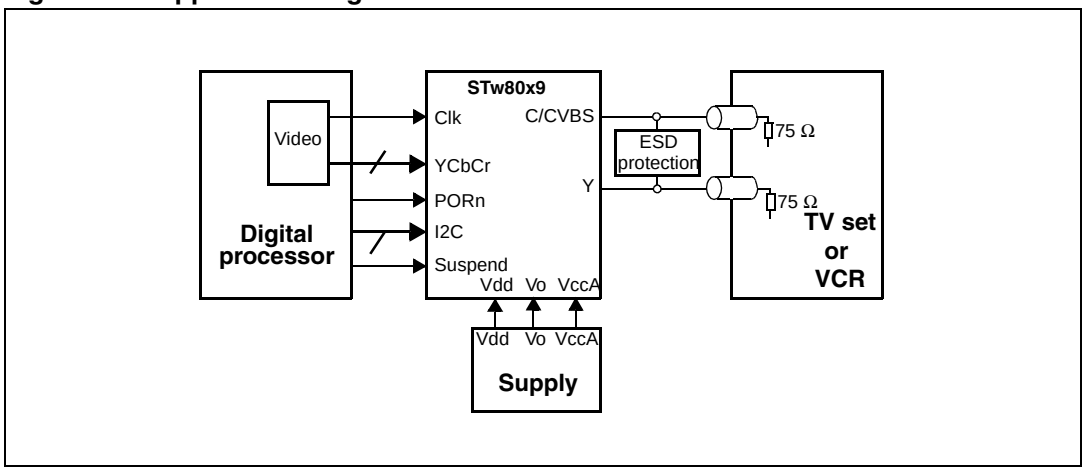
Featuring ultra low power consumption, it suits perfectly mobile appliances that interface occasionally with TV sets or VCRs. It is also the ideal companion for digital application processors such as ST's Nomadik family.

To minimize PCB space usage, the device features a high level of integration. The 35 mA high performance DAC allows direct drive of 37.5 Ω load.

STw8009/STw8019 drives directly the video input, CVBS of a TV set or the Y/C video input of a VCR through optional ESD protection devices. It is powered by three voltage supplies, 2.8/3.3 V, 1.8 V and 1.2 V (VccA, VI/O, Vdd).

The 27 MHz clock and the device power management are controlled through the digital processor interface [PORn, Suspend and 2-wire I2C compatible serial MPU]. This digital processor interface also controls the operating modes (off, sleep, standby and active).

**Figure 1. Application diagram**




## Naming convention

Unless clearly specified in the document, STw8009/STw8019 stands for both STw8009 and STw8019.

# 2 Functional block diagram

**Figure 2. STw8009 block diagram**

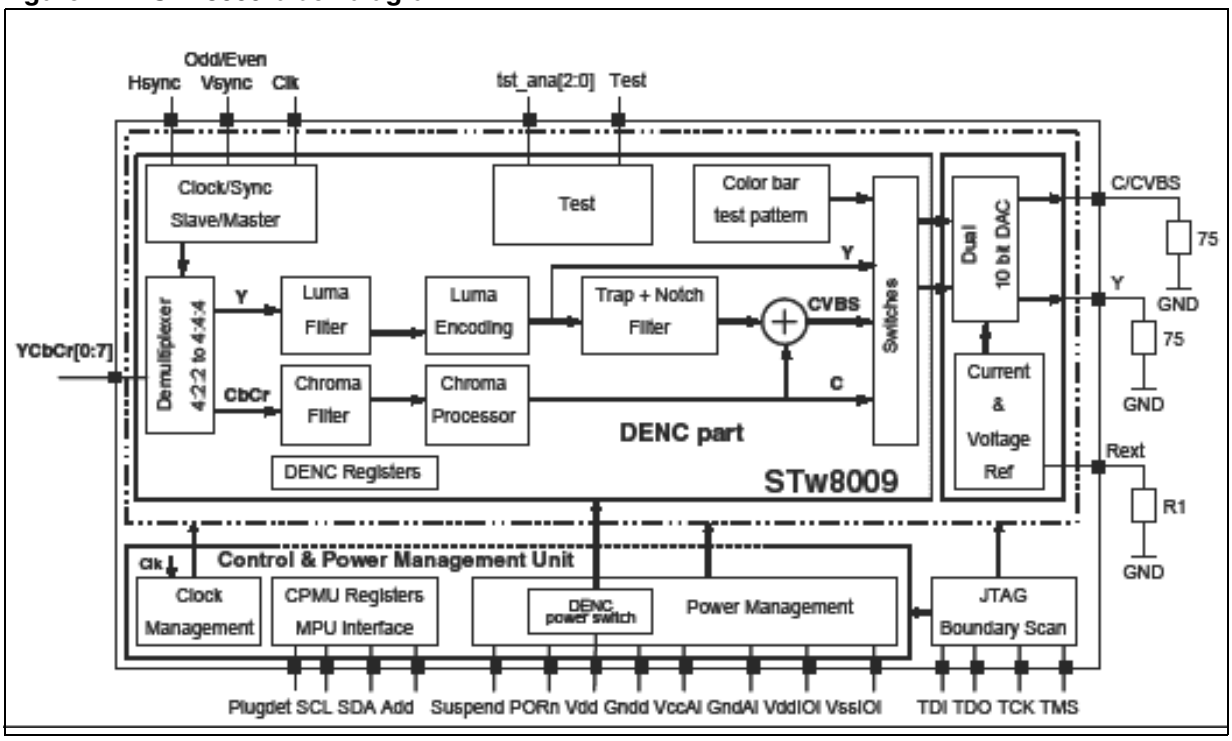
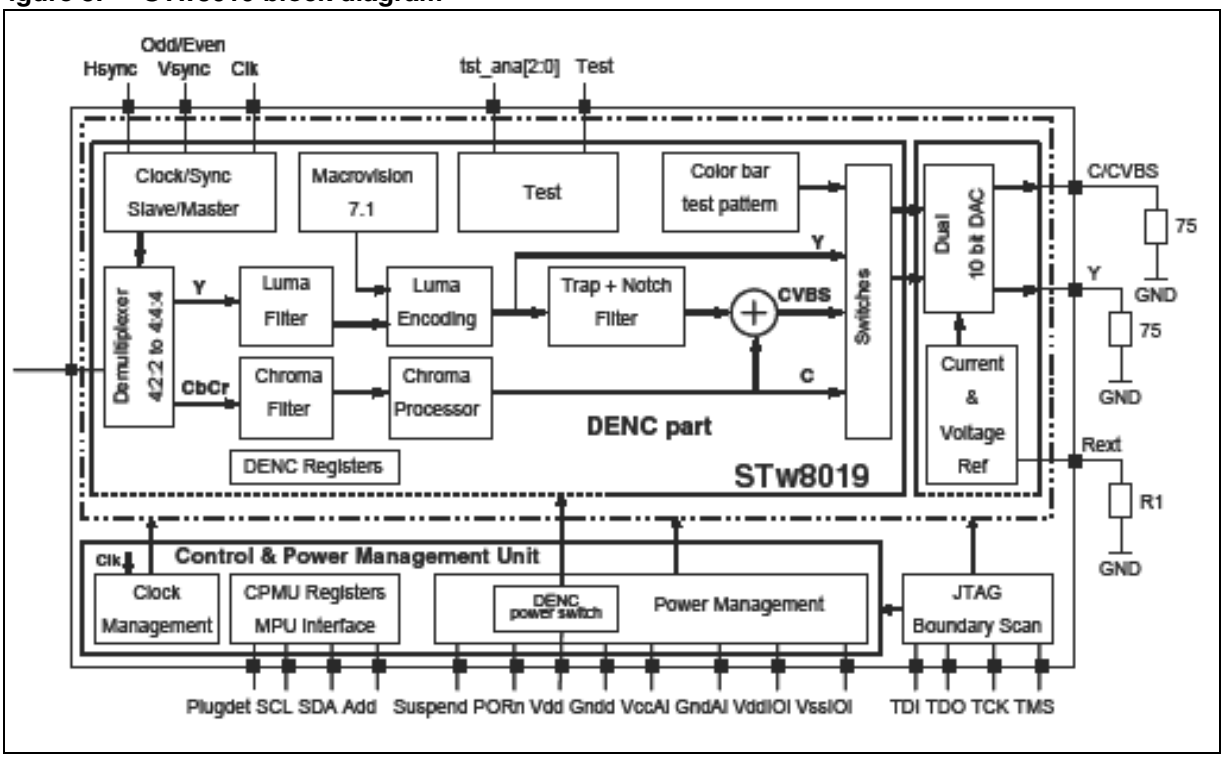



**Figure 3. STw8019 block diagram**



# 3 Ball/pin information

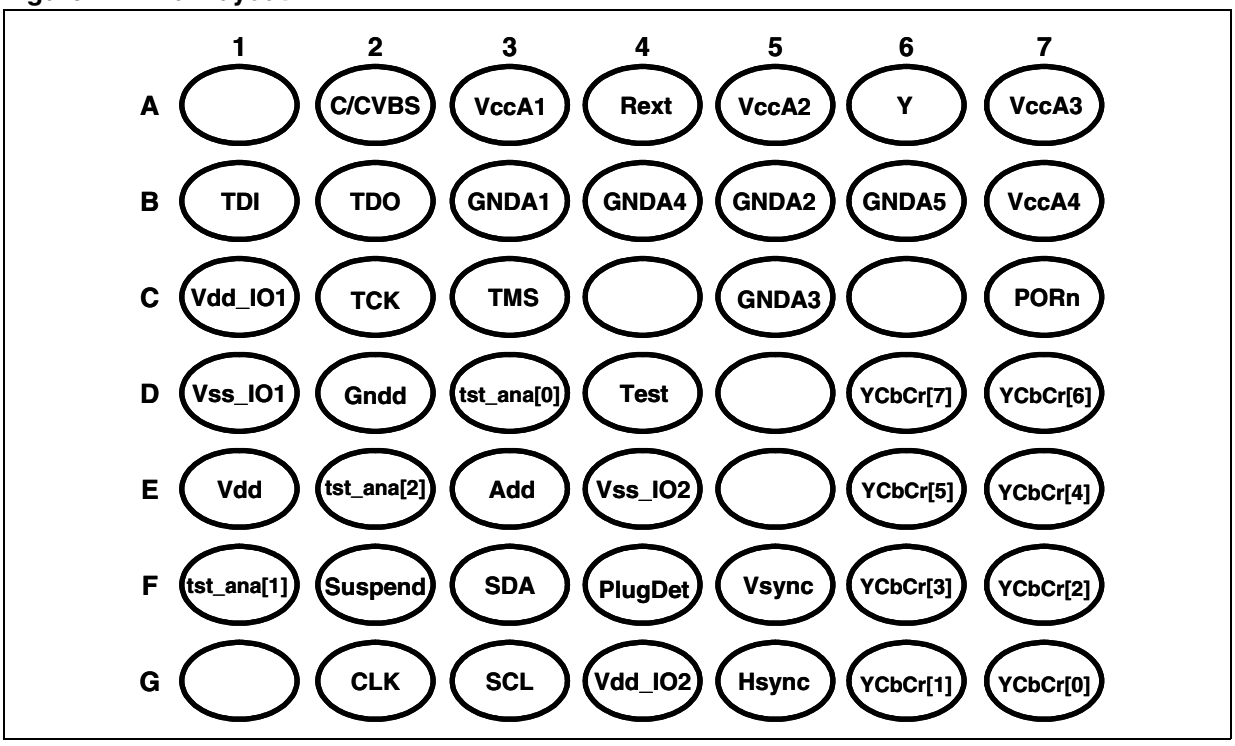
**Table 1. Product name ball functions**

| Ball | Name | Type | Voltage | Description |
|---|---|---|---|---|
| E1 | Vdd | Power | 1.2 V | Digital core chip supply |
| D2 | Gndd | GND | 0 V | Digital core chip ground |
| C1 | Vdd_IO1 | Power | 1.8 V | Digital I/O supply |
| D1 | Vss_IO1 | GND | 0 V | Digital I/O ground |
| G4 | Vdd_IO2 | Power | 1.8 V | Digital I/O supply |
| E4 | Vss_IO2 | GND | 0 V | Digital I/O ground |
| A3 | VccA1 | Power | 2.8 /3.3V | DAC1 matrix analog power supply |
| A5 | VccA2 | Power | 2.8 /3.3 V | DAC2 matrix analog power supply |
| A7 | VccA3 | Power | 2.8 /3.3 V | 2.8/3.3 V digital feature supply |
| B7 | VccA4 | Power | 2.8 /3.3 V | 2.8 /3.3 V digital feature supply |
| B3 | GNDA1 | GND | 0 V | DAC1 ground |
| B5 | GNDA2 | GND | 0 V | DAC2 ground |
| C5 | GNDA3 | GND | 0 V | 2.8 /3.3 V digital feature ground |
| B4 | GNDA4 | GND | 0 V | Rext ground connection |
| B6 | GNDA5 | GND | 0 V | Analog ground |
| A4 | Rext | Analog | | DAC current reference setting |
| G2 | CLK | Digital Input | 1.8 V | 27 MHz master pixel clock (pixclk) |
| G7, G6, F7, F6, E7, E6, D7, D6 | YCbCr[0:7] | Digital Input | 1.8 V | Time multiplexed 4:2:2 luminance and chrominance data as defined in CCIR 601 and CCIR 656 (excepted for TTL input signals) |
| G5 | Hsync | Digital I/O | 1.8 V | Horizontal Synchronization signal:<br>- Input in slave mode, except when sync is extracted from YcbCr data<br>- Output in master mode and when sync is extracted from YcbCr signal. |
| F5 | Vsync Odd/Even | Digital I/O | 1.8 V | Vertical Synchronization – Odd/Even signal:<br>- Input in slave mode, except when sync is extracted from YcbCr data<br>- Output in master mode and when sync is extracted from YcbCr signal. |
| F3 | SDA | Digital I/O | 1.8 V | 2 wire serial MPU data line |
| G3 | SCL | Digital Input | 1.8 V | 2 wire serial MPU clock |
| E3 | Add | Digital input | 1.8 V | Device address selection |
| C7 | PORn | Digital input | 1.8 V | Power On Reset (Active low) |
| F2 | Suspend | Digital input | 1.8 V | Suspend input |

**Table 1. Product name ball functions**

| | | | | |
|---|---|---|---|---|
| A2 | C/CVBS | Analog output | | The output can be selected to be composite video or chroma signal for s-video. |
| A6 | Y | Analog output | | Luminance signal for s-video |
| B1 | TDI | Digital input | 1.8 V | JTAG test data in |
| B2 | TDO | Digital output | 1.8 V | JTAG test data out |
| C2 | TCK | Digital input | 1.8 V | JTAG test clock |
| C3 | TMS | Digital input | 1.8 V | JTAG test mode select |
| D4 | Test | Digital input | 1.8 V | Put the device in test mode |
| D3, F1, E2 | tst_ana[0:2] | Digital output | 1.8 V | DENC test |
| F4 | PlugDet | Digital input | 1.8 V | TV / VCR plug connection detection / CMOS input |

**Figure 4. Ball layout**



# 4 Functional description

## 4.1 General

STw8009/STw8019 operates either in master mode where it supplies all sync signal or in slave mode.

The digital input is an 8-bit bus carrying Y, Cb and Cr at 13.5 MHz. Input samples are latched in on the rising edge of the clock input signal.

STw8009/STw8019 is able to encode interlaced (in all standards) and non interlaced (in PAL and NTSC) video.

STw8009/STw8019 outputs interlaced or non-interlaced video in PAL-B,D,G,H,I,PAL-N,PAL-M or NTSC-M standards (“NTSC-4.43” is also possible).

The burst sequences are internally generated, subcarrier generation being performed numerically with the 27 MHz as reference. 4-frame bursts are generated for PAL or 2-frame bursts for NTSC. Rise and fall times of synchronization tips and burst envelope are internally controlled according to the relevant ITU_R and SMPTE recommendations.

## 4.2 Master & slave modes

In master mode, STw8009/STw8019 supplies Hsync and Odd/Even sync signals (with independently programmable polarities) to drive other blocks. STw8009/STw8019 starts encoding and counting clock cycles as soon as the master mode has been loaded into the control register (Reg 0). Configuration bits “Syncout_ad[1:0]” (Reg 4) allow to shift the relative position of the sync signals by up to 3 clock cycles to cope with any YcbCr phasing.

In slave modes, several modes are available, Odd/Even+Hsync based, Vsync+Hsync based, Odd/Even-only based, Vsync-only based or Sync-in-data based.

## 4.3 Auto test mode

An auto test mode is available, which causes STw8009/STw8019 to produce a color bar pattern, in the appropriate standard, independently from the video input.

## 4.4 Input demultiplexor

The incoming YcbCr 4:2:2 data are demultiplexed into chroma information stream, a “blue-difference” and a “red-difference”, and a luma information stream. Incoming data bits are treated as blue, red or luma samples according to their relative position with respect to the sync signals. Brightness, Saturation and Contrast are then performed on demultiplexed data.

The ITU-R601 recommendation defines the black luma level as Y=16dec and the maximum white luma level as Y=235dec. Similarly it defines 255 quantification levels for the color difference components (Cr, Cb) centered around 128. Accordingly, incoming YcbCr samples can be saturated. In this case STw8009/STw8019 provides a saturation limitation feature to avoid having heavily saturated signal before digital to analog conversion and to avoid generating a distorted signal at STw8009/STw8019 CVBS or Y/C outputs.

## 4.5 Sub-carrier generation

A Direct Digital Frequency Synthesizer (DDFS) generates the required color sub-carrier frequency using a 24-bit phase accumulator. Sub-carrier frequency is programmable with a 1.6 Hz step.

## 4.6 Luminance encoding

The luminance that is added to the chrominance to create the composite CVBS signal can be trap-filtered at 3.58 MHz (NTSC) or 4.43 MHz (PAL). This supports application oriented towards low-end TV sets which are subject to cross-color.

A 7.5 IRE pedestal can be programmed if needed with all standards. This allows in particular to encode Argentinian and non-Argentinian PAL-N, or Japanese NTSC.

A programmable delay can be inserted on the luminance path to offset any chroma/luma delay introduced by off-chip filtering.

STw8009/STw8019 output signals are IF modulated in NTSC M standard so that a sound notch filter is required. The notch filter which is on the Luma path is defined by a set of coefficients and is implemented in the STw8009/STw8019 as default values. The set is also programmable.

**Figure 5. Luma filtering**

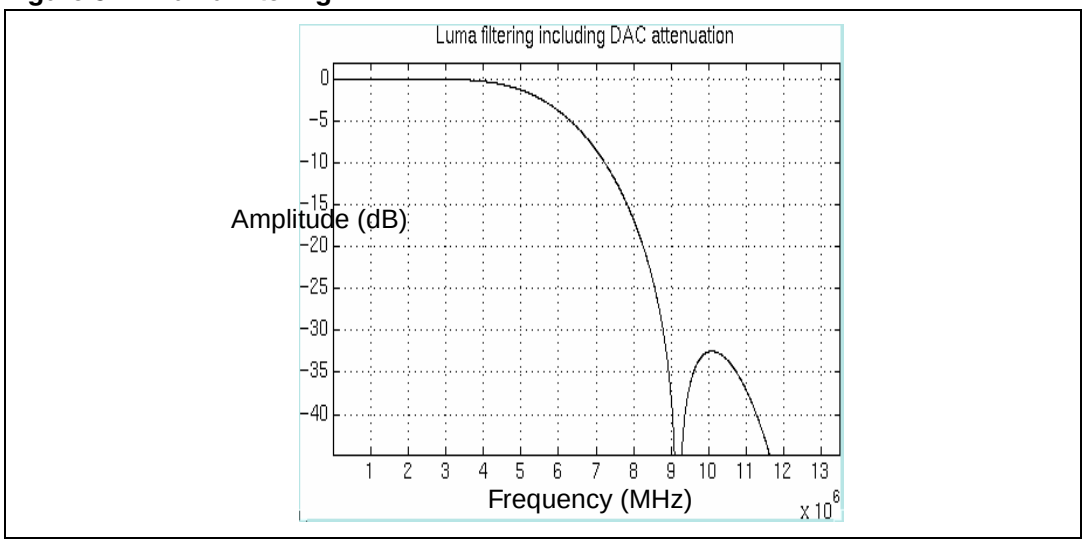


**Figure 6. Luma filtering with 3.58 MHz trap**

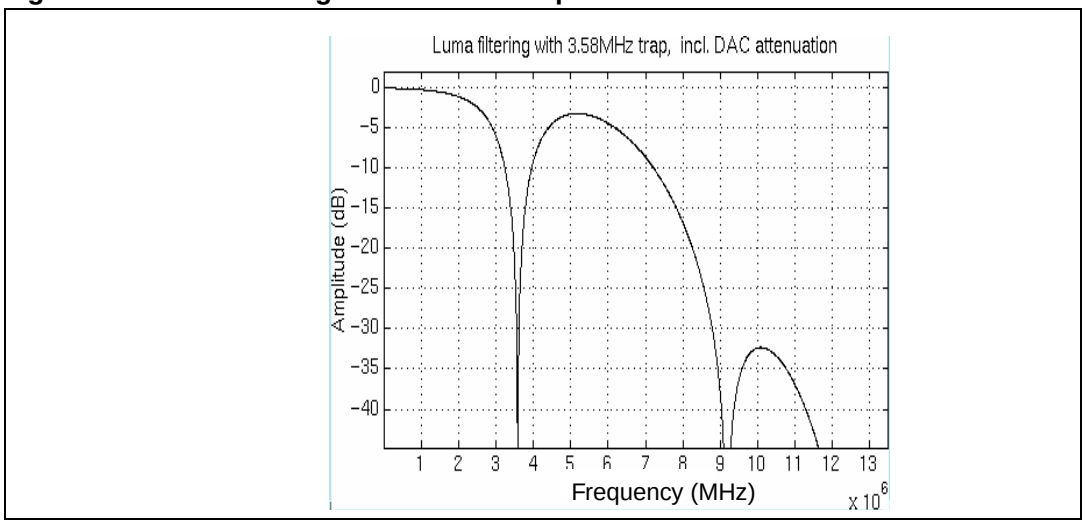
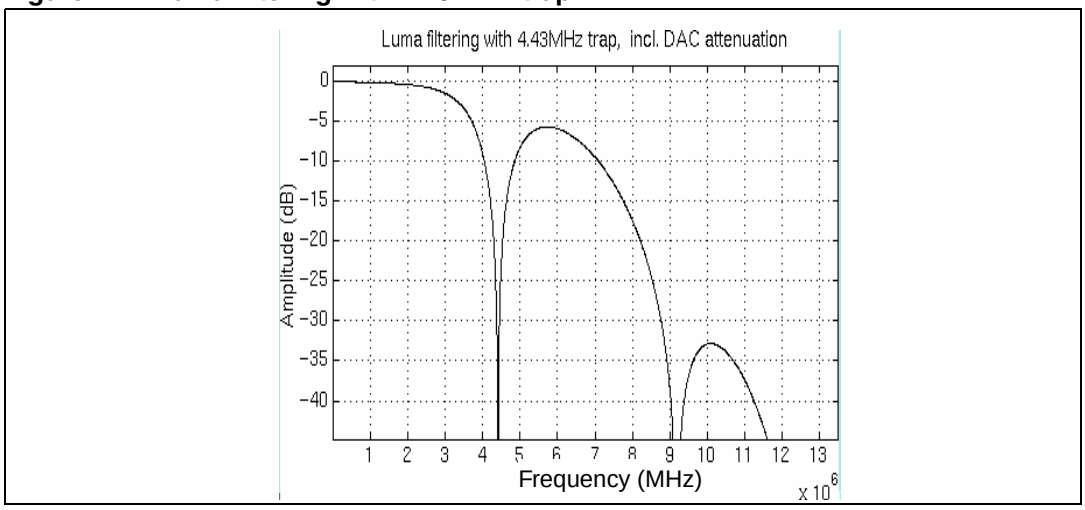



**Figure 7. Luma filtering with 4.43 MHz trap**




## 4.7 Chrominance encoding

Chroma components are computed from demultiplexed Cb, Cr samples. Before modulating the subcarrier, the chroma components are band-limited and interpolated at pixel clock rate. A set of 4 different filters is available for chroma filtering to suit a wide variety of applications in the different standards and filters recommended by ITU-R 624-4 and SMPTE170-M. The available –3dB bandwidths are 1.1, 1.3, 1.6 and 1.9 MHz.

Narrow bandwidths are useful against cross-luminance artifacts while wide bandwidths allow to keep higher chroma contents.

**Figure 8. 1.1 MHz chroma filter**

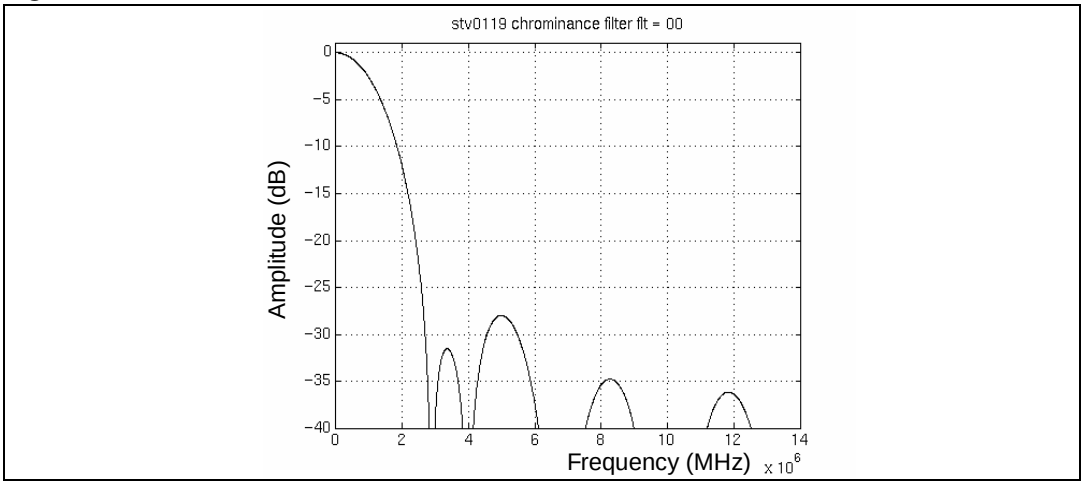



**Figure 9. 1.3 MHz chroma filter**

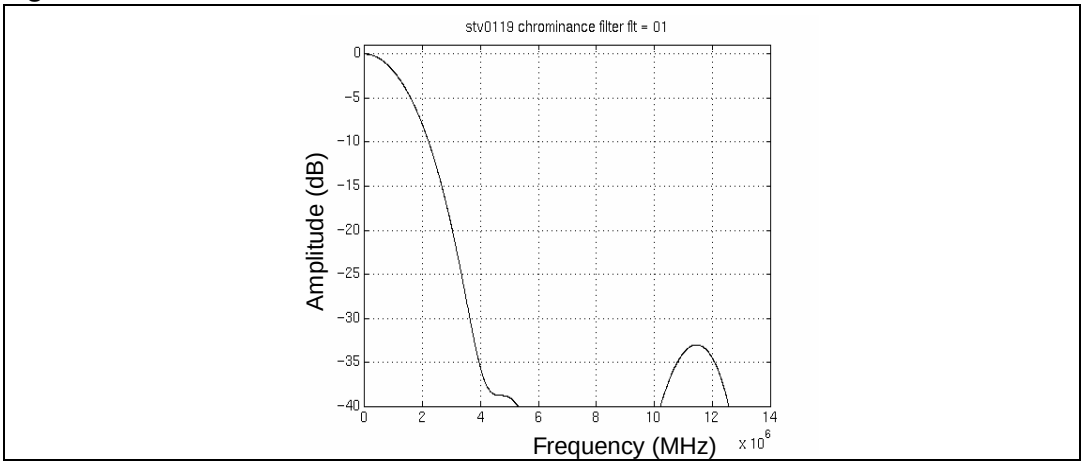



**Figure 10. 1.6 MHz chroma filter**

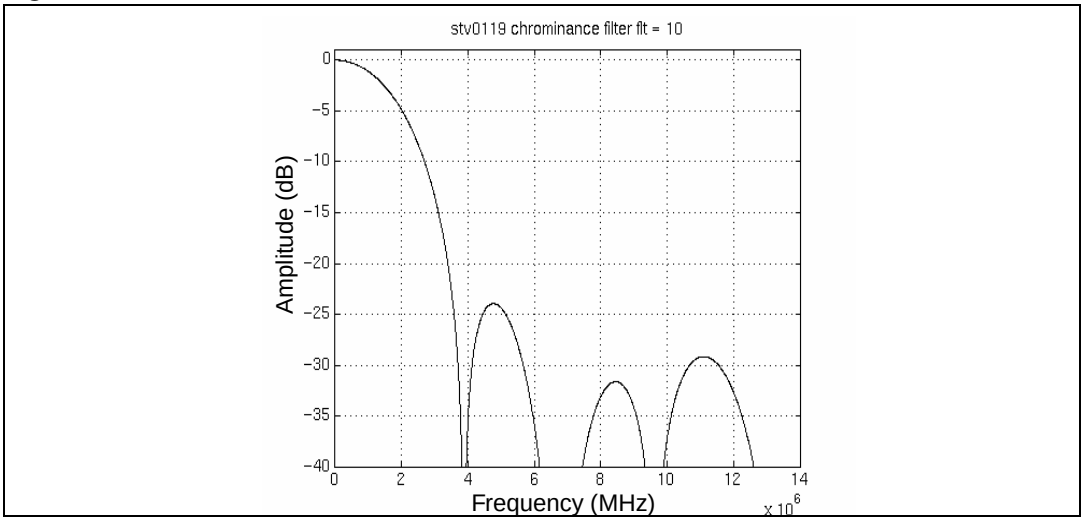
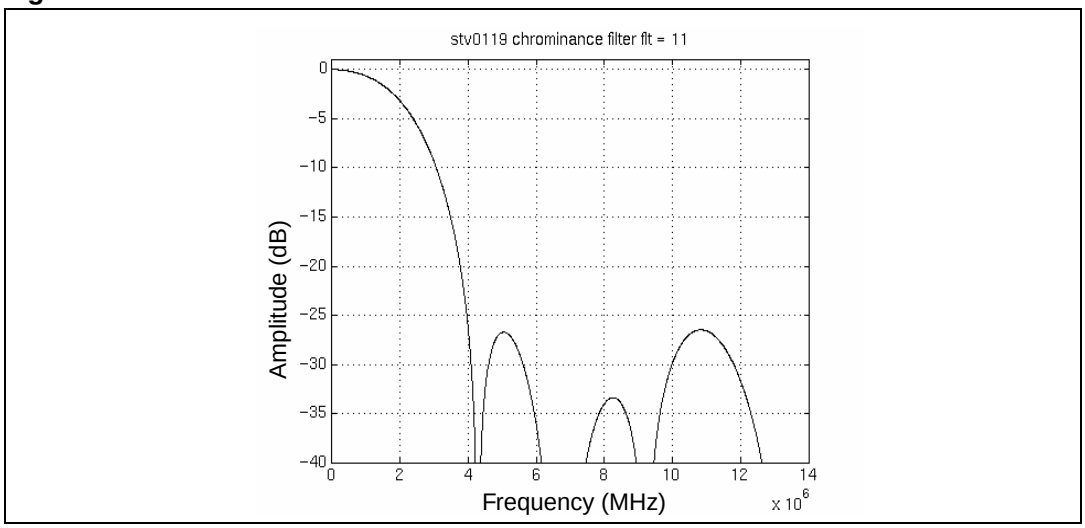


**Figure 11. 1.9 MHz chroma filter**




## 4.8 Composite video signal generation

The composite video signal is created by adding the luminance and the chrominance components. A saturation function is included in the adder to avoid overflow errors.

## 4.9 Macrovision™ copy protection

STw8019 provides Macrovision™ copy protection rev 7.1.L1 feature.

## 4.10 TV/VCR plug insertion detection

Plugdet ball is used to detect the connection of a TV or a VCR. The host can read the status in a dedicated register in standby and active modes.

## 4.11 DAC

STw8009/STw8019 outputs generate Composite video signal on one output or Y/C video signals on two outputs.

Two embedded 10-bit DACs allow the STw8009/STw8019 to directly drive 37.5 Ohms loads on each output.

## 4.12 Power management

Power management includes power supplies, reset signals, clock gating and a set of dedicated pins and registers. Power management is used to set the STw8009/STw8019 in different operating modes.

### 4.12.1 Operating modes

STw8009/STw8019 can be in the following operating modes.

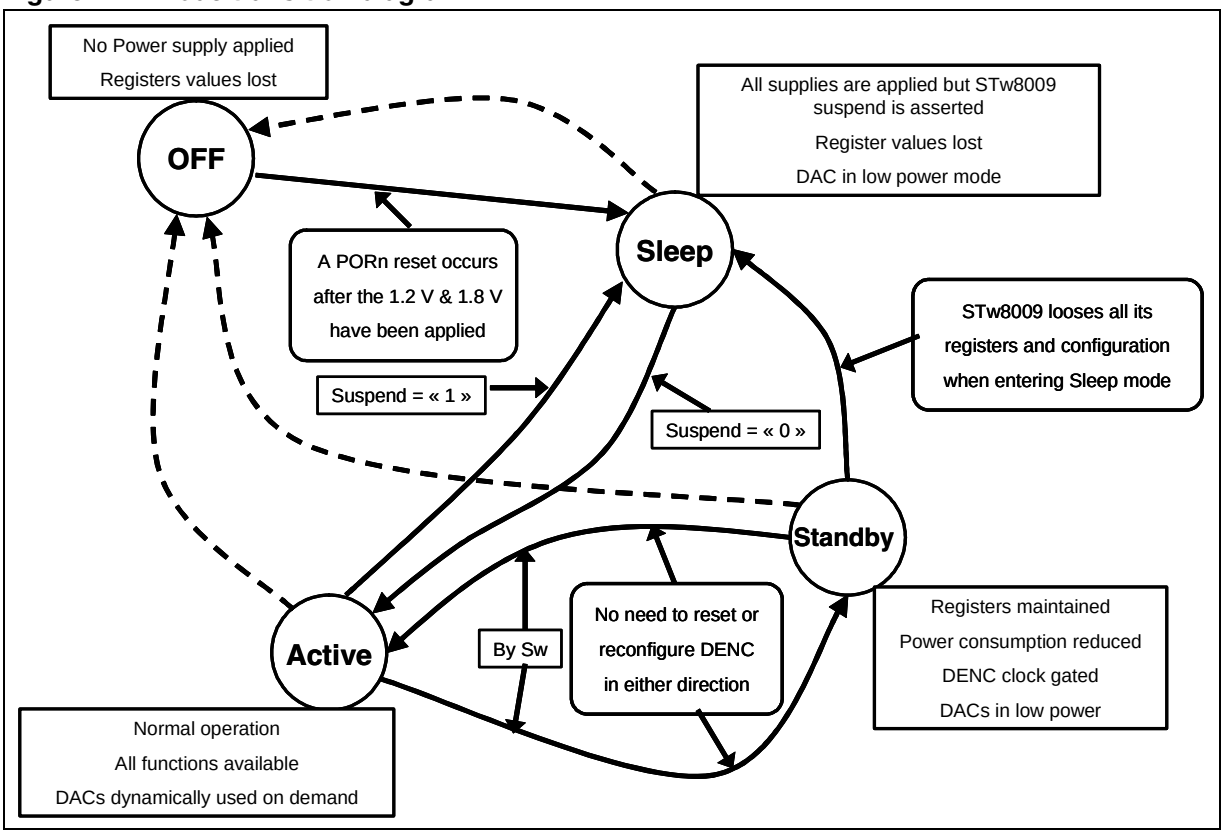
- OFF
  - 1.2 V, 1.8 V, 2.8 /3.3 V are not present.
  - All values from STw8009/STw8019 registers are lost.
- Sleep
  - 1.2 V, 1.8 V, 2.8 /3.3 V are present.
  - The suspend signal is active.
  - The DACs are in their minimum power consumption mode.
  - All values from the STw8009/STw8019 registers are lost.
- Standby
  - All power supplies are present: 1.2 V, 1.8 V, 2.8 /3.3 V.
  - The 27 MHz pixel clock must be activated.
  - The suspend signal is inactive.
  - STw8009/STw8019 is set in standby mode by programming the Control and power Management Unit registers (Reg 128 to 132) through the 2 wire serial MPU interface. STw8009/STw8019 saves the register values.
  - The other registers (Reg 00 to 109) are not accessible in this mode.
  - The DACs are in their minimum power consumption mode.
  - This mode is a low power state that enables a fast switching to active mode.
- Active
  - All power supplies are present: 1.2 V, 1.8 V, 2.8 /3.3 V.
  - STw8009/STw8019 receives the 27 MHz pixel clock.
  - The suspend signal is inactive.
  - STw8009/STw8019 is placed in active mode by programming the control and power management unit registers (Reg 128 to 132), through the 2 wire serial MPU interface. STw8009/STw8019 saves the register values.
  - The 27 MHz pixel clock is distributed in all STw8009/STw8019.

The DACs are supplied by the 2.8 /3.3 V and can be individually activated or deactivated. For example only one DAC in CVBS output and both DACs in Y/C output.

### 4.12.2 Mode transition diagram

The following mode transition diagram shows the main possible transitions between the modes and the actions.

**Figure 12. Mode transition diagram**




#### Transitions to OFF mode

The possible transitions are indicated in *Figure 12: Mode transition diagram*10 in dotted lines. No internal data needs to be saved and the STw8009/STw8019 can be turned OFF from any mode. The only restriction is to comply with the power supply rules described here after.

#### Transition from OFF mode to Sleep mode then to Active mode

Power up must be done by starting from OFF to Sleep mode and then from Sleep to Active mode. Sleep to Standby is not possible.

Following the transition from OFF to Sleep mode, STw8009/STw8019 must receive PORn signal (Power On Reset) to initialize the Control and power Management Unit registers (Reg 128 to 132).

The host sends the order for the STw8009/STw8019 to switch from Sleep to Active mode by releasing Suspend ball and enabling pixel clock (27 MHz). The device then generates a reset sequence to the DENC part.

### Transition from Active mode to Sleep mode

In Sleep mode, DENC is not powered on. When Suspend signal changes from « 0 » to « 1 », the device goes from Active to Sleep mode and an internal Reset signal is generated by the Control Power Unit management to the DENC part. This signal has a 6 pixclk duration (pixclk = 27 MHz).

### Transition between Standby and Active modes

Transitions between these two modes are applied by software configuration through I2C interface.

### Supply management

At power up, supplies must be applied according to the following sequence:

VddIO1, VddIO2 (1.8 V) then,

Vdd (1.2 V) then,

VccA1, VccA2, VccA3, VccA4 (2.8 /3.3 V)

and removed according to the following sequence:

VccA1, VccA2, VccA3, VccA4 (2.8 /3.3 V) then,

Vdd (1.2 V) then,

VddIO1, VddIO2 (1.8 V)

## 4.13 JTAG interface

To ease the integration of STw8009/STw8019 in its system application, a JTAG interface is available.

# 5 Control registers

## 5.1 Register addresses

**Table 2. Register addresses**

| Name | Type | N° | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|
| **DENC registers** | | | | | | | | | | |
| configuration0 | R/W | 00 | std1 | std0 | sync2 | sync1 | sync0 | polh | polv | freerun |
| configuration1 | R/W | 01 | blkli | flt1 | flt0 | sync_ok | coki | setup_main | [0] | [0] |
| configuration2 | R/W | 02 | nintrl | enrst | bursten | xxx | selrst | rstosc_buf | valrst1 | valrst0 |
| configuration3 | R/W | 03 | main_entrap | trap_4.43 | [0] | [0] | main_del_en | val_422_ck_mux | xxx | [0] |
| configuration4 | R/W | 04 | syncin_ad1 | syncin_ad0 | syncout_ad1 | syncout_ad0 | aline | hue_en | xxx | xxx |
| configuration5 | R/W | 05 | selrst_inc | bkdac1 | bkdac2 | [0] | [0] | [0] | [0] | dacinv |
| configuration6 | R/W | 06 | softreset | jump | dec_ninc | free_jump | cfc1 | cfc0 | [0] | maxdyn |
| configuration7 | R/W | 07 | [0] | [0] | [0] | xxx | [0] | bypass_sync_corr | [0] | [0] |
| configuration8 | R/W | 08 | ph_rst_mode1 | ph_rst_mode0 | xxx | val_422_m ux | blk_all | xxx | xxx | xxx |
| Status | R | 09 | hok | atfr | | | fldct2 | flsct1 | fldct0 | jump |
| increment_dfs | R/W | 10 | d23 | d22 | d21 | d20 | d19 | d18 | d17 | d16 |
| increment_dfs | R/W | 11 | d15 | d14 | d13 | d12 | d11 | d10 | d9 | d8 |
| increment_dfs | R/W | 12 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| phase_dfs | R/W | 13 | xxx | xxx | xxx | xxx | xxx | xxx | o23 | o22 |
| phase_dfs | R/W | 14 | o21 | o20 | o19 | o18 | o17 | o16 | o15 | o14 |
| dac1mult | R/W | 17 | dac1_mult5 | dac1_mult4 | dac1_mult3 | dac1_mult2 | dac1_mult1 | dac1_mult0 | [1] | [0] |
| reserved | R/W | 20 | xxx | xxx | xxx | xxx | xxx | xxx | xxx | xxx |
| line_reg | R/W | 21 | ltarg8 | ltarg7 | ltarg6 | ltarg5 | ltarg4 | ltarg3 | ltarg2 | ltarg1 |
| line_reg | R/W | 22 | ltarg0 | lref8 | lref7 | lref6 | lref5 | lref4 | lref3 | lref2 |
| line_reg | R/W | 23 | lref1 | lref0 | - | - | - | - | - | - |
| Reserved | R | 24 | - | - | - | - | - | - | - | - |
| reserved | xxx | 45 | xxx | xxx | xxx | xxx | xxx | xxx | xxx | xxx |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| reserved | xxx | 63 | xxx | xxx | xxx | xxx | xxx | xxx | xxx | xxx |
| c_mult & ttx | R/W | 65 | c_mult3 | c_mult2 | c_mult1 | c_mult0 | [0] | xxx | [0] | bcs_en_main |
| Brightness | R/W | 69 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Contrast | R/W | 70 | c7 | c6 | c5 | c4 | c3 | c2 | c1 | c0 |
| Saturation | R/W | 71 | s7 | s6 | s5 | s4 | s3 | s2 | s1 | s0 |
| Chroma_coef_0 | R/W | 72 | flt_s | plg_div1 | plg_div0 | c0(4) | c0(3) | c0(2) | c0(1) | c0(0) |
| Chroma_coef_1 | R/W | 73 | xxx | c8(8) | c1(5) | c1(4) | c1(3) | c1(2) | c1(1) | c1(0) |
| Chroma_coef_2 | R/W | 74 | xxx | c2(6) | c2(5) | c2(4) | c2(3) | c2(2) | c2(1) | c2(0) |

**Table 2. Register addresses**

| Name | Type | N° | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Chroma_coef_3 | R/W | 75 | xxx | c3(6) | c3(5) | c3(4) | c3(3) | c3(2) | c3(1) | c3(0) |
| Chroma_coef_4 | R/W | 76 | c4(7) | c4(6) | c4(5) | c4(4) | c4(3) | c4(2) | c4(1) | c4(0) |
| Chroma_coef_5 | R/W | 77 | c5(7) | c5(6) | c5(5) | c5(4) | c5(3) | c5(2) | c5(1) | c5(0) |
| Chroma_coef_6 | R/W | 78 | c6(7) | c6(6) | c6(5) | c6(4) | c6(3) | c6(2) | c6(1) | c6(0) |
| Chroma_coef_7 | R/W | 79 | c7(7) | c7(6) | c7(5) | c7(4) | c7(3) | c7(2) | c7(1) | c7(0) |
| Chroma_coef_8 | R/W | 80 | c8(7) | c8(6) | c8(5) | c8(4) | c8(3) | c8(2) | c8(1) | c8(0) |
| configuration9 | R/W | 81 | main_del3 | main_del2 | main_del1 | main_del0 | xxx | plg_div_y1 | plg_div_y0 | flt_ys |
| luma_coef_0 | R/W | 82 | xxx | xxx | l8(8) | l0(4) | l0(3) | l0(2) | l0(1) | l0(0) |
| luma_coef_1 | R/W | 83 | l9(9) | l9(8) | l1(5) | l1(4) | l1(3) | l1(2) | l1(1) | l1(0) |
| luma_coef_2 | R/W | 84 | l6(8) | l2(6) | l2(5) | l2(4) | l2(3) | l2(2) | l2(1) | l2(0) |
| luma_coef_3 | R/W | 85 | l7(8) | l3(6) | l3(5) | l3(4) | l3(3) | l3(2) | l3(1) | l3(0) |
| luma_coef_4 | R/W | 86 | l4(7) | l4(6) | l4(5) | l4(4) | l4(3) | l4(2) | l4(1) | l4(0) |
| luma_coef_5 | R/W | 87 | l5(7) | l5(6) | l5(5) | l5(4) | l5(3) | l5(2) | l5(1) | l5(0) |
| luma_coef_6 | R/W | 88 | l6(7) | l6(6) | l6(5) | l6(4) | l6(3) | l6(2) | l6(1) | l6(0) |
| luma_coef_7 | R/W | 89 | l7(7) | l7(6) | l7(5) | l7(4) | l7(3) | l7(2) | l7(1) | l7(0) |
| luma_coef_8 | R/W | 90 | l8(7) | l8(6) | l8(5) | l8(4) | l8(3) | l8(2) | l8(1) | l8(0) |
| luma_coef_9 | R/W | 91 | l9(7) | l9(6) | l9(5) | l9(4) | l9(3) | l9(2) | l9(1) | l9(0) |
| configuration11 | R/W | 93 | [0] | [0] | [1] | [0] | xxx | main_if_del | xxx | xxx |
| configuration12 | R/W | 94 | [0] | [0] | [0] | [0] | [0] | ennotch | [0] | xxx |
| configuration13 | R/W | 95 | [0] | [0] | dac12_conf | [0] | [0] | [0] | [0] | [1] |
| hue_control | R/W | 105 | hue_cont(7) | hue_cont(6) | hue_cont(5) | hue_cont(4) | hue_cont(3) | hue_cont(2) | hue_cont(1) | hue_cont(0) |
| dac2_mult | R/W | 106 | - | - | dac2_mult5 | dac2_mult4 | dac2_mult3 | dac2_mult2 | dac2_mult1 | dac2_mult0 |
| Chroma_delay | R/W | 108 | [0] | [0] | [0] | [0] | main_chr_del3 | main_chr_del2 | main_chr_del1 | main_chr_del0 |
| Chroma_delay_en | R/W | 109 | - | - | - | - | - | [0] | [0] | main_chr_del_en |
| **Control & power management unit registers** | | | | | | | | | | |
| Cpmu_conf0 | R/W | 128 | - | - | - | - | - | - | - | standby |
| Cpmu_conf1 | R/W | 129 | - | - | - | - | - | - | - | cpmuswrst |
| Dac1ctrl | R/W | 130 | - | - | - | - | - | poff1 | notzero-d1 | pedestalOnd1 |
| Dac2ctrl | R/W | 131 | - | - | - | - | - | poff2 | notzerod2 | pedestalOnd2 |
| Plugdet | R | 132 | - | - | - | - | - | - | - | loadD |
| I_test0 | R/W | 133 | - | - | - | - | - | - | - | - |

## 5.2 Description

(*) = DEFAULT mode when not_reset pin is active (LOW level)

**Caution:** All binary values quoted should be understood as MSB.....LSB

### 5.2.1 DENC registers

**REGISTER 0 configuration0 Address: 0x0000 Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | std1 | std0 | sync2 | sync1 | sync0 | polh | polv | freerun |
| **default** | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

**Table 3. std1, std0**

| | std1 | std0 | Standard selected |
|---|---|---|---|
| | 0 | 0 | PAL BDGHI |
| | 0 | 1 | PAL N (see bit set-up) |
| (*) | 1 | 0 | NTSC M(1) |
| | 1 | 1 | PAL M |

1. Standard on hardware reset is NTSC; any standard modification selects automatically the right parameters for correct subcarrier generation.

**Table 4. sync2, sync1, sync0**

| | sync2 | sync1 | sync0 | Configuration |
|---|---|---|---|---|
| | 0 | 0 | 0 | ODDEV-only based SLAVE mode (frame locked) |
| | 0 | 0 | 1 | 'F' based SLAVE mode (frame locked) |
| (*) | 0 | 1 | 0 | ODDEV+HSYNC based SLAVE mode (line locked) |
| | 1 | 0 | 0 | VSYNC-only based SLAVE mode (frame locked)(1) |
| | 1 | 0 | 1 | VSYNC+HSYNC based SLAVE mode (line locked) |
| | 1 | 1 | 0 | MASTER mode |
| | 1 | 1 | 1 | AUTOTEST mode (colour bar pattern) |

1. In VSYNC-only based slave mode (sync[2:0]="100"), HSYNC is nevertheless needed as an input.

**polh**: synchro: active edge of HSYNC selection (when input) or polarity of HSYNC (when output)

(*) 0 = HSYNC is a negative pulse (128 Tpix_clk wide) or falling edge is active

1 = HSYNC is a positive pulse (128 Tpix_clk wide) or rising edge is active

**polv**: synchro: active edge of ODDEV/VSYNC selection (when input)

0 = falling edge of ODDEV flags start of field1 (odd field) or VSYNC is active low

(*) 1 = rising edge of ODDEV flags start of field1 (odd field) or VSYNC is active high

**freerun**:

(*) 0 = disabled

1 = enabled

*Note: This bit is taken into account in ODDEV-only or VSYNC-only based slave modes and is irrelevant for other synchronization modes.*

**REGISTER 1 configuration1 Address: 0x0001 Type: R/W**

| **content** | blkli | flt1 | flt0 | sync_ok | coki | setup_ main | | |
|---|---|---|---|---|---|---|---|---|
| **default** | 0 | 1 | 0 | 0 | 0 | 1 | [0] | [0] |

**blkli:** Vertical Blanking Interval selection for active video lines area

(*) 0 = (‘partial blanking’) Only the following lines inside Vertical Interval are blanked

NTSC-M: lines [1; 9], [263(half); 272] (525-SMPTE)

PAL-M: lines [523; 6], [260(half); 269] (525-CCIR)

Other PAL: lines [623(half); 5], [311; 318] (625-CCIR)

1 = “full blanking” All lines inside VBI are blanked

NTSC-M: lines [1; 19], [263(half); 282] (525-SMPTE)

PAL-M: lines [523; 16], [260(half); 279] (525-CCIR)

Other PAL: ines [623(half); 22], [311; 335] (625-CCIR)

**flt[1:0]**: U/V Chroma filter bandwidth selection

**Table 5. Register 1**

| | **flt1** | **flt0** | **3dB bandwidth** | **Typical application** |
|---|---|---|---|---|
| | 0 | 0 | $f_{-3dB}$=1.1MHz | low def NTSC filter |
| | 0 | 1 | $f_{-3dB}$=1.3MHz | low def PAL filter |
| (*) | 1 | 0 | $f_{-3dB}$=1.6MHz | high def. NTSC filter (ATSC compliant) & PAL M/N (ITU-R 624.4 compliant) |
| | 1 | 1 | $f_{-3dB}$=1.9MHz | high def. PAL filter: Rec 624 - 4 for PAL BDG/I compliant. |

**sync_ok**: availability of sync signals (analog and digital) in case of input synchronization loss with no free-run active (i.e. freerun=0)

(*) 0 = no synchro output signals

1 = output synchro signals available on YS, CVBS and, when applicable, HSYNC (if output port), ODDEV (if output port): i.e same behavior as free-run except that video outputs are blanked in the active portion of the line.

**coki**: colour killer

(*) 0 = color ON

1 = color suppressed on CVBS output signal (CVBS=YS) but colour still present on C output. For color suppression on chroma DAC ‘C’, see register 5 bit bkdac2.

**setup_main**: pedestal

0 = Blanking level and black level are identical on all lines.
(e.g.: Argentinian PAL-N, Japan NTSC-M, PAL-BDGHI)

(*) 1 = Black level is 7.5 IRE above blanking level on all lines outside VBI
(e.g. Paraguayan and Uruguayan PAL-N).

In all cases, gain factor is adjusted to obtain the required levels for chrominance.

*Note: Depending on the different output configurations chosen by programming bit from dac12_conf, pedestal is automatically selected on it.*

**REGISTER 2 configuration2 Address: 0x0002 Type: R/W**

| **content** | nintrl | enrst | bursten | xxx | selrst | rstosc_buf | valrst1 | valrst0 |
|---|---|---|---|---|---|---|---|---|
| **default** | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

**nintrl**: non-interlaced mode select

(*) 0 = interlaced mode (625/50 or 525/60 system)

1 = non-interlaced mode(2x312/50 or 2x262/60 system)

**enrst**: cyclic update of DDFS phase

(*) 0 = no cyclic subcarrier phase reset

1 = cyclic subcarrier phase reset depending of valrst1 and valrst0 (see below)

**bursten**: chrominance burst control

0 = burst is turned off on CVBS, chrominance output is not affected

(*) 1 = burst is enabled

**selrst**: selects set of reset values for Direct Digital Frequency Synthesizer accumulator

(*) 0 = hardware reset values for phase of subcarrier oscillator (see description of registers 13 and14 for values)

1 = loaded reset values selected (see contents of registers 13 and 14)

**rstosc_buf**: software phase reset of DDFS (Direct Digital Frequency Synthesizer) buffer

(*) 0

1 = when a 0-to-1 transition occurs either the hard-wired default phase value or the value loaded in Reg. 13-14 (according to bit ‘selrst’) is put to the phase buffer. This value is then loaded into accumulator (phase of sub-carrier) when the bits ‘ph_rst_mode’ from register 8 are programmed or when standard changes or when a soft reset occur.

*Note: Bit ‘rstosc_buf’ is automatically set back to ‘0’ after the buffer is loaded.*

**valrst [1:0]**

*Note: valrst[1:0] is taken into account only if bit ‘enrst’ is set.*

**Table 6. valrst1 and valrst0 selection**

| | valrst1 | valrst0 | selection |
|---|---|---|---|
| (*) | 0 | 0 | Automatic reset of the oscillator every line |
| | 0 | 1 | Automatic reset of the oscillator every 2nd field |
| | 1 | 0 | Automatic reset of the oscillator every 4th field |
| | 1 | 1 | Automatic reset of the oscillator every 8th field |

Resetting the oscillator means forcing the value of the phase accumulator to its nominal value to avoid accumulating errors due to the finite number of bits used internally. The value at which the accumulator is reset is either the hard-wired default phase value or the value loaded in Reg. 13-14 (according to bit 'selrst') at which a $0^0$, $90^0$, $180^0$, or $270^0$ correction is applied according to the field and line at which the reset is performed.

**REGISTER 3 configuration3 Address: 0x0003 Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | main_ entrap | trap_4.43 | | | main_del_ en | val_422_ ck_ mux | xxx | |
| **default** | 0 | 0 | [0] | [0] | 0 | 0 | 0 | [0] |

**main_entrap**: enable trap filter

(*) 0 = trap filter disabled

1 = trap filter enabled

**trap_4.43**: trap filter centered frequency value selection

(*) 0 = trap filter centered around 3.58 MHz

1 = trap filter centered around 4.43 MHz

*Note: 'trap_4.43' is taken into account only if bit 'main_entrap' is set.*

**main_del_en**: Enable chroma to luma delay programming on cvbs output:

(*) 0 = disabled (DENC automatically set this delay)

1 = enabled (chroma to luma delay is programmed by del(3:0) bits from register 81.

*Note: This delay affects only the cvbs output. The component outputs Y/C remain unaffected. Refer to register 109 to program chroma to luma delay on Y/C output.*

**val_422_ck_mux:** should be programmed to "0" only.

**REGISTER 4** **configuration4** **Address: 0x0004** **Type: R/W**

| **content** | syncin_ ad1 | syncin_ ad0 | syncout_ ad1 | syncout_ ad0 | aline | hue_en | xxx | xxx |
|---|---|---|---|---|---|---|---|---|
| **default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**syncin_ad[1:0]**: Adjustment of incoming sync signals.
Used to insure correct interpretation of incoming video samples as Y, Cr or Cb when the encoder is slaved to incoming sync signals (inc. ‘F/H’ flags stripped off ITU-R656/D1 data).

**Table 7. syncin_ad[1:0]**

| | **syncin_ad1** | **syncin_ad0** | **Internal delay undergone by incoming sync** |
|---|---|---|---|
| (*) | 0 | 0 | nominal* |
| | 0 | 1 | +1 pix_clk |
| | 1 | 0 | +2 pix_clk |
| | 1 | 1 | +3 pix_clk |

**syncout_ad[1:0]**: Adjustment of outgoing sync signals.
Used to ensure correct interpretation of incoming video samples as Y, Cr or Cb when the encoder is master and supplies sync signals.

**Table 8. syncout_ad[1:0]**

| | **syncout_ad1** | **syncout_ad0** | **Delay added to sync signals before they are output** |
|---|---|---|---|
| (*) | 0 | 0 | nominal* |
| | 0 | 1 | +1 pix_clk |
| | 1 | 0 | +2 pix_clk |
| | 1 | 1 | +3 pix_clk |

**aline**: video active line duration control

(*) 0 = Full digital video line encoding (720 pixels - 1440 clock cycles)

1 = Active line duration follows ITU-R/SMPTE ‘analog’ standard requirements

**hue_en**: Enables variance in phase of the subcarrier, as programmed in register_105, during active video with respect to the phase of the subcarrier during the color burst. Once set, this bit is automatically reset to ‘0’.

(*) 0 = Disabled

1 = Enabled

**REGISTER 5 configuration5 Address: 0x0005 Type: R/W**

| content | selrst_ inc | bkdac1 | bkdac2 | | | | | dacinv |
|---|---|---|---|---|---|---|---|---|
| default | 0 | 0 | 0 | [0] | [0] | [0] | [0] | 0 |

**selrst_inc**: Choice of Digital Frequency Synthesizer increment after soft reset or when ph_rst_mode = '01' . See Register 8.

(*) 0 = hard wired value (depending on TV standard)

1 = soft (value from registers 10 to 12)

**bkdacN**: blanking of DACs (N = 1 or 2)

(*) 0 = DAC N in normal operation

1 = DAC N input code forced to black level for C output or blanking level for Y or CVBS output depending of dac12_conf bit of configuration13 register.

**dacinv**: 'Inverts' DAC codes to compensate for an inverting output stage in the application

(*) 0 = non inverted DAC inputs (outputs)

1 = inverted DAC inputs (outputs)

**REGISTER 6 configuration6 Address: 0x0006 Type: R/W**

| content | softreset | jump | dec_ninc | free_ jump | cfc1 | cfc0 | | maxdyn |
|---|---|---|---|---|---|---|---|---|
| default | 0 | 0 | 0 | 1 | 0 | 0 | [0] | 0 |

**softreset**: software reset

(*) 0 = no reset

1 = software reset

*Note: Bit 'softreset' is automatically reset after internal reset generation. Software reset is active during 4 PIX_CLK periods. When softreset is activated, all the device is reset as with hardware reset except for the first nine user registers (registers 0 to 8: configurations).Registers 10 up to 14 (increment and phase of oscillator), 25-30, 31-33 and 39-42 are never reset (hard/soft).*

**Table 9. jump, dec_ninc, free_jump**

| | jump | dec_ninc | free_jump | update mode |
|---|---|---|---|---|
| | 0 | 0 | 0 | Normal mode (no line skip/insert capability)<br>ITU-R (CCIR): 313/312 or 263/262<br>non-interlaced: 312/312 or 262/262 |
| (*) | 0 | x | 1 | Manual mode for line insert ("dec_ninc"=0) or skip ("dec_ninc"=1) capability.<br>Both fields of all the frames following the writing of this value are modified according to "lref" and "ltar" bits of registers 21-22-23 (by default, "lref"=0 and "ltar"=1 which leads to normal mode above). |

**Table 9. jump, dec_ninc, free_jump**

| | jump | dec_ninc | free_jump | update mode |
|---|---|---|---|---|
| | 1 | 0 | 0 | Automatic line insert mode.<br>The 2nd field of the frame following the writing of this value is increased. Line insertion is done after line 245 in 525/60 and after line 290 in 625/50.<br>“lref” and “ltar” are ignored.(1) |
| | 1 | 1 | 0 | Automatic line skip mode.<br>The 2nd field of the frame following the writing of this value is decreased. Line suppression is done after line 245 in 525/60 and after line 290 in 625/50.<br>“lref” and “ltar” are ignored.(1) |
| | 1 | x | 1 | Not to be used. |

1. Two lines are skipped (inserted) in 525/60 and four lines in 625/50 standards

*Note: bit “jump” is automatically reset after use.*

**Table 10. cfc[1:0]: colour frequency control via CFC line**

| | cfc1 | cfc0 | update mode |
|---|---|---|---|
| (*) | 0 | 0 | disabled (update is done by loading of registers 10,11 and12) |
| | 0 | 1 | update of increment for DDFS just after serial loading via CFC |
| | 1 | 0 | update of increment for DDFS on next active edge of HSYNC |
| | 1 | 1 | update of increment for DDFS just before next color burst |

**maxdyn**: max dynamic magnitude allowed on YCrCb inputs for encoding.

(*) 0 = 10hex to EBhex for Y, 10hex to F0hex for chrominance (Cr,Cb)

1= 01hex to FEhex for Y, Cr and Cb

*Note: In any case, EAV and SAV words are replaced by blanking values before being fed to the luminance and Chrominance processing.*

**REGISTER 7 configuration7 Address: 0x0007 Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | | | | xxx | | bypass_sync_corr | | |
| **default** | [0] | [0] | [0] | 0 | [0] | 0 | [0] | [0] |

**bypass_sync_corr**: tst_dac bypass mode with sync correction. This is a test mode in which data coming from port tst_dac can be output with or without sync correction and given to the dacs.

(*) 0 = There is no sync correction applicable to the data coming from tst_dac.

1 = Sync correction takes place before setting the dacs provided tst_ana(0) is set to ‘1’. Please note that in this case only 8 MSBs are used to generate a 10-bit sync corrected output from the filter.

**REGISTER 8** **configuration8** **Address: 0x0008** **Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | ph_rst_mode1 | ph_rst_mode0 | xxx | val_422_mux | blk_all | xxx | xxx | xxx |
| **default** | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

**Table 11. ph_rst_mode[1:0]:sub-carrier phase reset**

| | **ph_rst_mode1** | **ph_rst_mode0** | **update mode** |
|---|---|---|---|
| (*) | 0 | 0 | disabled |
| | 0 | 1 | enabled - phase is updated with value from phase buffer register (see Reg2 bit rstosc_buf) at the beginning of the next video line. In the mean time, the increment is updated with hard or soft values depending on selreg_inc value (see Register 5) |
| | 1 | 0 | enabled - phase is updated with values from Registers 10 and 11, based on the next increment update from cfc (depending on cfc loading moment and Register6 cfc(1:0) bits. |
| | 1 | 1 | enabled - phase is reset following the detection of rst bit on cfc line, up to 9 pix_clk after loading of cfc's LSB. |

*Note: Bits 'ph_rst_mode(1:0)' are automatically set back to '00' following the oscillator reset in modes '01' and '10'.*

**val_422_mux: should be programmed to "1" only after each reset.**

**blk_all**: blanking of all video lines

(*) 0 = disabled

1 = enabled

(all inputs are ignored - 80hex instead of Cr and Cb and 10hex instead of Y and Y4)

**REGISTER 9** **Address: 0x0009** **Type: Read only**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | hok | atfr | | | fieldct2 | fieldct1 | fieldct0 | jump |

(*) = DEFAULT mode when not_reset pin is active (LOW level)

**hok**: Hamming decoding of frame sync flag embedded within ITU-R656 / D1 compliant YCrCb streams

0 = Consecutive errors

(*) 1 = A single or no error

*Note: Signal quality detector is issued from Hamming decoding of EAV, SAV from YcrCb*

**atfr**: Frame synchronization flag

(*) 0 = encoder not synchronized

1 = in slave mode: encoder synchronized

**fieldct[2:0]**: Digital field identification number

000 = indicates field 1

...

111 = indicates field 8

fieldct[0] also represents the odd/even information (odd='0', even='1')

**jump**: indicates whether a frame length modification has been programmed at '1' from programming of bit' jump' to end of frame(s) concerned.

(*)default = 0

Refer to register 6 and registers 21-22-23

**REGISTERS 10, 11, 12 Increment_dfs** **Address: 0x000A to 0x000C** **Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **register_10** | d23 | d22 | d21 | d20 | d19 | d18 | d17 | d16 |
| **register_11** | d15 | d14 | d13 | d12 | d11 | d10 | d9 | d8 |
| **register_12** | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |

These registers contain the 24-bit increment used by the DDFS if bit 'selrst_inc' equals '1' to generate the subcarrier phase i.e. the address that is supplied to the sine ROM. It therefore allows to customize the subcarrier synthesized frequency.

1 LSB ~ 1.609325 Hz

The procedure to validate the usage of these registers rather than the hard-wired values is the following:

- Load the registers with the required value

- Set bit 'selrst_inc' to 1 (Reg 5)

- Perform a software reset (Reg 6)

*Note: 1 The values loaded in Reg10-12 are taken into account after a software reset, and ONLY IF bit 'selrst_inc'='1' (Reg. 5).*

*2 These registers are never reset and must be explicitly written into to contain sensible information.*

*3 On hardware or on software reset with selrst_inc='0', the DDFS is initialized with a hardwired increment, independent of Registers 10-12. These hardwired values being out of any user register cannot be read.*
*These values are:*

| **Value** | **Frequency synthesized** |
|---|---|
| d(23:0): 21F07C hexa for NTSC M | f=3.5795452 MHz |
| d(23:0): 2A098B hexa for PAL B,G,H,I,N | f=*4.43361875MHz* |
| d(23:0): 21F694 hexa for PAL N | f=3.5820558 MHz |
| d(23:0): 21E6F0 hexa for PAL M | *f=3.57561149 MHz* |

**REGISTERS 13, 14** **Phase_dfs** **Address: 0x000D to 0x000E** **Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **register_13** | xxx | xxx | xxx | xxx | xxx | xxx | o23 | o22 |
| **register_14** | o21 | o20 | o19 | o18 | o17 | o16 | o15 | o14 |

**Static phase offset for digital frequency synthesizer (10 bits only)**

Under certain circumstances (detailed below), these registers contain the 10 MSBs of the value with which the phase accumulator of the DDFS is initialized after a 0-to-1 transition of bit 'rstosc_buf' of Reg 2, or after a standard change, or when cyclic phase readjustment has been programmed (see bits valrst[1:0] of Reg 2). The 14 remaining LSBs loaded into the accumulator in these cases are all '0's (this allows to define the phase reset value with a $0.35^{o}$ accuracy).

The procedure to validate the usage of these registers rather than the hard-wired values is the following:

- Load the registers with the required value

- Set bit 'selrst' to 1 (Reg 2)

- Perform a software reset or set 'rstosc_buf' to 1 (Reg 2) (to put soft phase value into a tampon register) and ph_rst_mode[1:0]

*Note: 1 Registers 13-14 are never reset and must be explicitly written into to contain sensible information.*

*2 If bit 'selrst'=0 (e.g. after a hardware reset) the phase offset used every time the DDFS is re initialized is a hard-wired value. The hard-wired values being out of any register, they cannot be read out.*

*Reset values:*

*D9C000hex for PAL BDGHI, N, M,*

*1FC000hex for NTSC-M,*

*000000hex (blue lines)*

**REGISTER 17** **dac1 multiplying factors** **Address: 0x0011** **Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | dac1_mult5 | dac1_mult4 | dac1_mult3 | dac1_mult2 | dac1_mult1 | dac1_mult0 | | |
| **default** | 1 | 0 | 0 | 0 | 0 | 0 | [1] | [0] |

**dac1_mult[5:0]:** multiplying factor on dac1_y digital signal before the D/A converters with 0.78% step.

**Table 12. dac1_mult[5:0]: multiplying factor on dac1_y digital signal**

| | dac1_mult[5:0] | | | | | | |
|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 | 0 | 75.00% |
| | 0 | 0 | 0 | 0 | 0 | 1 | 75.78% |
| | 0 | 0 | 0 | 0 | 1 | 0 | 76.56% |
| | 0 | 0 | 0 | 0 | 1 | 1 | 77.34% |
| | ... | ... | ... | ... | | | ... |
| (*) | 1 | 0 | 0 | 0 | 0 | 0 | 100% |
| | ... | ... | ... | ... | | | ... |
| | 1 | 1 | 1 | 1 | 1 | 1 | 124.22% |

**REGISTERS 21, 22, 23**
**clig_i_reg = ltarg[8:0] and lref[8:0]** **Address: 0x0015 to 0x0017** **Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **register 21** | ltarg8 | ltarg7 | ltarg6 | ltarg5 | ltarg4 | ltarg3 | ltarg2 | ltarg1 |
| **register 22** | ltarg0 | lref8 | lref7 | lref6 | lref5 | lref4 | lref3 | lref2 |
| **register 23** | lref1 | lref0 | - | - | - | - | - | - |

These registers may be used to jump from a reference line (end of that line) to a target line of the SAME FIELD. However, not all lines can be skipped or repeated with no problems and, if needed, this functionality should BE USED WITH CAUTION.

lref[8:0] contains, in binary format, the reference line from which a jump is required. ltarg[8:0] contains the target line as a binary number.

Default values: lref[8:0]:= 000000000 and ltarg[8:0]:= 000000001.

**REGISTER 65** **C_mult&ttxs** **Address: 0x0041** **Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | c_mult3 | c_mult2 | c_mult1 | c_mult0 | | xxx | | bcs_en_main |
| **default** | 0 | 0 | 0 | 0 | [0] | 0 | [0] | 1 |

**c_mult[3:0]**: multiplying factor of C digital output (before D/A convertors) and of color part of CVBS signal.

**Table 13. c_mult[3:0]: multiplying factor of C digital output**

| | c_mult3 | c_mult2 | c_mult1 | c_mult0 | factor value (c_mult) |
|---|---|---|---|---|---|
| (*) | 0 | 0 | 0 | 0 | 1.000000 (1.000000 Dec.) |
| | 0 | 0 | 0 | 1 | 1.000001 (1.015625 Dec.) |
| | 0 | 0 | 1 | 0 | 1.000010 (1.031250 Dec.) |
| | 0 | 0 | 1 | 1 | 1.000011 (1.046875 Dec.) |
| | ... | ... | ... | ... | ... |
| | 1 | 1 | 1 | 1 | 1.001111 (1.234375 Dec.) |

**bcs_en_main**: Brightness, Contrast and Saturation control by Registers 69 to 71 on 4:4:4 video input

0 = disable

(*) 1 = enable

**REGISTER 69** **Brightness** **Address: 0x0045** **Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| **default** | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

To adjust the luminance intensity of the display video image, the following formula is used:

$Y_{out} = Y_{in} + b - 128$

$Y_{in}$ is the 8-bit input luminance

$Y_{out}$ is the result of 'Brightness' operation (still on 8 bits)

This value is saturated at 235 (16) or 254 (1) according to register6 bit 'maxdyn',

b: brightness (unsigned value with center at 128, default 128)

**REGISTER 70 Contrast Address: 0x0046 Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | c7 | c6 | c5 | c4 | c3 | c2 | c1 | c0 |
| **default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Adjustment of the relative difference between high and low intensity luminance values of the displayed image is made according to the following formula:

$$Yout = \frac{(Yin-128)(c+128)}{128} + 128$$

$Y_{in}$ is the 8-bit input luminance,

$Y_{out}$ is the result of 'Contrast' operation (still on 8 bits)

This value is saturated at 235 (16) or 254 (1) according to register6 bit 'maxdyn',

c: contrast (2's complement value from -128 to 127, default 0)

**REGISTER 71 Saturation Address: 0x0047 Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | s7 | s6 | s5 | s4 | s3 | s2 | s1 | s0 |
| **default** | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

To adjust the colour intensity of the displayed video image, the following formula is used:

$$Cbout = \frac{s(Cbin-128)}{128} + 128$$

$$Crout = \frac{s(Crin-128)}{128} + 128$$

$Cr_{in}$,$Cb_{in}$ 8-bit input chroma,

$Cr_{out}$, $Cb_{out}$ the result of 'Saturation' operation (still on 8 bits)

This value is saturated at 240 (16) or 254 (1) according to bit 'maxdyn' (Reg 6),

s: saturation value (unsigned value with centre at 128, default 128)

**REGISTERS 72 to 80**
**Chroma filter coefficients**

**Address:**
**0x0048 to 0x0050**

**Type: R/W**

**Table 14. Chroma main_coef_[8:0]**

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| chroma_main_coef_0 | reg_72 | main_flt_s | main_plg_div1 | main_plg_div0 | coef0(4) | coef0(3) | coef0(2) | coef0(1) | coef0(0) |
| chroma_main_coef_1 | reg_73 | xxx | coef8(8) | coef1(5) | coef1(4) | coef1(3) | coef1(2) | coef1(1) | coef1(0) |
| chroma_main_coef_2 | reg_74 | xxx | coef2(6) | coef2(5) | coef2(4) | coef2(3) | coef2(2) | coef2(1) | coef2(0) |
| chroma_main_coef_3 | reg_75 | xxx | coef3(6) | coef3(5) | coef3(4) | coef3(3) | coef3(2) | coef3(1) | coef3(0) |
| chroma_main_coef_4 | reg_76 | coef4(7) | coef4(6) | coef4(5) | coef4(4) | coef4(3) | coef4(2) | coef4(1) | coef4(0) |
| chroma_main_coef_5 | reg_77 | coef5(7) | coef5(6) | coef5(5) | coef5(4) | coef5(3) | coef5(2) | coef5(1) | coef5(0) |
| chroma_main_coef_6 | reg_78 | coef6(7) | coef6(6) | coef6(5) | coef6(4) | coef6(3) | coef6(2) | coef6(1) | coef6(0) |
| chroma_main_coef_7 | reg_79 | coef7(7) | coef7(6) | coef7(5) | coef7(4) | coef7(3) | coef7(2) | coef7(1) | coef7(0) |
| chroma_main_coef_8 | reg_80 | coef8(7) | coef8(6) | coef8(5) | coef8(4) | coef8(3) | coef8(2) | coef8(1) | coef8(0) |

Values from these registers are used only when bit main_flt_s (Reg 72) is set to 1. Bit main_flt_s has the highest priority over the rest. With main_flt_s bit set to 1, all bits from main_plg_div[1:0] need to be programmed to the chroma coefficients. Alternatively, the coefficients default values are loaded depending on the selected mode or the selected filter type in a particular mode with flt(1:0) bits from register 1.

The values are soft loaded when main_flt_s = 1. The value to be loaded in the register should be the actual coefficient value + an offset. The hardware will internally subtract this offset to get the actual coefficient value.

**main_flt-s** default value: 0

The main_plg_div value is chosen according to the sum of all the coefficients.

**main_plg_div** = 11 when sum of coeffs = 4096

**main_plg_div** = 10 when sum of coeffs = 2048

**main_plg_div** = 01 when sum of coeffs = 1024, (default)

**main_plg_div** = 00 when sum of coeffs = 512

Offset change before loading to user register:

**chroma_main_coef0** = Actual value + 16;

**chroma_main_coef1** = Actual value + 32;

**chroma_main_coef2** = Actual value + 64;

**chroma_main_coef3** = Actual value + 32;

**chroma_main_coef4** = Actual value + 32;

**chroma_main_coef5** = Actual value + 32;

**chroma_main_coef6** = Actual value

**chroma_main_coef7** = Actual value

**chroma_main_coef8** = Actual value

Default values:

**chroma_main_coef0[4:0]** = 10001 means c0 = 1.

**chroma_main_coef1[5:0]** = 100111 means c1 = 7;

**chroma_main_coef2[6:0]** = 1010100 means c2= 20;

**chroma_main_coef3[6:0]** = 1000111 means c3 = 39;

**chroma_main_coef4[7:0]** = 01011111 means c4 = 63;

**chroma_main_coef5[7:0]** = 01110111 means c5 = 87;

**chroma_main_coef6[7:0]** = 01101100 means c6 = 108;

**chroma_main_coef7[7:0]** = 01111011 means c7 = 123;

**chroma_main_coef8[8:0]** = 010000000 means c8 = 128.

The FIR symmetrical filter has the following response:

$$H(z) = c_0 + c_1 z^{-1} + c_2 z^{-2} + \quad + c_7 z^{-7} + c_8 z^{-8} + c_7 z^{-9} + \quad + c_2 z^{-14} + c_1 z^{-15} + c_0 z^{-16}$$

The filter working frequency is comprised in the range [pix_clk, 27 MHz] and the filtering is done on upsampled signal (half pix_clk to pix_clk frequency by padding by zeros).

**REGISTER 81** **Configuration 9** **Address: 0x0051** **Type: R/W**

| content | main_del3 | main_del2 | main_del1 | main_del0 | xxx | plg_div_y1 | plg_div_y0 | flt_ys |
|---|---|---|---|---|---|---|---|---|
| default | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |

**main_del[3:0]**: delay on chroma path with reference to luma path, on the encoded signal coming from the main outputs. The delay value varies with modes, delays are hardwired to have different delays in different modes. If the delays are to be made programmable, set bit main_del_en to 1 (Reg 03) to enable soft delay from main_del[3:0].

**Table 15. main_del[3:0]**

| | main_del3 | main_del2 | main_del1 | main_del0 | Delay on chroma path with reference to luma path encoding [One pixel corresponds to 2/$f_{pix_clk}$] |
|---|---|---|---|---|---|
| (*) | 0 | 0 | 1 | 0 | - 0.5 pixel delay on chroma |
| | 0 | 0 | 1 | 1 | - 1 pixel delay on chroma |
| | 0 | 1 | 0 | 0 | - 1.5 pixel delay on chroma |
| | 0 | 1 | 0 | 1 | - 2 pixel delay on chroma |
| | 1 | 1 | 0 | 0 | + 2.5 pixel delay on chroma |
| | 1 | 1 | 0 | 1 | + 2 pixel delay on chroma |
| | 1 | 1 | 1 | 0 | + 1.5 pixel delay on chroma |
| | 1 | 1 | 1 | 1 | + 1 pixel delay on chroma |
| | Others | | | 1 | 0 pixel delay on chroma (**reference delay**) |
| | Others | | | 0 | + 0.5 pixel delay on chroma |

If main_del_en = 0 then the delays used are:

**main_del**[3:0] = 0010 when mode = PAL/NTSC in 4:2:2 format on CVBS

**main_del**[3:0] = 0001 when mode = PAL/NTSC in 4:4:4.

**plg_div_y** = 00 when sum of coefficients = 256

**plg_div_y** = 01 when sum of coefficients = 512 (default)

**plg_div_y** = 10 when sum of coefficients = 1024

**plg_div_y** = 11 when sum of coefficients = 2048

Bit flt_ys enables the software loading capability of luma coefficients. Values from registers 82 to 91 are used only when bit “flt_ys” of this register is set to 1. Bit “flt_ys” has the highest priority. With this bit set to 1, all bits from plg_div_y[1:0] must be programmed as luma coefficients. Alternatively, the default values of the coefficients are loaded. The luma coefficients are mode and standard independent.

**flt_ys** default value is “0”.

**REGISTERS 82 to 91:** **luma filter coefficients** **Address: 0x0052 to 0x005B** **Type: R/W**

**Table 16. Luma_coef_[0:9]**

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **luma_coef_0** | reg_82 | xxx | xxx | l8(8) | l0(4) | l0(3) | l0(2) | l0(1) | l0(0) |
| **luma_coef_1** | reg_83 | l9(9) | l9(8) | l1(5) | l1(4) | l1(3) | l1(2) | l1(1) | l1(0) |
| **luma_coef_2** | reg_84 | l6(8) | l2(6) | l2(5) | l2(4) | l2(3) | l2(2) | l2(1) | l2(0) |
| **luma_coef_3** | reg_85 | l7(8) | l3(6) | l3(5) | l3(4) | l3(3) | l3(2) | l3(1) | l3(0) |
| **luma_coef_4** | reg_86 | l4(7) | l4(6) | l4(5) | l4(4) | l4(3) | l4(2) | l4(1) | l4(0) |
| **luma_coef_5** | reg_87 | l5(7) | l5(6) | l5(5) | l5(4) | l5(3) | l5(2) | l5(1) | l5(0) |
| **luma_coef_6** | reg_88 | l6(7) | l6(6) | l6(5) | l6(4) | l6(3) | l6(2) | l6(1) | l6(0) |
| **luma_coef_7** | reg_89 | l7(7) | l7(6) | l7(5) | l7(4) | l7(3) | l7(2) | l7(1) | l7(0) |
| **luma_coef_8** | reg_90 | l8(7) | l8(6) | l8(5) | l8(4) | l8(3) | l8(2) | l8(1) | l8(0) |
| **luma_coef_9** | reg_91 | l9(7) | l9(6) | l9(5) | l9(4) | l9(3) | l9(2) | l9(1) | l9(0) |

Values from these registers are used only when bit flt_ys of register 81 is set to 1.

The coefficient values of luma_coef_0 to luma_coef_7 should be entered as 2's complement, and the rest as normal positive values. The hardware will internally generate normal positive values. Default values:

**$a_0$ = luma_coef_0[4:0]** = 00001 means +1;

**$a_1$ = luma_coef_1[5:0]** = 111111 means -1;

**$a_2$ = luma_coef_2[6:0]** = 1110111 means -9;

**$a_3$ = luma_coef_3[6:0]** = 0000011 means +3;

**$a_4$ = luma_coef_4[7:0]** = 00011111 means +31;

**$a_5$ = luma_coef_5[7:0]** = 11111011 means -5;

**$a_6$ = luma_coef_6[8:0]** = 110101100 means -84;

**$a_7$ = luma_coef_7[8:0]** = 000000111 means +7;

**$a_8$ = luma_coef_8[8:0]** = 100111101 means +317;

**$a_9$ = luma_coef_9[9:0]** = 0111111000 means +504;

The FIR filter is symmetrical with the following response:

$$H(z) = a_0 + a_1 z^{-1} + a_2 z^{-2} + \quad + a_8 z^{-8} + a_9 z^{-9} + a_8 z^{-10} + \quad + a_2 z^{-16} + a_1 z^{-17} + a$$

Working frequency of this filter is the one of pix_clk (27, 24.545454 or 29.5 MHz), and the filtering is done on upsampled signal (half pix_clk to pix_clk frequency by padding by zeros).

**REGISTER 93** **Configuration 11** **Address: 0x005D** **Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | | | | | xxx | main_if_del | xxx | xxx |
| **default** | [0] | [0] | [1] | [0] | 1 | 0 | 0 | 0 |

**main_if_del:** The delay on the luma comparing to chroma in CVBS and S-VHS outputs. This delay is 5 clock cycles (27 MHz clock).

(*) 0 = enabled

1 = disabled

**REGISTER 94** **Configuration 12** **Address: 0x005E** **Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | | xxx | xxx | xxx | | ennotch | | xxx |
| **default** | [0] | 0 | 0 | 0 | [0] | 0 | [0] | 0 |

**ennotch:** Notch filtering on the cvbs output

(*) 0 = disabled

1 = enabled

**REGISTER 95** **Configuration 13** **Address: 0x005F** **Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | | | dac12_conf | | | | | |
| **default** | [0] | [0] | 0 | [0] | [0] | [0] | [0] | [1] |

**dac12_conf:** Please refer to the table below for all combinations to be observed at DACs.

**Table 17. dac12_conf**

| dac12_conf | dac1 | dac2 |
|---|---|---|
| (*)0 | C | Y |
| 1 | CVBS | |

**REGISTER 105** **Hue control** **Address: 0x0069** **Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | hue_cont (7) | hue_cont (6) | hue_cont (5) | hue_cont (4) | hue_cont (3) | hue_cont (2) | hue_cont (1) | hue_cont (0) |
| **default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Defines the phase shift in the subcarrier during active video with respect to the subcarrier phase during the color burst. Once enabled by Register_4(2) “hue_en”, phase variation would be in a range of +/- 22.324 degrees with increments of 0.17578127.

*Note: Pulse the Register_4(2) “hue_en” to make sure that a value programmed in this register is effective immediately after programming Hue_control. Once enabled, to disable any phase shift in active subcarrier wrt burst, write the default value into the Hue_control register followed by a pulse on Register_4(2) “hue_en”.*

**hue_control [6:0]**: absolute value of phase adjustment, range 1 to 127.
LSB (0x01) implies 0.17578127 degrees, 0x7F imply 22.324 degrees

**hue_control [7]**: Sign of phase

1 = +ve; (*) 0 = -ve

(*)

“00000000” : No phase shift

“10000000” : No phase shift

“11111111” : +22.324 degrees phase

“01111111” : -22.324 degrees phase

**REGISTER 106 dac2 multiplying factor Address: 0x006A Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | xxx | xxx | dac2_mult5 | dac2_mult4 | dac2_mult3 | dac2_mult2 | dac2_mult1 | dac2_mult0 |
| **default** | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

**dac2_mult(5:0)**: multiplying factor on dac2_C digital signal before the D/A converters with 0.78% step.

**Table 18. dac2_multi[5:0]**

| | **dac2_mult[5:0]** | | | | | | |
|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 | 0 | 75.00% |
| | 0 | 0 | 0 | 0 | 0 | 1 | 75.78% |
| | 0 | 0 | 0 | 0 | 1 | 0 | 76.56% |
| | 0 | 0 | 0 | 0 | 1 | 1 | 77.34% |
| | ... | ... | ... | ... | | | ... |
| (*) | 1 | 0 | 0 | 0 | 0 | 0 | 100% |
| | ... | ... | ... | ... | | | ... |
| | 1 | 1 | 1 | 1 | 1 | 1 | 124.22% |

**REGISTER 108 Chroma Delay Address: 0x006C Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | | | | | main_chr_del3 | main_chr_del2 | main_chr_del1 | main_chr_del0 |
| **default** | [0] | [0] | [0] | [0] | 0 | 0 | 1 | 0 |

**main_chr_del[3:0]**: delay on chroma path with reference to luma path on encoded component outputs. The delay value varies with modes and the delays are hardwired to have different delays in different modes. If the delays are to be made programmable make bitmain_chr_del_en = 1 (Reg 109). That way, soft delay from main_chr_del[3:0] is enabled.

**Table 19. main_chr_del[3:0]**

| | main_ chr_ del3 | main_ chr_ del2 | main_ chr_ del1 | main_ chr_ del0 | Delay on chroma path with reference to luma path encoding [One pixel corresponds to /fpix_clk] |
|---|---|---|---|---|---|
| (*) | 0 | 0 | 1 | 0 | - 0.5 pixel delay on chroma |
| | 0 | 0 | 1 | 1 | - 1 pixel delay on chroma |
| | 0 | 1 | 0 | 0 | - 1.5 pixel delay on chroma |
| | 0 | 1 | 0 | 1 | - 2 pixel delay on chroma |
| | 1 | 1 | 0 | 0 | + 2.5 pixel delay on chroma |
| | 1 | 1 | 0 | 1 | + 2 pixel delay on chroma |
| | 1 | 1 | 1 | 0 | + 1.5 pixel delay on chroma |
| | 1 | 1 | 1 | 1 | + 1 pixel delay on chroma |
| | Others | | | 1 | 0 pixel delay on chroma (**reference delay**) |
| | Others | | | 0 | + 0.5 pixel delay on chroma |

If main_chr_del_en = 0 then the delays used are:

**main_chr_del[3:0]** = 0010 when mode = PAL/NTSC in 4:2:2 format on CVBS.

**main_chr_del[3:0]** = 0001 when mode = PAL/NTSC in 4:4:4

**REGISTER 109 Chroma Delay Enable Address: 0x006D Type: R/W**

| **content** | | | | | | | | main_chr _del_en |
|---|---|---|---|---|---|---|---|---|
| **default** | - | - | - | - | - | [0] | [0] | 0 |

**main_chr_del_en**: Enable of luma to chroma delay on the 4:4:4 component outputs.

(*) 0 = disabled (DENC automatically sets this delay)

1 = enabled (chroma to luma delay is programmed by main_chr_del[3:0] bits (Reg 108).

*Note: This delay affects only the component Y/C. The cvbs output remains unaffected. Refer to register 3 to program chroma to luma delay on cvbs output signal.*

## 5.2.2 Control & power management unit registers

### Control and power management unit

**REGISTER 128 Configuration0 Address: 0x0080 Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | | | | | | | | standby |
| **default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**standby**: In this mode the analog subsystem is supplied by the 1.2 V and the 2.8 /3.3 V, but the DACs are set in power down mode, via poff[1:2] bits (Reg 130 & 131). Digital to analog data conversion is disabled.

(*) 0 = disabled (active mode)

1 = standby

### Control and power management unit reset

**REGISTER 129 Configuration 1 Address: 0x0081 Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | | | | | | | | cpmuswrst |
| **default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**cpmuswrst**: Control and power management unit reset

(*) 0 = disabled

1 = control and power management unit software reset

*Note: Bit cpmuswrst is automatically reset to its default value after internal reset generation and the I2C data transfer is stopped. This reset is kept available for a CLK cycle.*

**REGISTER 130 DAC1 control Address: 0x0082 Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | | | | | | poff1 | notzerod1 | pedestal Ond1 |
| **default** | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

**poff1**: DAC1 power off, then turn off DAC1 is in a low power consumption mode

0 = disabled (DAC1 active)

(*) 1 = turned off

*Note: As Default value is “1”, Digital processor must write “0” when going from sleep or standby to active mode.*

**notzerod1** : null digital data inputed on DAC1

0 = independently of what is coming from the digital part, “0000000000” is forced on DAC1 input.

(*) 1 = disabled, values issued from DENC are transmitted to DAC1.

**pedestalOnd1** : Black level video pedestal active on DAC1

(*) 0 = disabled

1 = video pedestal active

**REGISTER 131** **DAC2 control** **Address: 0x0083** **Type: R/W**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | | | | | | poff2 | notzerod2 | pedestal Ond2 |
| **default** | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

**poff2**: DAC2 power off, then turn off DAC2 is in a low power consumption mode.

0 = disabled (DAC2 active)

(*)1 = turned off

*Note: As Default value is "1", Digital processor must write "0" when going from sleep or standby to active mode.*

**notzerod2** : null digital data input on DAC2

0 = independently of that is coming from the digital part, "0000000000" is forced on DAC2 input.

(*)1 = disabled, values issued from DENC are transmitted to DAC2.

**pedestalOnd2**: Black level video pedestal active on DAC2

(*) 0 = disabled

1 = video pedestal active

**REGISTER 132** **Plugdet** **Address: 0x0084** **Type: R**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **content** | | | | | | | | LoadD |
| **default** | - | - | - | - | - | - | - | - |

**LoadD**: Reports Plugdet Ball status. Unless otherwise specified all voltages are referenced to GND.

0 = Plugdet ball voltage less than VIL

1 = Plugdet ball voltage higher than VIH

# 6 Bus interface

## 6.1 2 wire serial MPU control interface (I2C compatible)

STw8009/STw8019 serial MPU control interface is compliant with I2C standard and acts only as a slave device. It supports 100 kHz and 400 kHz speeds. In addition to the basic definition of the I2C standard (SDA & SCL signals), STw8009/STw8019 serial MPU interface has an additional “Add” input used to select one out of two slave addresses.

The device supports 7-bit and 10-bit addresses.

**Table 20. STw8009/STw8019 addresses**

| | 7-bit addresses | | 10-bit addresses | |
|---|---|---|---|---|
| | **Read** | **Write** | **Read** | **Write** |
| Add pin = 0 | 01000001 | 01000000 | 00001000001 | 00001000000 |
| Add pin = 1 | 01000011 | 01000010 | 00001000011 | 00001000010 |

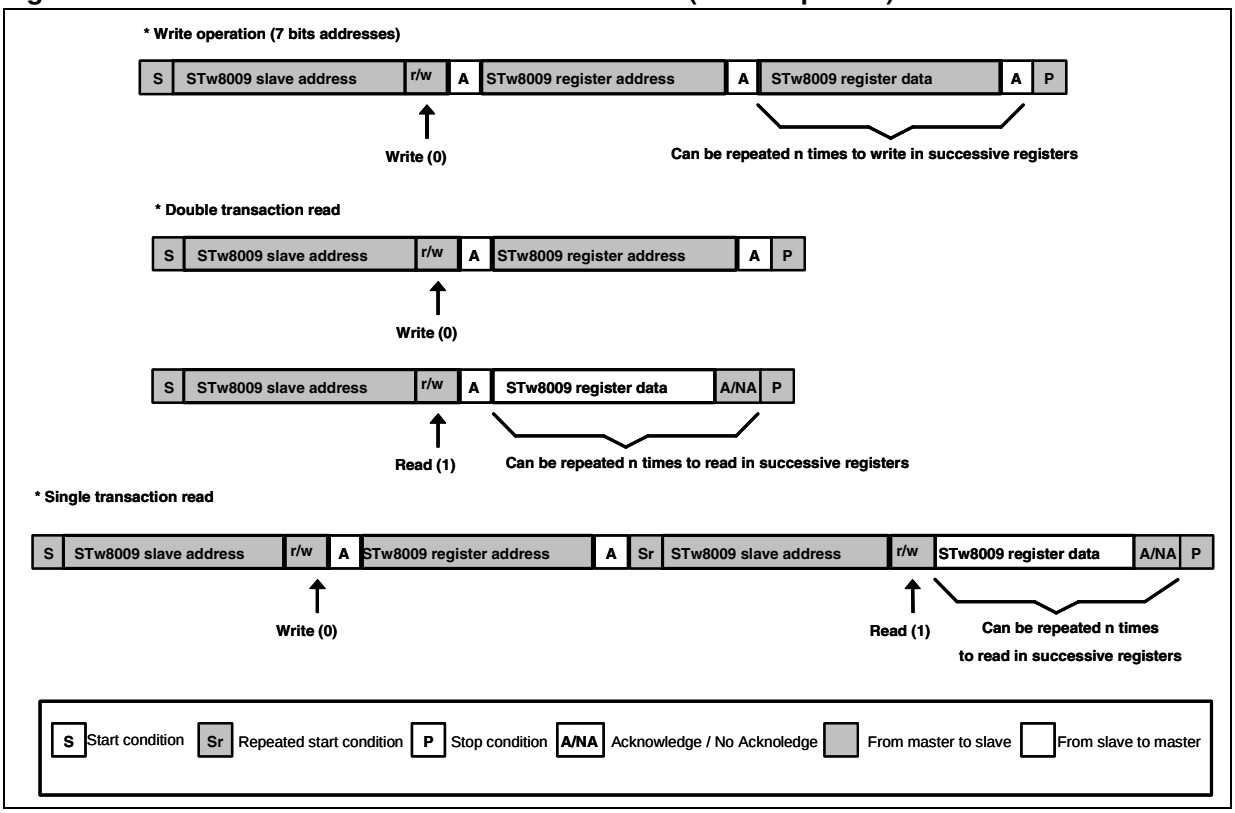
### 7-bit address mode

In Write mode, several data can be sent without re-initializing a transfer and data is written in successive registers. (*Figure 13: 2-wire serial MPU control interface format (I2C compatible) / 7-bit addresses*).

In Read mode: (*Figure 13*).

- Double transaction read: The operation is split into to transactions:
  The first one is a write that transmits the desired address. The I2C interface memorizes the address of the register.
  The second transfer is a read that can be repeated to read successive registers. After each read byte and except for the last one, the master issues an “acknowledge”. The master indicates that it is reading the last byte by issuing a “no acknowledge” instead of an “acknowledge”.
- Single transaction read:
  As opposed to the double transaction, instead of stopping the first transaction and starting the second one, the transactions are combined with a repeated start condition.

**Figure 13. 2-wire serial MPU control interface format (I2C compatible) / 7-bit addresses**




## 10 bits address mode

In Write mode, several data can be sent without re-initializing a transfer, in this case, data is written in successive registers. (*Figure 14: 2-wire serial MPU control interface format (I2C compatible) / 10-bit addresses*)

In Read mode: (*Figure 14*)

- Double transaction read:
  The operation is split into two transactions:

  The first one is a write that transmits the desired address. The I2C interface memorizes the address of the register.

  The second transfer is a read that can be repeated to read successive registers. After each read byte and except for the last one, the master issues an "acknowledge". The master indicates that it is reading the last byte by issuing a "no acknowledge" instead of an "acknowledge".

*Note: Only the higher part of the address is sent again before sending the read indication.*

- Single transaction read:
  As opposed to the double transaction, instead of stopping the first transaction and starting the second one, the transactions are combined with a repeated start condition.

**Figure 14. 2-wire serial MPU control interface format (I2C compatible) / 10-bit addresses**

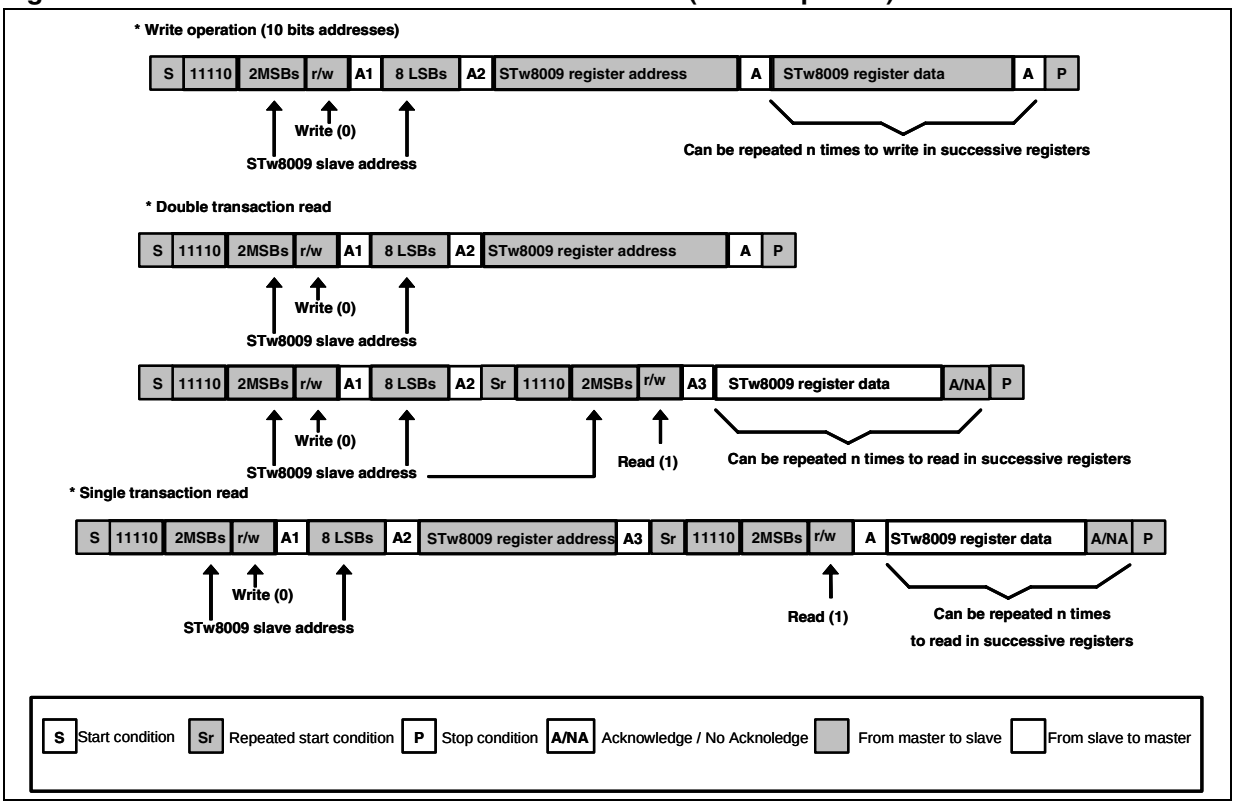
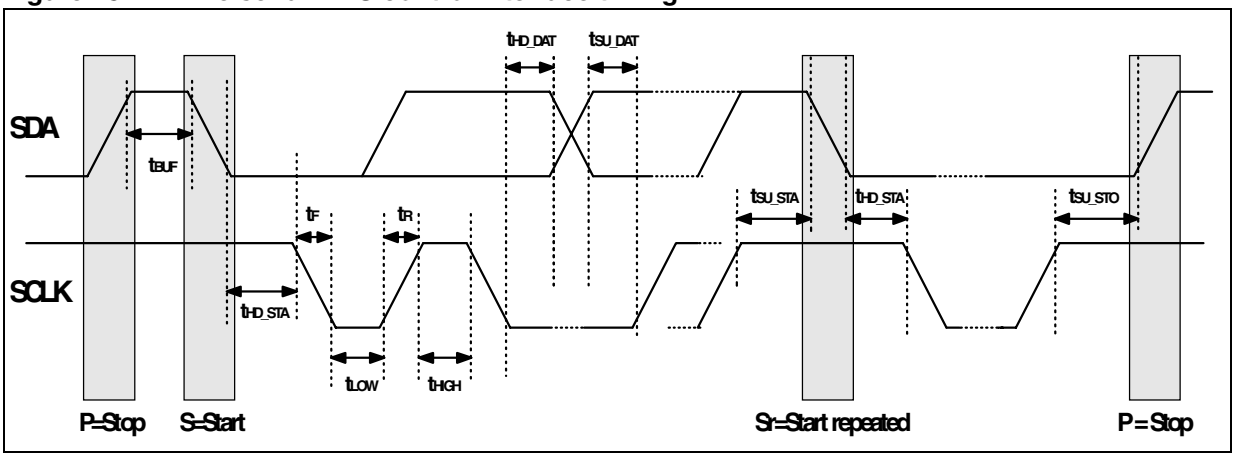
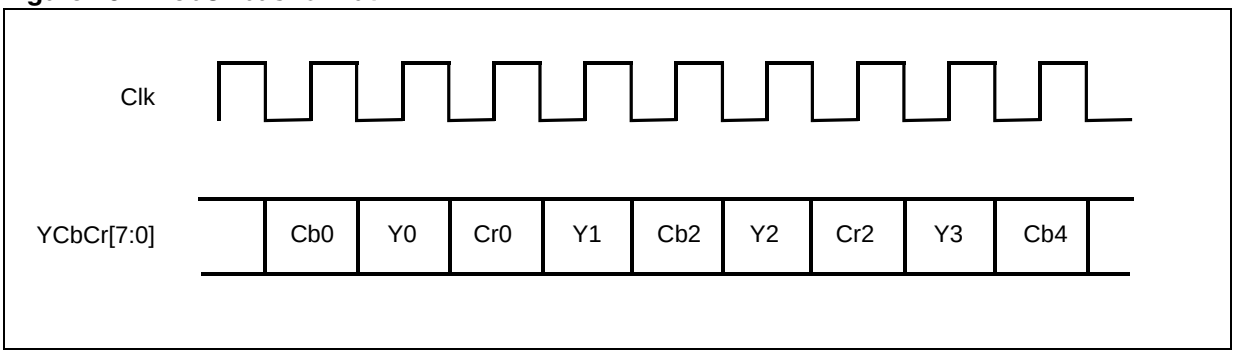



**Figure 15. 2-wire serial MPU control interface timing**



## 6.2 YcbCr bus

**Figure 16. YcbCr bus format**



# 7 Electrical characteristics

## 7.1 Absolute maximum rating

Unless otherwise specified: $T_A$=+25°C, all voltages are referenced to GND.

**Table 21. Absolute maximum ratings**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| Vdd | Digital core supply voltage | | -0.3 to +1.4 | V |
| Vdd_IO | I/O digital supply voltage | | -0.3 to +2.0 | V |
| VccA | Analog supply voltage | | -0.3 to +3.8 | V |
| VDCdig | DC input voltage on any digital pin | | -0.3 to +2.0 | V |
| VDCana | DC input voltage on any analog pin | | -0.3 to +3.8 | V |
| Pmax | Maximum power dissipation | | 700 | mW |
| $T_{stg}$ | Storage temperature range | | -40 to 125 | °C |
| Vesd | Electrostatic discharge voltage (IEC61000-4-2, level 4) | Human body model | -4 to +4 | KV |
| | | Contact discharge | -2 to +2 | KV |

## 7.2 Operating conditions

Unless otherwise specified: $T_A$=+25°C, all voltages are referenced to GND.

**Table 22. Operating conditions**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Vdd | Digital core supply voltage | 1.08 | 1.2 | 1.32 | V |
| Vdd_IO | I/O digital supply voltage | 1.65 | 1.8 | 1.95 | V |
| VccA | Analog supply voltage | 2.7 | | 3.6 | V |
| $T_A$ | Operating temperature | -30 | | +85 | °C |

## 7.3 Electrical and timing characteristics

Unless otherwise specified: $T_A$=+25°C, all voltages are referenced to GND.

**Table 23. 2 wire serial MPU control interface timing (*Figure 15*)**

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | Clock Frequency | | | | 400 | Khz |
| $t_{BUF}$ | Bus free time | | 1300 | | | ns |
| $t_{HD_STA}$ | Start condition hold time | | 600 | | | ns |
| $t_f$ | SDA & SCLK fall time | | | | 300 | ns |
| $t_{LOW}$ | SCLK pulse width low | | 1300 | | | ns |
| $t_r$ | SDA & SCLK rise time | | | | 300 | ns |
| $t_{HIGH}$ | SCLK pulse width high | | 600 | | | ns |
| $t_{HD_DAT}$ | Data input hold time | | 0 | | | ns |
| $t_{SU_DAT}$ | Data input set up time | | 250 | | | ns |
| $t_{SU_STA}$ | Start condition set up time | | 600 | | | ns |
| $t_{SU_STO}$ | Stop condition set up time | | 600 | | | ns |

**Table 24. Digital I/O interface**

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low voltage | All digital inputs | | | 0.4 | V |
| $V_{IH}$ | Input High voltage | All digital inputs | 1.3 | | | V |
| $V_{OL}$ | Output Low level | All digital outputs | | | 0.2 | V |
| $V_{OH}$ | Output High level | All digital outputs | 1.6 | | | V |
| $I_{IL}$ | Input Low current | All digital inputs / 0V < Vin < $V_{IL}$ | -10 | | 10 | µA |
| $I_{IH}$ | Input High current | All digital inputs / VCCIO < Vin < $V_{IH}$ | -10 | | 10 | µA |

**Table 25. YcbCr data bus timing**

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| FCLK | Clock Frequency | | | 27 | | MHz |
| $TCLK_{HIGH}$ | Clock pulse width high | | 15 | | | ns |
| $TCLK_{LOW}$ | Clock pulse width low | | 15 | | | ns |
| $DAT_{HD}$ | Data input hold time | | | TBD | | ns |
| $DAT_{SU}$ | Data input set up time | | | TBD | | ns |

**Table 26. Power consumption/R load = 37.5 Ω**

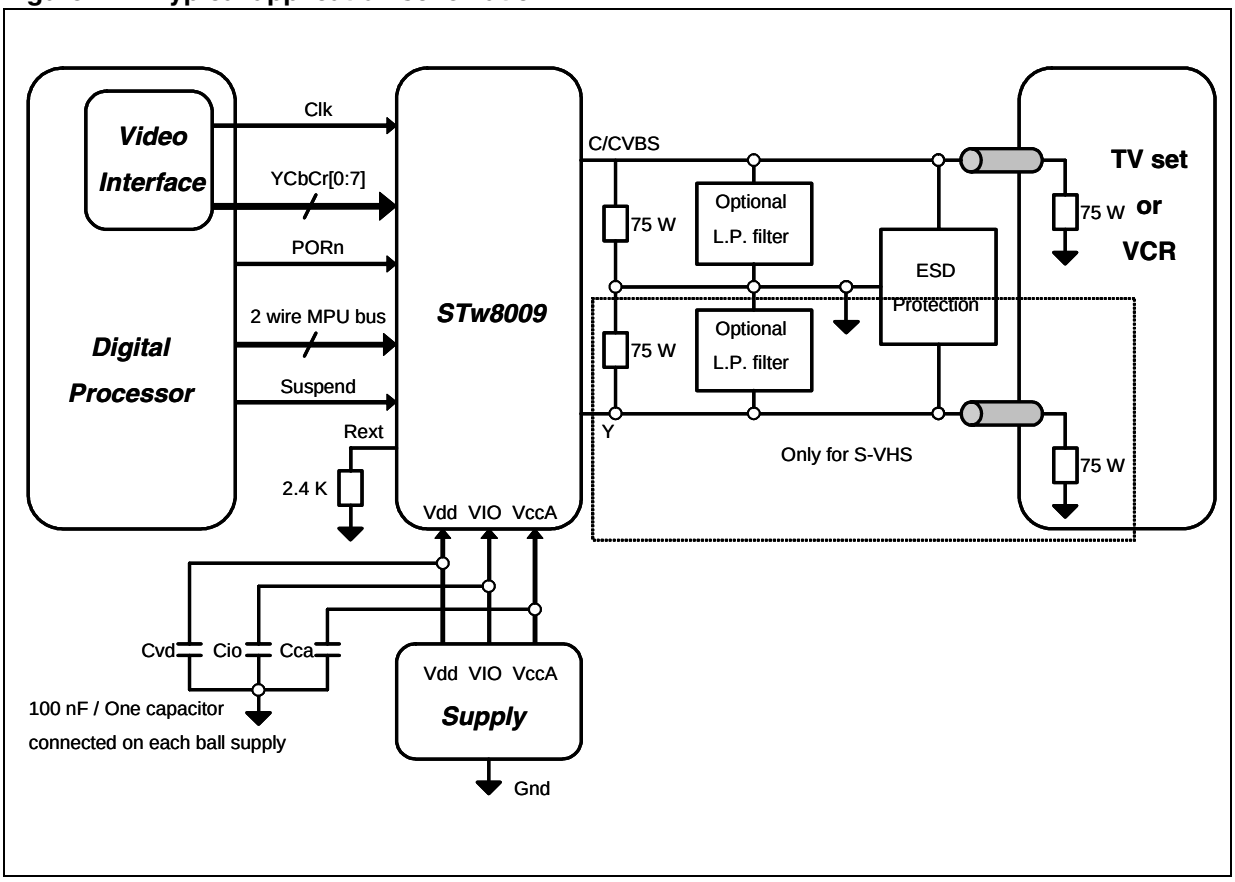
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $PSL_{Vdd}$ | Sleep mode / on Vdd | Vdd = 1.2 V<br>no 27 MHz clock | | 3 | | µW |
| $PST_{Vdd}$ | Stand by mode / on Vdd | Vdd = 1.2 V | | 150 | | µW |
| $PST_{Vcca}$ | Stand by mode / on Vcca | Vcca = 2.8 V | | 1 | | µW |
| $PAC_{Vdd}$ | Active mode / on Vdd | Vdd = 1.2 V<br>0, 1 or 2 DAC enabled | | 5 | | mW |
| $PAC0_{Vcca}$ | Active mode / on Vcca | Vcca = 2.8 V<br>no DAC enabled | | 2 | | µW |
| $PAC1_{Vcca}$ | Active mode / on Vcca | Vcca = 2.8 V<br>1 DAC enabled | | 120 | | mW |
| $PAC2_{Vcca}$ | Active mode / on Vcca | Vcca = 2.8 V<br>2 DAC enabled | | 240 | | mW |

**Table 27. DAC & Video output characteristics / Rload = 37.5 Ohms – F = 27 MHz – Rext = 2.4 kΩ**

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $R_{DAC}$ | Resolution | | | 10 | | Bits |
| $INL_{DAC}$ | Integral non linearity | | -1 | | +1 | LSB |
| $DNL_{DAC}$ | Differential non linearity | | -0.5 | | +0.5 | LSB |
| VFR1 | Full range output voltage | Pedestal on low | 1.14 | 1.21 | 1.27 | V |
| VFR2 | Full range output voltage | Pedestal on high | 1.24 | 1.31 | 1.38 | V |
| SFDR | Spurious free dynamic range | F = 1 MHz / 1 Vpp | TBD | 49 | | dB |
| SNR | Signal to noise ratio | With white level | 55 | 62 | | dB |
| PSRR | Power supply rejection ratio | 2.8 V supply / F = 200 Hz | | 65 | | dB |

# 8 Application information

**Figure 17. Typical application schematic**



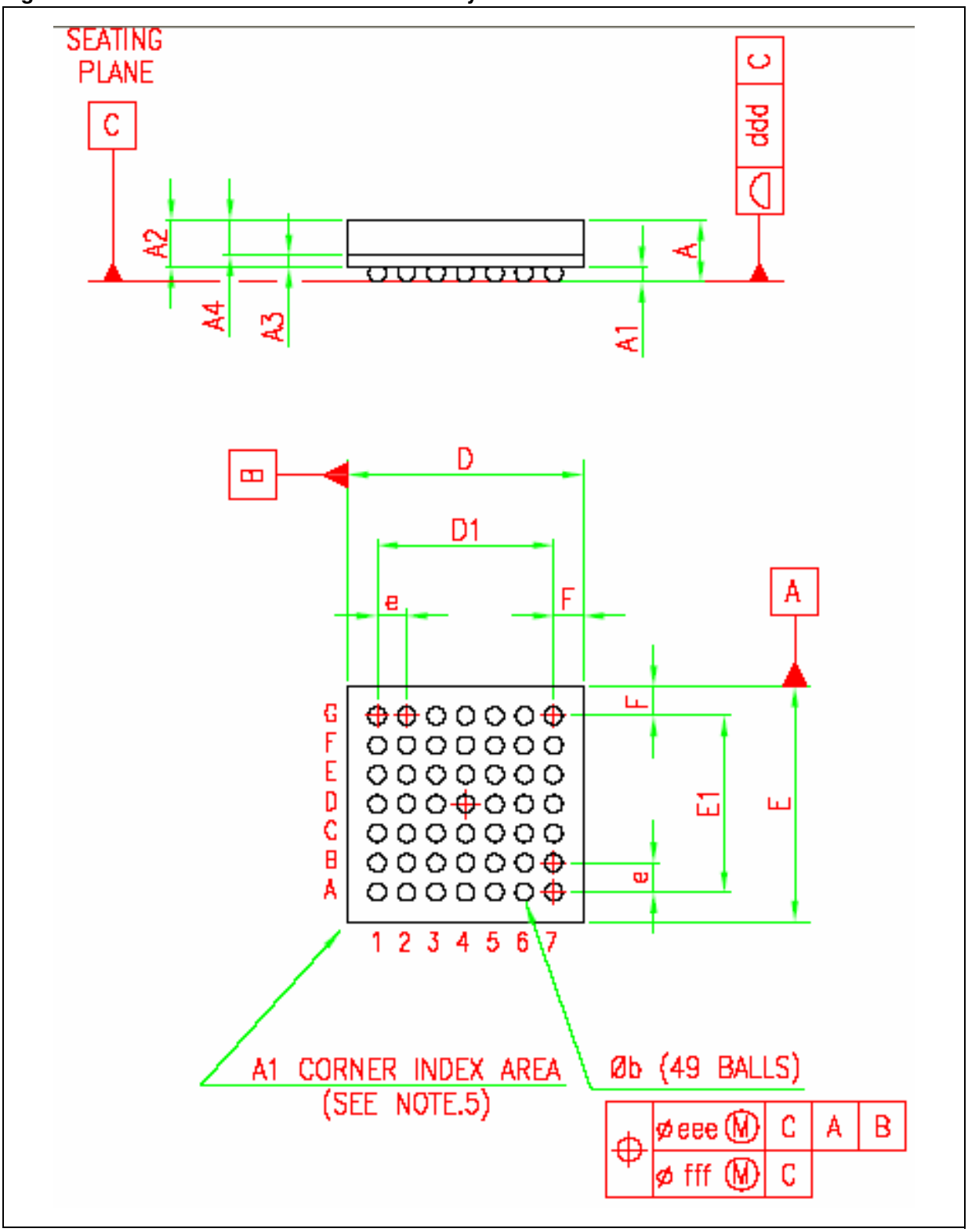
# 9 Package mechanical data

## 9.1 TFBGA 49 balls

**Table 28. TFBGA 4x4x1.2 mm**

| Dimensions (mm) | | | |
|---|---|---|---|
| **Reference** | **Min** | **Typ** | **Max** |
| A | | | 1.2 |
| A1 | 0.15 | | |
| A2 | | 0.8 | |
| A3 | | 0.2 | |
| A4 | | | 0.6 |
| b | 0.25 | 0.3 | 0.35 |
| D | 3.85 | 4.00 | 4.15 |
| D1 | | 3.00 | |
| E | 3.85 | 4.00 | 4.15 |
| E1 | | 3.00 | |
| e | | 0.50 | |
| F | | 0.5 | |
| ddd | | | 0.08 |
| eee | | | 0.15 |
| fff | | | 0.05 |

**Figure 18. TFBGA 49 balls 4 x 4 x 1.2 mm body size**



## 9.2 VFBGA 49 balls

**Table 29. VFBGA 3x3x1.0 mm - 49 balls - Pitch 0.4 ball 0.25**

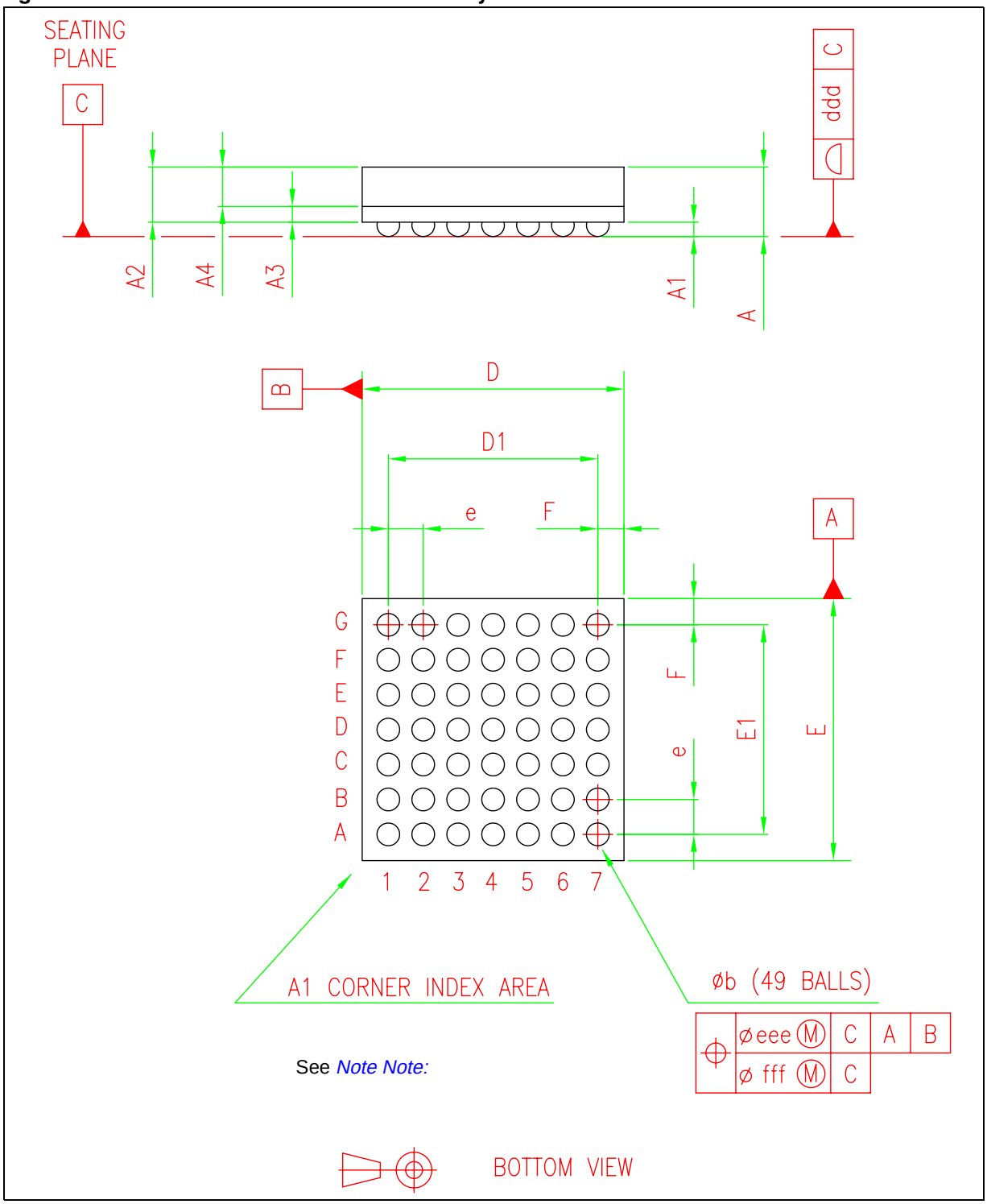
| Dimensions (mm) | | | |
|---|---|---|---|
| **Reference** | **Min** | **Typ** | **Max** |
| A(1) | | | 1.00 |
| A1 | 0.125 | | |
| A2 | | 0.615 | |
| A3 | | 0.18 | |
| A4 | | | 0.45 |
| b(2) | 0.22 | 0.26 | 0.30 |
| D | 2.95 | 3.00 | 3.05 |
| D1 | | 2.40 | |
| E | 2.95 | 3.00 | 3.05 |
| E1 | | 2.40 | |
| e | | 0.40 | |
| F | | 0.30 | |
| ddd | | | 0.08 |
| eee(3) | | | 0.13 |
| fff(4) | | | 0.04 |

1. VFBGA stands for **V**ery thin profile **F**ine pitch **B**all **G**rid **A**rray.
   Very thin profile: 0.80mm<A<=1.00mm/Fine pitch: e<1.00mm
   The maximum total package height is calculated by the following methodology

$$A2Typ + A1Typ + \left(\sqrt{A1^2 + A3^2 + A4^2}\,tolerancevalues\right)$$

2. The typical ball diameter before mounting is 0.25mm
3. VFBGA with 0.40mm ball pitch is not yet registered in JEDEC publications.
4. The tolerance of position that controls the location of the balls with respect to datum A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datum A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
   The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above.
   The axis of each ball must lie simultaneaously in both tolerance zones.

**Figure 19. VFBGA 49 balls 3 x 3 x 1.0 mm body size**




*Note: The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.*
*A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.*

# 10 Revision history

Table 30. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 2-Feb-2006 | 1 | Initial release. |

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