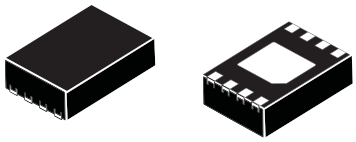
STTS2004

2.2 V memory module temperature sensor with a 4 Kb SPD EEPROM

Datasheet - production data



TDFN8
2 mm x 3 mm
(max height 0.80 mm)

Features

- 2.2 V memory module temperature sensor with integrated 4 Kb SPD EEPROM
- Fully compliant with JEDEC TSE2004B2 specifications
- Operating temperature range: –20 °C to +125 °C
- Single supply voltage 2.2 V to 3.6 V
- 2 mm x 3 mm TDFN8, height: 0.80 mm (max): JEDEC MO-229, W2030D compliant RoHS compliant, halogen-free

Temperature sensor

- Temperature sensor resolution: programmable (9-12 bits) 0.25 °C (typ)/LSB - (10-bit) default
- Temperature sensor accuracy (max) of: ± 1 °C (from +75 °C to +95 °C); ± 2 °C (from +40 °C to +125 °C); ± 3 °C (from –20 °C to +125 °C)
- ADC conversion time: 125 ms (max) / 70 ms (typ) at default resolution (10-bit)
- Typical operating supply current 160 µA (EEPROM standby)
- Temperature hysteresis selectable set points from 0, 1.5, 3, 6.0 °C

4 Kb SPD EEPROM

- Functionality identical to ST's M34E04 SPD EEPROM
- 4 Kbits organized as two pages of 256 bytes each
- Each page is composed of two 128-byte blocks
- Software data protection for each 128-byte block
- Byte Write within 5 ms
- 16 bytes Page Write within 5 ms
- More than 1 million write cycles
- More than 40-year data retention

Two-wire bus

- Two-wire I^2C compatible serial interface
- Supports up to 1 MHz transfer rate (I^2C Fast Mode+)
- Does not initiate clock stretching
- Supports SMBus timeout 25 ms - 35 ms

This is information on a product in full production. www.st.com

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1 Description

The STTS2004 is targeted for DDR4 DIMM modules in servers, desktops, and mobile personal computing platforms (laptops and other industrial applications). The thermal sensor (TS) in the STTS2004 is compliant with the JEDEC specification TSE2004a2, which defines memory module thermal sensor requirements for use in DRAM DIMMs (Dual Inline Memory Modules) with Serial Presence Detect (SPD), in which all the information concerning the DRAM module configuration (such as access speed, size, and organization) can be kept write-protected in one or more of the blocks of memory. The 4-Kbit serial EEPROM (SPD) in the STTS2004 is organized as two pages of 256 bytes each, or 512 bytes of total memory. Each page is comprised of two 128-byte blocks. The SPD is able to selectively lock the data in any or all of the four 128-byte blocks. The STTS2004 can interface to buses which have multiple devices on a shared bus, and each device has its own unique address on this bus. The device can achieve substantial power savings by using the software-programmed shutdown mode.

The TS-SPD EEPROM combination provides space as well as cost savings for mobile and server platform dual inline memory modules (DIMM) manufacturers, as it is packaged in the compact 2 mm x 3 mm 8-lead TDFN package with a thinner maximum height of 0.80 mm. The DN package is compliant to JEDEC MO-229, variation W2030D.

The digital temperature sensor has a programmable 9-12 bit analog-to-digital converter (ADC) which monitors and digitizes the temperature to a resolution of up to 0.0625 °C. The default resolution is 0.25 °C/LSB (10-bit). The typical accuracies over these temperature ranges are:

- ±2 °C over the full temperature measurement range of –20 °C to 125 °C
- ±1 °C in the +40 °C to +125 °C active temperature range, and
- ±0.5 °C in the +75 °C to +95 °C monitor temperature range

The temperature sensor in the STTS2004 is specified for operating at supply voltages from 2.2 V to 3.6 V. Operating at 3.3 V, the typical supply current is 160 µA (includes I^2C communication current).

The on-board sigma-delta ADC converts the measured temperature to a digital value that is calibrated in °C. For Fahrenheit applications, a lookup table or conversion routine is required. The STTS2004 is factory-calibrated and requires no external components to measure temperature.

The digital temperature sensor component has user-programmable registers that provide the capabilities for DIMM temperature-sensing applications. The open drain event output pin is active when the monitoring temperature exceeds a programmable limit, or it falls above or below an alarm window. The user has the option to set the event output as a critical temperature output. This pin can be configured to operate in either a comparator mode for thermostat operation or in interrupt mode.

The STTS2004 is protocol-compatible with the 2 Kbit SPD in the STTS2002 and uses a page selection method which is applied to the lower or upper pages of the 4 Kbit SPD. Unlike the STTS2002, the STTS2004 does not support the Permanently Set Write Protect (PSWP) feature.

Locking a 128-byte block of the EEPROM is accomplished by using a software write protection mechanism in conjunction with a high input voltage V_{HV} on the A0 input pin. A specific I^2C sequence is used to protect each block from writes until write protection is

electrically reversed using a separate I^2C sequence which also requires V_{HV} on input A0 pin of the device.

Write protection for all four blocks is cleared simultaneously, and write protection may be re-asserted after being cleared.

2 Serial communications

The STTS2004 has a simple 2-wire I^2C-compatible digital serial interface which allows the user to access both the 4 Kb serial EEPROM and the data in the temperature register at any time. It communicates via the serial interface with a master controller which operates at speeds of up to 1 MHz. It also gives the user easy access to all of the STTS2004 registers in order to customize device operation.

The device behaves as a slave device in the I^2C protocol, with all operations synchronized by the serial clock. Read and write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a device select code and R/W bit (as described in *Table 2 on page 10*), terminated by an acknowledge bit.

The STTS2004 device is selected when decoding the correct device select byte. The device select byte is comprised of the 4-bit Device Type Identifier (DTI) and the 3-bit select address.

The SPD and TS portions of the STTS2004 device are designed to operate in parallel. Accesses to each portion of the device may be interleaved as long as the command protocol is followed.

When writing data to the memory, the STTS2004 inserts an acknowledge bit during the 9^{th} clock cycle, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a bus master generated STOP condition after an ACK for WRITE, and after a No ACK for READ.

The TS portion of the STTS2004 device uses a pointer register to access all registers in the device. Additionally, all data transfers to and from this section of the device are performed as block read/write operations. The data is transmitted/received as 2 bytes, Most Significant Byte (MSB) first, and terminated with a No ACK and STOP after the Least Significant Byte (LSB). Data and address information is transmitted and received Most Significant Bit first.

Note: Clock stretching is not supported by the device.

Violations of the command protocol result in unpredictable operation.

2.1 Device type identifier (DTI) code

The JEDEC temperature sensor and EEPROM each have their own unique I^2C address, which ensures that there are no compatibility or data translation issues. This is due to the fact that each of the devices have their own 4-bit DTI code, while the remaining three bits are configurable. This enables the EEPROM and thermal sensors to provide their own individual data via their unique addresses and still not interfere with each other's operation in any way.

The TS registers of the STTS2004 are accessed using a DTI of (0011).

A0, A1, and A2 inputs are directly combined with the DTI and the SPD page address bit to qualify I^2C addresses. Each of the address pins (A0, A1, A2) is tied to V_{DD} or V_{SS} for the Logical Serial Address (LSA) which is equal to the code on the address pins (refer to *Table 1*).

The SPD memory may be accessed using a DTI of (1010), and to perform the SWPn, RSPn, or CWP operations, a DTI of (0110) is required.

The DTI codes are:

- '0011' for the TS, and
- '1010' for addressing the EEPROM memory array, and
- '0110' to access the software write protection settings of the EEPROM

2.1.1 I²C slave sub-address decoding

The 7-bit address for STTS2004 device consists of the 4-bit DTI code and the 3-bit device select code from the state of the 3 address pins (device select code) which are combined as shown in *Table 2*.

The 8th bit is the Read/Write bit (R/W). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on serial data (SDA) during the 9th bit time.

The physical address for the TS is different than that used by the EEPROM. The TS physical address is binary 0 0 1 1 A2 A1 A0 RW, where A2, A1, and A0 are the three slave sub- address pins, and the LSB "RW" is the READ/WRITE flag.

The EEPROM physical address is binary 1 0 1 0 A2 A1 A0 RW for the memory array and is 0 1 1 0 A2 A1 A0 RW for permanently set write protection mode.

Thus up to eight STTS2004 devices can be connected on a single I²C bus. Each device is given a unique 3-bit Logical Serial Address code. The LSA is a decoding of information on the address pins A0, A1, and A2 as described in *Table 1*. When the Device Select Code is received, the device only responds if the Select Address is the same as the Logical Serial Address.

Table 1. Logical serial address according to A2, A1, A0

Logical serial address (LSA)	Device select code		
	A2	A1	A0
000	0 (V_{SS})	0 (V_{SS})	0 (V_{SS})
001	0 (V_{SS})	0 (V_{SS})	1 (V_{DD})
010	0 (V_{SS})	1 (V_{DD})	0 (V_{SS})
011	0 (V_{SS})	1 (V_{DD})	1 (V_{DD})
100	1 (V_{DD})	0 (V_{SS})	0 (V_{SS})
101	1 (V_{DD})	0 (V_{SS})	1 (V_{DD})
110	1 (V_{DD})	1 (V_{DD})	0 (V_{SS})
111	1 (V_{DD})	1 (V_{DD})	1 (V_{DD})

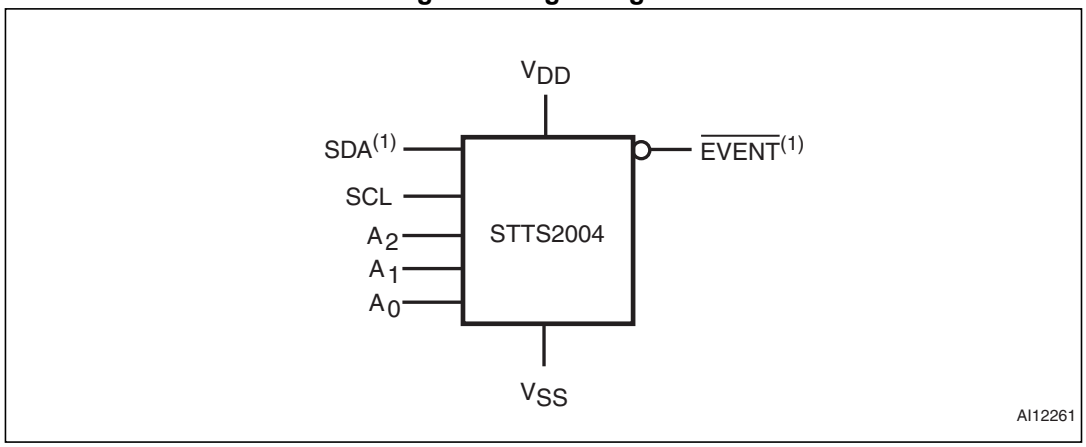
Write protection commands SWPn, CWP, and RPSn, and the SPD page address commands SPAn and RPA, do not use the select address A(n) or logical serial address (LSA), therefore all devices on the bus will act on these commands simultaneously. Since it is impossible to determine which device is responding to RPSn or RPA commands, for example, these functions are primarily used for external device programmers rather than in-system applications.

Table 2. Device select code

Function	Symbol	Device Type Identifier (DTI)[1]				Logical Serial Address (LSA)[2][3]			R/W	A0 pin[4]
		b7	b6	b5	b4	b3	b2	b1	b0	
Read temperature registers	RTR	0	0	1	1	A2	A1	A0	1	0 or 1
Write temperature registers	WTR								0	
Read EE memory	RSPD	1	0	1	0	A2	A1	A0	1	0 or 1
Write EE memory	WSPD								0	
Set write protection, block 0	SWP0	0	1	1	0	0	0	1	0	V_{HV}
Set write protection, block 1	SWP1					1	0	0	0	V_{HV}
Set write protection, block 2	SWP2					1	0	1	0	V_{HV}
Set write protection, block 3	SWP3					0	0	0	0	V_{HV}
Clear all write protection	CWP					0	1	1	0	V_{HV}
Read protection status, block 0[5]	RPS0					0	0	1	1	0, 1 or V_{HV}
Read protection status, block 1[5]	RPS1					1	0	0	1	0, 1 or V_{HV}
Read protection status, block 2[5]	RPS2					1	0	1	1	0, 1 or V_{HV}
Read protection status, block 3[5]	RPS3					0	0	0	1	0, 1 or V_{HV}
Set EE page address to 0[6]	SPA0					1	1	0	0	0, 1 or V_{HV}
Set EE page address to 1[6]	SPA1					1	1	1	0	0, 1 or V_{HV}
Read EE page address[7]	RPA					1	1	0	1	0, 1 or V_{HV}
Reserved	--					All other encodings				

1. The most significant bit, b7, is sent first.
2. Logical Serial Addresses (LSA) are generated by the combination of inputs on the address pin (refer to *Table 1*)
3. For backward compatibility with previous devices, the order of block select bits (b3 and b1) are not a simple binary encoding of the block number
4. A0 pin is driven to 0 = V_{SS}, 1 = V_{DD} or V_{HV}.
5. Reading the block protection status results in Ack when the block is not write-protected, and results in NoAck when the block is write-protected.
6. Setting the SPD (EEPROM) page address to 0 selects the lower 256 bytes of EEPROM, setting to 1 selects the upper 256 bytes of EEPROM. Subsequent Read EE or Write EE commands operate on the selected EE page.
7. Reading the EE page address results in ACK when the current page is 0 and NACK when the current page is 1.

Figure 1. Logic diagram



1. SDA and $\overline{\text{EVENT}}$ are open drain.

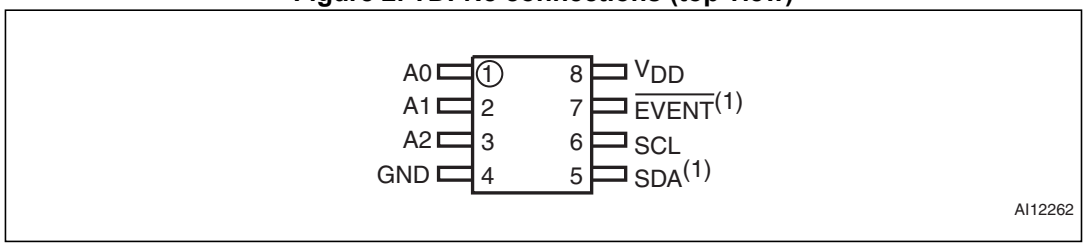
Table 3. Signal names

Pin	Symbol	Description	Direction
1	A0	Serial bus address selection pin. Can be tied to V_{SS} or V_{DD}.	Input
2	A1	Serial bus address selection pin. Can be tied to V_{SS} or V_{DD}.	Input
3	A2	Serial bus address selection pin. Can be tied to V_{SS} or V_{DD}.	Input
4	V_{SS}	Supply ground	
5	SDA(1)	Serial data	Input/output
6	SCL	Serial clock	Input
7	$\overline{\text{EVENT}}$(1)	Event output pin. Open drain and active-low.	Output
8	V_{DD}	Supply power (2.2 V to 3.6 V)	

1. SDA and $\overline{\text{EVENT}}$ are open drain.

Note: The STTS2004 also has a heat paddle, which is typically connected to the application ground plane, refer to Figure 23: Landing pattern - TDFN8 package (DN).

Figure 2. TDFN8 connections (top view)



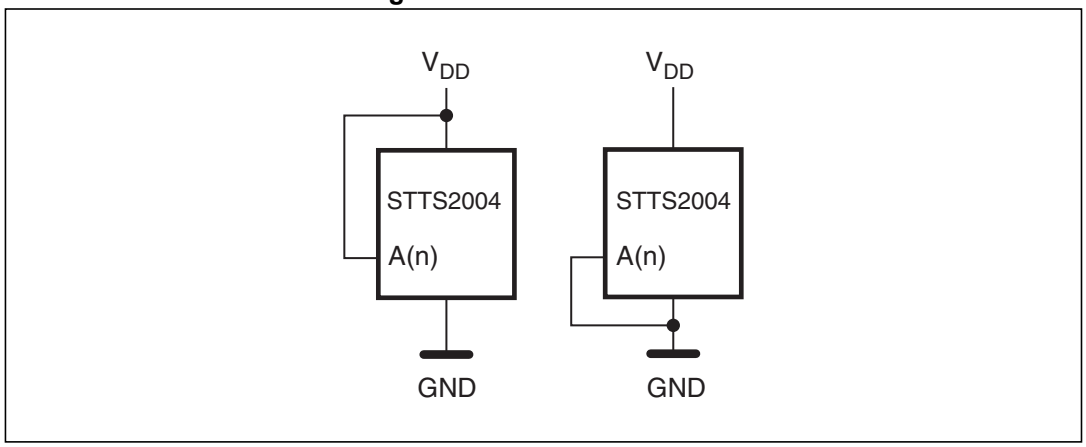
1. SDA and $\overline{\text{EVENT}}$ are open drain.

2.2 Pin descriptions

2.2.1 A0, A1, A2

A2, A1, and A0 are selectable address pins for the 3 LSBs of the I^2C interface address. These inputs must be tied to V_{DD} or GND as shown in *Figure 3* to provide 8 unique address selections. These pins are internally connected to the A2, A1, A0 (slave address inputs) of the EEPROM.

Figure 3. Device select code



2.2.2 V_{SS} (ground)

This is the reference for the power supply. It must be connected to system ground.

2.2.3 SDA (open drain)

This is the serial data input/output pin. SDA(out) is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull-up resistor must be connected from Serial Data (SDA) to V_{DD}. *Figure 20* indicates how the value of the pull-up resistor can be calculated.

2.2.4 SCL

This is the serial clock input pin.

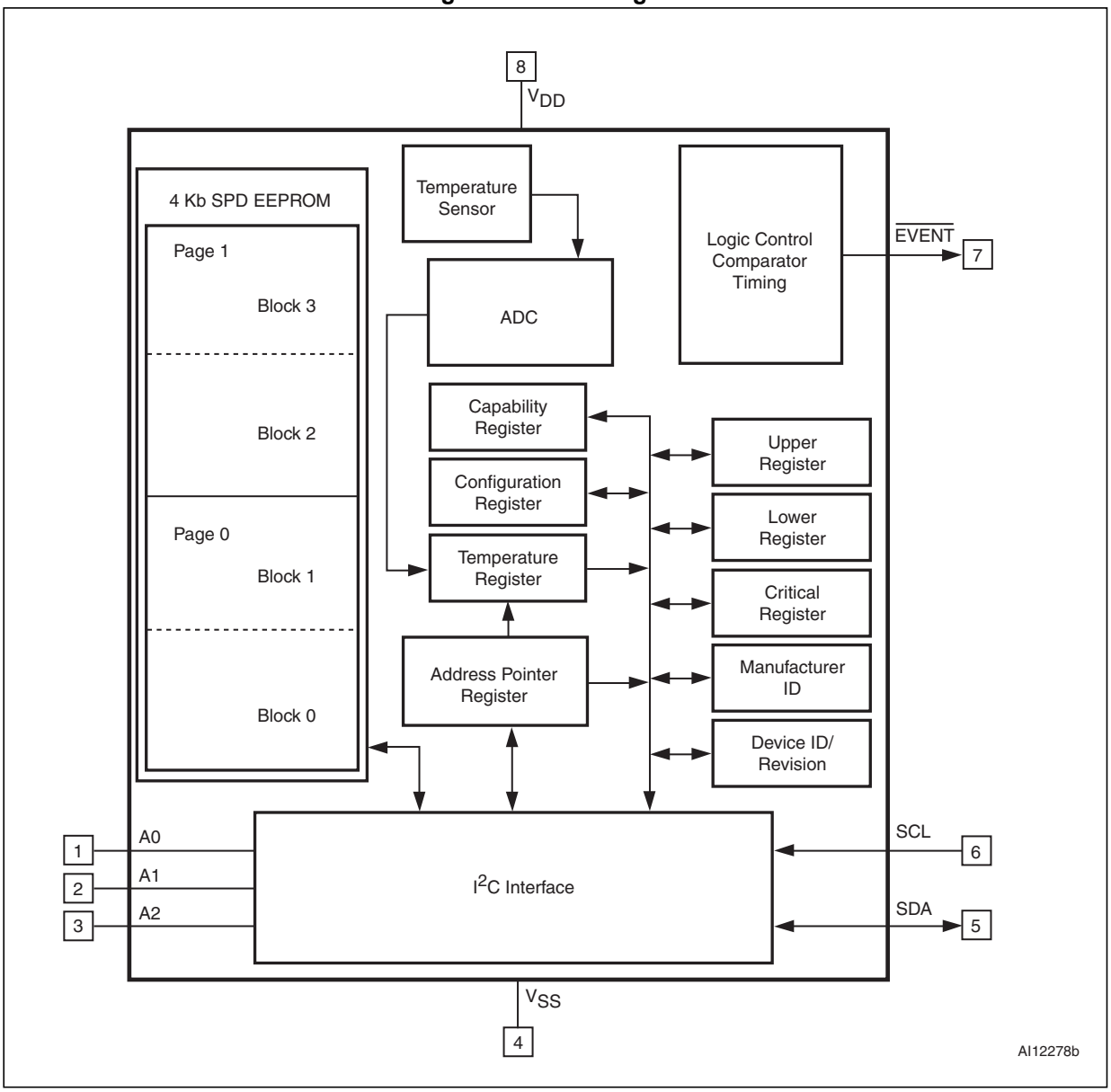
2.2.5 $\overline{\text{EVENT}}$ (open drain)

This output pin is open drain and active-low. A pull-up resistor must be connected to this pin.

2.2.6 V_{DD} (power)

This is the supply voltage pin, and ranges from 2.2 V to 3.6 V.

Figure 4. Block diagram



3 Temperature sensor operation

The temperature sensor continuously monitors the ambient temperature and updates the temperature data register. Temperature data is latched internally by the device and may be read by software from the bus host at any time.

The I^2C slave address selection pins allow up to 8 such devices to co-exist on the same bus. This means that up to 8 memory modules can be supported, given that each module has one such slave device address slot.

After initial power-on, the configuration registers are set to the default values. The software can write to the configuration register to set bits per the bit definitions in *Section 3.1: I^2C communications*.

For details of operation and usage of 4 Kb SPD EEPROM, refer to *Section 5: SPD EEPROM operation*.

3.1 I^2C communications

The registers in this device are selected by the pointer register. At power-up, the pointer register is set to “00”, which is the capability register location. The pointer register latches the last location it was set to. Each data register falls into one of three types of user accessibility:

1. Read-only
2. Write-only, and
3. WRITE/READ same address

A WRITE to this device will always include the address byte and the pointer byte. A WRITE to any register other than the pointer register, requires two data bytes.

Reading this device is achieved in one of two ways:

- If the location latched in the pointer register is correct (most of the time it is expected that the pointer register will point to one of the read temperature registers because that will be the data most frequently read), then the READ can simply consist of an address byte, followed by retrieval of the two data bytes.
- If the pointer register needs to be set, then an address byte, pointer byte, repeat start, and another address byte will accomplish a READ.

The data byte transfers the MSB first. At the end of a READ, this device can accept either an acknowledge (ACK) or no acknowledge (No ACK) status from the master. The No ACK status is typically used as a signal for the slave that the master has read its last byte. This device subsequently takes up to 125 ms (max), 70 ms (typ) to measure the temperature for the default temperature resolution.

Note: The STTS2004 does not initiate clock stretching which is an optional I^2C bus feature.

Figure 5. I²C write to pointer register

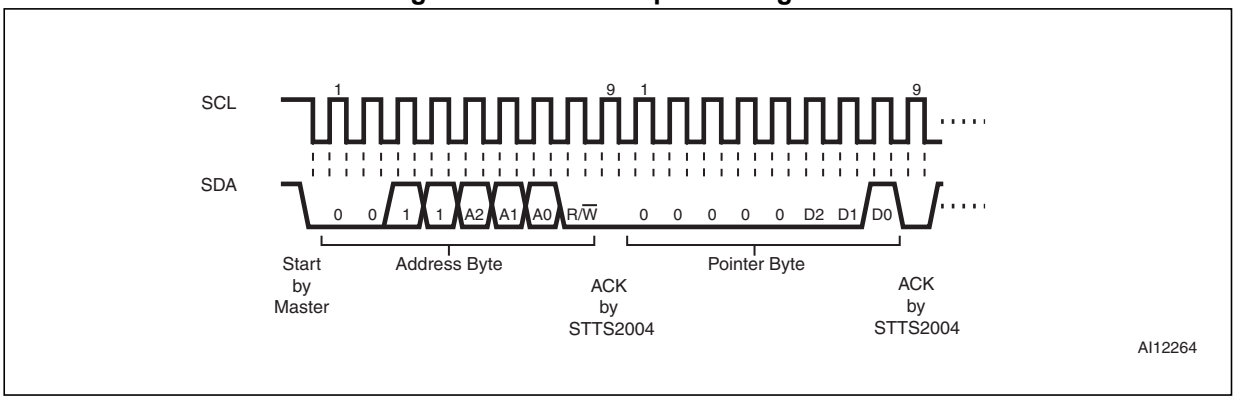


Figure 6. I²C write to pointer register, followed by a read data word

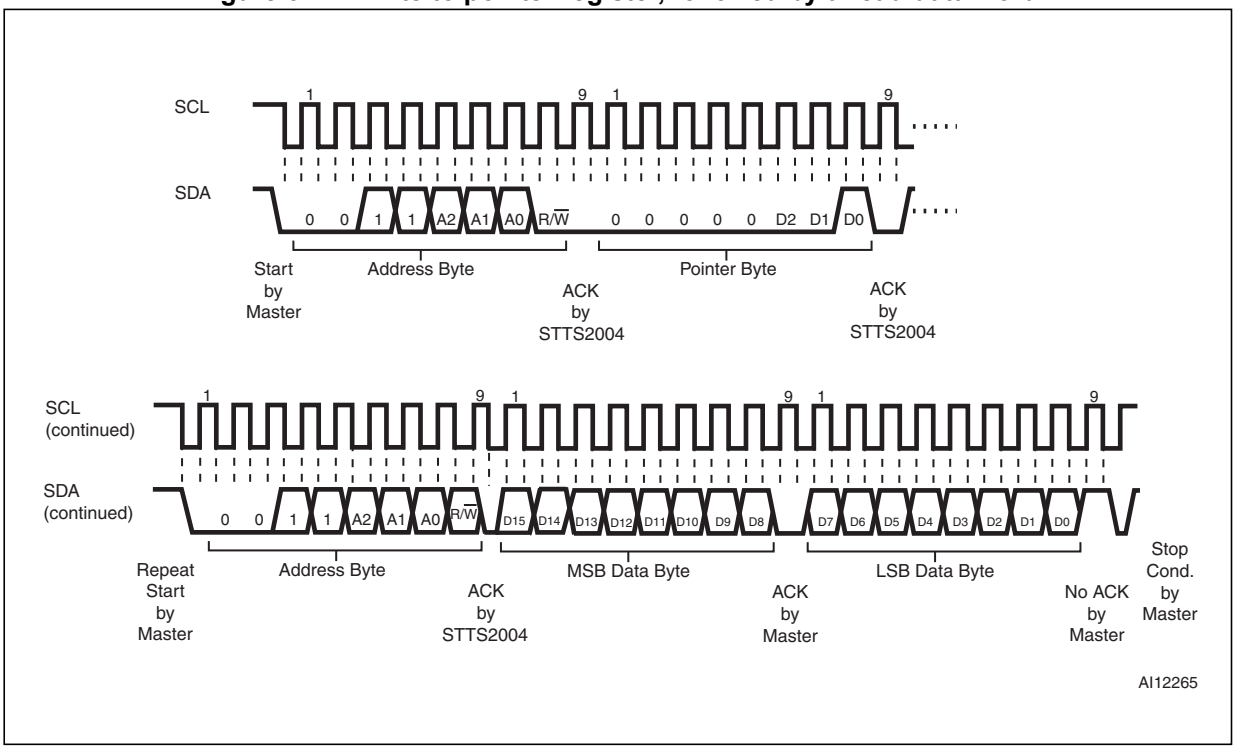
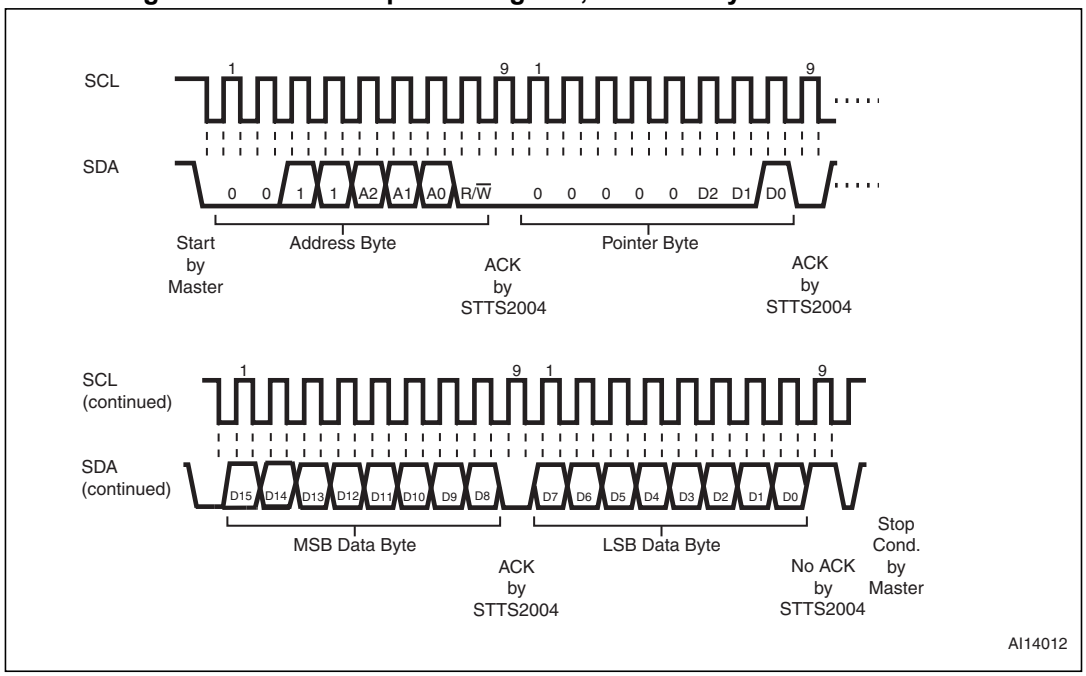


Figure 7. I²C write to pointer register, followed by a write data word



3.2 SMBus/I²C AC timing consideration

In order for this device to be both SMBus- and I²C-compatible, it complies to a subset of each specification. The requirements which enable this device to co-exist with devices on either an SMBus or an I²C bus include:

- The SMBus minimum clock frequency is required
- The SMBus timeout is maximum 35 ms

4 Temperature sensor registers

The temperature sensor component is comprised of various user-programmable registers. These registers are required to write their corresponding addresses to the pointer register. They can be accessed by writing to their respective addresses (see *Table 4*). Pointer register bits 7 - 4 must always be written to '0' (see *Table 5*). This must be maintained, as not setting these bits to '0' may keep the device from performing to specifications.

The main registers include:

- *Capability register (read-only)*
- *Configuration register (read/write)*
- *Temperature register (read-only)*
- *Temperature trip point registers (read/write)*, including
  - Alarm temperature upper boundary
  - Alarm temperature lower boundary
  - Critical temperature
- *Manufacturer ID register (read-only)*
- *Device ID and device revision ID register (read-only)*
- *Temperature resolution register (TRES) (read/write)*

See *Table 6 on page 18* for pointer register selection bit details.

Table 4. Temperature sensor registers summary

Address (hex)	Register name		Power-on default
Not applicable	Address pointer		Undefined
00	Capability	B-grade	0x00EF
01	Configuration		0x0000
02	Alarm temperature upper boundary trip		0x0000
03	Alarm temperature lower boundary trip		0x0000
04	Critical temperature trip		0x0000
05	Temperature		Undefined
06	Manufacturer’s ID		0x104A
07	Device ID/revision		0x2201
08	Temperature resolution register		0x0001

Note: Registers beyond the specified (00-08) are reserved for STMicroelectronics’ internal use only, for device test modes in product manufacturing. The registers must NOT be accessed by the user (customer) in the system application or the device may not perform according to specifications.

Table 5. Pointer register format

MSB							LSB
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
0	0	0	0	P3	P2	P1	P0
				Pointer/register select bits			

Table 6. Pointer register select bits (type, width, and default values)

P3	P2	P1	P0	Name	Register description		Width (bits)	Type (R/$\overline{W}$)	Default state (POR)
0	0	0	0	CAPA	Thermal sensor capabilities	B-grade only	16	R	00 EF
0	0	0	1	CONF	Configuration		16	R/$\overline{W}$	00 00
0	0	1	0	UPPER	Alarm temperature upper boundary		16	R/$\overline{W}$	00 00
0	0	1	1	LOWER	Alarm temperature lower boundary		16	R/$\overline{W}$	00 00
0	1	0	0	CRITICAL	Critical temperature		16	R/$\overline{W}$	00 00
0	1	0	1	TEMP	Temperature		16	R	00 00
0	1	1	0	MANU	Manufacturer ID		16	R	10 4A
0	1	1	1	ID	Device ID/revision		16	R	22 01
1	0	0	0	TRES	Temperature resolution register		8	R/$\overline{W}$	01

4.1 Capability register (read-only)

This 16-bit register is read-only, and provides the TS capabilities which comply with the minimum JEDEC TSE2004av specifications (see *Table 7* and *Table 8 on page 19*). The STTS2004 resolution is programmable via writing to pointer 08 register. The power-on default value is 0.25 °C/LSB (10-bit).

Table 7. Capability register format

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
EVSD	TMOUT	V_{HV}	TRES1	TRES0	Wider range	Higher precision	Alarm and critical trips

Table 8. Capability register bit definitions

Bit	Definition
0	Basic capability – 0 = Alarm and critical trips turned OFF. – 1 = Alarm and critical trips turned ON.
1	Accuracy – **1 = High accuracy ±1 °C over the active range and ±2 °C over the monitoring range (B-grade) (default)**.
2	Range width – 0 = Values lower than 0 °C will be clamped and represented as binary value '0'. – 1 = Temperatures below 0 °C can be read and the Sign bit will be set accordingly.
4:3	Temperature resolution – 00 = 9 bit, 0.5 °C/LSB – 01 = 10 bit, 0.25 °C/LSB - default resolution – 10 = 11 bit, 0.125 °C/LSB – 11 = 12 bit, 0.0625 °C/LSB
5	(V_{HV}) high voltage support for **A0 (pin 1)** – 1 = STTS2004 supports a voltage up to 10 volts on the A0 pin - (default)
6	TMOUT - bus timeout support – 1 = **Default for STTS2004-SMBus compatible 25 ms - 35 ms**
7	EVSD - $\overline{\text{EVENT}}$ behavior upon shutdown (default) – 1 = The $\overline{\text{EVENT}}$ pin output is deasserted (not driven) when entering shutdown, and remains deasserted upon exit from shutdown until the next thermal sample is taken, or possibly sooner if $\overline{\text{EVENT}}$ is programmed for comparator mode. In interrupt mode, $\overline{\text{EVENT}}$ may or may not be asserted when exiting shutdown if a pending interrupt has not been cleared.
15:8	Reserved These values must be set to '0'.

4.2 Configuration register (read/write)

The 16-bit configuration register stores various configuration modes that are used to set up the sensor registers and configure according to application and JEDEC requirements (see *Table 9 on page 21* and *Table 10 on page 21*).

4.2.1 Event thresholds

All event thresholds use hysteresis as programmed in register address 0x01 (bits 10 through 9) to be set when they de-assert.

4.2.2 Interrupt mode

The interrupt mode allows an event to occur where software may write a '1' to the clear event bit (bit 5) to de-assert the event Interrupt output until the next trigger condition occurs.

4.2.3 Comparator mode

The comparator mode enables the device to be used as a thermostat. READs and WRITEs on the device registers will not affect the event output in comparator mode. The event signal will remain asserted until temperature drops outside the range or is re-programmed to make the current temperature “out of range”.

4.2.4 Shutdown mode

The STTS2004 features a shutdown mode which disables all power-consuming activities (e.g. temperature sampling operations), and leaves the serial interface active. This is selected by setting the shutdown bit (bit 8) to '1'. In this mode, the devices consume the minimum current (I_{SHDN}), as shown in *Table 30 on page 44*.

Note: Bit 8 cannot be set to '1' while bits 6 and 7 (the lock bits) are set to '1'.

The device may be enabled for continuous operation by clearing bit 8 to '0'. In shutdown mode, all registers may be read or written to. Power recycling will also clear this bit and return the device to continuous mode as well.

If the device is shut down while the $\overline{EVENT}$ pin is asserted, then the Event output will be de-asserted during shutdown. It will remain de-asserted until the device is enabled for normal operation. Once the device is enabled, it takes t_{CONV} before the device can re-assert the Event output.

Table 9. Configuration register format

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
RFU	RFU	RFU	RFU	RFU	Hysteresis	Hysteresis	Shutdown mode
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Critical lock bit	Alarm lock bit	Clear event	Event output status	Event output control	Critical event only	Event polarity	Event mode

The temperature sensor configuration register holds the control and status bits of the $\overline{\text{EVENT}}$ pin as well as general hysteresis on all limits. To avoid glitches on the $\overline{\text{EVENT}}$ output pin, users should disable EVENT or CRITICAL functions prior to programming or changing other device configuration settings.

Table 10. Configuration register bit definitions

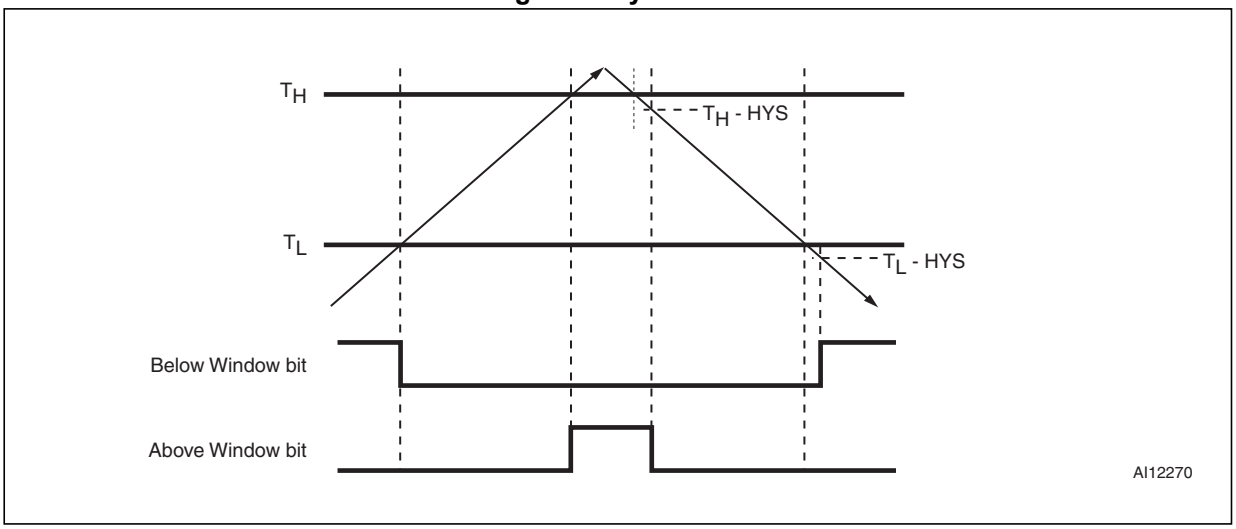
Bit	Definition
0	Event mode – 0 = Comparator output mode (this is the default). – 1 = Interrupt mode; when either of the lock bits (bit6 or bit7) is set, this bit cannot be altered until it is unlocked.
1	Event polarity(1) The event polarity bit controls the active state of the $\overline{\text{EVENT}}$ pin. The $\overline{\text{EVENT}}$ pin is driven to this state when it is asserted. – 0 = Active-low (this is the default). Requires a pull-up resistor to set the inactive state of the open-drain output. The power to the pull-up resistor should not be greater than V_{DD} + 0.2 V. Active state is logical “0”. – 1 = Active-high. The active state of the pin is then logical “1”.
2	Critical event only – 0 = Event output on alarm or critical temperature event (this is the default). – 1 = Event only if the temperature is above the value in the critical temperature register ($T_A > T_{CRIT}$); when the alarm window lock bit (bit6) is set, this bit cannot be altered until it is unlocked.
3	Event output control – 0 = Event output disabled (this is the default). – 1 = Event output enabled; when either of the lock bits (bit6 or bit7) is set, this bit cannot be altered until it is unlocked.
4	Event status (read-only)(2) – 0 = Event output condition is not being asserted by this device. – 1 = Event output condition is being asserted by this device via the alarm window or critical trip event.
5	Clear event (write-only)(3) – 0 = No effect. – 1 = Clears the active event in interrupt mode. The pin is released and will not assert until a new interrupt condition occurs.

Table 10. Configuration register bit definitions (continued)

Bit	Definition
6	Alarm window lock bit – 0 = Alarm trips are not locked and can be altered (this is the default). – 1 = Alarm trip register settings cannot be altered. This bit is initially cleared. When set, this bit returns a logic '1' and remains locked until cleared by an internal power-on reset. These bits can be written to with a single WRITE, and do not require double WRITEs.
7	Critical trip lock bit – 0 = Critical trip is not locked and can be altered (this is the default). – 1 = Critical trip register settings cannot be altered. This bit is initially cleared. When set, this bit returns a logic '1' and remains locked until cleared by an internal power-on reset. These bits can be written to with a single WRITE, and do not require double WRITEs.
8	Shutdown mode – 0 = TS is enabled, continuous conversion (this is the default). – 1 = Shutdown TS when the shutdown, device, and A/D converter are disabled in order to save power. No event conditions will be asserted; when either of the lock bits (bit6 or bit7) is set, then this bit cannot be altered until it is unlocked. It can be cleared at any time.
10:9	Hysteresis enable (see *Figure 8* and *Table 11*) – 00 = Hysteresis is disabled (default) – 01 = Hysteresis is enabled at 1.5 °C – 10 = Hysteresis is enabled at 3 °C – 11 = Hysteresis is enabled at 6 °C Hysteresis applies to all limits when the temperature is dropping below the threshold so that once the temperature is above a given threshold, it must drop below the threshold minus the hysteresis in order to be flagged as an interrupt event. Note that hysteresis is also applied to the $\overline{\text{EVENT}}$ pin functionality. When either of the lock bits is set, these bits cannot be altered.
15:11	Reserved for future use. These bits will always read ‘0’ and writing to them will have no effect. For future compatibility, all RFU bits must be programmed as ‘0’.

1. As this device is used in DIMM (memory modules) applications, it is strongly recommended that only the active-low polarity (default) is used. This will provide full compatibility with the STTS2002. This is the recommended configuration for the STTS2004.
2. The actual incident causing the event can be determined from the read temperature register. Interrupt events can be cleared by writing to the clear event bit (writing to this bit will have no effect on overall device functioning).
3. Writing to this register has no effect on overall device functioning in comparator mode. When read, this bit will always return a logic '0' result.

Figure 8. Hysteresis



1. T_H = Value stored in the alarm temperature upper boundary trip register
2. T_L = Value stored in the alarm temperature lower boundary trip register
3. HYS = Absolute value of selected hysteresis

Table 11. Hysteresis as applied to temperature movement

	Below alarm window bit		Above alarm window bit	
	Temperature slope	**Temperature threshold**	**Temperature slope**	**Temperature threshold**
Sets	Falling	T_L - HYS	Rising	T_H
Clears	Rising	T_L	Falling	T_H - HYS

4.2.5 Event output pin functionality

The STTS2004 $\overline{\text{EVENT}}$ pin is an open drain output that requires a pull-up to V_{DD} on the system motherboard or integrated into the master controller. $\overline{\text{EVENT}}$ has three operating modes, depending on configuration settings and any current out-of-limit conditions. These modes are interrupt, comparator or critical.

In interrupt mode the $\overline{\text{EVENT}}$ pin will remain asserted until it is released by writing a '1' to the "Clear Event" bit in the status register. The value to write is independent of the EVENT polarity bit.

In comparator mode the $\overline{\text{EVENT}}$ pin will clear itself when the error condition that caused the pin to be asserted is removed.

In the critical mode the $\overline{\text{EVENT}}$ pin will only be asserted if the measured temperature exceeds the critical limit. Once the pin has been asserted, it will remain asserted until the temperature drops below the critical limit minus hysteresis. *Figure 9 on page 25* illustrates the operation of the different modes over time and temperature.

When the hysteresis bits (bits 10 and 9) are enabled, hysteresis may be used to sense temperature movement around trigger points. For example, when using the "above alarm window" bit (temperature register bit 14, see *Table 13 on page 26*) and hysteresis is set to 3 °C, as the temperature rises, bit 14 is set (bit 14 = 1). The temperature is above the alarm window and the temperature register contains a value that is greater than the value set in the alarm temperature upper boundary register (see *Table 17 on page 28*).

If the temperature decreases, bit 14 will remain set until the measured temperature is less than or equal to the value in the alarm temperature upper boundary register minus 3 °C (see *Figure 8 on page 23* and *Table 11 on page 23* for details.

Similarly, when using the "below alarm window" bit (temperature register bit 13, see *Table 13 on page 26*) will be set to '0'. The temperature is equal to or greater than the value set in the alarm temperature lower boundary register (see *Table 18 on page 28*). As the temperature decreases, bit 13 will be set to '1' when the value in the temperature register is less than the value in the alarm temperature lower boundary register minus 3 °C (see *Figure 8 on page 23* and *Table 11 on page 23* for details.

If the device enters the shutdown mode with the $\overline{\text{EVENT}}$ output asserted, the output will be de-asserted.

Once the shutdown bit is cleared, the $\overline{\text{EVENT}}$ output will do the following, based on whether the device is configured for comparator or interrupt modes:

Comparator mode

The $\overline{\text{EVENT}}$ output will remain de-asserted until after the first temperature conversion (t_{CONV}) is completed. After this initial temperature conversion, T_A must satisfy the T_{UPPER} or T_{LOWER} boundary conditions in order for the $\overline{\text{EVENT}}$ output to be asserted.

Interrupt mode

The $\overline{\text{EVENT}}$ output will remain de-asserted until after the first temperature conversion (t_{CONV}) is completed. If the Clear event bit (bit 5 of configuration register) is never set, then the $\overline{\text{EVENT}}$ output will re-assert after the first temperature conversion.

Figure 9. Event output boundary timings

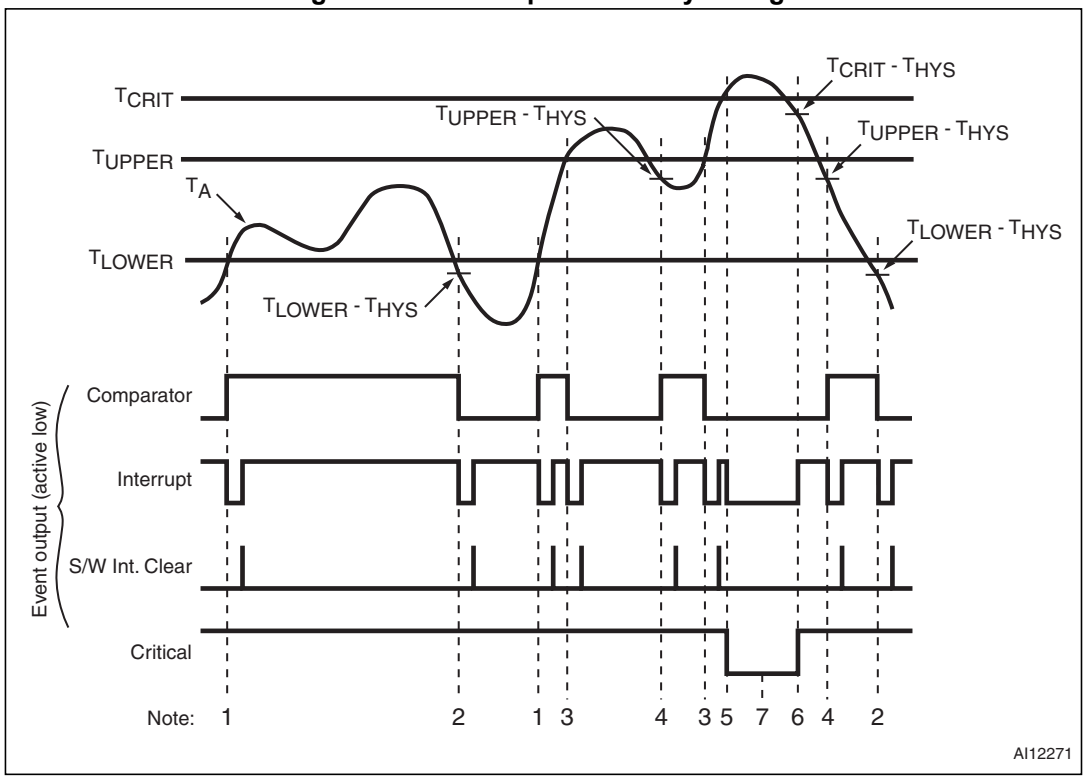


Table 12. Legend for *Figure 9: Event output boundary timings*

Note	Event output boundary conditions	Event output			T_A bits		
		Comparator	Interrupt	Critical	15	14	13
1	$T_A \geq T_{LOWER}$	H	L	H	0	0	0
2	$T_A < T_{LOWER} - T_{HYS}$	L	L	H	0	0	1
3	$T_A > T_{UPPER}$	L	L	H	0	1	0
4	$T_A \leq T_{UPPER} - T_{HYS}$	H	L	H	0	0	0
5	$T_A \geq T_{CRIT}$	L	L	L	1	0	0
6	$T_A < T_{CRIT} - T_{HYS}$	L	H	H	0	1	0
7	When $T_A \geq T_{CRIT}$ and $T_A < T_{CRIT} - T_{HYS}$, the event output is in comparator mode and bit 0 of the configuration register (interrupt mode) is ignored.						

Systems that use the active high mode for Event output must be wired point-to-point between the STTS2004 and the sensing controller. Wire-OR configurations should not be used with active high Event output since any device pulling the Event output signal low will mask the other devices on the bus. Also note that the normal state of Event output in active high mode is a ‘0’ which will constantly draw power through the pull-up resistor.

4.3 Temperature register (read-only)

This 16-bit, read-only register stores the temperature measured by the internal band gap TS as shown in *Table 13*. When reading this register, the MSBs (bit 15 to bit 8) are read first, and then the LSBs (bit 7 to bit 0) are read. The result is the current-sensed temperature. The data format is 2s complement with one LSB = 0.25 °C for the default resolution. The MSB has a 128 °C resolution.

The trip status bits represent the internal temperature trip detection, and are not affected by the status of the event or configuration bits (e.g. event output control or clear event). If neither of the above or below values are set (i.e. both are 0), then the temperature is exactly within the user-defined alarm window boundaries.

4.3.1 Temperature format

The 16-bit value used in the trip point set and temperature read-back registers is 2s complement, with the LSB equal to 0.0625 °C (see *Table 13*). For example:

1. a value of 019C h represents 25.75 °C
2. a value of 07C0 h represents 124 °C, and
3. a value of 1E74 h represents –24.75 °C

All unused resolution bits are set to zero. The MSB will have a resolution of 128 °C. The STTS2004 supports programmable resolutions (9-12 bits) which is 0.5 to 0.0625 °C/LSB. The default is 0.25 °C/LSB (10 bits) programmable.

The upper 3 bits indicate trip status based on the current temperature, and are not affected by the event output status.

Table 13. Temperature register format

			Sign MSB									LSB(1)			
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1(2)**	**Bit 0(3)**	
Flag bit	Flag bit	Flag bit	Sign	128	64	32	16	8	4	2	1	0.5	0.25	0.125	0.0625	°C/LSB
Above critical input(4)	Above alarm window(4)	Below alarm window(4)	Temperature (default - 10 bit)											0	0	
Flag bits			Example hex value of 07C0 corresponds to 124 °C (10-bit)													
0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	07C0 h
Flag bits			Example hex value of 1EC0 corresponds to –20 °C (10-bit)													
0	0	0	1	1	1	1	0	1	1	0	0	0	0	0	0	1EC0 h

1. Bit 2 is LSB for default 10-bit mode.
2. Depending on status of the resolution register, bit 1 may display 0.125 °C value.
3. Depending on status of the resolution register, bit 0 may display 0.0625 °C value.
4. See *Table 15* for explanation.

A 0.25 °C minimum granularity is supported in all registers. Examples of valid settings and interpretation of temperature register bits for 10-bit (0.25 °C) default resolution are provided in *Table 14*.

Table 14. Temperature register coding examples (for 10 bits)

B15:B0 (binary)	Value	Units
xxx0 0000 0010 11xx	+2.75	°C
xxx0 0000 0001 00xx	+1.00	°C
xxx0 0000 0000 01xx	+0.25	°C
xxx0 0000 0000 00xx	0	°C
xxx1 1111 1111 11xx	–0.25	°C
xxx1 1111 1110 00xx	–1.00	°C
xxx1 1111 1101 11xx	–2.25	°C
xxx1 1110 1100 00xx	–20.00	°C

Table 15. Temperature register bit definitions

Bit	Definition with hysteresis = 0
13	Below (temperature) alarm window – 0 = Temperature is equal to or above the alarm window lower boundary temperature. – 1 = Temperature is below the alarm window.
14	Above (temperature) alarm window. – 0 = Temperature is equal to or below the alarm window upper boundary temperature. – 1 = Temperature is above the alarm window.
15	Above critical trip – 0 = Temperature is below the critical temperature setting. – 1 = Temperature is equal to or above the critical temperature setting.

4.4 Temperature trip point registers (read/write)

The STTS2004 alarm mode registers provide for 11-bit data in 2s compliment format. The data provides for one LSB = 0.25 °C. All unused bits in these registers are read as '0'.

The STTS2004 has three temperature trip point registers (see *Table 16*):

- Alarm temperature upper boundary threshold (*Table 17*)
- Alarm temperature lower boundary threshold (*Table 18*), and
- Critical temperature trip point value (*Table 19*)

Note: If the upper or lower boundary threshold values are being altered in-system, all interrupts should be turned off until a known state can be obtained to avoid superfluous interrupt activity.

Table 16. Temperature trip point register format

P3	P2	P1	P0	Name	Register description	Width (bits)	Type (R/$\overline{W}$)	Default state (POR)
0	0	1	0	UPPER	Alarm temperature upper boundary	16	R/$\overline{W}$	00 00
0	0	1	1	LOWER	Alarm temperature lower boundary	16	R/$\overline{W}$	00 00
0	1	0	0	CRITICAL	Critical temperature	16	R/$\overline{W}$	00 00

4.4.1 Alarm window trip

The device provides a comparison window with an upper temperature trip point in the alarm upper boundary register, and a lower trip point in the alarm lower boundary register. When enabled, the event output will be triggered whenever entering or exiting (crossing above or below) the alarm window.

4.4.2 Critical trip

The device can be programmed in such a way that the event output is only triggered when the temperature exceeds the critical trip point. The critical temperature setting is programmed in the critical temperature register. When the temperature sensor reaches the critical temperature value in this register, the device is automatically placed in comparator mode, which means that the critical event output cannot be cleared by using software to set the clear event bit.

Table 17. Alarm temperature upper boundary register format

			Sign MSB									LSB(1)		
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit(2) 1**	**Bit(3) 0**
0	**0**	**0**	Alarm window upper boundary temperature											**0**	**0**

1. Bit 2 is LSB for default 10-bit mode.
2. Depending on status of the resolution register, bit 1 may display 0.125 °C value.
3. Depending on status of the resolution register, bit 0 may display 0.0625 °C value.

Table 18. Alarm temperature lower boundary register format

			Sign MSB									LSB(1)		
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit(2) 1**	**Bit(3) 0**
0	**0**	**0**	Alarm window lower boundary temperature											**0**	**0**

1. Bit 2 is LSB for default 10-bit mode.
2. Depending on status of the resolution register, bit 1 may display 0.125 °C value.
3. Depending on status of the resolution register, bit 0 may display 0.0625 °C value.

Table 19. Critical temperature register format

			Sign MSB										LSB(1)		
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit(2) 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit(3) 1**	**Bit(4) 0**
0	**0**	**0**	Critical temperature trip point											**0**	**0**

1. Bit 2 is LSB for default 10-bit mode.
2. If critical trip lockout bit (bit 7 of configuration register in *Table 10*) is set, then this register becomes read-only.
3. Depending on status of the resolution register, bit 1 may display 0.125 °C value.
4. Depending on status of the resolution register, bit 0 may display 0.0625 °C value.

Note: In all temperature register formats bits 0 and bits 1 are used when the resolution is more than 10 bits. These registers show temperature data for the default 10 bits.

4.5 Manufacturer ID register (read-only)

The manufacturer's ID (programmed value 104Ah) in this register is the STMicroelectronics Identification provided by the Peripheral Component Interconnect Special Interest Group (PCiSIG).

Table 20. Manufacturer ID register (read-only)

Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
0	0	0	1	0	0	0	0
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	1	0	0	1	0	1	0

4.6 Device ID and device revision ID register (read-only)

The device IDs and device revision IDs are maintained in this register. The register format is shown in *Table 21*. The device IDs and device revision IDs reflect the current device.

Table 21. Device ID and device revision ID register (read-only)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0	0	1	0	0	0	1	0
Device ID							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	1
Device revision ID							

The current device ID and revision ID value is 2201 h.

4.7 Temperature resolution register (read/write)

With this register a user can program the temperature sensor resolution from 9-12 bits as shown below. The power-on default is always 10 bit (0.25 °C/LSB). The selected resolution is also reflected in bits (4:3) (TRES1:TRES0) of the capability register.

Table 22. Temperature resolution register (TRES) (read/write)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	0	1
Resolution section register						Resolution bits	

Table 23. TRES details

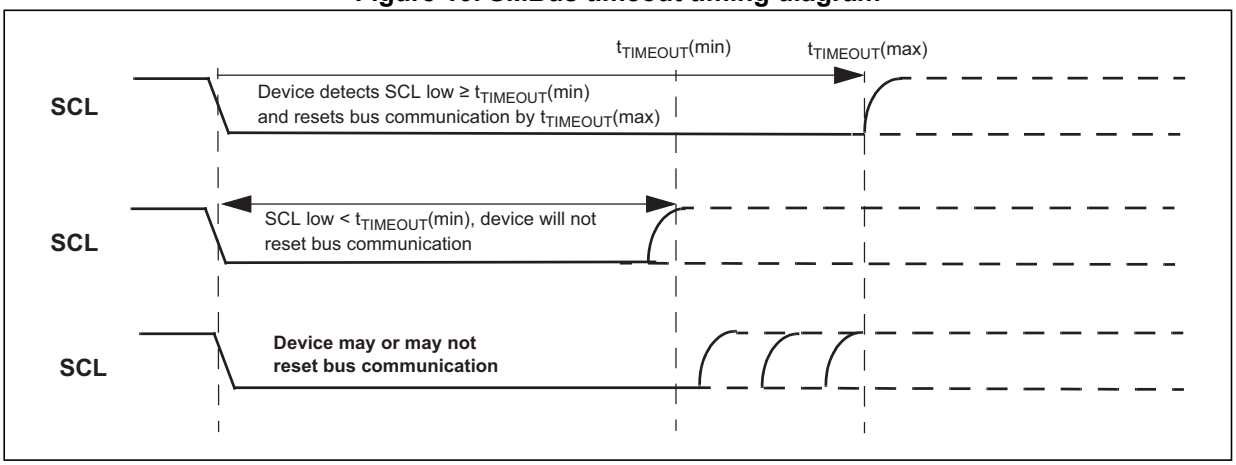
Resolution register bits				
Bit1	**Bit0**	**°C/LSB**	**Bits**	**Conversion time (max)**
0	0	0.5	9	65 ms
0	1	0.25	10	125 ms (default)
1	0	0.125	11	250 ms
1	1	0.0625	12	500 ms

The default value is 01 for TRES register.

4.8 SMBus timeout

The STTS2004 supports the SMBus timeout feature. If the host holds SCL low for more than $t_{timeout}$ (max), the STTS2004 resets itself and releases the bus. This feature is supported even when the device is in shutdown mode and when the device is driving SDA low.

Figure 10. SMBus timeout timing diagram



4.9 Device reset and initialization

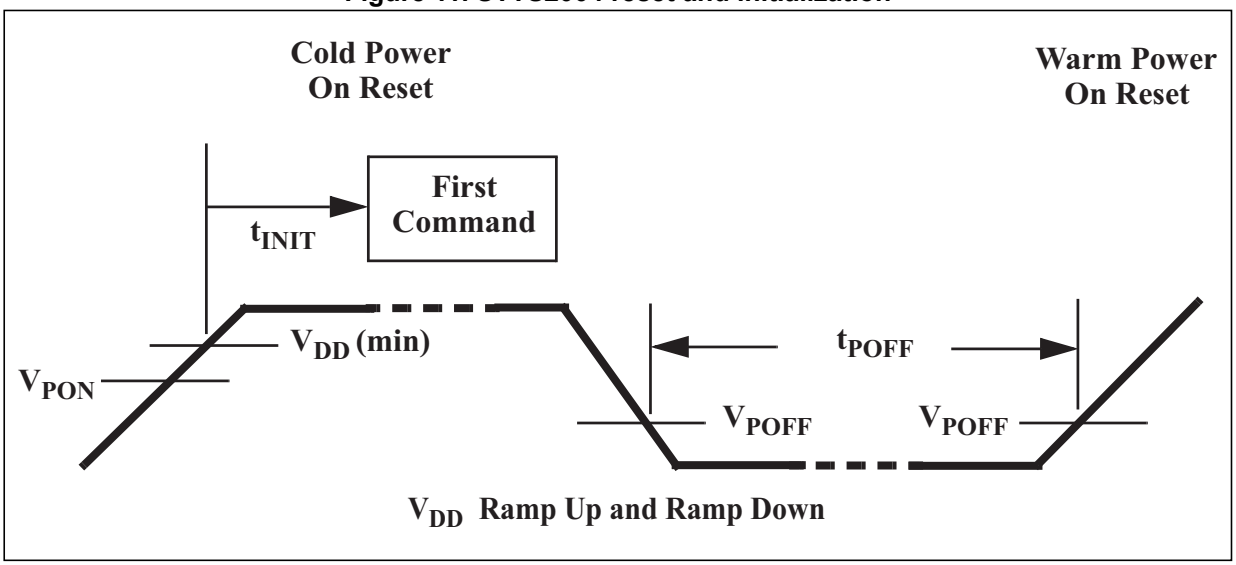
In order to prevent inadvertent operations during power-up, a Power-On Reset (POR) circuit is included. Upon a cold power-on, V_{DD} must rise monotonically between V_{PON} and V_{DD} (min) without ringback to ensure proper startup. Once V_{DD} has passed the V_{PON} threshold, the device is reset.

Prior to selecting the memory and issuing instructions, a valid and stable V_{DD} voltage must be applied, and no command may be issued to the device for t_{INIT}. The supply voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

At power-down (phase during which V_{DD} decreases continuously), as soon as V_{DD} drops from the normal operating voltage below the minimum operating voltage, the device stops responding to commands. Upon warm power cycling, V_{DD} must remain below V_{POFF} for the period t_{POFF}, and must meet cold power-on reset timing when restoring power.

Note: If V_{DD} drops below V_{PON} but stays above V_{POFF}, for less than or greater than t_{POFF}, and then returns to V_{DD}(min), a POR MAY occur.

Figure 11. STTS2004 reset and initialization



Power-up conditions

The V_{DD} voltage has to rise continuously from 0 V up to the minimum V_{DD} operating voltage defined in *Table 29* and the rise time must not vary faster than 1 V/µs.

5 SPD EEPROM operation

5.1 4 Kb SPD EEPROM operation

The STTS2004 includes a 4-Kbit serial EEPROM organized as two pages of 256 bytes each, or 512 bytes of total memory. Each page is composed of two 128-byte blocks. The devices are able to selectively lock the data in any or all of the four 128-byte blocks.

The SPD is a 512-byte EEPROM device designed to operate the two-wire bus at a maximum of 1 MHz transfer rate, in the 2.2 V - 3.6 V voltage range.

The SPD in the STTS2004 is protocol-compatible with the previous operation in the STTS2002. The page selection method allows commands used with the STTS2002 to be applied to the lower or upper pages of the EEPROM.

Individually locking a 128-byte block may be accomplished using a software write protection mechanism in conjunction with a high input voltage V_{HV} on input A0. By sending the device a specific SMBus sequence, each block may be protected from writes until the write protection is electrically reversed using a separate I^2C sequence which also requires V_{HV} on input A0. The write protection for all four blocks is cleared simultaneously, and may be re-asserted after being cleared.

5.2 Internal device reset - SPD EEPROM

In order to prevent inadvertent Write operations during power-up, a Power-On Reset (POR) circuit is included.

At power-up (phase during which V_{DD} is lower than V_{DD}min but increases continuously), the device will not respond to any instruction until V_{DD} has reached the Power-On Reset threshold voltage (this threshold is lower than the minimum V_{DD} operating voltage defined in *Table 29: Operating and AC measurement conditions*). Once V_{DD} has passed the POR threshold, the device is reset.

Prior to selecting the memory and issuing instructions, a valid and stable V_{DD} voltage must be applied. This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

At power-down (phase during which V_{DD} decreases continuously), as soon as V_{DD} drops from the normal operating voltage below the Power-On Reset threshold voltage, the device stops responding to any instruction sent to it.

5.3 Memory addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in *Table 2* (on serial data (SDA), most significant bit first).

The device select code consists of a 4-bit device type identifier, and a 3-bit slave address (A2, A1, A0). To address the memory array, the 4-bit device type identifier is 1010b; to access the write-protection settings, it is 0110b.

Up to eight STTS2004 SPD devices can be connected on a single I^2C bus. Each one is given a unique 3-bit code on the slave address (A0, A1, A2) inputs. When the device select

code is received, the device only responds if the slave address is the same as the value on the slave address (A0, A1, A2) inputs.

The 8th bit is the Read/$\overline{\text{Write}}$ bit ($\overline{\text{RW}}$). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on serial data (SDA) during the 9th bit time. If the device does not match the device select code, it deselects itself from the bus, and goes into standby mode. The operating modes are detailed in *Table 24*.

Table 24. Operating modes

Mode	$\overline{\text{RW}}$ bit	Bytes	Initial sequence
Current address read	1	1	START, device select, $\overline{\text{RW}}$ = 1
Random address read	0	1	START, device select, $\overline{\text{RW}}$ = 0, address
	1		reSTART, device select, $\overline{\text{RW}}$ = 1
Sequential read	1	≥ 1	Similar to current or random address read
Byte write	0	1	START, device select, $\overline{\text{RW}}$ = 0
Page write	0	≤ 16	START, device select, $\overline{\text{RW}}$ = 0
TS write	0	2	START, device select, R/$\overline{\text{W}}$ = 0, pointer data, stop
TS read	1	2	START, device select, R/$\overline{\text{W}}$ = 1, pointer data, stop

5.4 Setting the write protection

There are four independent memory blocks, and each block may be independently

protected. The memory blocks are:

- Block 0 = memory addresses 0x00 to 0x7F (decimal 0 to 127), page address = 0
- Block 1 = memory addresses 0x80 to 0xFF (decimal 128 to 255), page address = 0
- Block 2 = memory addresses 0x00 to 0x7F (decimal 0 to 127), page address = 1
- Block 3 = memory addresses 0x80 to 0xFF (decimal 128 to 255), page address = 1

The device has three software commands for setting, clearing, or interrogating the write protection status.

- SWPn: Set Write Protection for block n
- CWP: Clear Write Protection for all blocks
- RPSn: Read Protection status for block n

The level of write protection (set or cleared), that has been defined using these instructions, remains defined even after a power cycle.

The DTICs of the SWP, CWP, and RPS instructions are defined in *Table 2*.

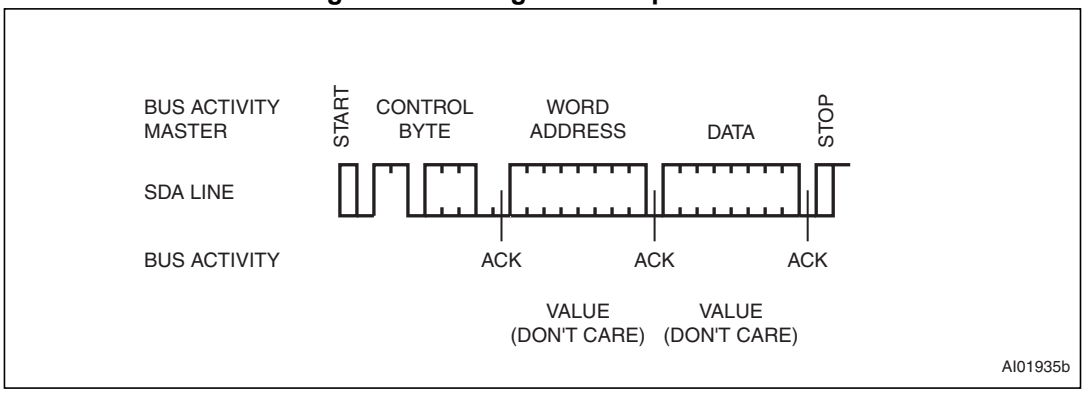
5.4.1 Set and clear the write protection (SWPn and CWP)

If the software write protection has been set with the SWPn instruction, it may be cleared again with a CWP instruction. SWPn acts on a single block as specified in the SWPn command, but CWP clears the write protection for all blocks.

When decoded, SWPn and CWPn trigger a write cycle lasting t_W (see *Table 33*).

The DTICs of the SWP and CWP instructions are defined in *Table 2*.

Figure 12. Setting the write protection



5.4.2 RPSn: read protection status

The controller issues an RPSn command specifying which block to report upon. If the software write protection has not been set, the device replies to the data byte with an Ack. If it has been set, the device replies to the data byte with a NoAck.

5.4.3 SPAn: set SPD page address

The controller issues an SPAn command to select the lower 256 bytes (SPA0) or upper 256 bytes (SPA1). After a cold or warm power-on reset, the SPD page address is always 0, selecting the lower 256 bytes.

5.4.4 RPA: read SPD page address

The controller issues an RPA command to determine if the currently selected SPD page is 0 (device returns Ack) or 1 (device returns NoAck).

5.5 Write operations

Following a Start condition, the bus master sends a device select code with the $\overline{RW}$ bit reset to 0. The device acknowledges this, as shown in *Figure 13*, and waits for an address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

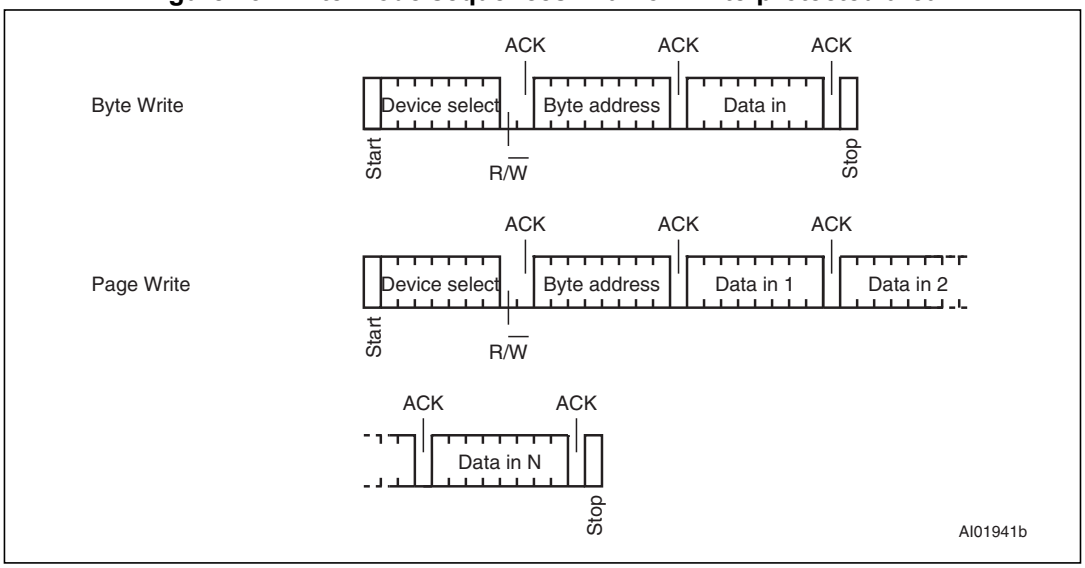
When the bus master generates a Stop condition immediately after a data byte Ack bit (in the “10^{th} bit” time slot), either at the end of a Byte write or a Page write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) and Serial Clock (SCL) are ignored, and the device does not respond to any requests.

5.5.1 Byte write

After the device select code and the address byte, the bus master sends one data byte. If the addressed location is hardware write-protected, the device replies to the data byte with NoAck, and the location is not modified. If, instead, the addressed location is not write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 13*.

Figure 13. Write mode sequences in a non write-protected area



5.5.2 Page write

The Page write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits are the same. If more bytes are sent than will fit up to the end of the page, a condition known as ‘roll-over’ occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

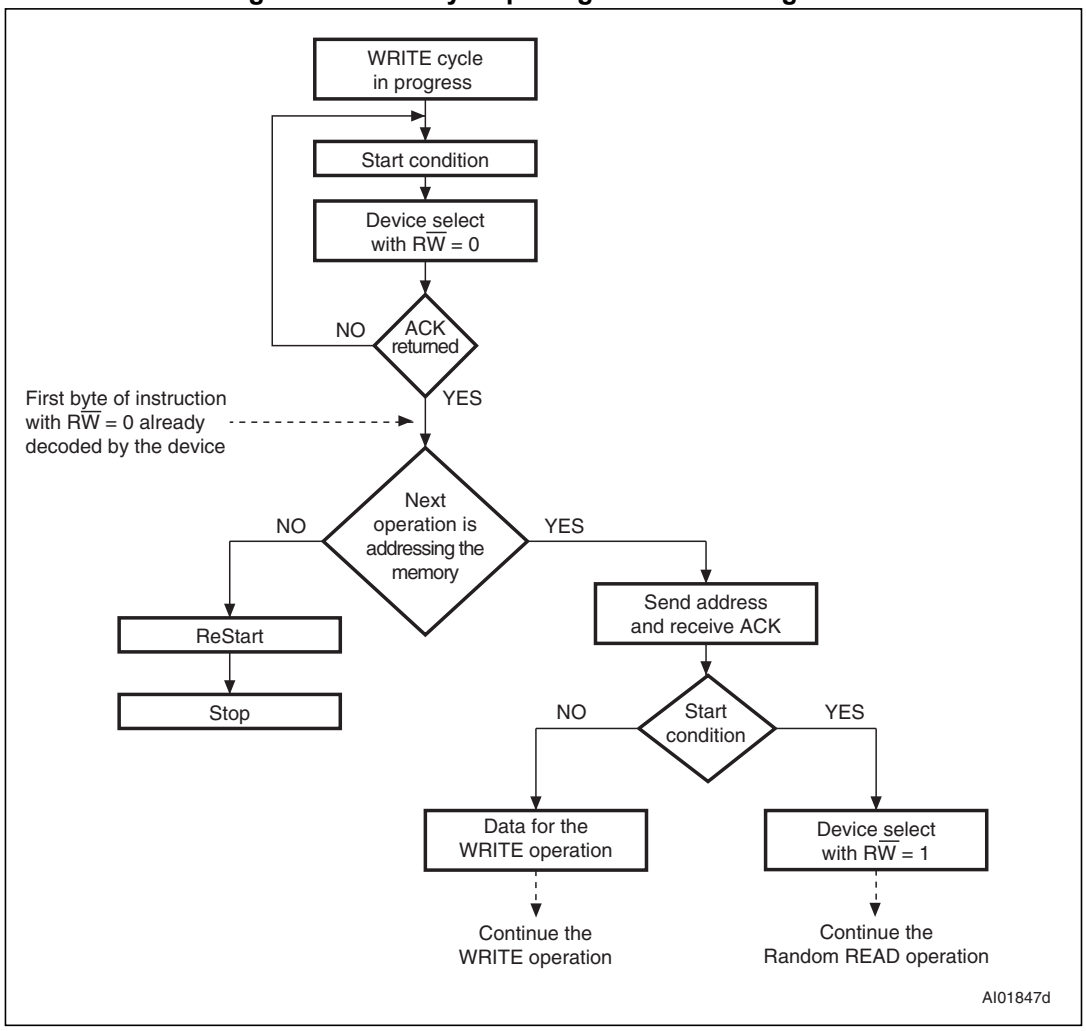
The bus master sends from 1 to 16 bytes of data, each of which is acknowledged by the device if Write Control ($\overline{WC}$) is low. If the addressed location is hardware write-protected, the device replies to the data byte with NoAck, and the locations are not modified. After each byte is transferred, the internal byte address counter (the 4 least significant address bits only) is incremented. The transfer is terminated by the bus master generating a Stop condition.

5.5.3 Minimizing system delays by polling on ACK

The sequence, as shown in *Figure 14*, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 14. Write cycle polling flowchart using ACK



During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_w) is shown in *Table 33*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

5.6 Read operations

Read operations are performed independently of whether a hardware or software protection has been set.

The device has an internal address counter which is incremented each time a byte is read.

5.6.1 Random address read

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 15*) but without sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the RW bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must not acknowledge the byte, and terminates the transfer with a Stop condition.

5.6.2 Current address read

For the Current address read operation, following a Start condition, the bus master only sends a device select code with the RW bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 15*, without acknowledging the byte.

5.6.3 Sequential read

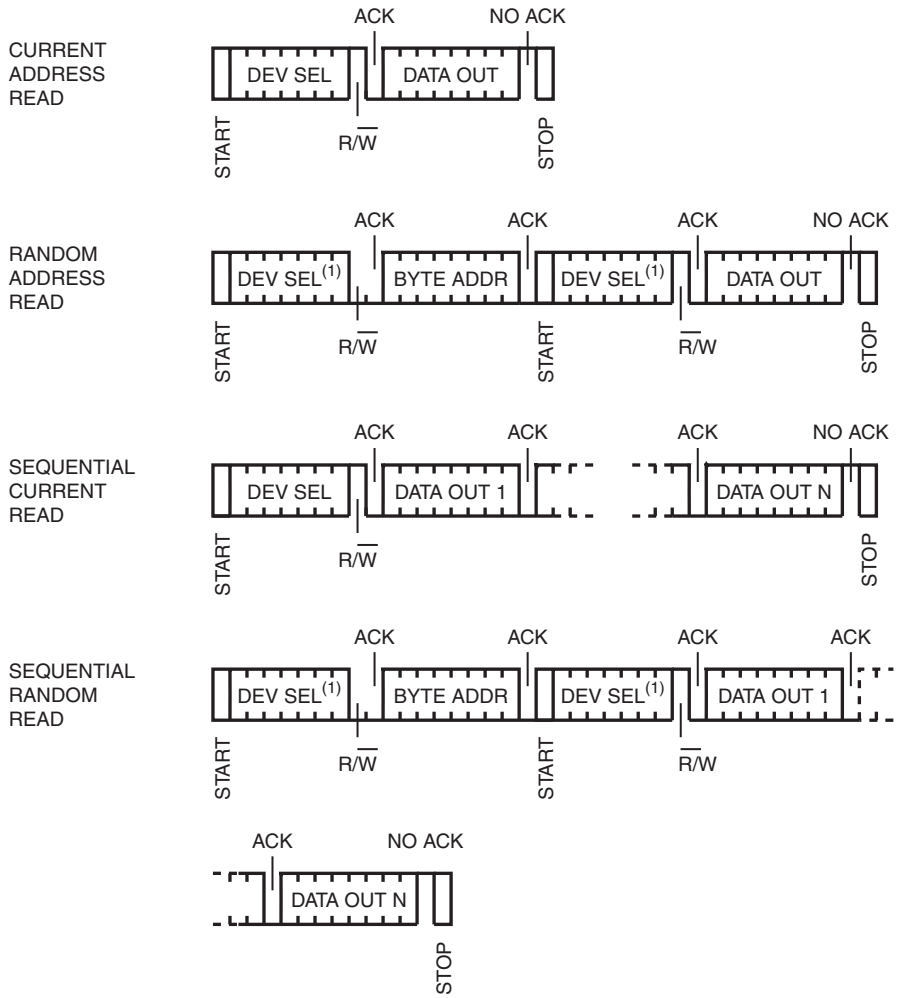
This operation can be used after a current address read or a random address read. The bus master does acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must not acknowledge the last byte, and must generate a Stop condition, as shown in *Figure 15*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

5.6.4 Acknowledge in read mode

For all Read commands, after each byte read, the device waits for an acknowledgment during the 9^{th} bit time. If the bus master does not drive Serial Data (SDA) low during thistime, the device terminates the data transfer and switches to its Standby mode.

Figure 15. Read mode sequences



6 Use in a memory module

In the Dual In line Memory Module (DIMM) application, the SPD is soldered directly on to the printed circuit module. The three slave address inputs (A0, A1, A2) must be connected to V_{SS} or V_{DD} directly (that is without using a pull-up or pull-down resistor) through the DIMM socket (see *Table 25*).

Table 25. DRAM DIMM connections

DIMM position	A2	A1	A0
0	V_{SS} (0)	V_{SS} (0)	V_{SS} (0)
1	V_{SS}(0)	V_{SS} (0)	V_{DD} (1)
2	V_{SS} (0)	V_{DD} (1)	V_{SS} (0)
3	V_{SS} (0)	V_{DD} (1)	V_{DD}(1)
4	V_{DD} (1)	V_{SS} (0)	V_{SS} (0)
5	V_{DD} (1)	V_{SS} (0)	V_{DD} (1)
6	V_{DD} (1)	V_{DD} (1)	V_{SS} (0)
7	V_{DD} (1)	V_{DD} (1)	V_{DD} (1)

6.1 Programming the SPD

The SPD EEPROM can be programmed when:

- the DIMM is isolated (not inserted on the PCB motherboard)
- the DIMM is inserted on the PCB motherboard

6.1.1 Isolated DIMM

With specific programming equipment, it is possible to define the SPD EEPROM content using byte and page write instructions, and to set its write-protection using the SWPn and CWP instructions. To issue the SWPn and CWP instructions, the DIMM must be inserted in the application-specific slot where the A0 signal must be driven to V_{HV} during the whole instruction. This programming step is mainly intended for use by DIMM makers, whose end-application manufacturers will want to clear this write-protection with the CWP on their own specific programming equipment, to modify the protection bytes.

The read protection status (RPSn), Set SPD Page address (SPAn), and the Read SPD Page Address (RPA) commands are fully supported when the DIMM is isolated.

6.1.2 DIMM inserted in the application motherboard

As the final application cannot drive the A0 pin to V_{HV}, this option is not available.

Table 26 and *Table 27* show how the Ack bits can be used to identify the write-protection status.

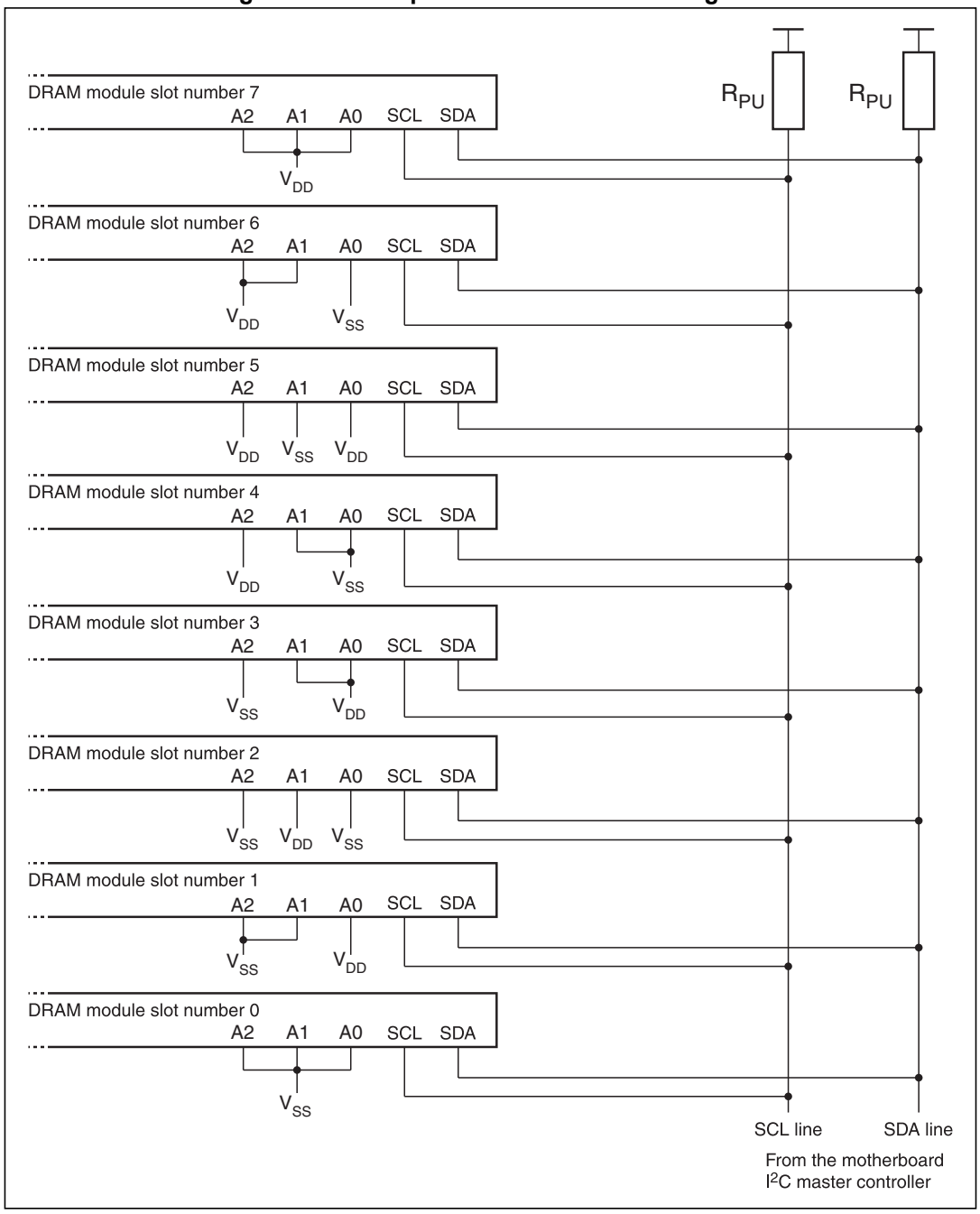
Table 26. Acknowledge when writing data or defining the write-protection status (instructions with R/W_n bit = 0)

Status	Instruction	Ack	Address	Ack	Data byte	Ack	Write cycle (t_W)
Protected	SWPn	NoAck	Not significant	NoAck	Not significant	NoAck	No
	CWP	Ack	Not significant	Ack	Not significant	Ack	Yes
	Page or byte write in protected block	Ack	Address	Ack	Data	NoAck	No
Not protected	SWPn or CWP	Ack	Not significant	Ack	Not significant	Ack	Yes
	Page or byte write	Ack	Address	Ack	Data	Ack	Yes

Table 27. Acknowledge when reading the protection status (instructions with R/W_n bit = 1)

SWPn status	Instruction	Ack	Address	Ack	Data byte	Ack
Set	RPSn	NoAck	Not significant	NoAck	Not significant	NoAck
Not set	RPSn	Ack	Not significant	NoAck	Not significant	NoAck

Figure 16. Serial presence detect block diagram



1. A2, A1 and A0 are wired at each DRAM module slot in a binary sequence for a maximum of 8 devices.
2. Common clock and common data are shared across all the devices.

7 Maximum ratings

Stressing the device above the ratings listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 28. Absolute maximum ratings

Symbol	Parameter		Value	Unit
T_{STG}	Storage temperature		–65 to 150	°C
T_{SLD}(1)	Lead solder temperature for 10 seconds		260	°C
V_{IO}	Input or output voltage	A0	V_{SS} – 0.3 to 10.0	V
		others	V_{SS} – 0.3 to 4.3	V
V_{DD}	Supply voltage		V_{SS} – 0.3 to 4.3	V
I_O	Output current		10	mA
P_D	Power dissipation		320	mW
θ_{JA}	Thermal resistance		87.4	°C/W

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.

8 DC and AC parameters

This section summarizes the operating measurement conditions, and the dc and ac characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in *Table 29*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 29. Operating and AC measurement conditions

Parameter	Conditions	Unit
V_{DD} supply voltage	2.2 to 3.6	V
Operating temperature	–20 to 125	°C
Input rise and fall times	≤ 50	ns
Load capacitance	100	pf
Input pulse voltages	$0.2V_{DD}$ to $0.8V_{DD}$	V
Input and output timing reference voltages	$0.3V_{DD}$ to $0.7V_{DD}$	V

Figure 17. AC measurement I/O waveform

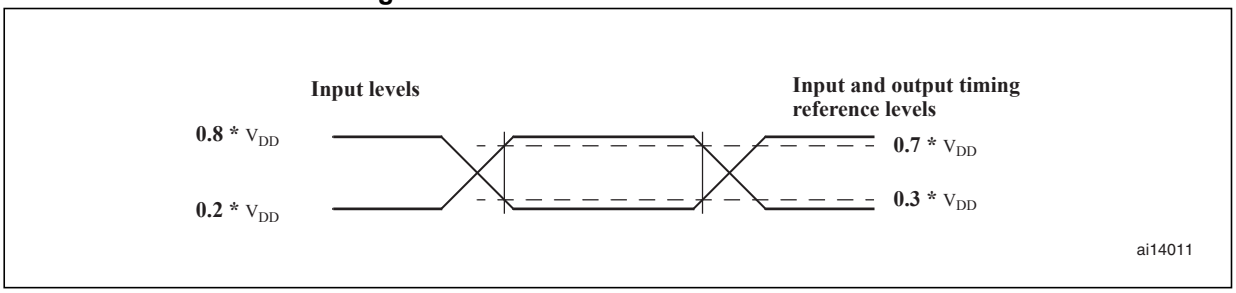


Table 30. DC characteristics - temperature sensor component with EEPROM

Sym	Description	Test condition(1)	Min	Typ(2)	Max	Unit
V_{DD}	Supply voltage		2.2	3.3	3.6	V
I_{DD}	V_{DD} supply current (no load)	EEPROM active(3) F = 1000 kHz		0.4	2.0	mA
		EEPROM standby, F = 1000 kHz		160	350	µA
I_{DDW}	V_{DD} supply current (write)	V_{DD} = 3.3 V, F = 1000 kHz(4)			3	mA
I_{DD1}	Shutdown mode supply current	EEPROM standby, TS shutdown		3	5	µA
I_{ILI}	Input leakage current (SCL, SDA)	V_{IN} = V_{SS} or V_{DD}			±5	µA
I_{ILO}	Output leakage current	V_{OUT} = V_{SS} or V_{DD}, SDA in Hi-Z			±5	µA

Table 30. DC characteristics - temperature sensor component with EEPROM (continued)

Sym	Description	Test condition(1)	Min	Typ(2)	Max	Unit
V_{IL}	Input logic low	SCL, SDA, A0-A2	–0.5		$0.3V_{DD}$	V
V_{IH}	Input logic high	SCL, SDA, A0-A2	$0.7V_{DD}$		V_{DD} + 1.0	V
f_{SCL}	I^2C clock frequency		10		1000	kHz
$t_{timeout}$	SMBus timeout		25		35	ms
V_{HV}	A0 high voltage	$V_{HV} \geq V_{DD} + 4.8$ V	7		10	V
V_{OL1}	Output low voltage	I_{OL} = 3.0 mA, V_{DD} > 2.2 V			0.4	V
I_{OL}	Low-level output current	V_{OL} = 0.4 V	20			mA
V_{HYST}	Input hysteresis (SCL, SDA)		$0.05V_{DD}$			V
V_{PON}	Power-on reset (POR) threshold	Monotonic rise between V_{PON} and V_{DD} (min) without ringback	1.6			V
V_{POFF}	Power-off threshold for warm power-on cycle				0.9	V
V_{PU}	$\overline{EVENT}$ pin pull-up voltage				V_{DD} + 1.0	V

1. Guaranteed operating temperature for combined module: T_A = –20 °C to 125 °C; V_{DD} = 2.2 V to 3.6 V (except where noted).
2. Typical numbers taken at V_{DD} = 3.3 V, T_A = 25 °C.
3. Read current only
4. Verified by design and characterization, not necessarily tested on all devices

Table 31. Input parameters

Symbol	Parameter(1)	Test condition	Min	Max	Units
C_{IN}	Input capacitance			8	pF
Z_{AIL}	A0, A1, A2 input impedance	V_{IN} < 0.3 V_{DD}	30		kΩ
Z_{AIH}	A0, A1, A2 input impedance	V_{IN} > 0.7$_{VDD}$	800		kΩ
t_{SP}	Spike suppression pulse width of spikes that must be suppressed by the input filter on SCL and SDA			50	ns

1. Verified by design and characterization, not necessarily tested on all devices

Table 32. Temperature to digital conversion performance

Symbol	Parameter	Test condition	Min	Typ	Max	Units
B-grade	Accuracy for corresponding range 2.2 V . VDD . 3.6 V	+75 °C < T_A < +95		±0.5	±1.0	°C
		+40 °C < T_A < +125		±1.0	±2.0	
		–20 °C < T_A < +125		±2.0	±3.0	
	Resolution		0.5	0.25	0.0625	°C/LSB
			9	10	12	bits
t_{CONV}	Conversion time	10-bit - default		70	125	ms

Figure 18. SMBus/I^{2}C timing diagram

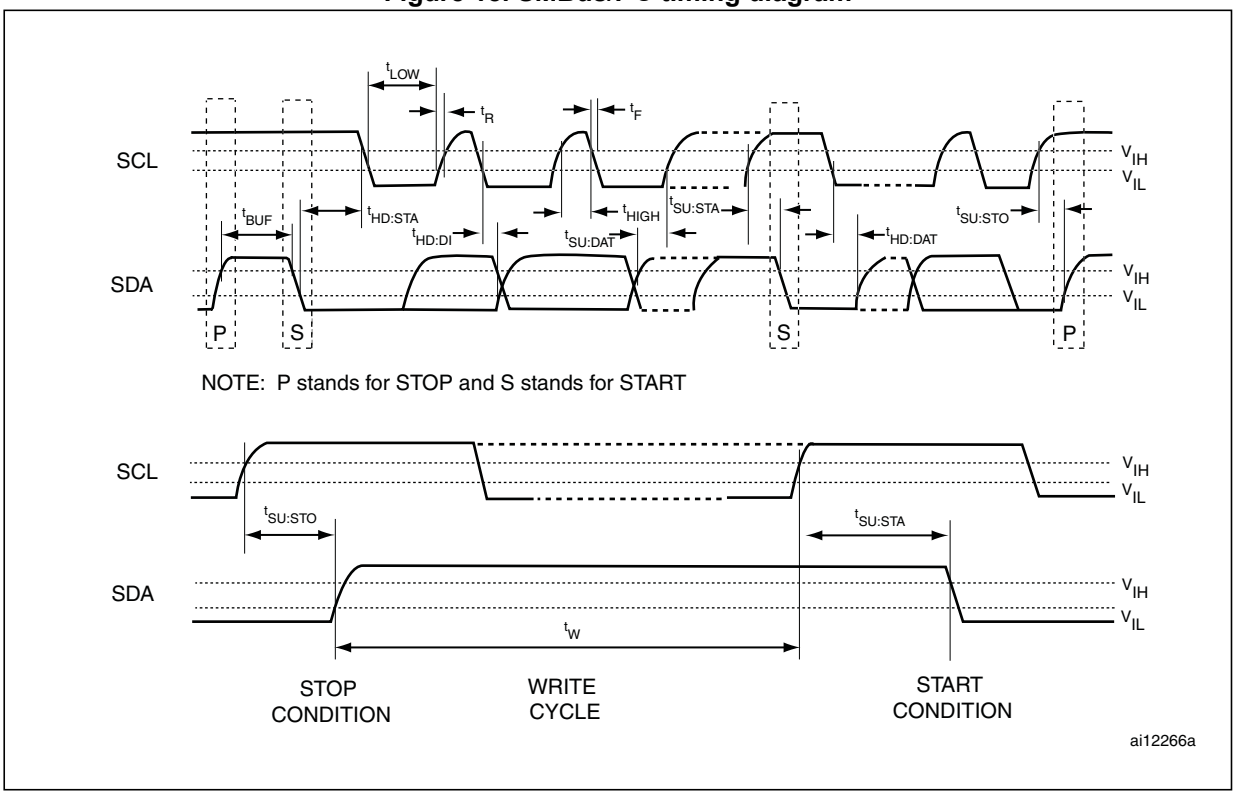


Table 33. AC characteristics of STTS2004 for SMBus and I²C compatibility timings

Symbol	Parameter	Min	Max	Units
f_{SCL}	I²C clock frequency	10	1000	kHz
t_{HIGH}	Clock high period	260	–	ns
t_{LOW}(1)	Clock low period	500	–	ns
t_R(2)	Clock/data rise time	–	120	ns
t_F(2)	Clock/data fall time	–	120	ns
$t_{SU:DAT}$	Data-in setup time	50	–	ns
$t_{HD:DI}$	Data-in hold time	0	–	ns
$t_{HD:DAT}$	Data-out hold time	0	350	ns
$t_{SU:STA}$(3)	Repeated start condition setup time	260	–	ns
$t_{HD:STA}$	Hold time after (repeated) start condition. After this period, the first clock cycle is generated.	260	–	ns
$t_{SU:STO}$	Stop condition setup time	260	–	ns
t_{BUF}	Bus free time between stop (P) and start (S) conditions	500	–	ns
t_W(4)	WRITE time for EEPROM	–	5	ms
$t_{timeout}$(5)	Bus timeout	25	35	ms
t_{POFF}	Warm power cycle off time	1	–	ms
t_{INIT}	Time from power-on to first command	10	–	ms
C_B(6)	Capacitive load for each bus line		550	pf

1. The STTS2004 will not initiate clock stretching which is an I²C bus optional feature.
2. Guaranteed by design and characterization, not necessarily tested.
3. For a restart condition, or following a WRITE cycle.
4. This parameter reflects maximum WRITE time for EEPROM.
5. The I²C bus masters can terminate a transaction in process and reset devices on the bus by asserting SCL low for $t_{TIMEOUT,MAX}$ or longer. The STTS2004, upon detecting this condition, will reset communication and be able to receive a new START condition no later than $t_{TIMEOUT,MAX}$. The STTS2004 will not reset if SCL stretching is less than $t_{TIMEOUT,MIN}$.
6. The maximum bus capacitance allowable may vary from this value depending on the actual operating voltage and frequency of the application.

Figure 19. Maximum R_{PU} value versus bus parasitic capacitance (C_{BUS}) for an I^2C bus at maximum frequency f_C = 1 MHz

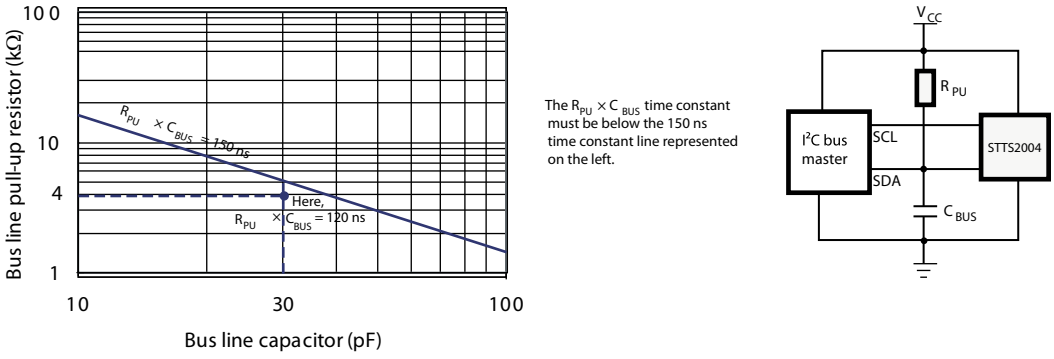
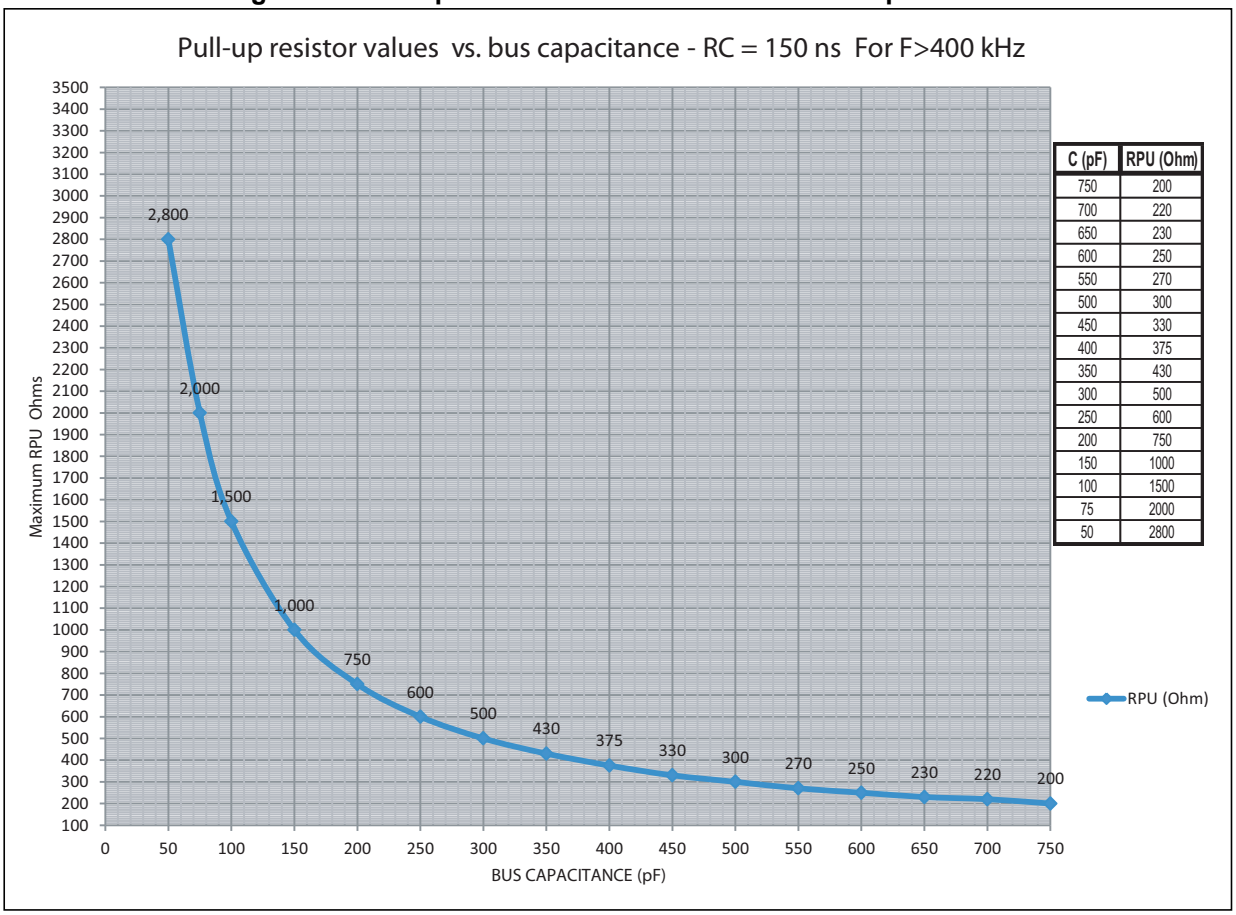


Figure 20. Pull-up resistor values versus bus line capacitance

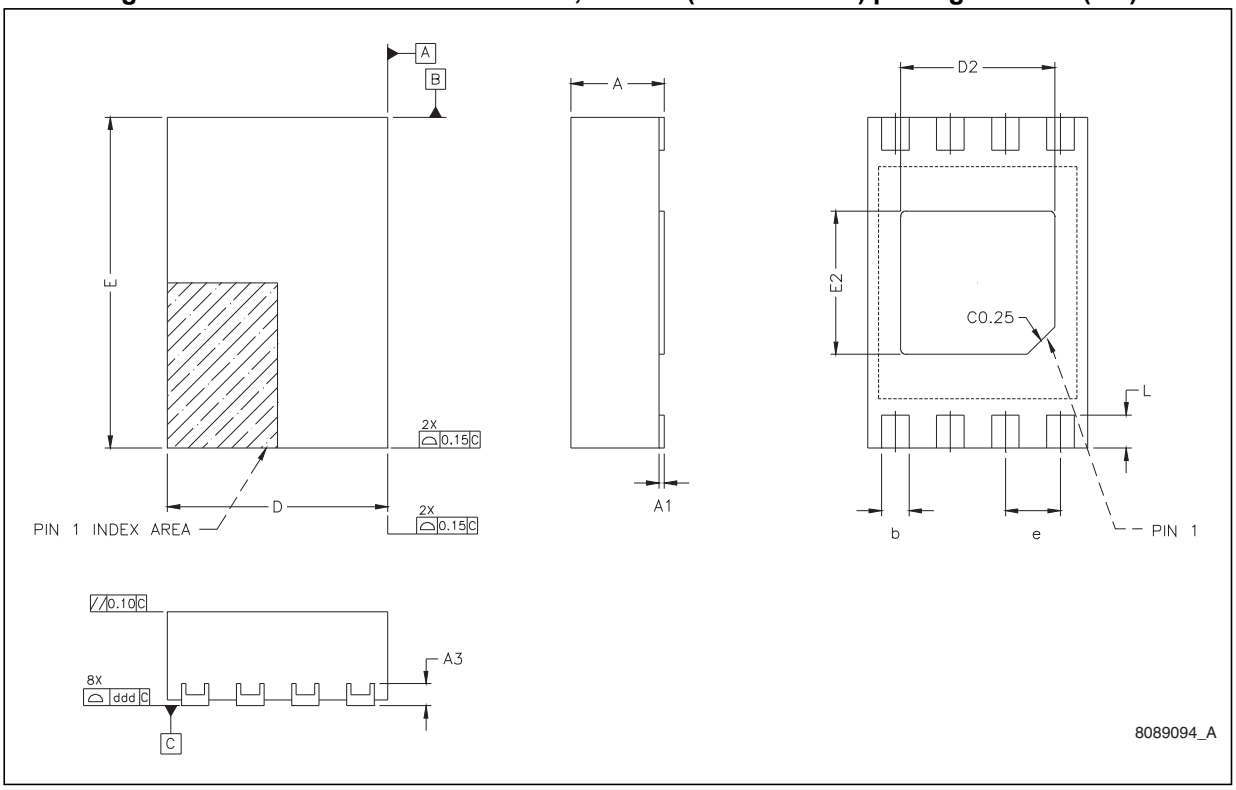


C (pF)	RPU (Ohm)
750	200
700	220
650	230
600	250
550	270
500	300
450	330
400	375
350	430
300	500
250	600
200	750
150	1000
100	1500
75	2000
50	2800

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 21. TDFN8 – 8-lead thin dual flat, no-lead (2 mm x 3 mm) package outline (DN)



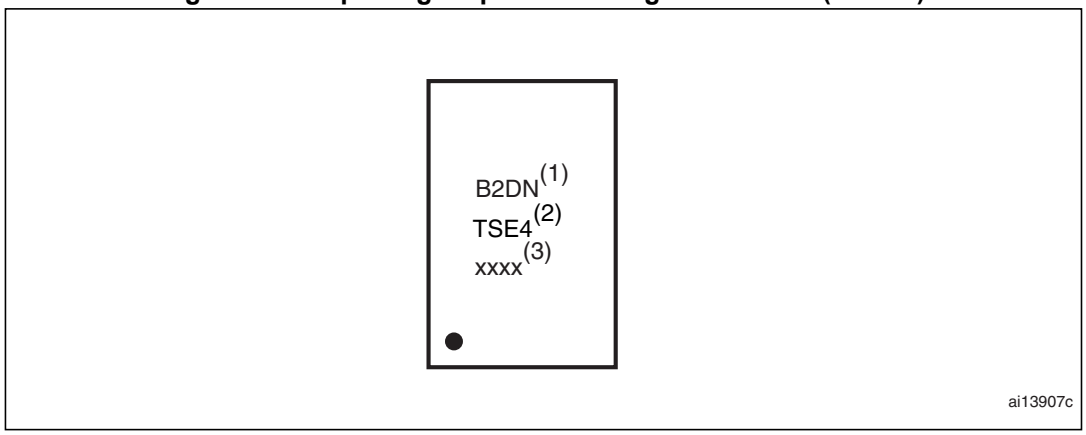
Note: JEDEC MO-229, variation W2030D

Table 34. TDFN8 – 8-lead thin dual flat, no-lead (2 mm x 3 mm) mechanical data (DN)

Sym	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.00	0.05	0.000	0.000	0.002
A3		0.20			0.008	
b	0.20	0.25	0.30	0.008	0.010	0.012
D	1.95	2.00	2.05	0.077	0.079	0.081
D2	1.35	1.40	1.45	0.053	0.055	0.057
E	2.95	3.00	3.05	0.116	0.118	0.120
E2	1.25	1.30	1.35	0.049	0.051	0.053
e		0.50			0.020	
L	0.30	0.35	0.40	0.012	0.014	0.016
ddd			0.08			0.003

Note: JEDEC MO-229, variation W2030D

Figure 22. DN package topside marking information (TDFN8)



1. Temperature grade and package
   B = B-grade, stacked
   2 = Minimum operating voltage of 2.2 V
   DN = 0.80 mm TDFN package
2. Device name
   TSE4 = STTS2004
3. Traceability codes

The landing pattern recommendations per the JEDEC proposal for the TDFN package (DN) are shown in *Figure 23*.

The preferred implementation with wide corner pads enhances device centering during assembly, but a narrower option is defined for modules with tight routing requirements.

Figure 23. Landing pattern - TDFN8 package (DN)

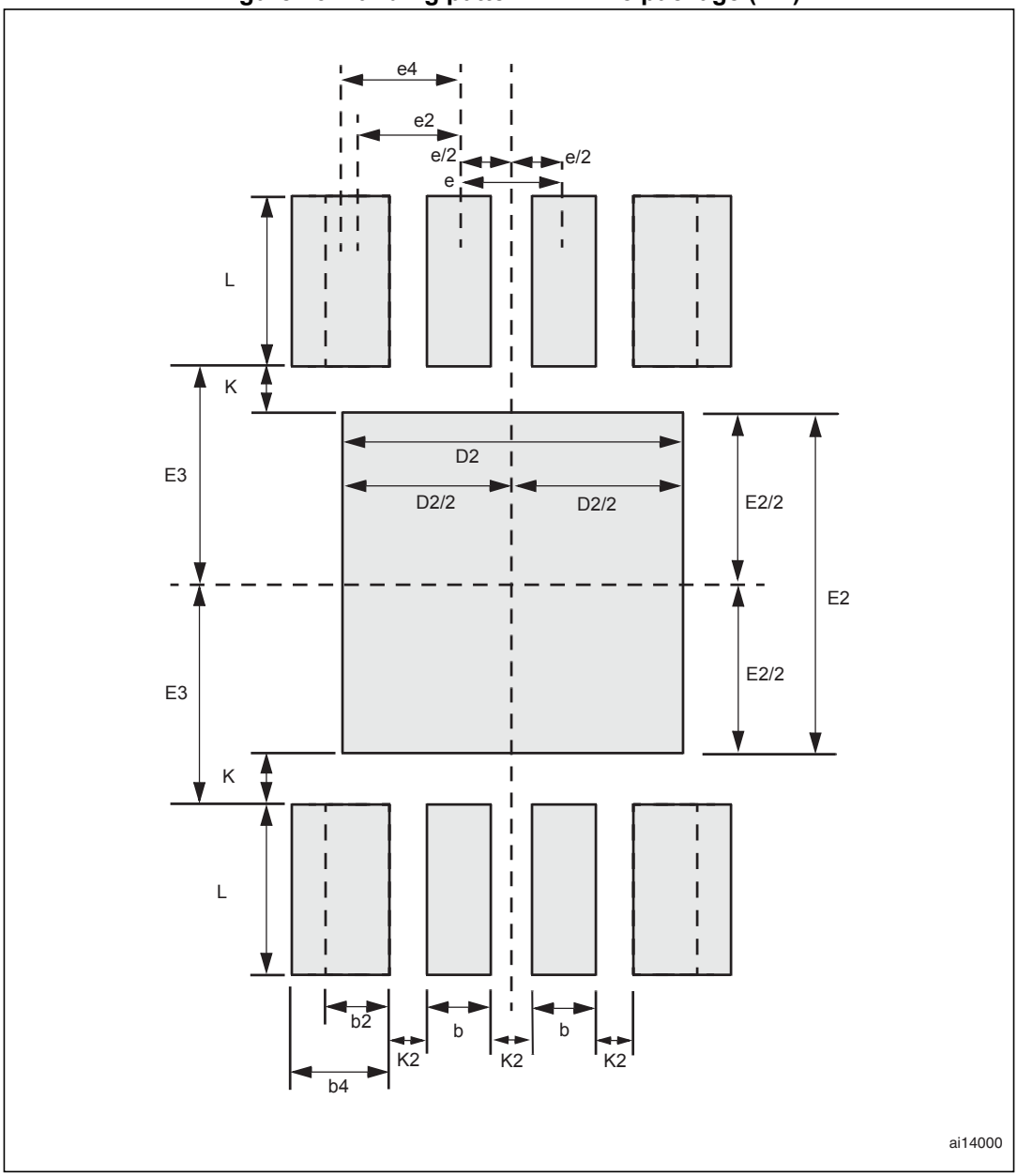


Table 35 lists variations of landing pattern implementations, ranked as “Preferred” and Minimum Acceptable” based on the JEDEC proposal.

Table 35. Parameters for landing pattern - TDFN8 package (DN)

Parameter	Description	Dimension		
		Min	Nom	Max
D2	Heat paddle width	1.40	-	1.60
E2	Heat paddle height	1.40	-	1.60
E3	Heat paddle centerline to contact inner locus	1.00	-	-
L	Contact length	0.70	-	0.80
K	Heat paddle to contact keepout	0.20	-	-
K2	Contact to contact keepout	0.20	-	-
e	Contact centerline to contact centerline pitch for inner contacts	-	0.50	-
b	Contact width for inner contacts	0.25	-	0.30
e2	Landing pattern centerline to outer contact centerline, “minimum acceptable” option(1)	-	0.50	-
b2	Corner contact width, “minimum acceptable option”(1)	0.25	-	0.30
e4	Landing pattern centerline to outer contact centerline, “preferred” option(2)	-	0.60	-
b4	Corner contact width, “preferred” option(2)	0.45	-	0.50

1. Minimum acceptable option to be used when routing prevents preferred width contact.
2. Preferred option to be used when possible.

10 Part numbering

Table 36. Ordering information scheme

Example: STTS2004 B 2 DN 3 F

Device

STTS2004

Accuracy grade

B: Maximum accuracy 75 °C to 95 °C = ± 1 °C

Voltage

2 = 2.2 V - 3.6 V

Package

DN = TDFN8

Temperature range

3 = –20 °C to 125 °C

Shipping method

F = ECOPACK® package, tape & reel packing

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

11 Revision history

Table 37. Document revision history

Date	Revision	Changes
22-Feb-2013	1	Initial release
28-Aug-2013	2	Document status promoted from preliminary to production data Updated *Table 30: DC characteristics - temperature sensor component with EEPROM* Added *Table 31: Input parameters* Added *Table 32: Temperature to digital conversion performance* Moved *Figure 18: SMBus/I²C timing diagram* to *Section 8* Updated and moved *Table 33: AC characteristics of STTS2004 for SMBus and I²C compatibility timings* to *Section 8*
18-Oct-2013	3	Updated V_{PU} in *Table 30: DC characteristics - temperature sensor component with EEPROM*
28-Jan-2019	4	Removed tape and reel information from *Section 9: Package information*

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