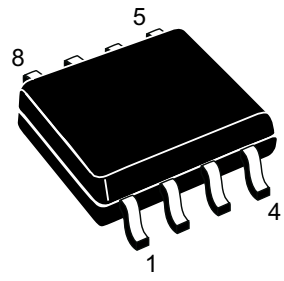
STS5P3LLH6

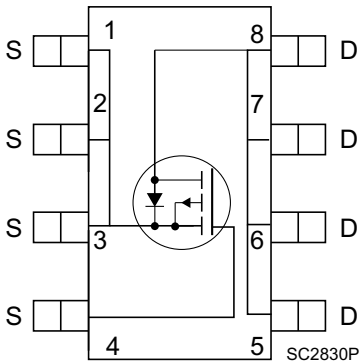
P-channel 30 V, 0.048 Ω typ., 5 A STripFET™ H6 DeepGATE™ Power MOSFET in an SO-8 package

Datasheet - preliminary data



SO-8

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STS5P3LLH6	30 V	0.056 Ω at 10 V	5 A

- Very low on-resistance $R_{DS(on)}$
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order code	Marking	Package	Packaging
STS5P3LLH6	5K3L	SO-8	Tape and reel

Note: For the P-channel MOSFET actual polarity of voltages and current has to be reversed.

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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2.1 Electrical characteristics (curves) 6

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_{amb} = 25 °C	5	A
I_D	Drain current (continuous) at T_{amb} = 100 °C	3.2	A
I_{DM} (1)	Drain current (pulsed)	20	A
P_{TOT}	Total dissipation at T_{amb} = 25 °C	2.7	W
T_J	Operating junction temperature	150	°C
T_{stg}	Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}amb}$ (1)	Thermal resistance junction-amb	47	°C/W

1. When mounted on 1 inch² FR-4 board, 2 oz. Cu., t ≤ 10 sec

Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 30 V,			1	µA
		V_{GS} = 0 V, V_{DS} = 30 V, T_J = 125 °C			10	
I_{GSS}	Gate body leakage current	V_{DS} = 0, V_{GS} = ±20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.5 A		0.048	0.056	Ω
		V_{GS} = 4.5 V, I_D = 2.5 A		0.075	0.09	

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f=1 MHz V_{GS} = 0	-	639	-	pF
C_{oss}	Output capacitance		-	79	-	
C_{rss}	Reverse transfer capacitance		-	52	-	
Q_g	Total gate charge	V_{DD} = 15 V, I_D = 5 A V_{GS} = 4.5 V	-	6	-	nC
Q_{gs}	Gate-source charge		-	1.9	-	
Q_{gd}	Gate-drain charge		-	2.1	-	

Table 6. Switching times

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 15 V, I_D = 5 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	5.4	-	ns
t_r	Rise time		-	5	-	
$t_{d(off)}$	Turn-off delay time		-	19.2	-	
t_f	Fall time		-	3.4	-	

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 5 A, V_{GS} = 0	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs, V_{DD}= 16 V, T_J = 150 °C	-	11.2		ns
Q_{rr}	Reverse recovery charge		-	3.5		nC
I_{RRM}	Reverse recovery current		-	0.6		A

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Note: For the P-channel MOSFET the actual polarity of the voltages and the current must be reversed.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

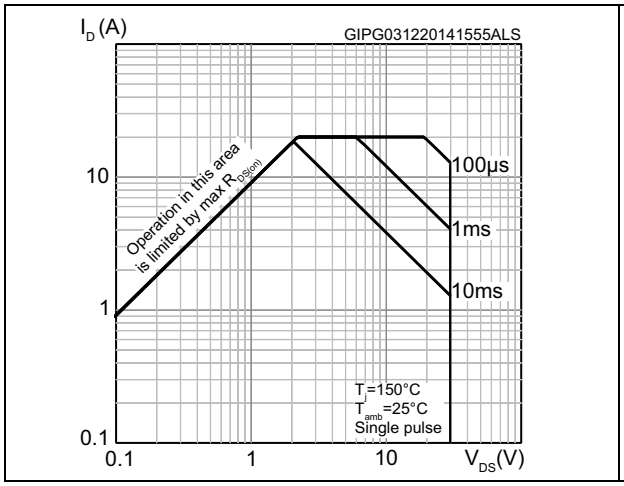


Figure 3. Thermal impedance

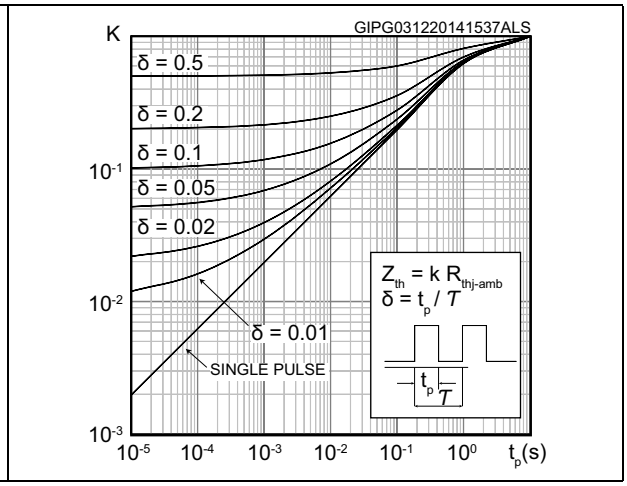


Figure 4. Output characteristics

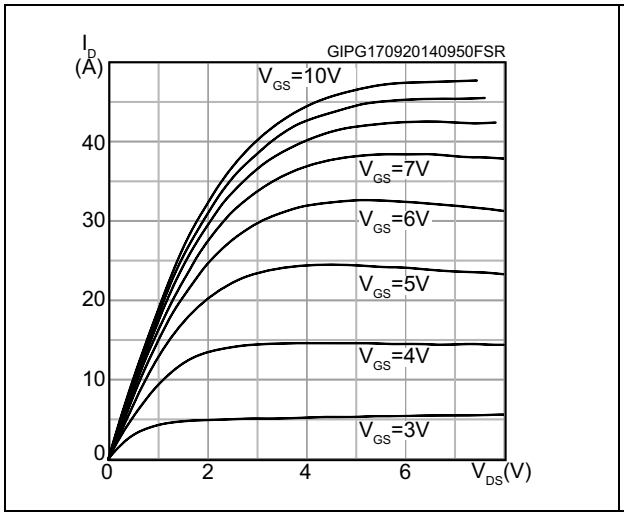


Figure 5. Transfer characteristics

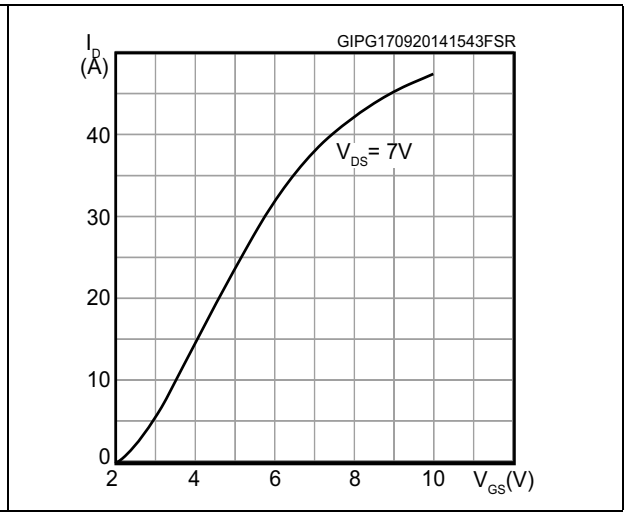


Figure 6. Gate charge vs gate-source voltage

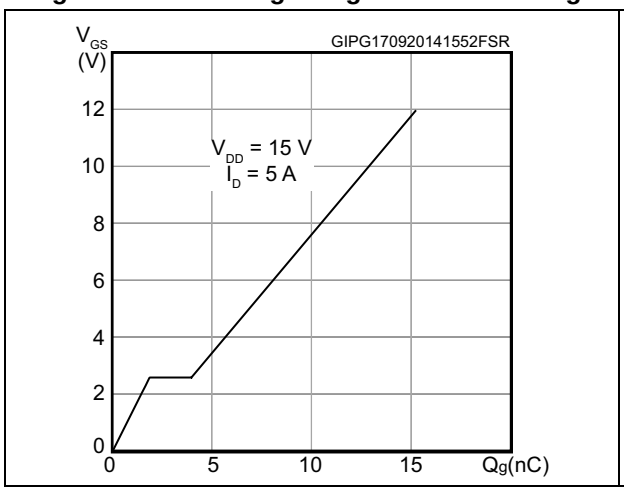


Figure 7. Static drain-source on-resistance

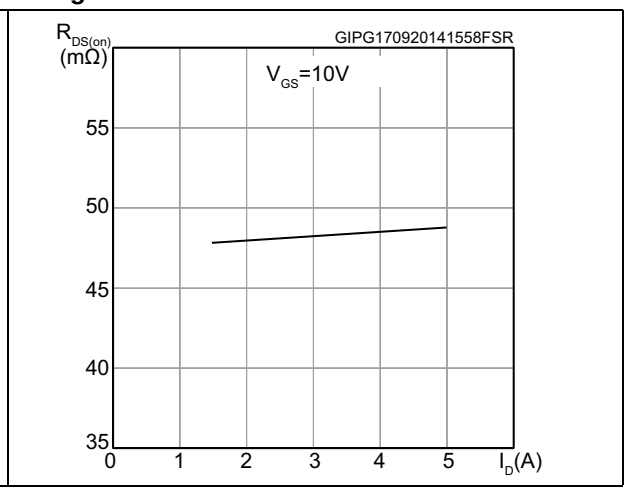


Figure 8. Normalized $V_{(BR)DSS}$ vs temperature

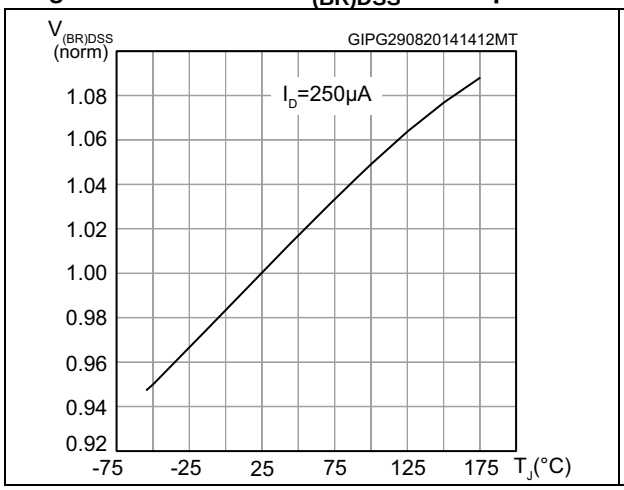


Figure 9. Capacitance variations

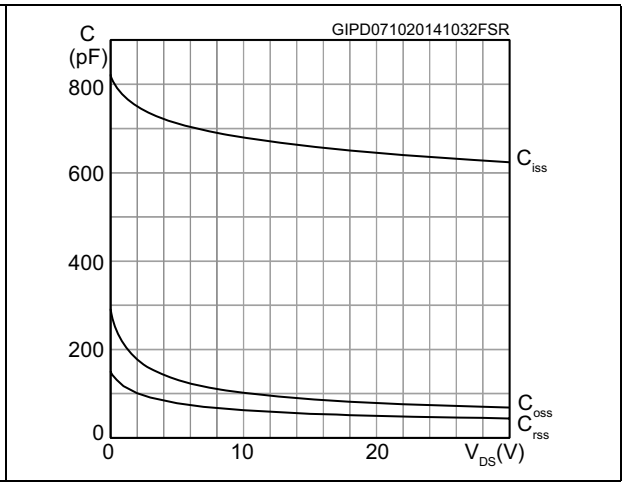


Figure 10. Normalized gate threshold voltage vs. temperature

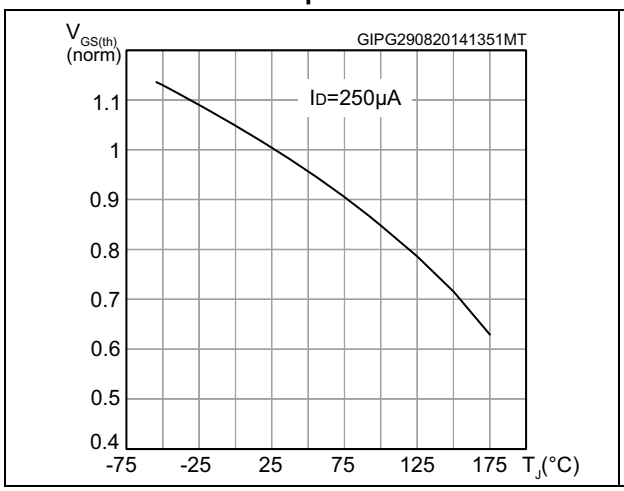


Figure 11. Normalized on-resistance vs. temperature

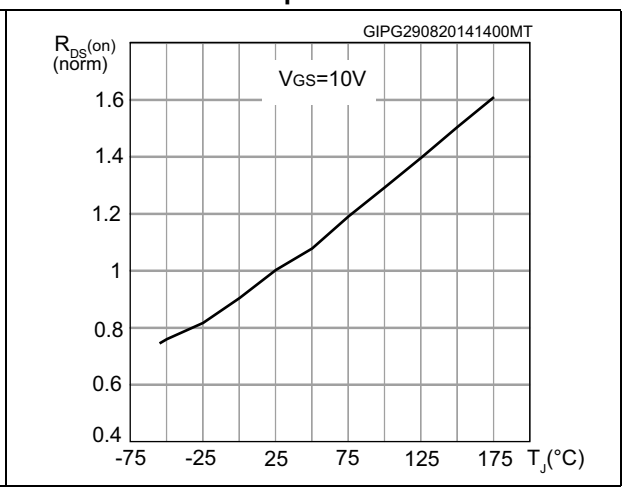
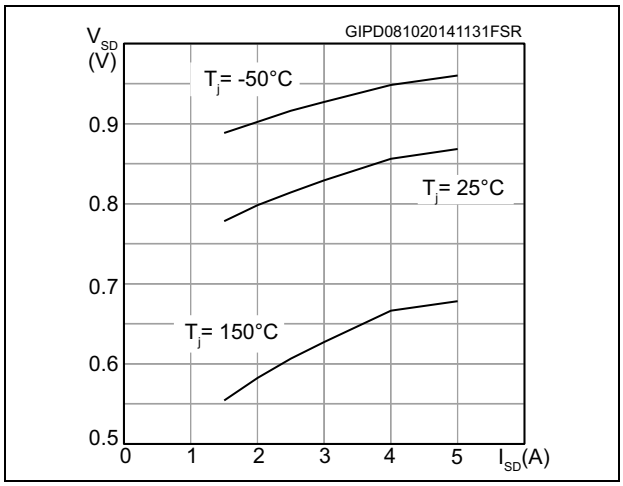


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

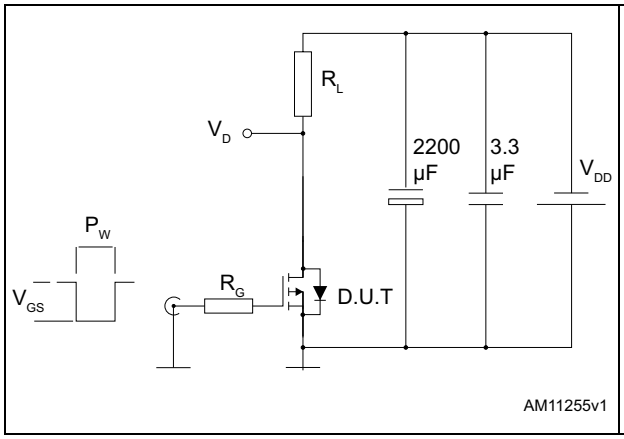


Figure 14. Gate charge test circuit

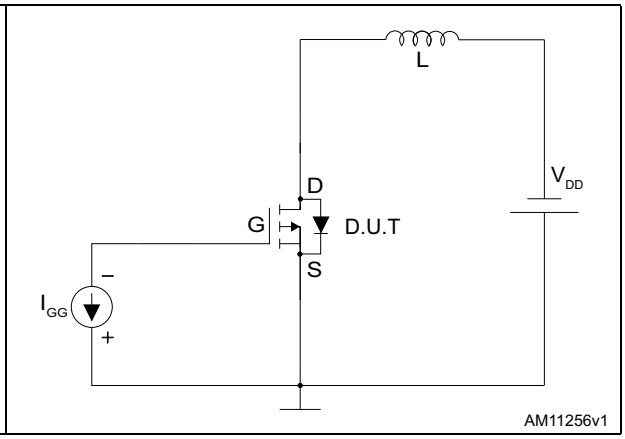
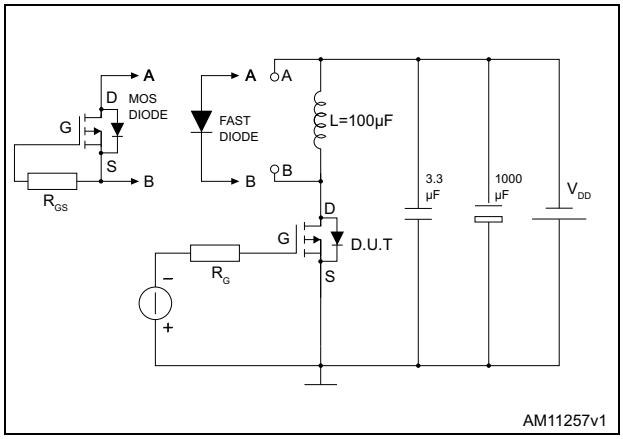


Figure 15. Test circuit for inductive load switching and diode recovery times



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 16. SO-8 drawing

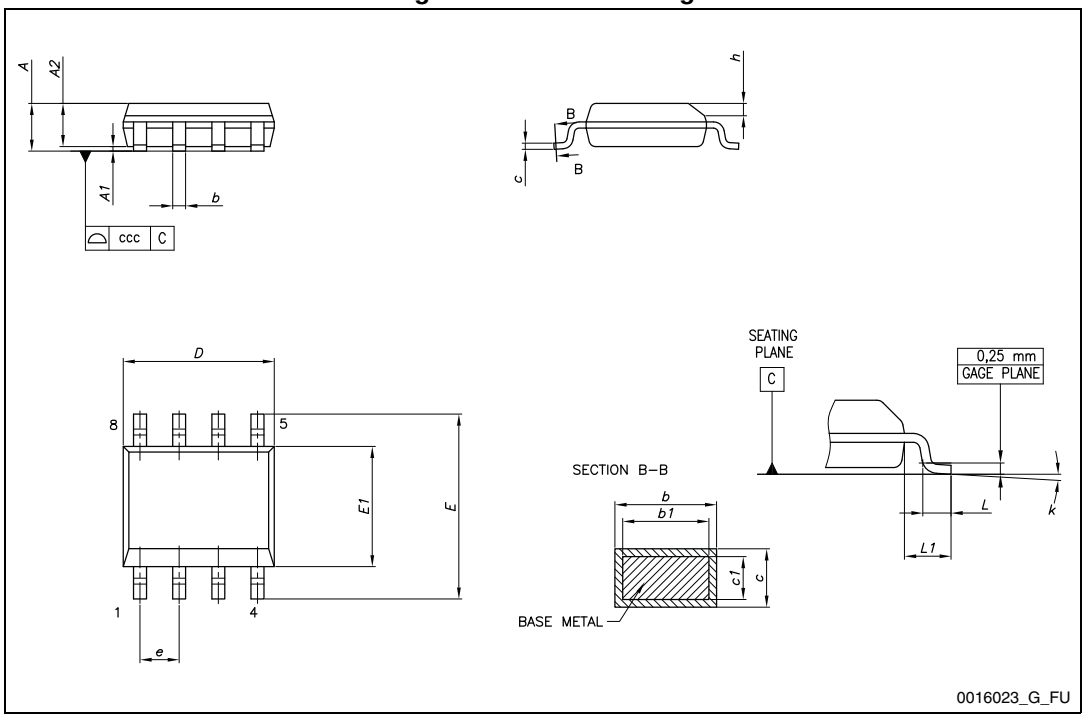
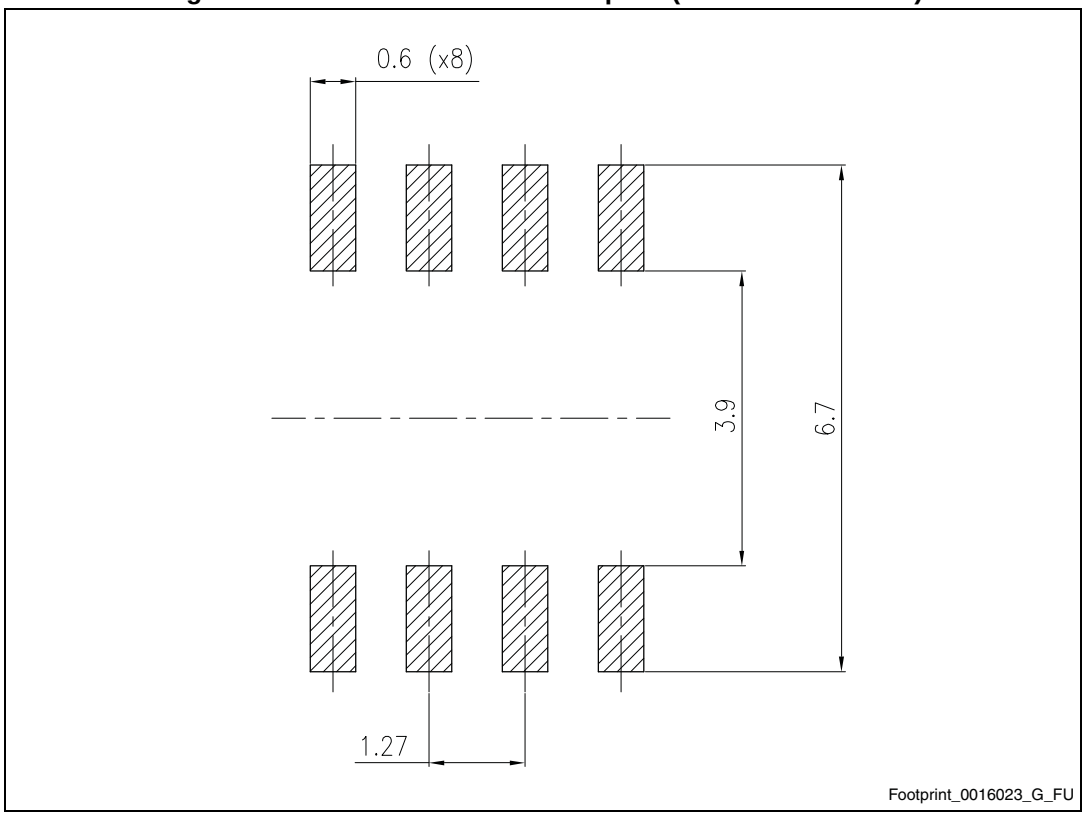


Table 8. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 17. SO-8 recommended footprint (dimensions in mm)

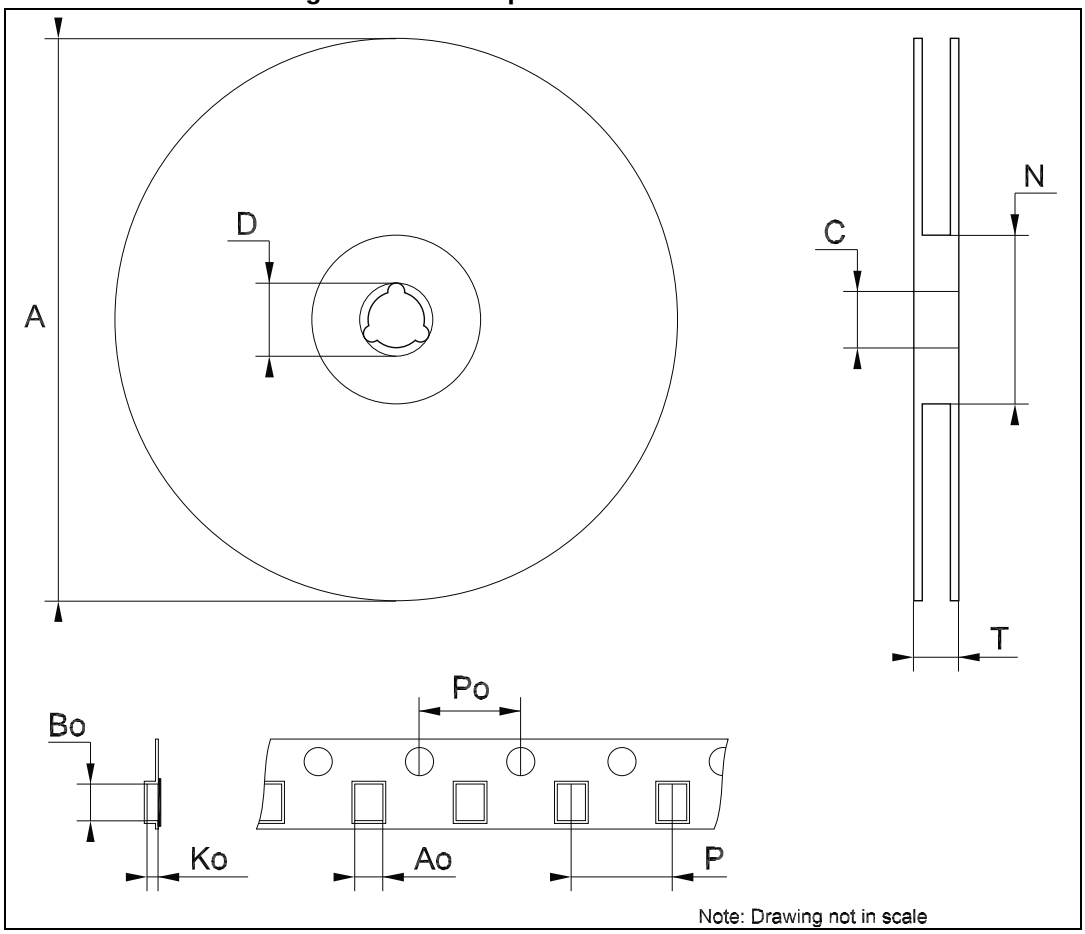


5 Packaging mechanical data

Table 9. SO-8 tape and reel mechanical data

Dim	mm		
	Min	Typ	Max
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	8.1		8.5
Bo	5.5		5.9
Ko	2.1		2.3
Po	3.9		4.1
P	7.9		8.1

Figure 18. SO-8 tape and reel dimensions



6 Revision history

Table 10. Revision history

Date	Revision	Changes
09-May-2013	1	First revision.
11-Dec-2014	2	Text edits throughout document On cover page: – changed title description – updated *Features* – updated *Description* In *Table 4*, changed $R_{DS(on)}$ values In *Table 5*, changed values and test conditions In *Table 6*, changed values and test conditions In *Table 7*, changed values and test conditions Added *Section 2.1: Electrical characteristics (curves)* Updated *Section 3: Test circuits* Updated *Section 4: Package mechanical data*

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