STS10P4LLF6

P-channel 40 V, 0.0125 Ω typ., 10 A, StripFET™ F6 Power MOSFET in SO-8 package

Datasheet - production data

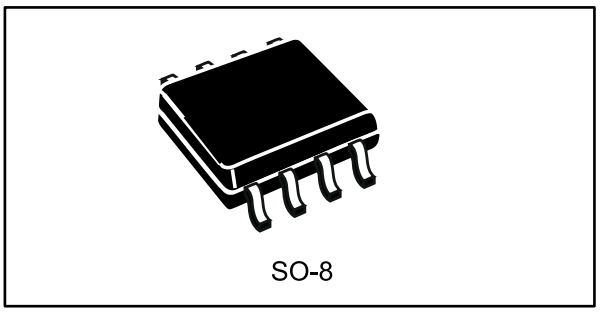
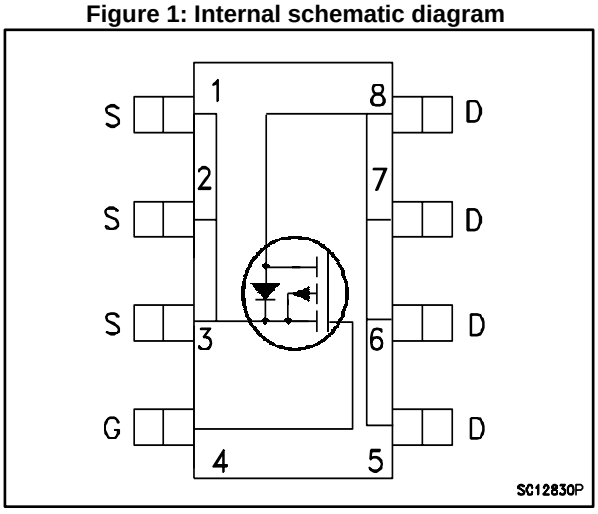


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STS10P4LLF6	40 V	0.015	10 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Table 1: Device summary

Order code	Marking	Package	Packaging
STS10P4LLF6	10K4L	SO-8	Tape and reel

For the P-channel MOSFET actual polarity of voltages and current have to be reversed

This is information on a product in full production.

www.st.com

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate- source voltage	±20	V
I_D	Drain current (continuous) at T_{amb} = 25 °C	10	A
I_D	Drain current (continuous) at T_{amb} = 100 °C	5.6	A
I_{DM} (1)	Drain current (pulsed)	40	A
P_{TOT} (1)	Total dissipation at T_{amb} = 25 °C	2.7	W
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Operating junction temperature	150	°C

Notes:

(1)Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}amb}$ (1)	Thermal resistance junction-ambient	47	°C/W

Notes:

(1)When mounted on 1 inch² FR-4 board, 2 oz. Cu., t ≤ 10 sec

For the P-channel MOSFET actual polarity of voltages and current have to be reversed

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA	40			V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 40 V			1	µA
		V_{DS} = 30 V, T_C= 125 °C			10	
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 3 A		0.0125	0.015	Ω
		V_{GS} = 4.5 V, I_D = 3 A		0.017	0.02	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	3525	-	pF
C_{oss}	Output capacitance		-	344	-	pF
C_{rss}	Reverse transfer capacitance		-	238.5	-	pF
Q_g	Total gate charge	V_{DD} = 20 V I_D = 10 A V_{GS} = 4.5 V	-	34	-	nC
Q_{gs}	Gate-source charge		-	11.3	-	nC
Q_{gd}	Gate-drain charge		-	13.8	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 20 V, I_D = 5 A R_G = 4.7 Ω V_{GS} = 10 V	-	49.4	-	ns
t_r	Rise time			60.6		
$t_{d(off)}$	Turn-off delay time			170		
t_f	Fall time			20		

For the P-channel MOSFET actual polarity of voltages and current have to be reversed

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 3 A, V_{GS} = 0	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs V_{DD} = 10 V, T_j = 150 °C	-	29		ns
Q_{rr}	Reverse recovery charge		-	27.6		nC
I_{RRM}	Reverse recovery current		-	1.9		A

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

For the P-channel MOSFET actual polarity of voltages and current have to be reversed

3 Electrical characteristics (curves)

Figure 2: Safe operating area

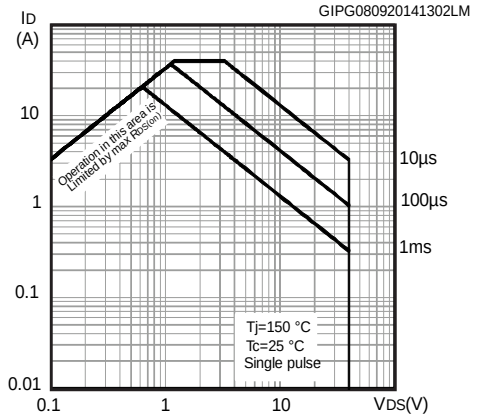


Figure 3: Thermal impedance

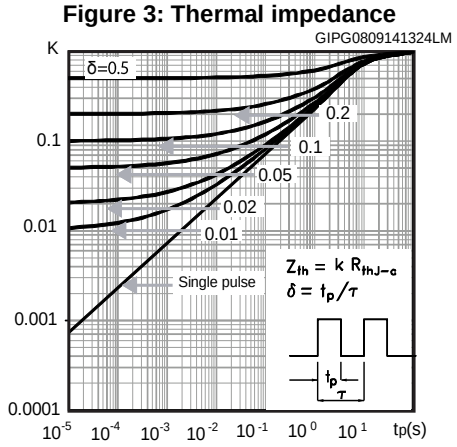


Figure 4: Output characteristics

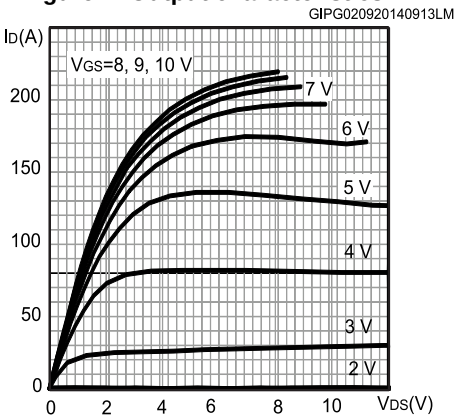


Figure 5: Transfer characteristics

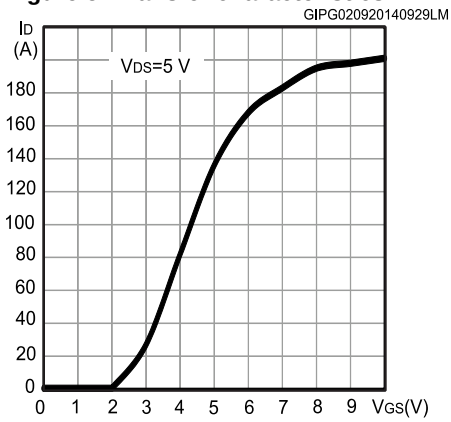


Figure 6: Gate charge vs gate-source voltage

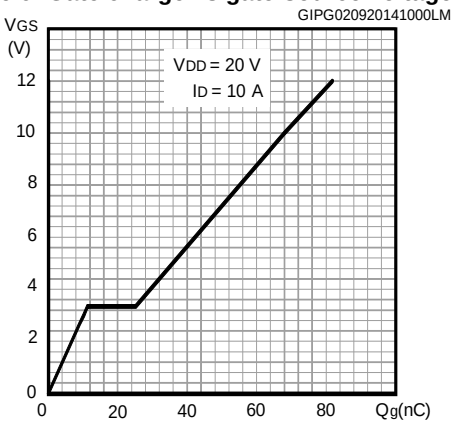


Figure 7: Static drain-source on-resistance

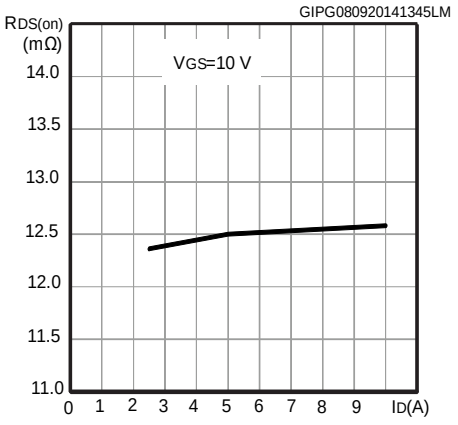


Figure 8: Capacitance variation

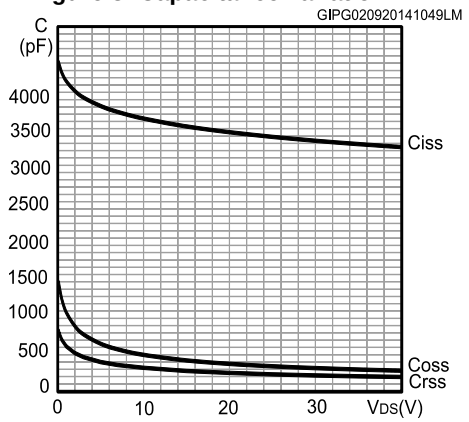


Figure 9: Normalized gate threshold voltage vs temperature

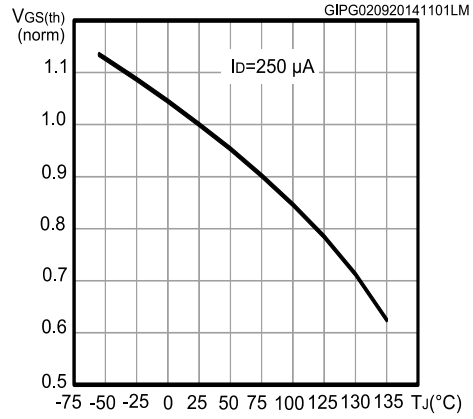


Figure 10: Normalized on-resistance vs temperature

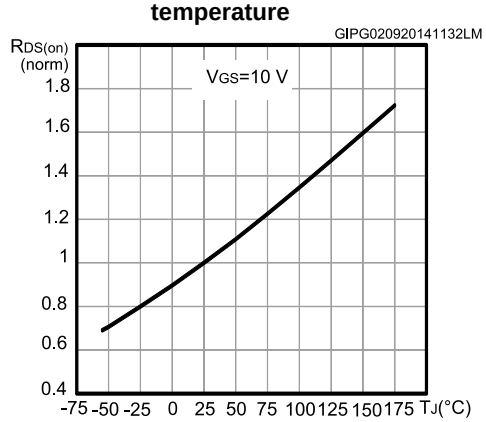


Figure 11: Normalized VBR(DSS) vs temperature

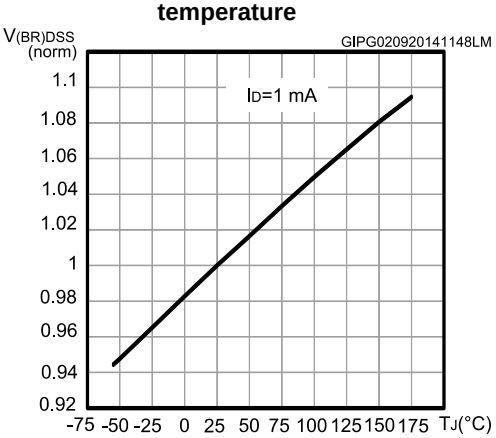
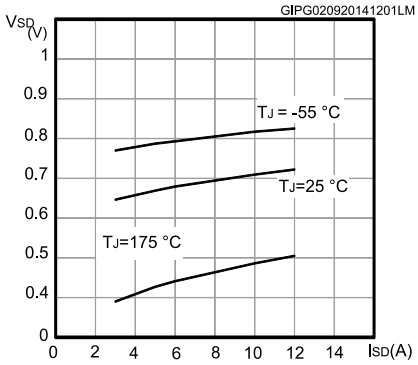


Figure 12: Source-drain diode forward characteristics



4 Test circuits

Figure 13: Switching times test circuit for resistive load

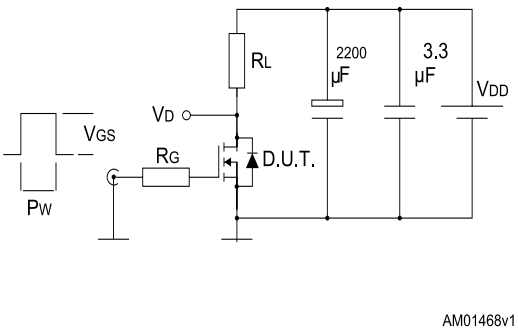


Figure 14: Gate charge test circuit

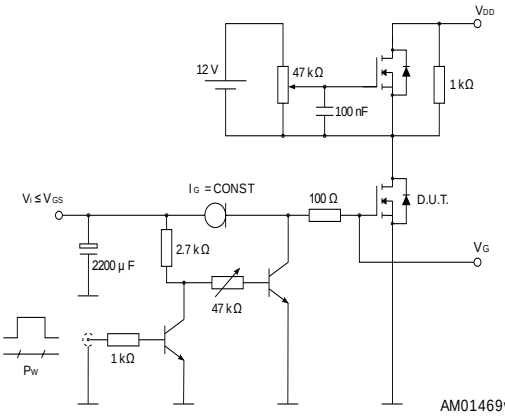


Figure 15: Test circuit for inductive load switching and diode recovery times

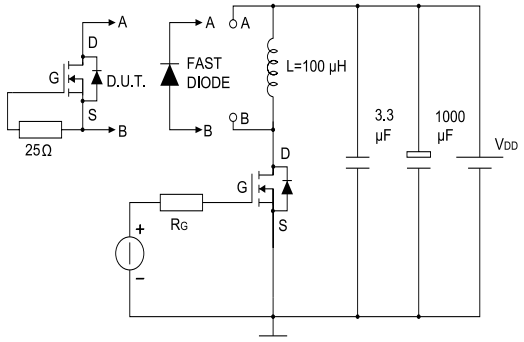


Figure 16: Unclamped inductive load test circuit

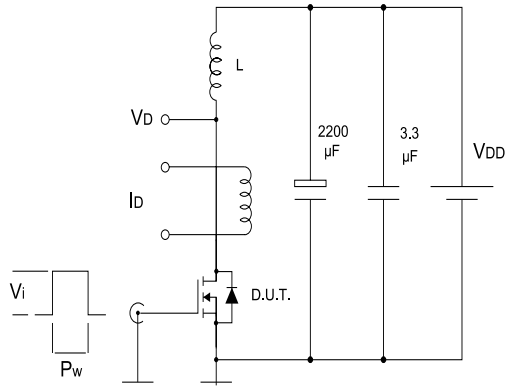


Figure 17: Unclamped inductive waveform

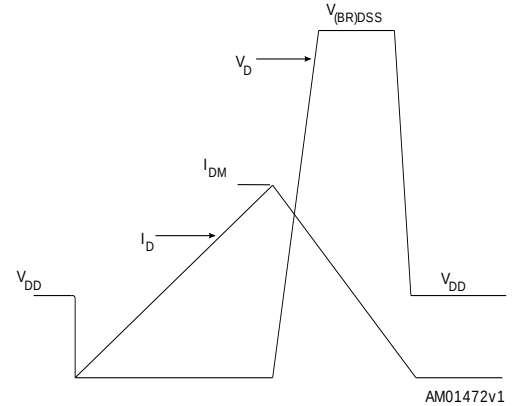
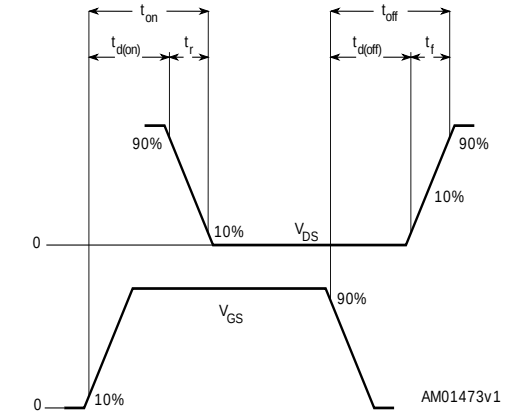


Figure 18: Switching time waveform



5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.1 SO-8 package mechanical data

Figure 19: SO-8 drawings

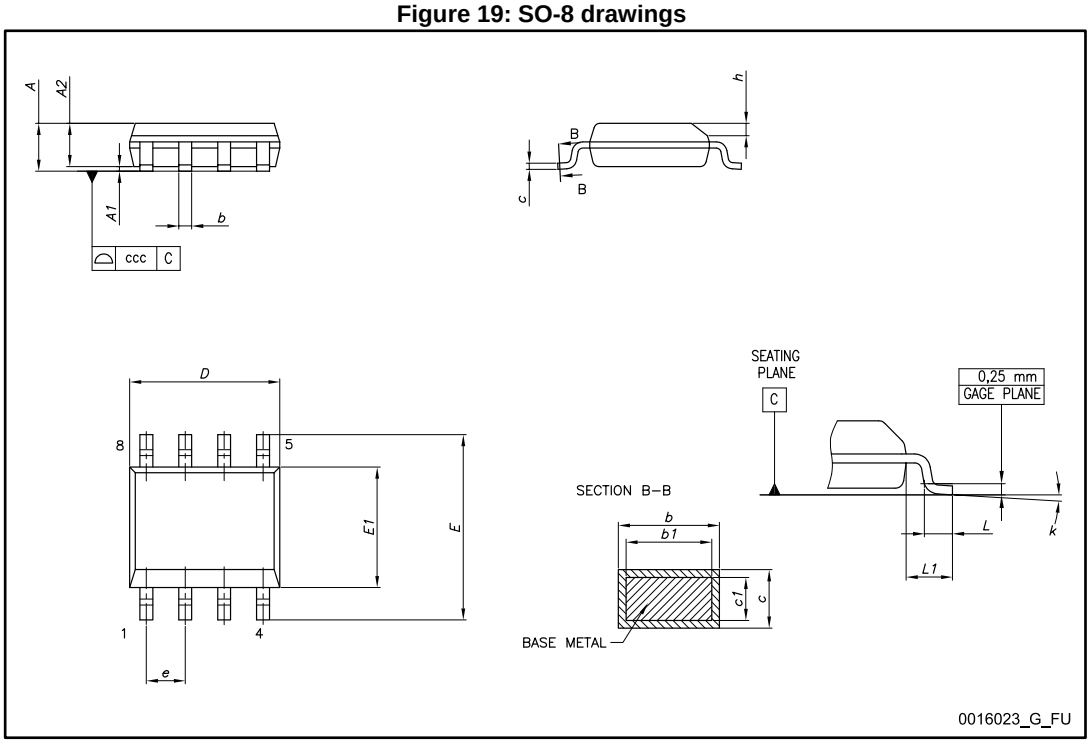
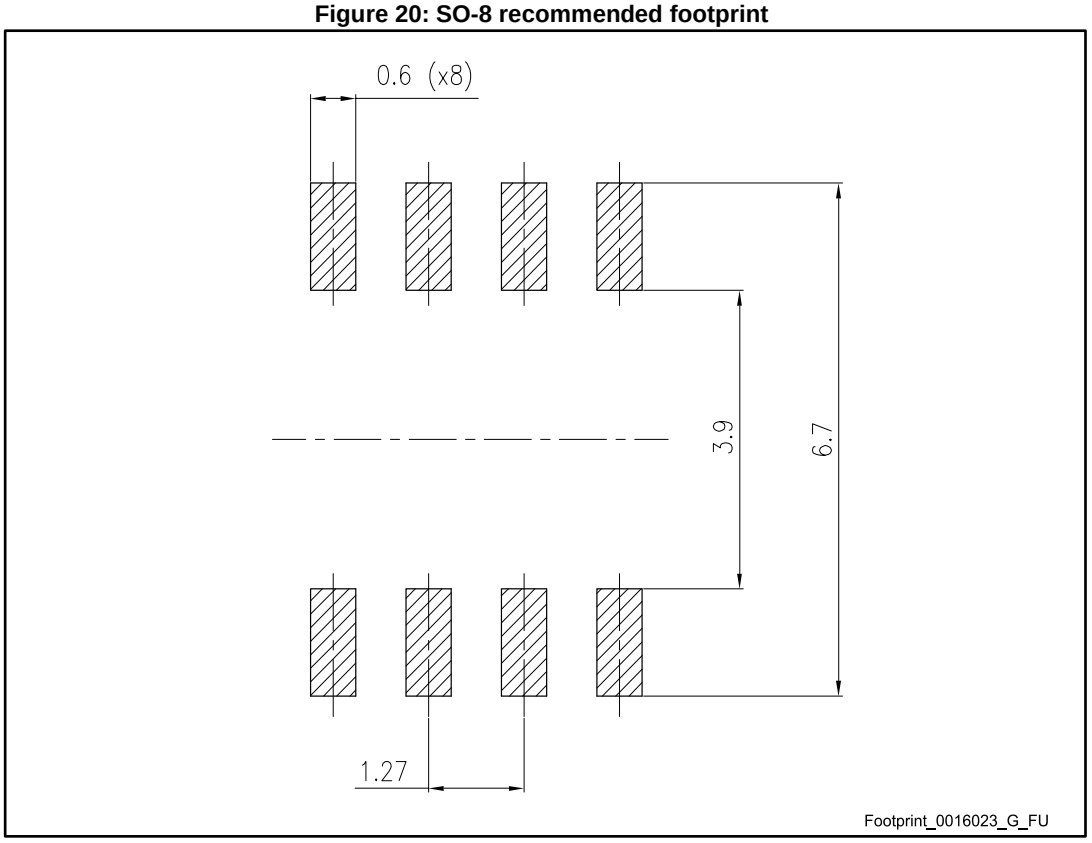


Table 8: SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 20: SO-8 recommended footprint



All dimensions are in mm

6 Packaging mechanical data

Figure 21: SO-8 tape and reel dimensions

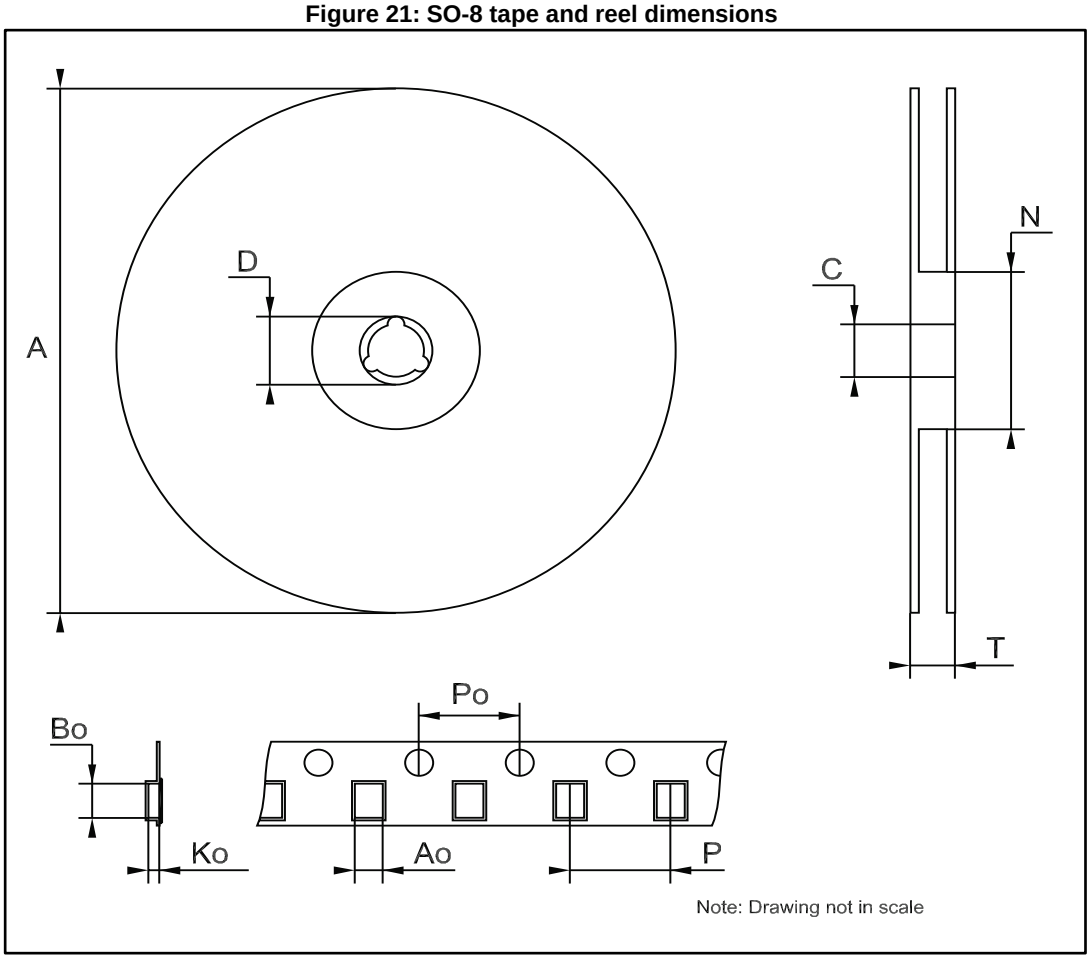


Table 9: SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	8.1		8.5
Bo	5.5		5.9
Ko	2.1		2.3
Po	3.9		4.1
P	7.9		8.1

7 Revision history

Table 10: Revision history

Date	Revision	Changes
20-Jan-2014	1	First revision.
09-Sep-2014	2	Changed the title. Updated *Section "Features"* and *Section "Description"*. Updated *Table 4: "On/off states"*, *Table 5: "Dynamic"*, *Table 6: "Switching times"*, *Table 7: "Source-drain diode"*. Added *Section 3: "Electrical characteristics (curves)"*.
16-Dec-2014	3	Document status promoted from preliminary data to production data. Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2014 STMicroelectronics – All rights reserved