STP6625

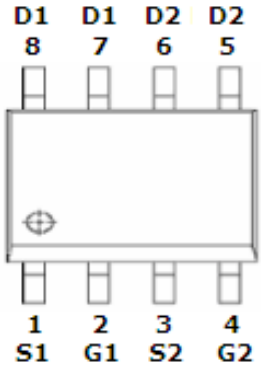
P Channel Enhancement Mode MOSFET

-5.0A

SCRIPTION

STP6625 is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, noteook power management ane ther battery powered circuits where high-side witching.

PIN CONFIGURATION
SOP-8



FEATURE

- -60V/-5.0A, $R_{DS(ON)}$ = 60mΩ (Typ.) @V_{GS} =-10
- -60V/-3.0A, $R_{DS(ON)}$ = 85mΩ @V_{GS} = -4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

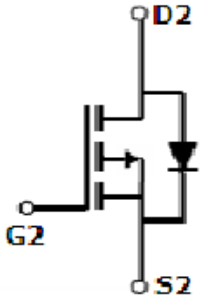
PART MARKING
SOP-8



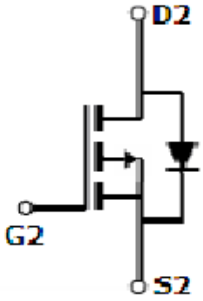
Y: Year Code

A: Date Code

Q: Process Code



P-Channel



P-Channel

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ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		**Symbol**	Typical	**Unit**
Drain-Source Voltage		V_{DSS}	-60	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (TJ=150℃)	T_A=25℃ T_A=70℃	I_D	-5.0 -4.0	A
Pulsed Drain Current		I_{DM}	-25	A
Continuous Source Current (Diode Conduction)		I_S	-3	A
Power Dissipation	T_A=25℃ T_A=70℃	P_D	2.3 1.3	W
Operation Junction Temperature		T_J	-55/150	℃
Storgae Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	70	℃/W

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ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250 uA	-0.8		-2.5	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-48V,V_{GS}=0V			-1	uA
		V_{DS}=-48V,V_{GS}=0V T_J=85℃			-10	
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-5A V_{GS}=-4.5V, I_D=-3A		0.060 0.085	0.072 0.095	Ω
Forward Tran Conductance	gfs	V_{DS}=-5V,I_D=-6.7A		18		S
Diode Forward Voltage	V_{SD}	I_S=-2.3A,V_{GS}=0V		-0.7	-1.0	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-30V,V_{GS}=-10 I_D≡-6.2A		45		nC
Gate-Source Charge	Q_{gs}			5.2		
Gate-Drain Charge	Q_{gd}			9.3		
Input Capacitance	Ciss	V_{DS} =-30V,V_{GS}=0V f=1MHz		2010		pF
Output Capacitance	Coss			130		
Reverse TransferCapacitance	Crss			105		
Turn-On Time	$t_{d(on)}$ tr	V_{DS}=-30V,R_L=4.7Ω V_{GS}=-10V,R_{GEN}=3Ω		9		nS
				6.1		
Turn-Off Time	$t_{d(off)}$ tf			44		
				12.9		

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TYPICAL CHARACTERICTICS

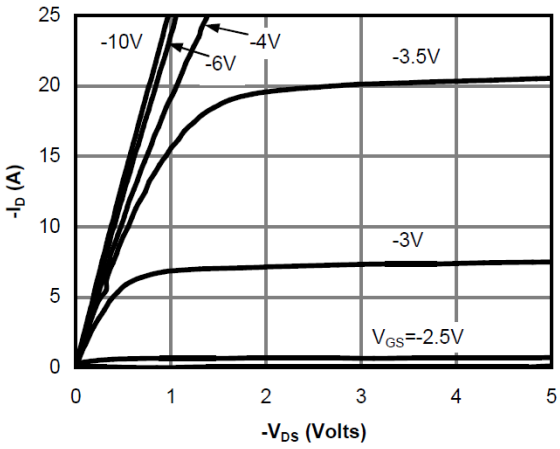


Fig 1: On-Region Characteristics

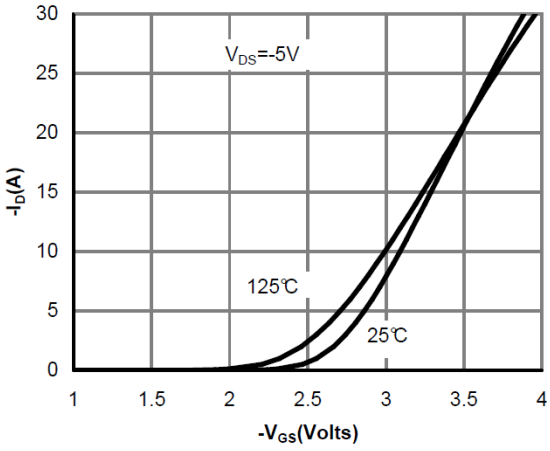


Figure 2: Transfer Characteristics

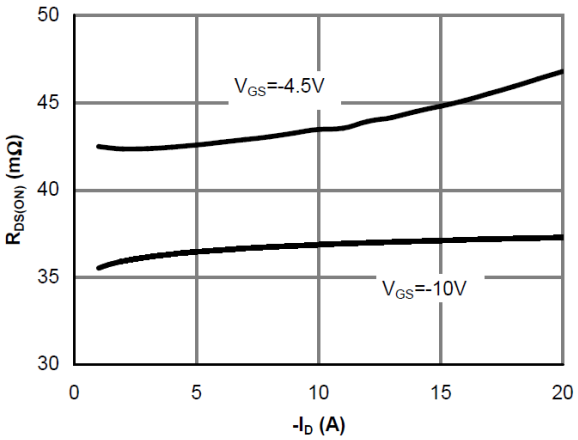


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

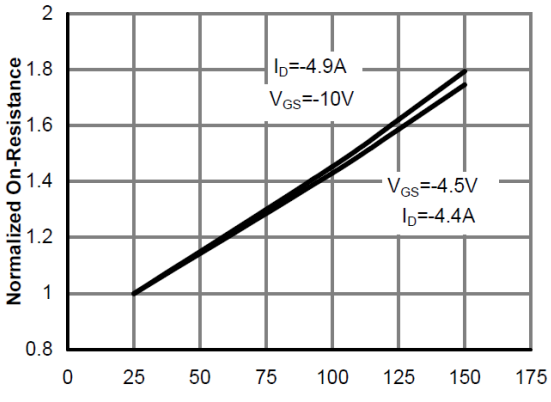


Figure 4: On-Resistance vs. Junction Temperature

TYPICAL CHARACTERICTICS

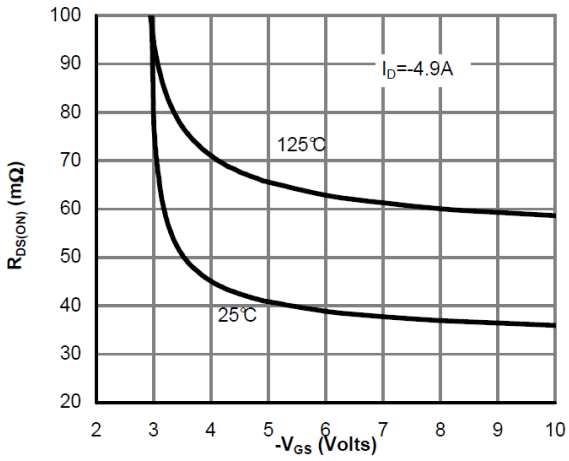


Figure 5: On-Resistance vs. Gate-Source Voltage

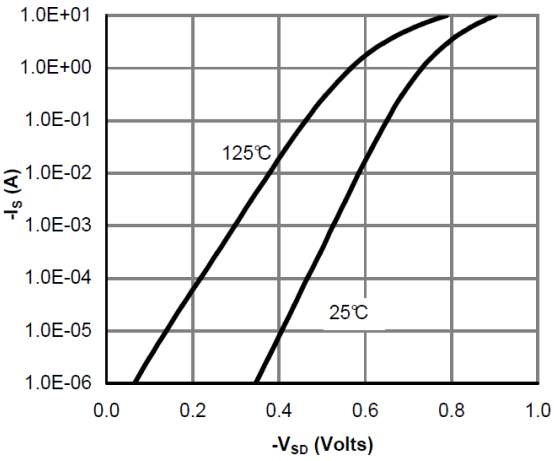


Figure 6: Body-Diode Characteristics

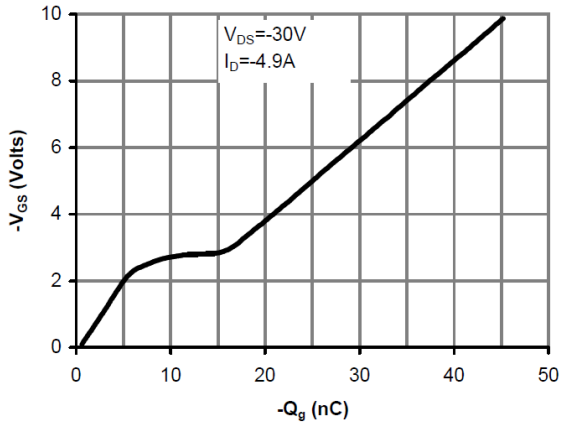


Figure 7: Gate-Charge Characteristics

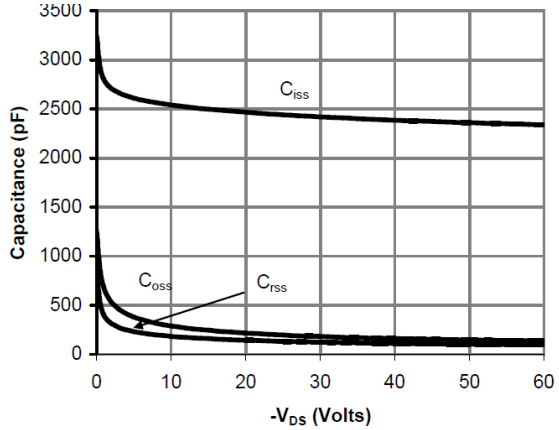


Figure 8: Capacitance Characteristics

TYPICAL CHARACTERICTICS

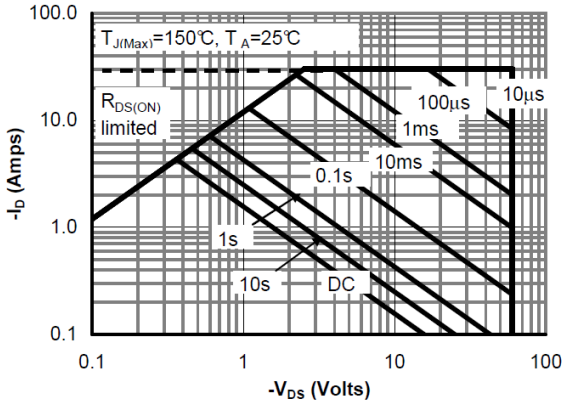


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

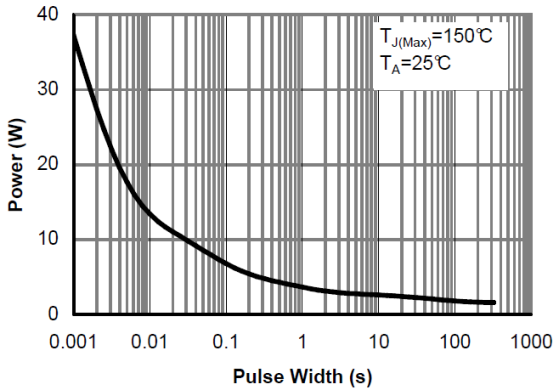


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

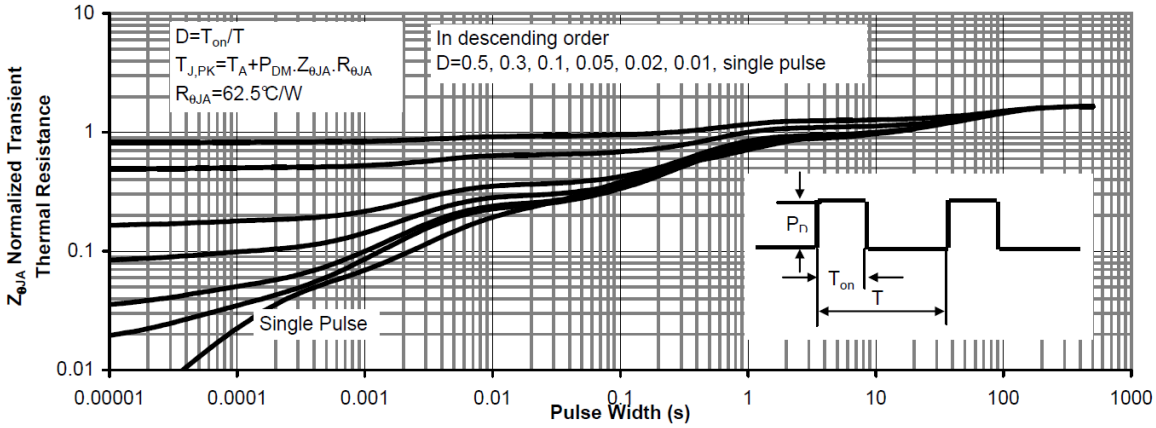
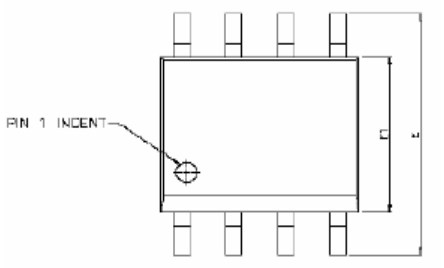
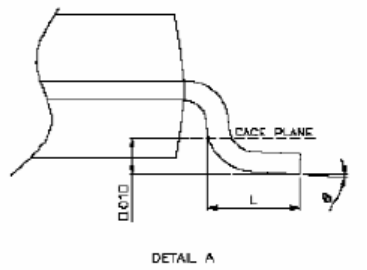
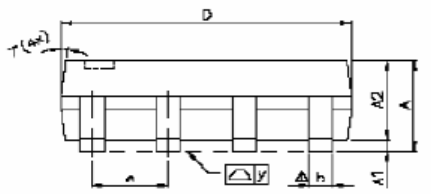


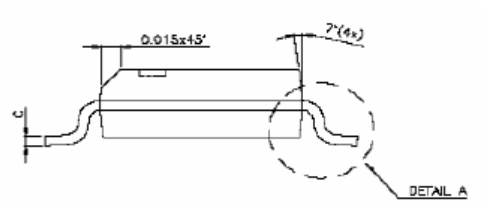
Figure 11: Normalized Maximum Transient Thermal Impedance

SOP-8 PACKAGE OUTLINE









SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	——	0.25	0.004	——	0.010
A2	——	1.45	——	——	0.057	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	——	1.27	——	——	0.050	——
L	0.38	0.71	1.27	0.015	0.028	0.050
y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°

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