

N-channel 600 V, 1.7 Ω typ., 4 A Zener-protected SuperMESH™
Power MOSFETs in TO-220 and TO-220FP packages

Datasheet - production data

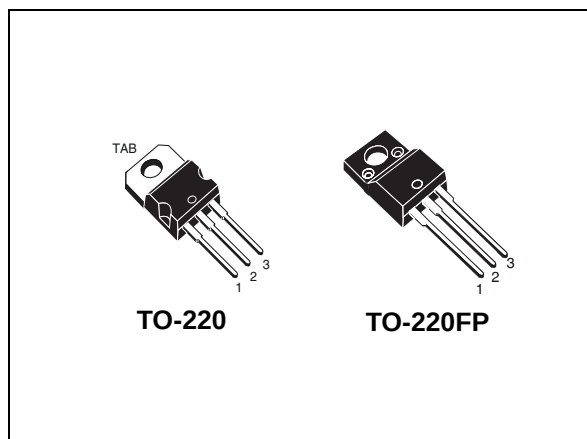
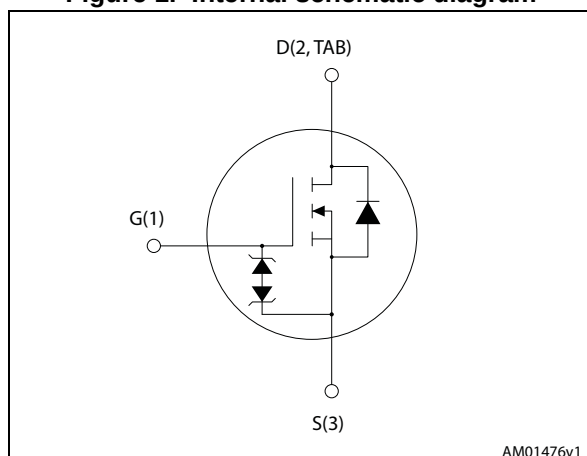


Figure 1. Internal schematic diagram



Features

Order codes	V _{DS}	R _{DS(on)} max.	P _{TOT}	I _D
STP4NK60Z	600 V	2 Ω	70 W	4 A
STP4NK60ZFP				

- 100% avalanche tested
- Very low intrinsic capacitances
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Zener-protected Power MOSFETs developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Table 1. Device summary

Order codes	Marking	Packages	Packaging
STP4NK60Z	P4NK60Z	TO-220	Tube
STP4NK60ZFP	P4NK60ZFP	TO-220FP	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
V_{DS}	Drain-source voltage	600		V
V_{GS}	Gate- source voltage	± 30		V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	4	4 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	2.5	2.5 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	16	16 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	70	25	W
	Derating factor	0.56	0.2	W/ $^{\circ}\text{C}$
ESD	Gate-source human body model (C=100 pF, R=1.5 k Ω)	3		kV
$dv/dt^{(3)}$	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; $T_C=25\text{ }^{\circ}\text{C}$)		2500	V
T_{stg}	Storage temperature	-55 to 150		$^{\circ}\text{C}$
T_j	Max operating junction temperature	150		$^{\circ}\text{C}$

1. Limited by maximum junction temperature.

2. Pulse width limited by safe operating area

3. $I_{SD} \leq 4\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$.

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	1.79	5	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5		$^{\circ}\text{C}/\text{W}$

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_{jmax})	4	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D=I_{AR}$, $V_{DD}=50\text{ V}$)	120	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 600\text{ V}$ $V_{DS} = 600\text{ V}, T_C = 125\text{ °C}$			1 50	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 2\text{ A}$		1.7	2	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}, I_D = 2\text{ A}$	-	3		S
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	510		pF
C_{oss}	Output capacitance		-	67		pF
C_{rss}	Reverse transfer capacitance		-	13		pF
$C_{oss\text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{DS} = 0, V_{DS} = 0\text{ to }480\text{ V}$	-	38.5		pF
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}, I_D = 2\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 17)	-	12		ns
t_r	Rise time		-	9.5		ns
$t_{d(off)}$	Turn-off delay time		-	29		ns
t_f	Fall time		-	16.5		ns
$t_{r(Voff)}$	Off-voltage rise time	$V_{DD} = 480\text{ V}, I_D = 4\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 19)	-	12		ns
t_f	Fall time		-	12		ns
t_c	Cross-over time		-	19.5		ns
Q_g	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 4\text{ A},$ $V_{GS} = 10\text{ V}$ (see Figure 18)	-	18.8	26	nC
Q_{gs}	Gate-source charge		-	3.8		nC
Q_{gd}	Gate-drain charge		-	9.8		nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		16	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	400		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 24\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$	-	1700		nC
I_{RRM}	Reverse recovery current	(see Figure 19)	-	8.5		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2. Pulse width limited by safe operating area

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

Figure 8. Transconductance

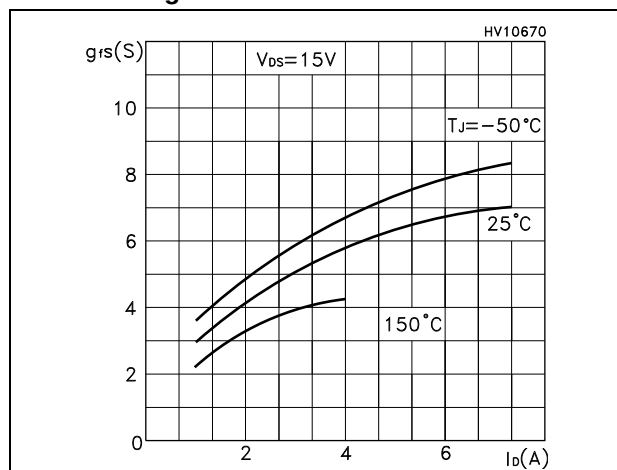


Figure 9. Static drain-source on-resistance

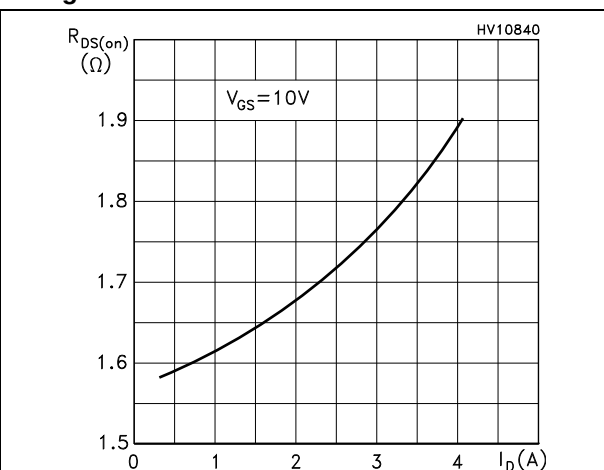


Figure 10. Gate charge vs gate-source voltage

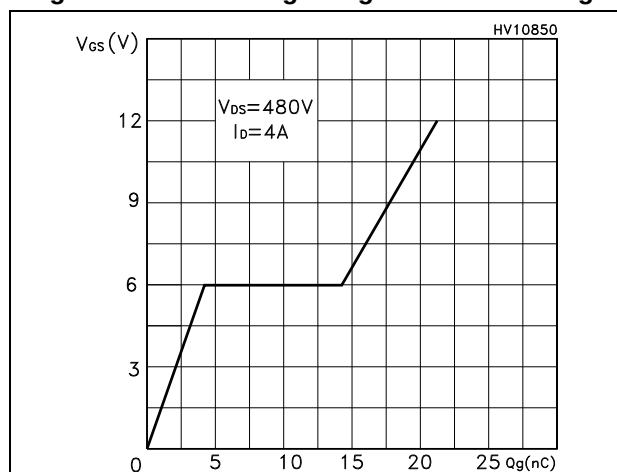


Figure 11. Capacitance variations

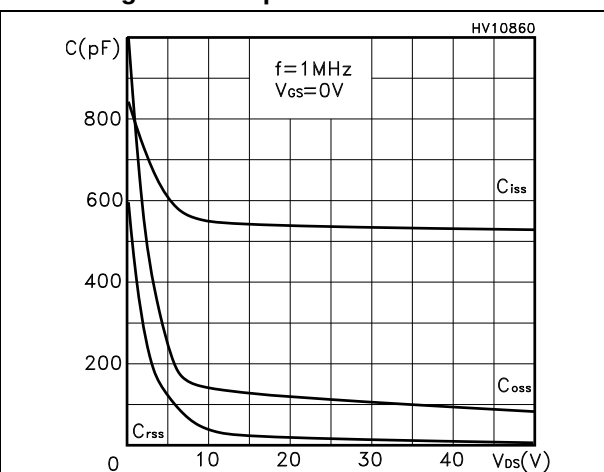


Figure 12. Normalized gate threshold voltage vs temperature

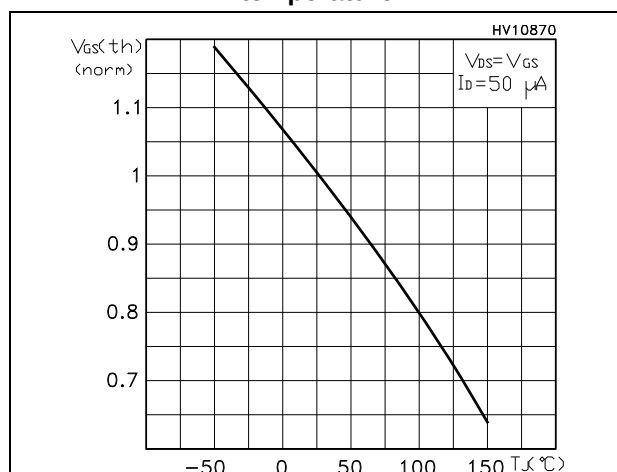
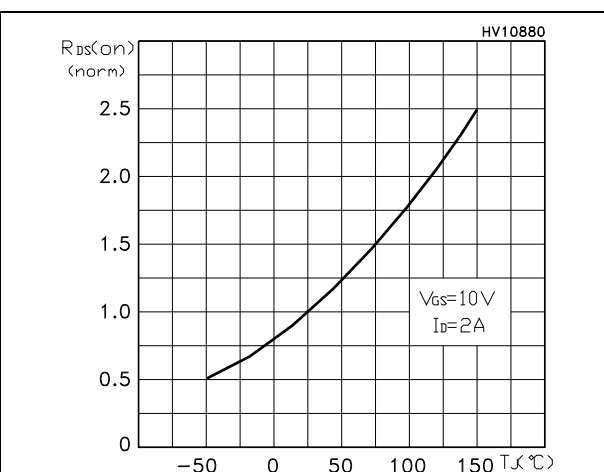
Figure 13. Normalized $R_{DS(on)}$ vs temperature

Figure 14. Source-drain diode forward characteristic

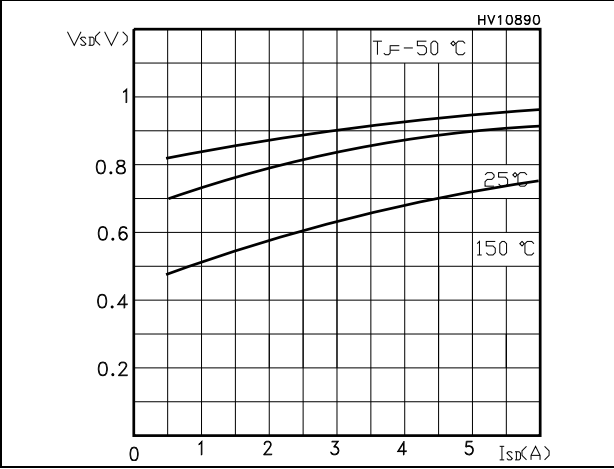


Figure 15. Normalized V_{DS} vs temperature

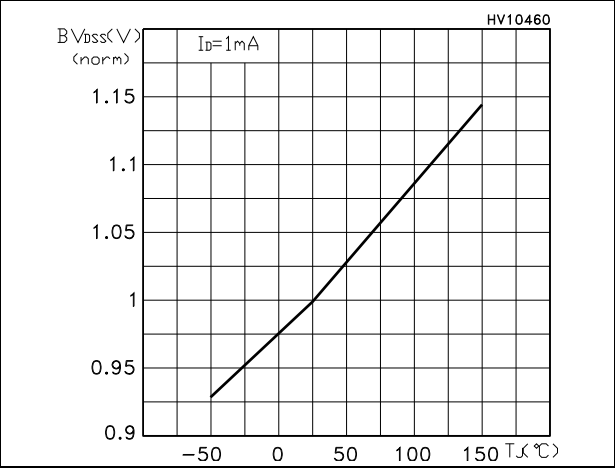
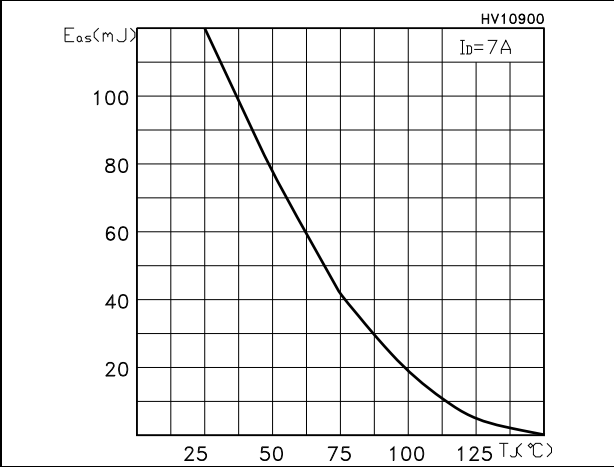


Figure 16. Avalanche energy vs temperature



3 Test circuits

Figure 17. Switching times test circuit for resistive load



Figure 18. Gate charge test circuit



Figure 19. Test circuit for inductive load switching and diode recovery times



Figure 20. Unclamped inductive load test circuit



Figure 21. Unclamped inductive waveform



Figure 22. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 23. TO-220 type A drawing

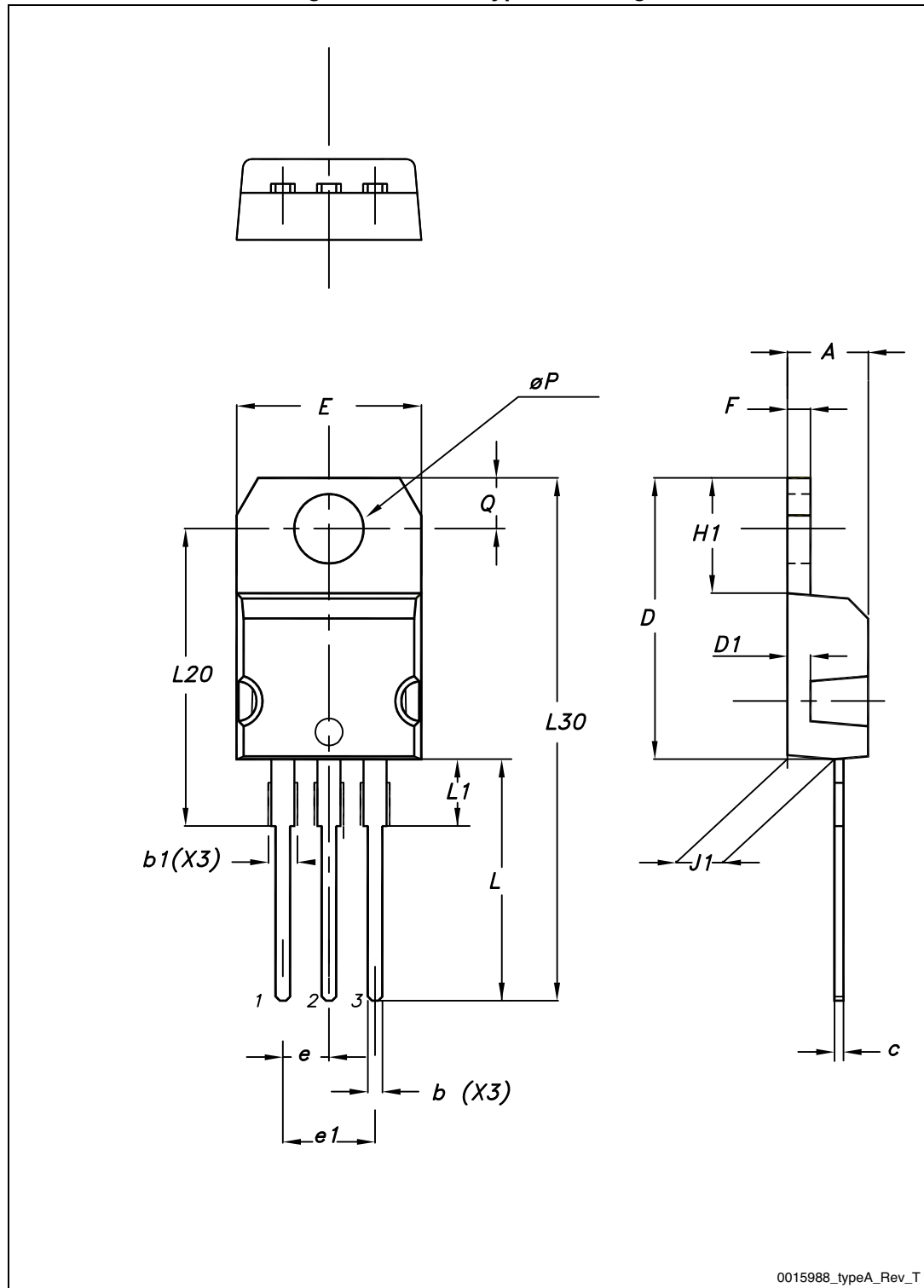


Table 9. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 24. TO-220FP drawing

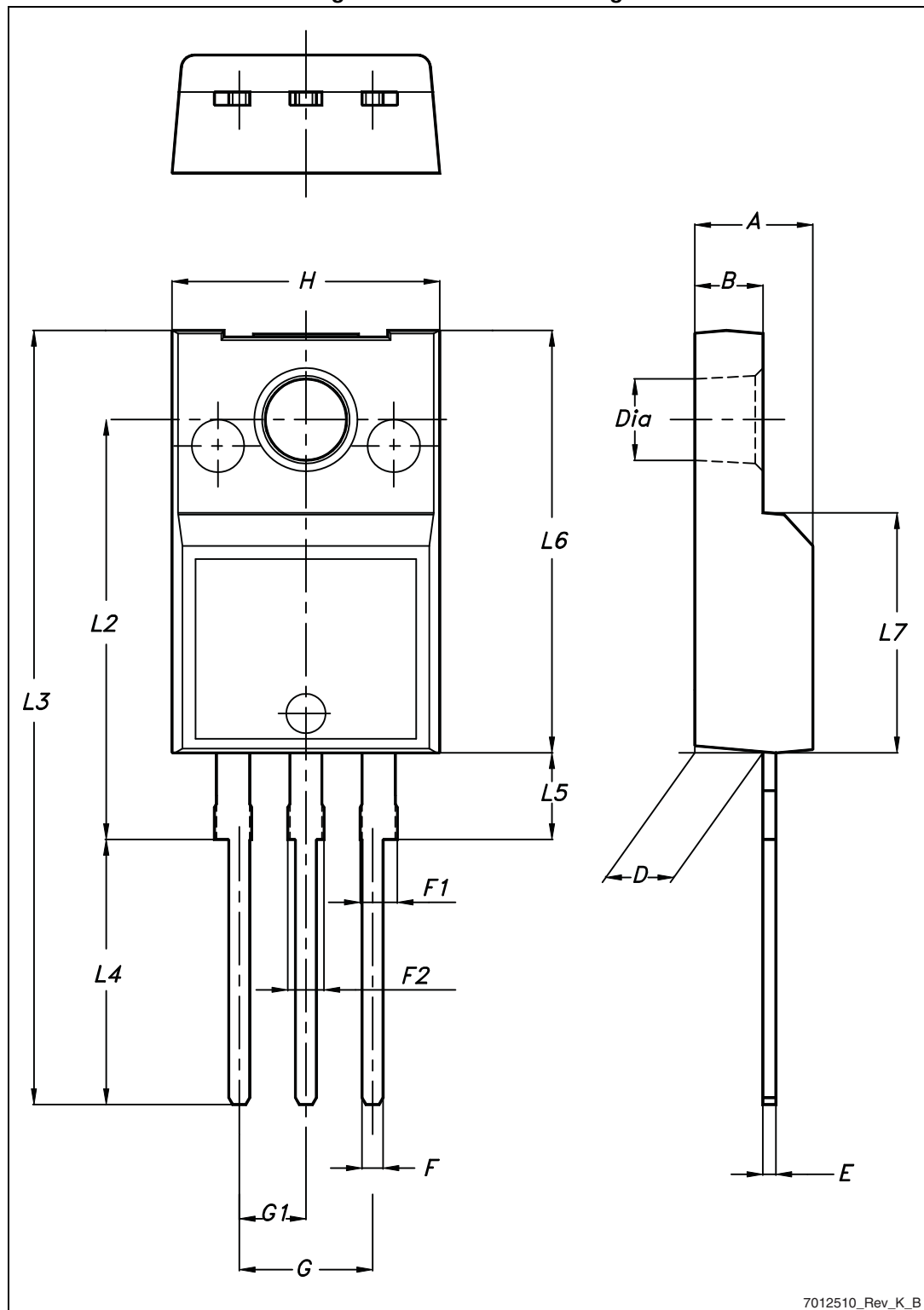


Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Revision history

Table 11. Document revision history

Date	Revision	Changes
19-Jul-2013	1	First release. Part numbers previously included in datasheet DocID8882
22-Jan-2014	2	– Modified: figure in cover page – Minor text changes

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