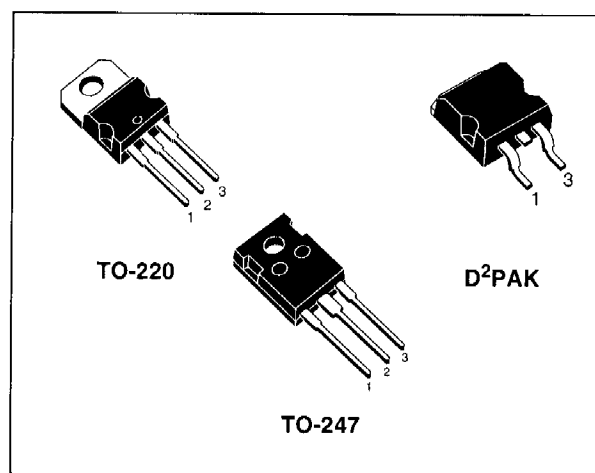


STP12NK80Z - STB12NK80Z STW12NK80Z

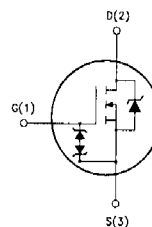
N-CHANNEL 800V - 0.65 Ω - 10.5A TO-220 / D²PAK / TO-247
Zener-Protected SuperMESH™ Power MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _w
STP12NK80Z	800 V	< 0.75 Ω	10.5 A	190 W
STB12NK80Z	800 V	< 0.75 Ω	10.5 A	190 W
STW12NK80Z	800 V	< 0.75 Ω	10.5 A	190 W

- TYPICAL R_{DS(on)} = 0.65 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY

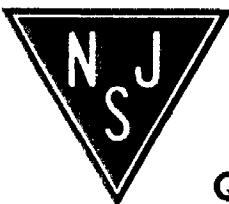


INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES



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Quality Semi-Conductors

STP12NK80Z - STB12NK80Z - STW12NK80Z**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	800	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20\text{ k}\Omega$)	800	V
V_{GS}	Gate- source Voltage	± 30	V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	10.5	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	6.6	A
$I_{DM}(\bullet)$	Drain Current (pulsed)	42	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	190	W
	Derating Factor	1.51	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5K Ω)	6000	V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5	V/ns
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150	$^\circ\text{C}$

(●) Pulse width limited by safe operating area

(1) $I_{SD} \leq 10.5\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

(*) Limited only by maximum temperature allowed

THERMAL DATA

		TO-220/ D ² PAK	TO-247	
$R_{thj-case}$	Thermal Resistance Junction-case Max	0.66		$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	62.5	50	$^\circ\text{C}/\text{W}$
T_l	Maximum Lead Temperature For Soldering Purpose	300		$^\circ\text{C}$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	10.5	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	400	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	$I_{gs} = \pm 1\text{ mA}$ (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

STP12NK80Z - STB12NK80Z - STW12NK80Z

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 1 mA, V _{GS} = 0	800			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 50	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	3.75	4.5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 5.25 A		0.65	0.75	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 15 V, I _D = 5.25 A		12		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		2620 250 53		pF pF pF
C _{oss eq.} (3)	Equivalent Output Capacitance	V _{GS} = 0V, V _{DS} = 0V to 640V		100		pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t _{d(on)} t _r	Turn-on Delay Time Rise Time	V _{DD} = 400 V, I _D = 5.25 A R _G = 4.7Ω V _{GS} = 10 V (Resistive Load see, Figure 3)		30 18		ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 640V, I _D = 10.5 A, V _{GS} = 10V		87 14 44		nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t _{d(off)} t _f	Turn-off Delay Time Fall Time	V _{DD} = 400 V, I _D = 5.25 A R _G = 4.7Ω V _{GS} = 10 V (Resistive Load see, Figure 3)		70 20		ns ns
t _{r(Voff)} t _f t _c	Off-voltage Rise Time Fall Time Cross-over Time	V _{DD} = 640 V, I _D = 10.5 A, R _G = 4.7Ω, V _{GS} = 10V (Inductive Load see, Figure 5)		16 15 28		ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I _{SD} I _{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				10.5 42	A A
V _{SD} (1)	Forward On Voltage	I _{SD} = 10.5 A, V _{GS} = 0			1.6	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I _{SD} = 10.5 A, di/dt = 100A/μs V _{DD} = 100 V, T _J = 150°C (see test circuit, Figure 5)		635 5.9 18.5		ns μC A

Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

3. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.