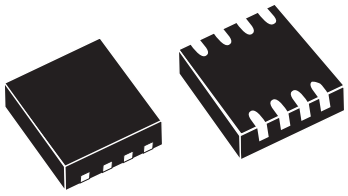
STM6510

Dual push-button Smart Reset™ with capacitor-adjustable delays

Features

- Dual Smart Reset™ push-button inputs with capacitor-adjustable extended reset setup delay (t_{SRC})
- Capacitor-adjustable reset pulse duration (t_{REC})
- Power-on reset
  - $\overline{RST}$ active-low, open-drain
- Factory-programmable thresholds to monitor V_{CC} in the range of 1.575 to 4.625 V typ.
- Operating voltage 1.0 V (active-low output valid) to 5.5 V
- Low supply current (1.4 µA)
- Operating temperature: industrial grade –40 °C to +85 °C
- TDFN8 package: 2 mm x 2 mm x 0.75 mm
- RoHS compliant



TDFN8 (DG)
2 mm x 2 mm

Applications

- Mobile phones, smartphones
- e-books
- MP3 players
- Games
- Portable navigation devices
- Any application that requires delayed reset push-button(s) response for improved system stability

Contents

1 **Description** 5

1.1 Smart Reset™ devices 5

1.2 STM6510 5

1.3 Pin descriptions 9

1.3.1 Power supply (V_{CC}) 9

1.3.2 Ground (V_{SS}) 9

1.3.3 Smart Reset™ push-button inputs ($\overline{SR0}$, $\overline{SR1}$) 9

1.3.4 Adjustable delay of Smart Reset™ input (SRC pin) 9

1.3.5 Reset output ($\overline{RST}$) 10

1.3.6 Adjustable reset timeout ($TREC_{ADJ}$ pin) 10

2 **Typical operating characteristics** 11

3 **Maximum ratings** 13

4 **DC and AC parameters** 14

5 **Package mechanical data** 17

6 **Part numbering** 23

7 **Package marking** 24

8 **Revision history** 25

List of tables

Table 1. Signal names . . . 6
Table 2. tSRC programmed by an ideal external capacitor . . . 9
Table 3. tREC programmed by an ideal external capacitor . . . 10
Table 4. Absolute maximum ratings . . . 13
Table 5. Operating and measurement conditions . . . 14
Table 6. DC and AC characteristics . . . 15
Table 7. Possible VCC voltage thresholds . . . 16
Table 8. TDFN – 8-lead 2 x 2 x 0.75 mm, 0.5 mm pitch package mechanical data . . . 18
Table 9. Parameter for landing pattern - TDFN – 8-lead 2 x 2 mm package . . . 19
Table 10. Carrier tape dimensions . . . 20
Table 11. Reel dimensions . . . 21
Table 12. Ordering information scheme . . . 23
Table 13. Package marking . . . 24
Table 14. Document revision history . . . 25

List of figures

Figure 1. Logic diagram . . . 6
Figure 2. Pin connections . . . 6
Figure 3. Block diagram . . . 7
Figure 4. Single-button Smart Reset™ typical hookup . . . 8
Figure 5. Dual-button Smart Reset™ typical hookup . . . 8
Figure 6. Timing waveforms . . . 9
Figure 7. Supply current (I_{CC}) vs. temperature . . . 11
Figure 8. Smart Reset™ delay (t_{SRC}) vs. temperature, C_{SRC} = 0.56 µF . . . 11
Figure 9. Reset timeout period (t_{REC}) vs. temperature, C_{tREC} = 0.01 µF . . . 12
Figure 10. Reset threshold (V_{RST}) vs. temperature, “S” threshold option, V_{CC} falling . . . 12
Figure 11. AC testing input/output waveforms . . . 14
Figure 12. TDFN – 8-lead 2 x 2 x 0.75 mm, 0.5 mm pitch package outline . . . 18
Figure 13. Landing pattern - TDFN – 8-lead 2 x 2 mm without thermal pad . . . 19
Figure 14. Carrier tape . . . 20
Figure 15. Reel dimensions . . . 21
Figure 16. Tape trailer/leader . . . 22
Figure 17. Pin 1 orientation . . . 22
Figure 18. Package marking, top view . . . 24

1 Description

1.1 Smart Reset™ devices

The Smart Reset™ device family STM65xx provides a useful feature that ensures inadvertent short reset push-button closures do not cause system resets. This is done by implementing an extended Smart Reset™ input delay (t_{SRC}). Once the valid Smart Reset™ input levels and setup delay are met, the device generates an output reset pulse with user-programmable timeout period (t_{REC}).

The typical application hookup shows that the dual Smart Reset™ inputs can be also connected to the applications interrupt to allow the control of both the interrupt pin and the hard reset functions. If the push-buttons are closed for a short time, the processor is only interrupted. If the system still does not respond properly, holding the push-buttons for the extended setup time (t_{SRC}) causes a hard reset of the processor through the reset output. The Smart Reset™ feature helps significantly increase system stability.

The STM65xx family of Smart Reset™ devices consists of low-current microprocessor reset circuits targeted at applications such as MP3 players, portable navigation devices or mobile phones, generally any application that requires delayed reset push-button(s) response for improved system stability. The STM65xx devices feature single or dual Smart Reset™ inputs (SRx). The delayed Smart Reset™ setup time (t_{SRC}) options are adjustable by adding an external capacitor on the SRC pin or selectable by three-state logic. The delayed setup period ignores switch closures shorter than t_{SRC}, thus preventing undesired resets.

The STM65xx devices have active-low (optionally active-high) open-drain reset ($\overline{RST}$) output(s) with or without an internal pull-up resistor or push-pull as output options, with or without the power-on reset function.

Some devices also have an undervoltage monitoring feature: the reset output is also asserted when the monitored supply voltage V_{CC} drops below the specified threshold. The reset output remains asserted for the reset timeout period (t_{REC}) after the monitored supply voltage goes above the specified threshold.

1.2 STM6510

The STM6510 has two combined Smart Reset™ inputs ($\overline{SR0}$ and $\overline{SR1}$) with Smart Reset™ setup delay (t_{SRC}) programmed by an external capacitor on the SRC pin. An additional STM6510 feature is adjustable output reset pulse time t_{REC} by adding an external capacitor (C_{tREC}).

Additionally, the V_{CC} is monitored and if it drops below the selected V_{RST} threshold, the reset output goes active and remains active while V_{CC} is below the V_{RST} threshold, plus the defined duration of the reset pulse t_{REC}.

Figure 1. Logic diagram

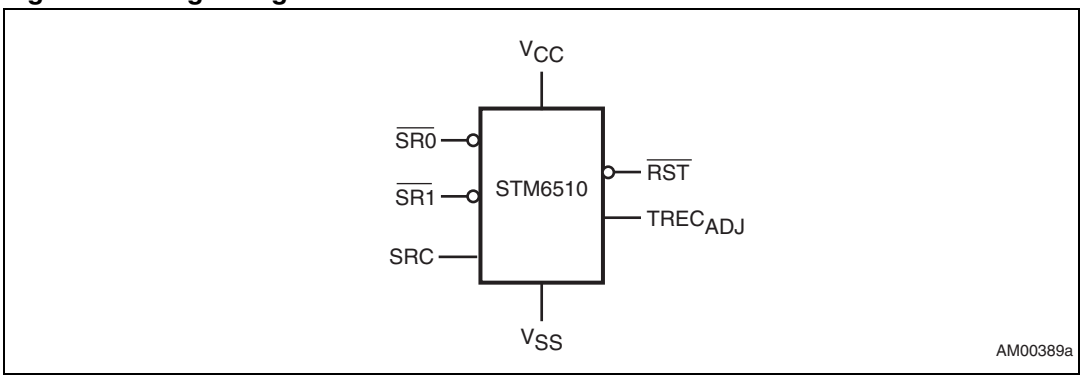


Figure 2. Pin connections

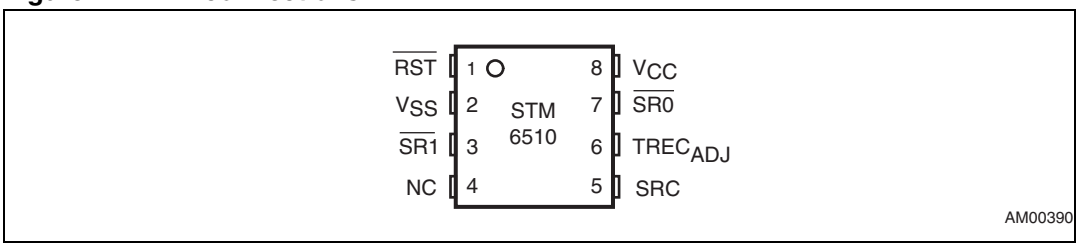


Table 1. Signal names

Symbol	Input/output	Description
$\overline{RST}$	Output	Reset output, active-low (open-drain).
$\overline{SR0}$	Input	Primary push-button Smart Reset™ input. Active-low, internal 65 kΩ pull-up resistor to V_{CC}.
$\overline{SR1}$	Input	Secondary push-button Smart Reset™ input. Active-low, internal 65 kΩ pull-up resistor to V_{CC}.
SRC	Input	Smart Reset™ input delay setup control. Connect an external capacitor to this pin to adjust the delay setup time (t_{SRC}).
$TREC_{ADJ}$	Input	Input pin for t_{REC} reset pulse duration adjustment. Connect an external capacitor (C_{tREC}) to this pin to determine t_{REC}.
V_{CC}	Supply	Supply voltage input. Power supply for the device and an input for the monitored supply voltage. A 0.1 µF decoupling ceramic capacitor is recommended to be connected between V_{CC} and V_{SS} pins.
V_{SS}	Supply	Ground
NC		No connect (not bonded); should be connected to V_{SS}.

Figure 3. Block diagram

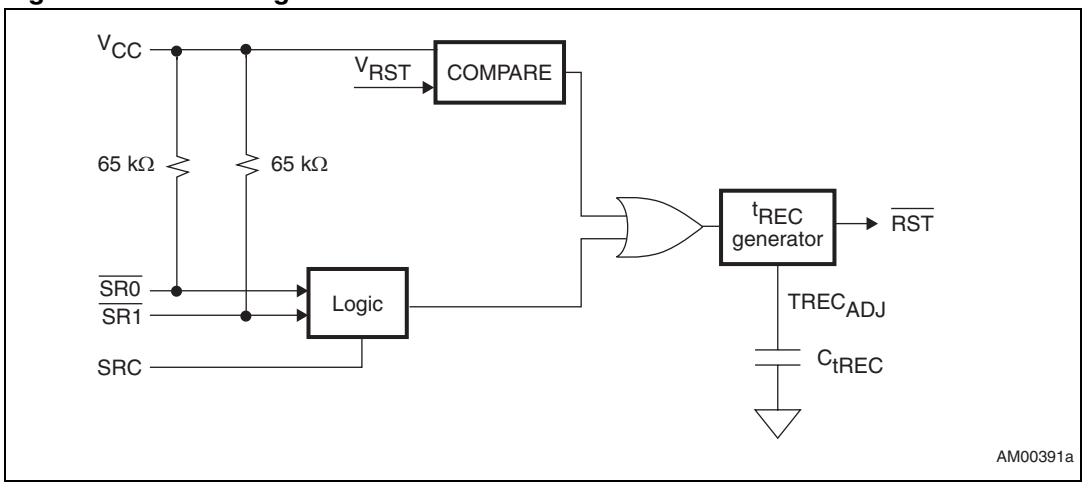
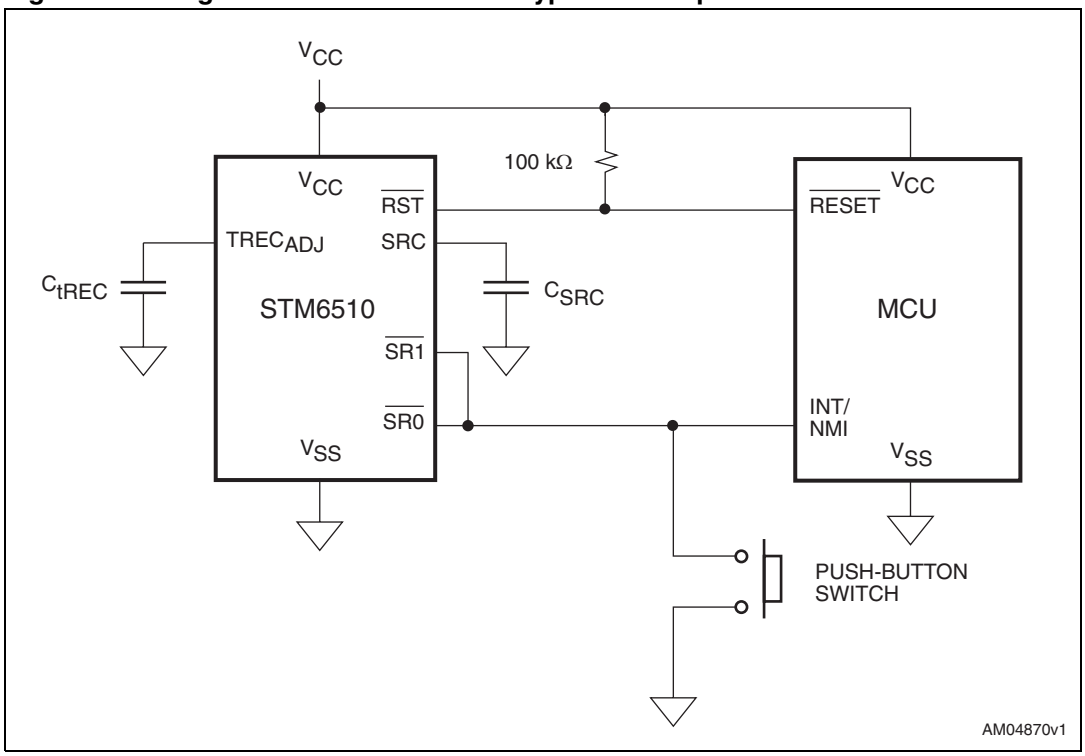
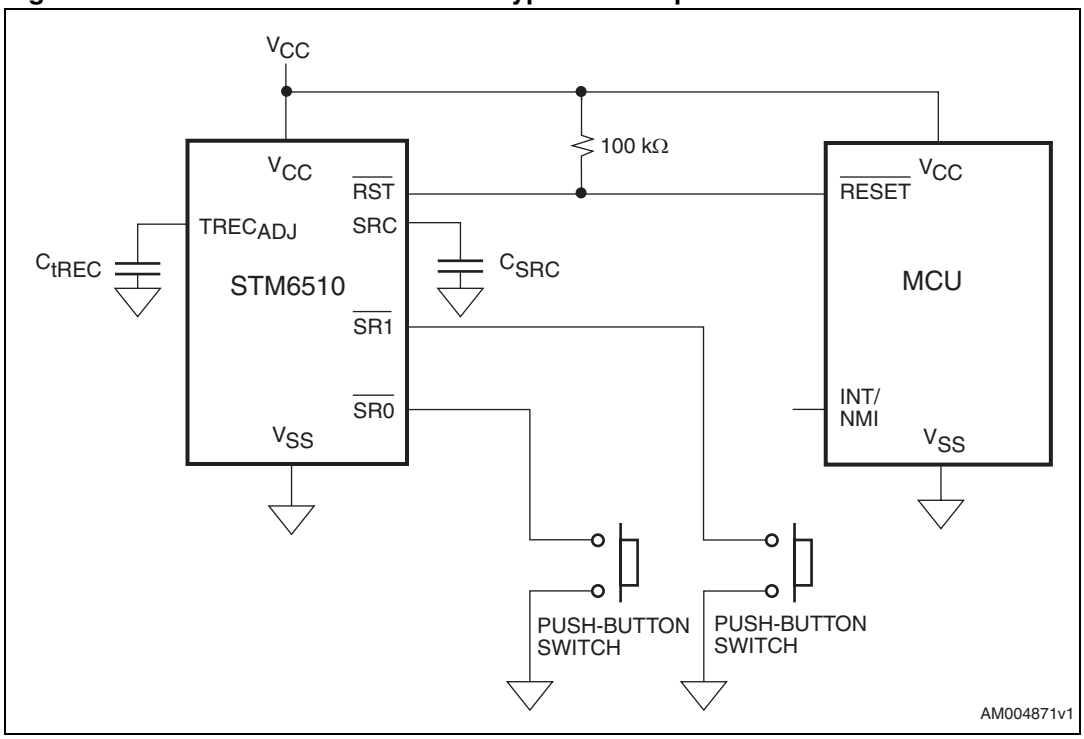


Figure 4. Single-button Smart Reset™ typical hookup



Note: When only one Smart Reset™ input push-button is used, tie both the $\overline{SR}$ inputs together.

Figure 5. Dual-button Smart Reset™ typical hookup



1.3 Pin descriptions

1.3.1 Power supply (V_{CC})

This pin is used to provide the power to the Smart Reset™ device and to monitor the power supply. A 0.1 µF decoupling ceramic capacitor is recommended to be connected between the V_{CC} and V_{SS} pins.

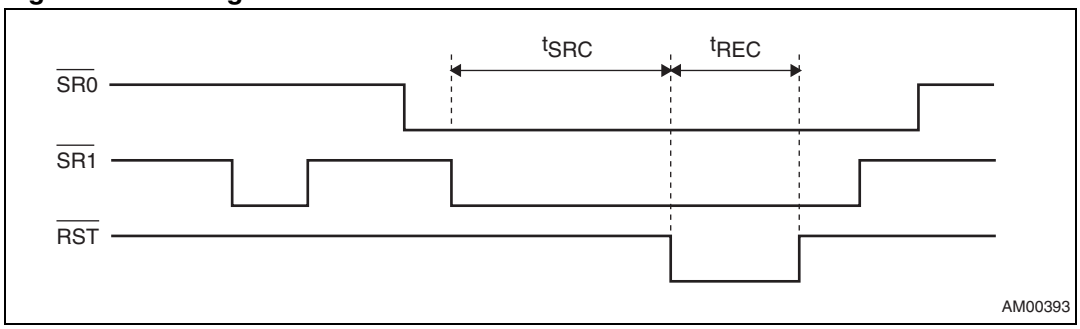
1.3.2 Ground (V_{SS})

This is the supply ground for the device.

1.3.3 Smart Reset™ push-button inputs ($\overline{SR0}$, $\overline{SR1}$)

Both $\overline{SR0}$ and $\overline{SR1}$ need to be held active at the same time for at least t_{SRC} to activate the reset output pulse. Include an internal 65 kΩ pull-up resistor to V_{CC} for each input.

Figure 6. Timing waveforms



1.3.4 Adjustable delay of Smart Reset™ input (SRC pin)

This pin controls the setup time before the push-button action is validated by the reset output. It is connected to an external capacitor (C_{SRC}), which is tied to ground to provide the desired value of setup time (t_{SRC}).

Calculated t_{SRC} and C_{SRC} examples are given in *Table 2*. Refer also to *Table 6*.

Table 2. t_{SRC} programmed by an ideal external capacitor

Calculated C_{SRC} value [µF]	Setup delay t_{SRC} [s](1)(2)			Closest common C_{SRC} value [µF]
	Min.	Typ.	Max.	
0.2	2	3	4	0.22
0.3	3	4.5	6	0.33
0.6	6	9	12	0.56
1	10	15	20	1

1. Example calculations based on an ideal capacitor. During application design and component selection it should be considered that the current flowing into the external t_{SRC} programming capacitor (C_{SRC}) is on the order of 100 nA, therefore a low-leakage capacitor (ceramic or film capacitor) and an adequate PCB environment should be used to prevent t_{SRC} accuracy from being affected. A recommended minimum value of C_{SRC} is 0.01 µF.
2. In case of repeated activations of the t_{SRC} counter, an interval of 10 ms min. is needed between the activations to fully discharge C_{SRC}, so that the next t_{SRC} is as specified.

1.3.5 Reset output ($\overline{RST}$)

$\overline{RST}$ is active-low, open-drain.

1.3.6 Adjustable reset timeout ($TREC_{ADJ}$ pin)

The reset timeout (t_{REC}) is adjustable by connecting an external capacitor C_{tREC} to this pin. Calculated t_{REC} and C_{tREC} examples are given in *Table 3*. Refer also to *Table 6*.

Table 3. t_{REC} programmed by an ideal external capacitor

Calculated C_{tREC} value [µF]	t_{REC} [ms](1)(2)			Closest common C_{tREC} value [µF]
	Min.	Typ.	Max.	
0.001	10	15	20	0.001
0.002	20	30	40	0.0022
0.01	100	150	200	0.01
0.014	140	210	280	0.015
0.028	280	420	560	0.027
0.056	560	840	1120	0.056
0.112	1120	1680	2240	0.1

1. Example calculations based on an ideal capacitor. During application design and component selection it should be considered that the current flowing into the external t_{REC} programming capacitor (C_{tREC}) is on the order of 100 nA, therefore a low-leakage capacitor (ceramic or film capacitor) and an adequate PCB environment should be used to prevent t_{REC} accuracy from being affected. A recommended minimum value of C_{tREC} is 0.001 µF.
2. In case of repeated activations of the t_{REC} counter, an interval of 10 ms min. is needed between t_{REC} intervals to fully discharge C_{tREC}, so that the next t_{REC} is as specified.

2 Typical operating characteristics

Figure 7. Supply current (I_{CC}) vs. temperature

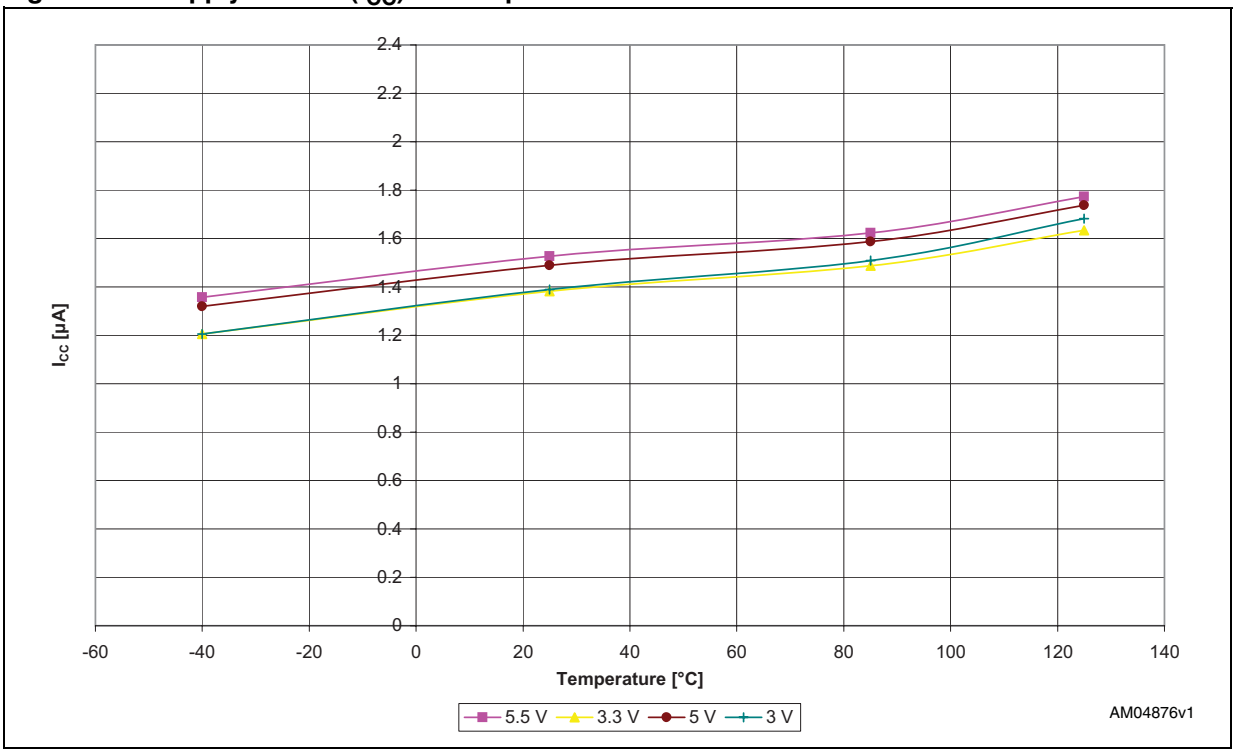


Figure 8. Smart Reset™ delay (t_{SRC}) vs. temperature, C_{SRC} = 0.56 µF

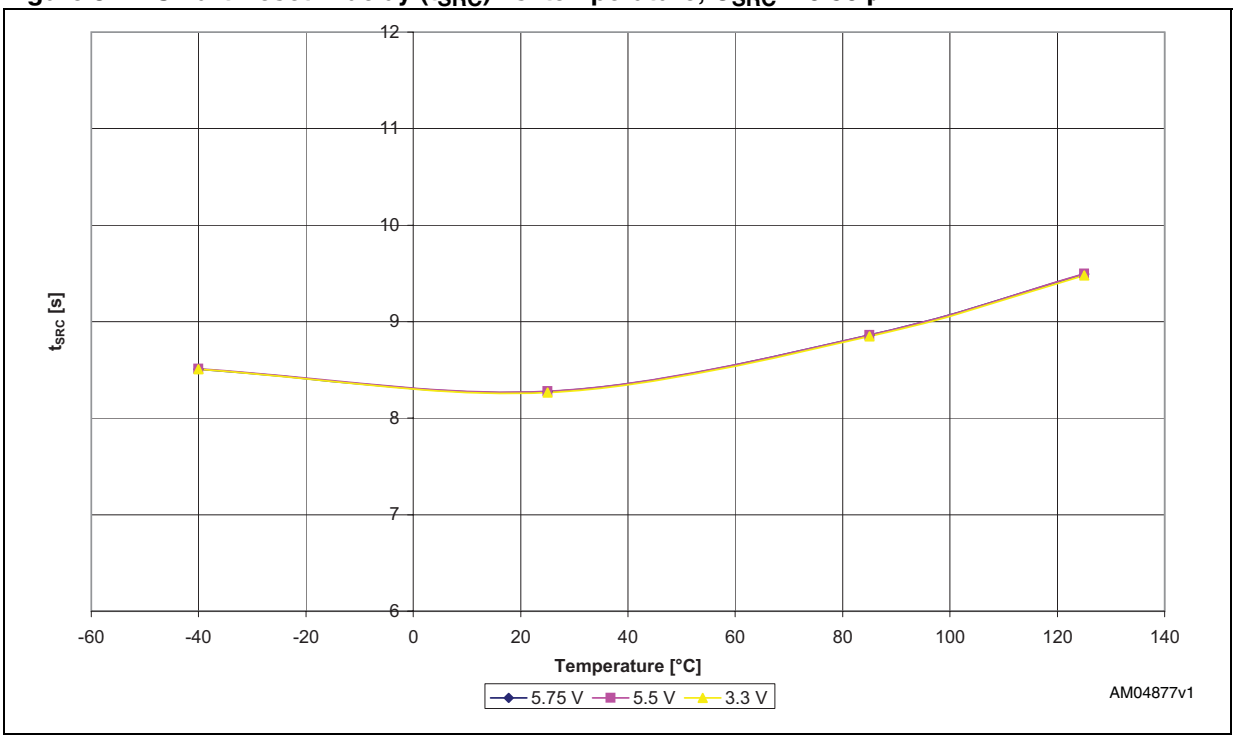


Figure 9. Reset timeout period (t_{REC}) vs. temperature, C_{tREC} = 0.01 µF

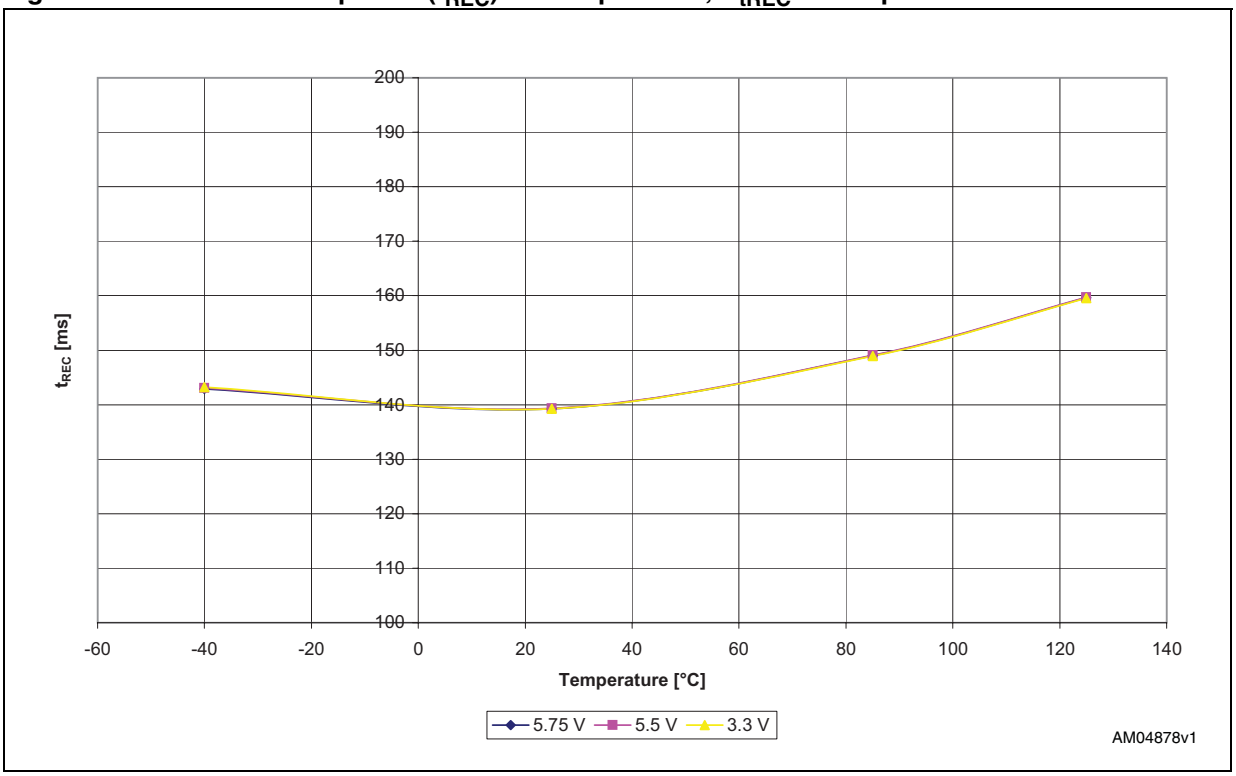
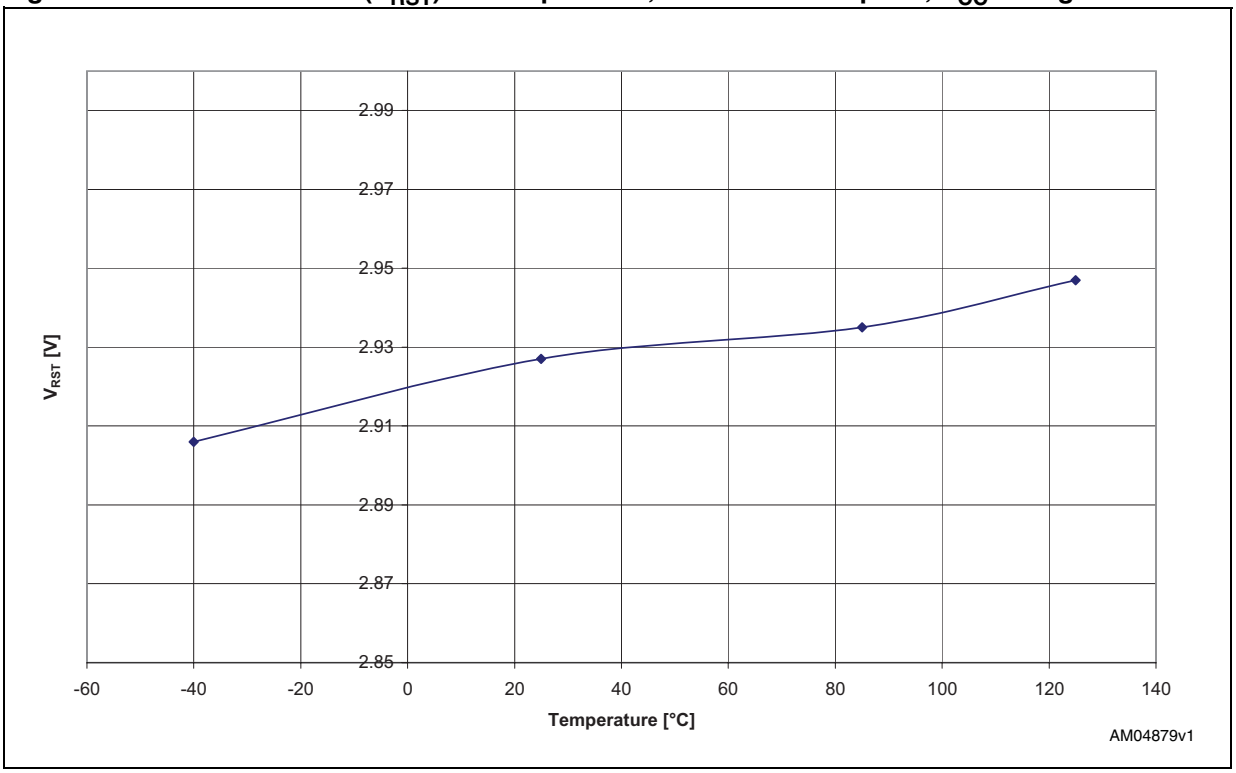


Figure 10. Reset threshold (V_{RST}) vs. temperature, "S" threshold option, V_{CC} falling



3 Maximum ratings

Stressing the device above the rating listed in the *Table 4: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics™ SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter		Value	Unit
T_{STG}	Storage temperature (V_{CC} off)		–55 to +150	°C
T_{SLD}(1)	Lead solder temperature for 10 seconds		260	°C
θ_{JA}	Thermal resistance (junction to ambient)	TDFN8	149.0	°C/W
V_{IO}	Input or output voltage		–0.3 to V_{CC} +0.3	V
V_{CC}	Supply voltage		–0.3 to 7	V

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.

4 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the *Table 6: DC and AC characteristics* that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 5: Operating and measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 5. Operating and measurement conditions

Parameter	Value	Unit
V_{CC} supply voltage	1.0 to 5.5	V
Ambient operating temperature (T_A)	–40 to +85	°C
Input rise and fall times	≤ 5	ns
Input pulse voltages	0.2 to 0.8 V_{CC}	V
Input and output timing ref. voltages	0.3 to 0.7 V_{CC}	V

Figure 11. AC testing input/output waveforms



Table 6. DC and AC characteristics

Symbol	Parameter	Test conditions[1]	Min.	Typ.[2]	Max.	Units
V_{CC}	Supply voltage range	Reset output valid - active-low	1.0		5.5	V
I_{CC}	Supply current (V_{CC})	V_{CC} = 5.0 V		1.5	2.4	µA
		V_{CC} = 3.0 V[3]		1.4		µA
V_{OL}	Reset output voltage low	$V_{CC} \geq$ 4.5 V, sinking 3.2 mA			0.3	V
		$V_{CC} \geq$ 3.3 V, sinking 2.5 mA			0.3	V
		$V_{CC} \geq$ 1.0 V, sinking 0.1 mA			0.3	V
V_{RST}	V_{CC} undervoltage reset threshold (refer to *Table 7*)	–40 to +85 °C	V_{RST} –2.5%	V_{RST}	V_{RST} +2.5%	V
		25 °C	V_{RST} –2.0%	V_{RST}	V_{RST} +2.0%	V
V_{HYST}	Hysteresis of V_{RST}	L, M		0.5%		
		T, S, R, Z, Y, W, V		1%		
	V_{CC} to reset delay[4]	V_{CC} falling from (V_{RST} + 100 mV) to (V_{RST} - 100 mV) at 10 mV/µs		20		µs
t_{REC}[4]	User-adjustable reset timeout period on $\overline{RST}$. Refer to *Table 3*.		10 000 x C_{tREC} (µF)	15 000 x C_{tREC} (µF)	20 000 x C_{tREC} (µF)	ms
Smart Reset™ inputs						
t_{SRC}[5]	User-adjustable delayed Smart Reset™ setup time. Refer to *Table 2*.		10 x C_{SRC} (µF)	15 x C_{SRC} (µF)	20 x C_{SRC} (µF)	s
V_{IL}	$\overline{SR0}$, $\overline{SR1}$ input voltage low				0.3 V_{CC}	V
V_{IH}	$\overline{SR0}$, $\overline{SR1}$ input voltage high		0.7 V_{CC}			V
R_{PUI}	Internal pull-up resistor, $\overline{SR0}$, $\overline{SR1}$ inputs			65		kΩ

1. Valid for ambient operating temperature: T_A = –40 to +85 °C; V_{CC} = 1.0 to 5.5 V (except where noted).
2. Typical value is at 25 °C and V_{CC} = 3.3 V unless otherwise noted.
3. For devices with V_{RST} < 3.0 V.
4. Guaranteed by design.
5. Input glitch immunity is equal to t_{SRC} (when both SR inputs are low, otherwise infinite).

Table 7. Possible V_{CC} voltage thresholds

V_{CC} voltage threshold V_{RST}	Typ.	±2.5% (–40 °C to +85 °C)		±2.0% (25 °C)		Unit
		Min.	Max.	Min.	Max.	
L (falling)	4.625	4.509	4.741	4.533	4.718	V
M (falling)	4.375	4.266	4.484	4.288	4.463	V
T (falling)	3.075	2.998	3.152	3.014	3.137	V
S (falling)	2.925	2.852	2.998	2.867	2.984	V
R (falling)	2.625	2.559	2.691	2.573	2.678	V
Z (falling)	2.313	2.255	2.371	2.267	2.359	V
Y (falling)	2.188	2.133	2.243	2.144	2.232	V
W (falling)	1.665	1.623	1.707	1.632	1.698	V
V (falling)	1.575	1.536	1.614	1.544	1.607	V

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 12. TDFN – 8-lead 2 x 2 x 0.75 mm, 0.5 mm pitch package outline

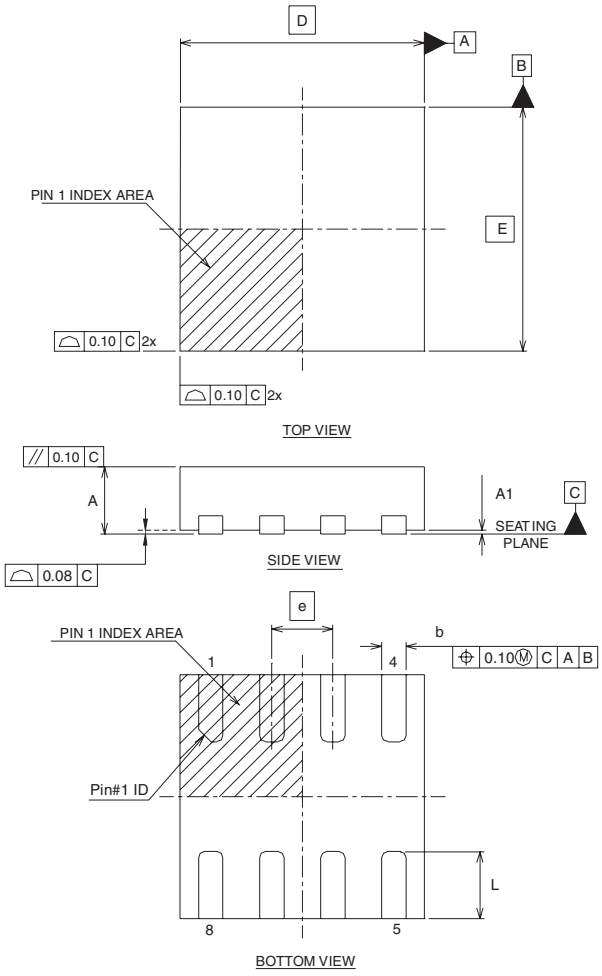


Table 8. TDFN – 8-lead 2 x 2 x 0.75 mm, 0.5 mm pitch package mechanical data

Symbol	Dimension (mm)			Dimension (inches)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D BSC		2.00			0.079	
E BSC		2.00			0.079	
e		0.50			0.020	
L	0.45	0.55	0.65	0.018	0.022	0.026

Figure 13. Landing pattern - TDFN – 8-lead 2 x 2 mm without thermal pad

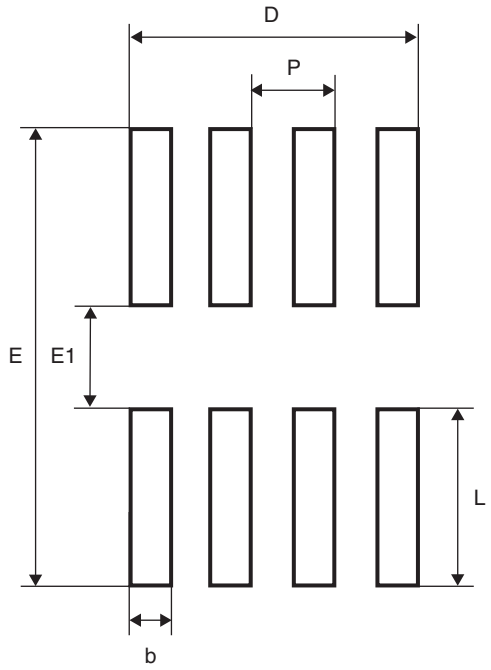


Table 9. Parameter for landing pattern - TDFN – 8-lead 2 x 2 mm package

Parameter	Description	Dimension (mm)		
		Min.	Nom.	Max.
L	Contact length	1.05	—	1.15
b	Contact width	0.25	—	0.30
E	Max. land pattern Y-direction	—	2.75	—
E1	Contact gap spacing	—	0.65	—
D	Max. land pattern X-direction	—	1.75	—
P	Contact pitch	—	0.5	—

Figure 14. Carrier tape

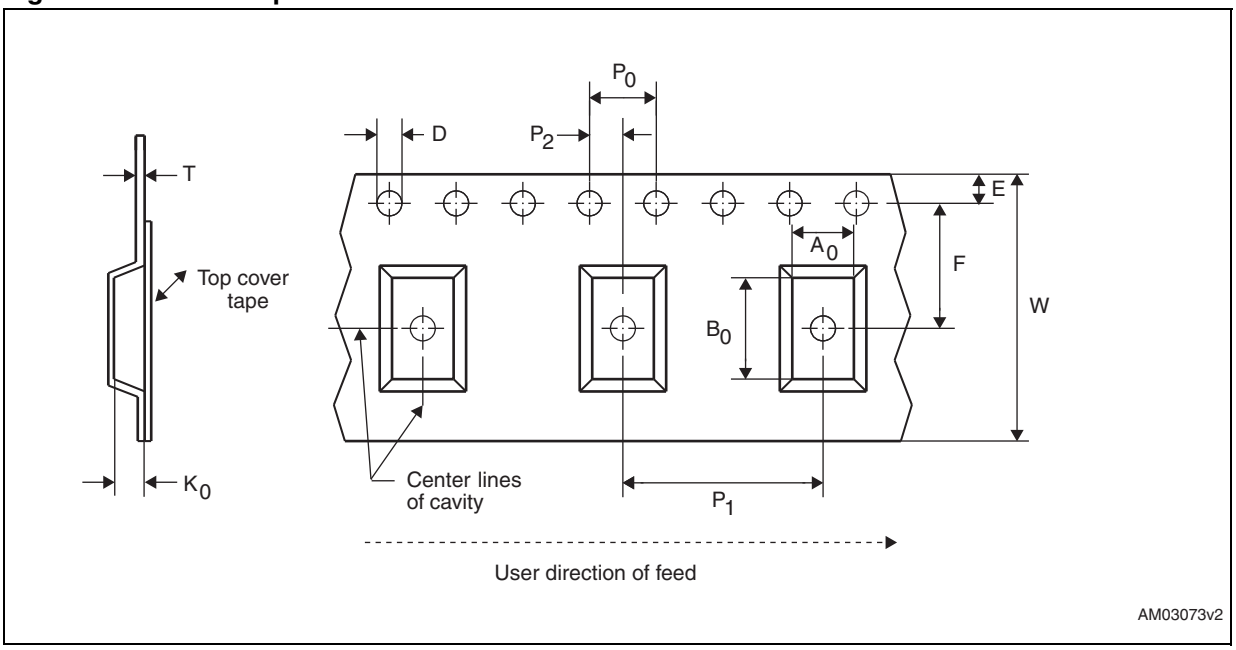


Table 10. Carrier tape dimensions

Package	W	D	E	P_0	P_2	F	A_0	B_0	K_0	P_1	T	Unit	Bulk qty.
TDFN8	8.00 +0.30 –0.10	1.50 +0.10/ –0.00	1.75 ±0.10	4.00 ±0.10	2.00 ±0.10	3.50 ±0.05	2.30 ±0.05	2.30 ±0.05	1.00 ±0.05	4.00 ±0.10	0.250 ±0.05	mm	3000

Figure 15. Reel dimensions

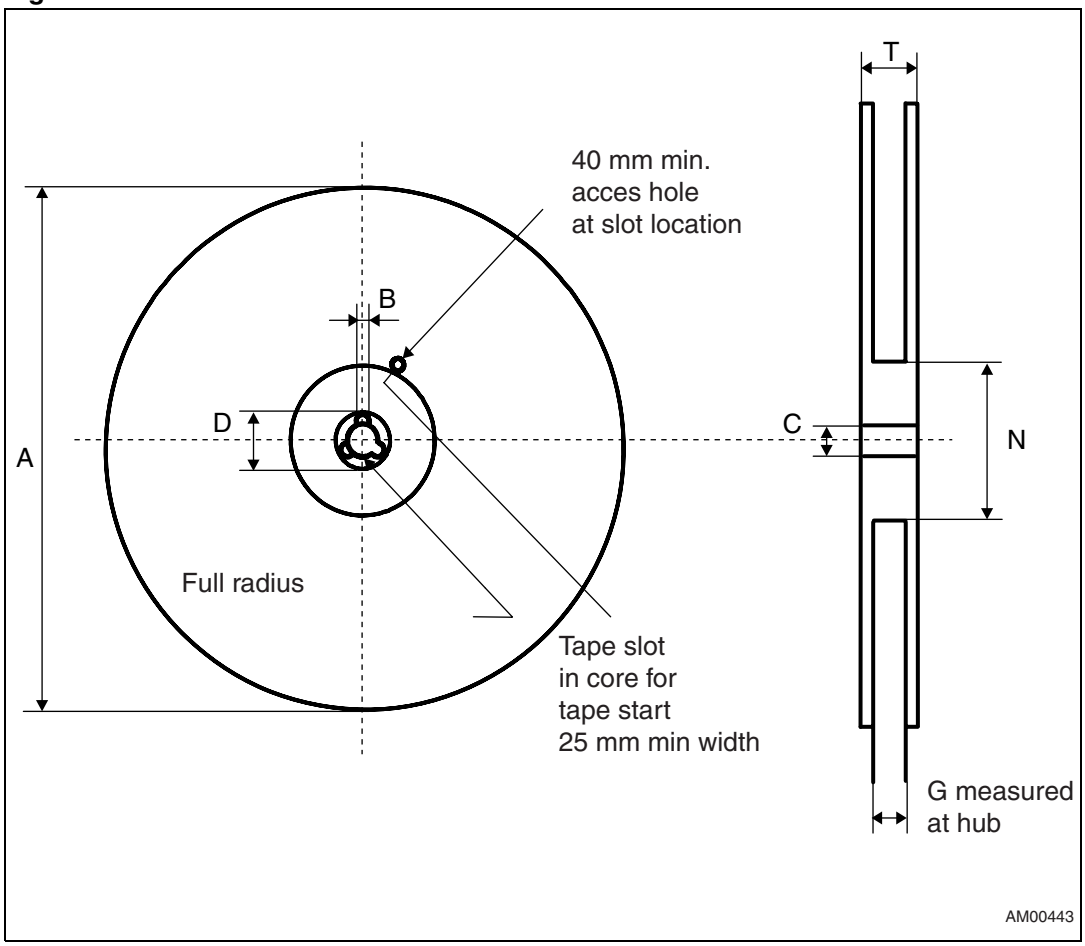


Table 11. Reel dimensions

Tape sizes	A max.	B min.	C	D min.	N min.	G	T max.
8 mm	180 (7 inches)	1.50	13.0 +/– 0.20	20.20	60	8.4 +2/–0	14.40

Figure 16. Tape trailer/leader

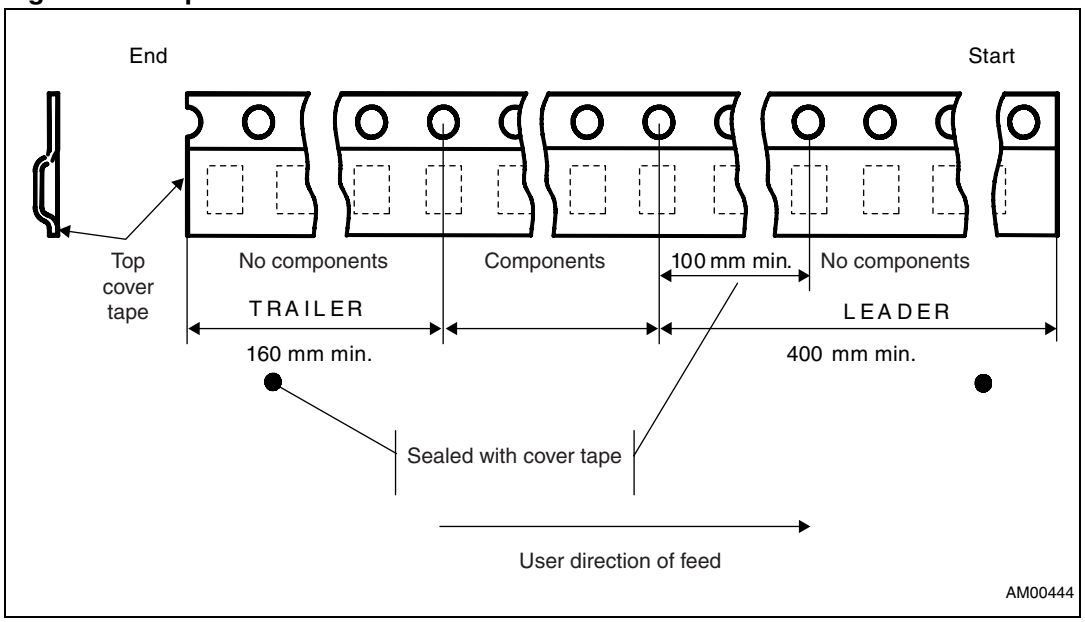
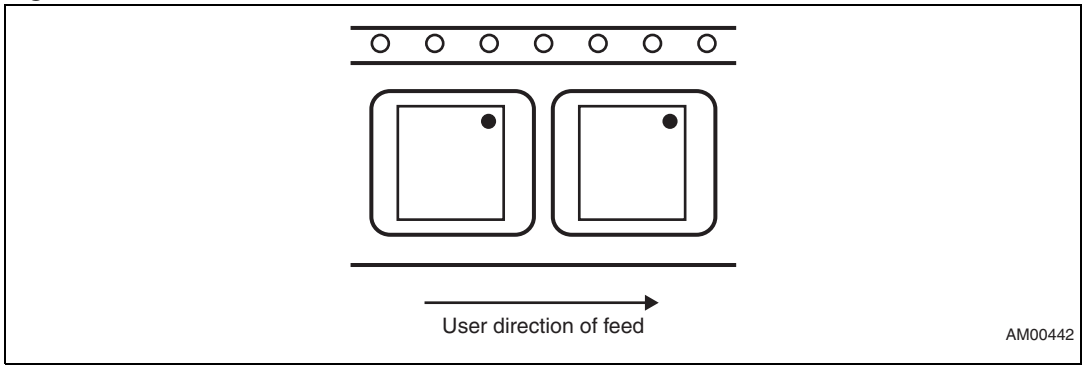


Figure 17. Pin 1 orientation



Note: 1 Drawings are not to scale.

2 All dimensions are in mm, unless otherwise noted.

6 Part numbering

Table 12. Ordering information scheme

Example: **STM6510 W C A C DG 6 F**

Device type

STM6510

Reset (V_{CC} monitoring threshold) voltage V_{RST}

L = 4.625 V (typ., falling)

M = 4.375 V

T = 3.075 V

S = 2.925 V

R = 2.625 V

Z = 2.313 V

Y = 2.188 V

W = 1.665 V

V = 1.575 V

Smart Reset™ setup delay control (t_{SRC}); presence of internal input pull-up on all Smart Reset™ inputs ($\overline{SR0}$, $\overline{SR1}$)

C = 1 to 15 s, user-programmable (external capacitor); 65 kΩ input pull-up

Output type

A = open-drain, active-low

Reset timeout period (t_{REC})

C = user-programmable (external capacitor)

Package

DG = TDFN8 - 2 x 2 x 0.75 mm, 0.5 mm pitch

Temperature range

6 = –40 °C to +85 °C

Shipping method

F = ECOPACK® package, tape and reel

For device options currently available refer to *Table 13*. For other options, voltage threshold values etc. or for more information on any aspect of this device, please contact the ST sales office nearest you.

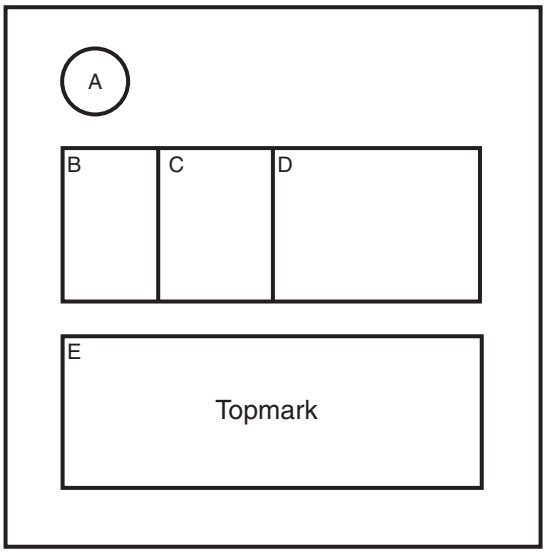
7 Package marking

Table 13. Package marking

Part name	t_{SRC} delay control	Smart Reset™ inputs type	V_{RST}	Reset output type	t_{REC} programming	Topmark
STM6510WCACDG6F	C_{SRC}	AL, PU	W	AL, OD	C_{tREC}	8WK
STM6510SCACDG6F	C_{SRC}	AL, PU	S	AL, OD	C_{tREC}	8SK
STM6510RCACDG6F	C_{SRC}	AL, PU	R	AL, OD	C_{tREC}	8RK

Note: AL = Active-Low, AH = Active-High; PU = with internal pull-up resistor, OD = Open-Drain.

Figure 18. Package marking, top view



A = dot (pin 1 reference)
B = assembly plant (P)
C = assembly year (Y, 0-9): 9 = 2009 etc.
D = assembly work week (WW, 01 to 52): 20 = WW20 etc.
E = marking area (topmark)

AM00479

8 Revision history

Table 14. Document revision history

Date	Revision	Changes
12-Feb-2010	1	Initial release.
26-Feb-2010	2	Updated title of datasheet, *Features*, *Applications*; updated footnote *1* of *Table 2*; updated *Table 6*, *12*, *13*; *Figure 3*; *Section 1.3.3*; minor textual and formatting changes.

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