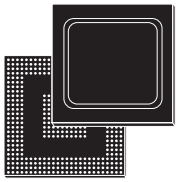
STLS2F02

Loongson 2F
high performance 64-bit superscalar MIPS® microprocessor

Preliminary Data

Features

- 64-bit superscalar architecture
- 900 MHz clock frequency
- Single/double precision floating-point units
- New streaming multimedia instruction set support (SIMD)
- 64 Kbyte instruction cache, 64 Kbyte data cache, on-chip 512 Kbyte unified L2 cache
- On chip DDR2-667 and PCI-X controller
- 4 W @ 900 MHz power consumption:
  - Best in class for power management
  - Voltage/frequency scaling
  - Standby mode support
  - L2 cache disable/enable option
- Leading edge 90 nm process technology
- 27x27 heat spreader flip-chip BGA package
- MIPS based (compatible with MIPSIII) instruction set



HFCBGA452 (27x27x2.9mm)

Description

The STLS2F02 is a MIPS based 64-bit superscalar microprocessor, able to issue four instructions per clock cycle among six functional units: two integer, two single/double-precision floating-point, one 64-bit SIMD and one load/store unit.

The micro architecture is organized with nine stages of pipeline and support of dynamic branch prediction.

The memory hierarchy is composed by the first level of 64 Kbyte 4-way set associative caches for instructions and data, the second level of 512 Kbyte unified 4-way set associative cache and the memory management unit with table lookside buffer.

The Loongson microprocessor family is the outcome of a successful collaboration started in 2004 between STMicroelectronics and the Institute of Computing Technology, part of the Chinese Academy of Science. Loongson microprocessors were co-developed by STMicroelectronics and the Institute of Computing Technology to address all the applications requiring high level of performance and low power dissipation.

Compared to the STLS2E02 processor, the STLS2F02 has an enhanced architecture providing higher performances, reduced power consumption, integrated DDR2 memory controller and PCI-X bus interface.

Table 1. Device summary

Order code	Package	Packing
STLS2F02	HFCBGA452 (27x27x2.9 mm)	Tray

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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1 Introduction

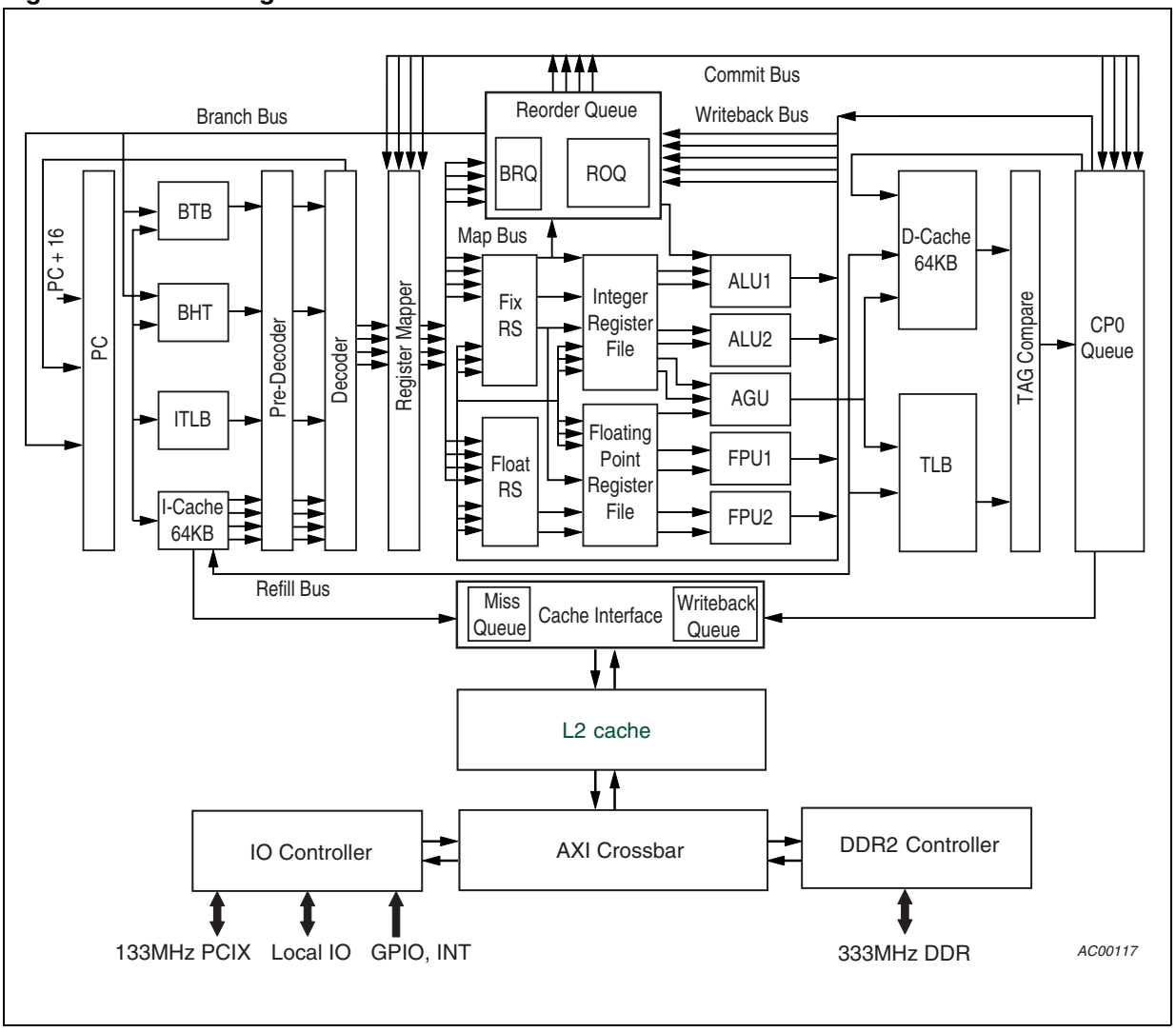
STLS processors are based on the Loongson CPU architecture licensed by STMicroelectronics from the Institute of Computing Technology (ICT), which is part of the Chinese Academy of Science. The STLS family contains 64-bit high-end processors for applications requiring high levels of performance and efficiency in terms of cost, power consumption and area.

The Loongson CPU architecture is compatible in user mode at the MIPSIII level of the MIPS64-bit architecture.

This microprocessor achieves a leading position in the MIPS family for its combination of multiple features, including high clock frequency, out-of-order superscalar execution and ability to run single-instruction-multiple data (SIMD).

STLS processors implement a superscalar, out-of-order execution pipeline with dynamic branch prediction and non-blocking cache.

Figure 1. Block diagram



The instruction pipeline allows fetch and coding of four instructions per cycle and dynamic issue of the decoded instructions to five fully-pipelined function components.

The STLS2F02 uses out-of-order execution and an aggressive memory hierarchy design to maximize pipeline efficiency.

Out-of-order execution is accomplished with a combination of register renaming, dynamic scheduling, and branch prediction techniques. The result is fewer pipeline stalls caused by WAR (write after read) and WAW (write after write) hazards, RAW (read after write) hazards, and control hazards. The STLS2F02 has a 64-entry physical register file for fixed- and floating-point register renaming, a 16-entry fixed-point reservation station, and a 16-entry floating-point reservation station that is responsible for out-of-order instruction issuing. A 64-entry ROQ (reorder queue) ensures that out-of-order executed instructions are committed in the program order. For precise branch prediction, a 16-entry BTB (branch target buffer), a 4K-entry BHT (branch history table), a 9-bit GHR (global history register), and a 4-entry RAS (return address stack) are used to record branch history information.

The STLS2F02 memory hierarchy is also engineered for high performance. There is a 64 Kbyte instruction cache, a 64 Kbyte data cache, and a 512 Kbyte level-two cache, all four-way set associative. The on-chip DDR memory allows the STLS2F02 to achieve high memory bandwidth with low latency. The fully associative translation lookahead buffer (TLB) has 64 entries, each mapping an odd and even page. A 24-entry memory access queue contains a content-addressable memory for dynamic memory disambiguation and allows the STLS2F02 to implement out-of-order memory access, non-blocking cache, load speculation, and store forwarding.

The STLS2F02 has two fixed-point functional units, two floating-point functional units, and one memory access unit. The floating-point units can also execute 32-bit or 64-bit fixed-point instructions and 8-bit or 16-bit SIMD fixed-point instructions through extension of the fmt field of the floating-point instructions. The SIMD unit extends the STLS2E02 with new XX SSE2 type instructions.

The basic pipeline stages of the STLS2F02 include instruction fetch, pre-decode, decode, register rename, dispatch, issue, register read, execution, and commit.

The STLS2F02 device:

- is manufactured in ST 90 nm CMOS technology.
- is an evolution of the STLS2E02 with enhanced I/O and memory accessing bandwidth and a software working frequency changing scheme.
- has a standard 32-bit PCI/PCI-X interface, a standard 64-bit DDR2 interface, an 8/16-bit local IO interface, a 4-bit GPIO interface.
- achieves a higher memory accessing bandwidth by utilizing a 64-bit DDR2 memory controller.

Compared to its predecessor, the STLS2F02 provides better power management ability by using a software manageable working frequency changing scheme. The operating system can use this feature to change the processor frequency according to the workload.

The STLS2F02 integrates a video accelerate module in its write data path to the PCI/PCI-X controller. Coupled with software drivers, the video accelerate module can transfer YUV format video data to RGB format and zoom automatically. This greatly reduces the processor's workload when the system utilizes a simple VGA controller.

The cores are centered on a 2x2 AXI cross bar with 128-bit width data bus. The CPU core and PCI/PCI-X slave takes up two master ports, and the DDR2 controller one slave port. All other modules including the PCI/PCI-X master share one slave port.

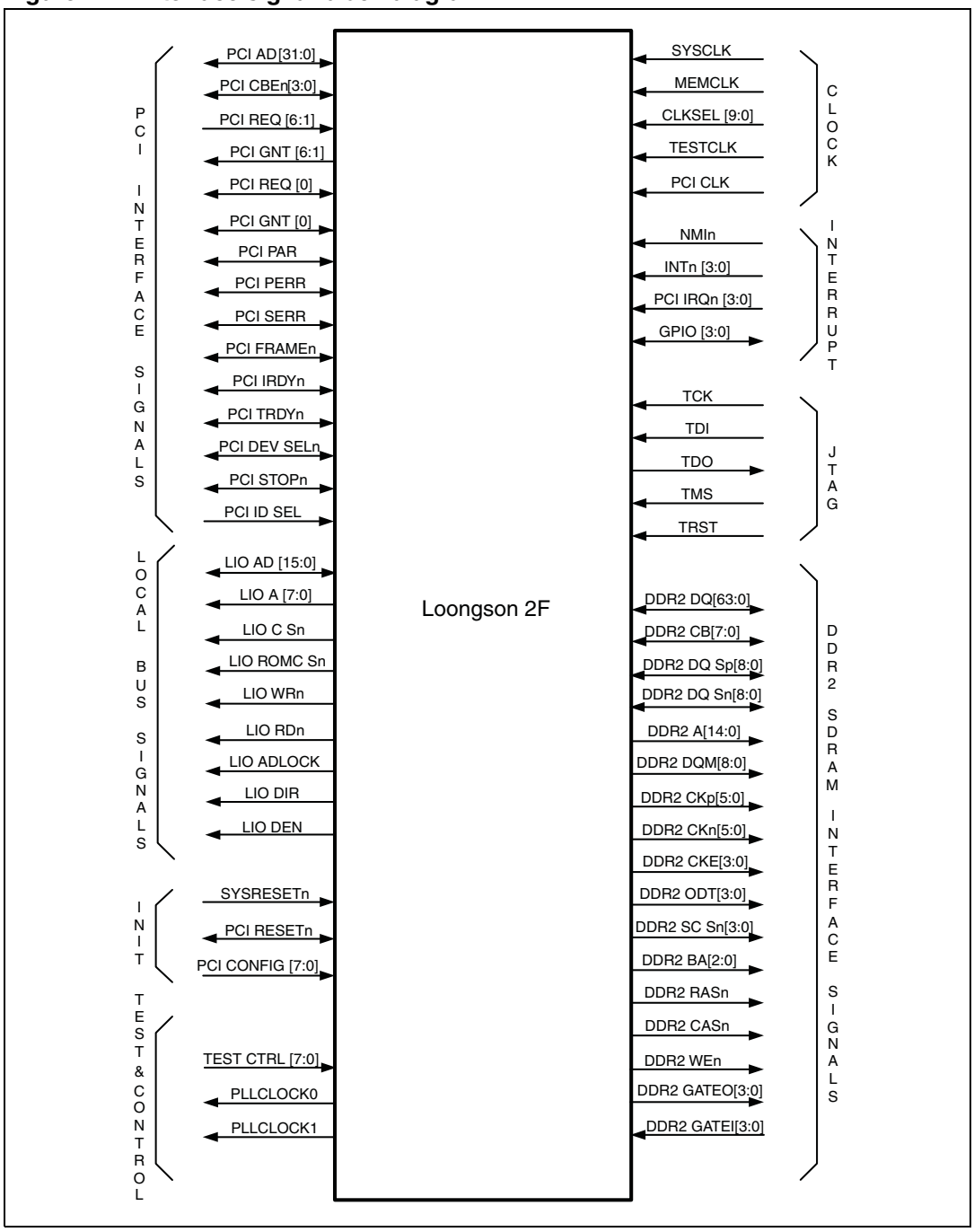
2 Interface description

2.1 Interface signal block diagram

The STLS2F02interface signals are shown in *Figure 2*.

Note: The arrow indicates signal directions, for example input, output or bi-direction.

Figure 2. Interface signal block diagram



2.2 PCI bus interface signal components

The STLS2F02 PCI bus signals include:

- 32-bit address data bus
- 4-bit command data ID bus
- 14-bit bus arbitrator
- 7-bit interface control
- 2-bit error report signals

The STLS2F02 PCI bus signals are shown in *Table 2*.

Table 2. PCI bus signals

Name	Input/output	Description
PCI_AD[63:0]	I/O	PCI address/data bus
PCI_CBEn[7:0]	I/O	PCI command/byte
PCI_PAR	I/O	Address/data parity check signal
PCI_REQn[6:1]	I	External request
PCI_REQn[0]	I/O	External request input/request output to external arbiter
PCI_GNT[6:1]	O	PCI bus grant to external device
PCI_GNT[0]	I/O	PCI bus grant to external device / grant input from external arbiter
PCI_FRAMEn	I/O	PCI bus cycle frame
PCI_IRDYn	I/O	PCI initiator ready
PCI_TRDYn	I/O	PCI target ready
PCI_STOPn	I/O	PCI stop
PCI_DEVSELn	I/O	PCI device select

2.3 DDR2 SDRAM interface signal components

The STLS2F02 includes a built-in memory controller fully compatible with DDR2 SDRAM industry standard (JESD79-2B). These signals include:

- 72-bit bidirectional data bus (ECC included)
- 9-bit bidirectional data strobe differential signal (ECC included)
- 9-bit data mask signal (ECC included)
- 15-bit address bus
- 7-bit bank and chip select signal
- 6-bit differential clock
- 4-bit clock enable
- 3-bit command bus
- 4-bit delay sample input/output signal
- 4-bit ODT (on die termination) signal

The STLS2F02 DDR2 SDRAM controller signals are shown in *Table 3*.

Table 3. DDR2 SDRAM controller interface signals

Name	Input/output	Description
DDR2_DQ[63:0]	IO	DDR2 SDRAM data bus
DDR2_CB[7:0]	IO	DDR2 SDRAM data ECC data bus
DDR2_DQSp[8:0]	IO	DDR2 SDRAM data strobe (ECC included)
DDR2_DQSn[8:0]	IO	DDR2 SDRAM data strobe (ECC included)
DDR2_DQM[8:0]	O	DDR2 SDRAM data mask (ECC included)
DDR2_A[14:0]	O	DDR2 SDRAM address bus
DDR2_BA[2:0]	O	DDR2 SDRAM bank address signal
DDR2_WEn	O	DDR2 SDRAM write enable
DDR2_CASn	O	DDR2 SDRAM column select enable
DDR2_RASn	O	DDR2 SDRAM row select enable
DDR2_SCSn[3:0]	O	DDR2 SDRAM chip select
DDR2_CKE[3:0]	O	DDR2 SDRAM clock enable
DDR2_CKp[5:0]	O	DDR2 SDRAM phase clock output
DDR2_CKn[5:0]	O	DDR2 SDRAM phase inversion clock output
DDR2_GATEI[3:0]	I	DDR2 SDRAM delay sample input signal
DDR2_GATEO[3:0]	O	DDR2 SDRAM delay sample output signal
DDR2_ODT[3:0]	O	DDR2 SDRAM on die termination signal

2.4 Local bus signals

The local bus provides a simple bus interface for system boot ROM and IO device. The interface is designed for chip-connect simplicity.

The local bus signals are shown in *Table 4*.

Table 4. Local bus signals

Name	Input/output	Description
LIO_AD[15:0]	I/O	Local IO address and data bus (when ADLOCK valid output the most significant 16-bit)
LIO_A[7:0]	O	Lowest significant 8-bit address bus
LIO_CSn	O	Local IO chip select
LIO_ROMCSn	O	Local IO ROM chip select
LIO_WRn	O	Local IO write enable
LIO_RDn	O	Local IO read enable
LIO_ADLOCK	O	Local IO address lock
LIO_DIR	O	Local IO direction
LIO_DEN	O	Local IO device enable

2.5 Initialization signals

Table 5 details the initialization signals.

Table 5. Initialization interface signals

<table>
<tr><th>Name</th><th>Input/output</th><th colspan="4">Description</th></tr>
<tr><td>SYSRESETn</td><td>I</td><td colspan="4">System reset. Low state of the signal must be maintained more than one SYSCLK period. It can be asynchronous to SYSCLK</td></tr>
<tr><td>PCI_RESETn</td><td>I/O</td><td colspan="4">PCI interface reset</td></tr>
<tr><td rowspan="8">PCI_CONFIG</td><td rowspan="8">I</td><td colspan="4">PCI configuration
7 undefined
6:5 PCIX BUS speed selection
4 PCIX BUS mode
3 Master mode
2 Start from PCI
1 External PCI arbitration
0 16-bit starting ROM
Note:</td></tr>
<tr><td>6</td><td>5</td><td>4</td><td>PCIX BUS mode</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>PCI 33/66</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>PCIX 66</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>PCIX 100</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>PCIX 133</td></tr>
</table>

The STLS2F02 processor includes two reset signals:

- SYSRESETn: This reset signal is the only way to reset whole STLS2F02 processor. SYSCLK and MEMCLK must provide stable clock when SYSRESETn is valid. The width of SYSRESETn should be more than one clock period. Internal reset-control begins to reset the internal logic when the reset signal is invalid. The internal reset is finished after 64K SYSCLK cycle. The reset exception vector can then be executed.
- PCI_RESETn: This signal works as an output when the processor works as a system main bridge. The reset of PCIX devices in the system must be controlled by this signal. When the processor works as a PCI/PCIX device, the signal works as reset input to the PCI interface of the processor.

Note: Resetting the PCI interface when a process is running may cause the processor to stop working.

PCI_CONFIG defines the working mode of the processor interface. It must be stable during system reset, so that software can read this value from an internal register after system start up. The PCI address of the first instruction is 0x1FC0 0000 when system start from PCI is configured. Otherwise the first instruction is fetched from address 0 of local bus ROM.

2.6 Interrupt signals

The STLS2F02 processor supports up to 12 external interrupts and one non-maskable interrupt (NMI). There are 4 PCI interrupt signals, 4 special interrupt signals and 4 configurable GPIO interrupt. There are also 3 internal interrupts, two PCI bus error report signals and one DDR2 control interrupt. When an interrupt occurs, the processor handles the exception. *Table 6* details the interrupt signals.

Table 6. Interrupt interface signals

Name	Input/output	Description
INTn[3:0]	I	4 external interrupt signals. OR operations are performed on these signals with interrupt register from bit 5 to bit 2 separately
NMIn	I	NMI. An OR operation is performed on the NOT-value of this signal and the interrupt register's 6th bit
GPIO[3:0]	I/O	These interrupts should be enabled in the interrupt controller and can be configured as different active power level and different trigger mode. These interrupts could be routed to interrupt register bit 0/1
PCI_IRQ[3:0]	I	These interrupts should be enabled in the interrupt controller and low active. These interrupts could be routed to interrupt register bit 0/1
PCI_PERR	I/O	PCI bus parity error, high pulse active. These interrupts could be routed to interrupt register bit 0/1
PCI_SERR	I/O	PCI bus error, high pulse active. These interrupts could be routed to interrupt register bit 0/1

2.7 JTAG signals

The STLS2F02 provides a JTAG-compliant boundary scan interface. The JTAG interface is particularly suitable for testing the processor pins for connectivity. *Table 7* details the JTAG signals.

Table 7. JTAG interface signals

Name	Input/output	Description
TDI	I	JTAG serial scan data input
TDO	O	JTAG serial scan data input
TMS	I	JTAG command, indicating that the input serial data is a command.
TCK	I	JTAG serial scan clock

2.8 Test and control signals

On the STLS2F02 chip, the test signals are only used for chip physical test, for example scan chain test. When the chip works normally, these signals are set invalid (to 1).

2.9 Clock signals

Table 8 details the STLS2F02 chip clocks. The processor has three system input clock signals. (SYSCLK, MEMCLK and PCI_CLK). TESTCLK is only used for chip test.

The CPU core clock and DDR2 control clock are generated separately by the PLL using SYSCLK and MEMCLK. The frequency division is controlled by CLKSEL. For further information about the division factor, see *Table 9* and *Table 10*. MEMCLK frequency can also be configured through control register CR88 except pins CLKSEL [9:5]. Please refer to register CR88 in the STLS2F02 user manual.

Table 8. Clock signals

Name	Input/output	Description
SYSCLK	I	System input clock, which drives the built-in PLL to generate core clock. It also used as clock of system reset circuit
MEMCLK	I	DDR2 controller input clock, which is used by the built-in PLL to generate DDR2 control clock
CLKSEL[4:0]	I	PLL frequency division control signal of core clock, see *Table 9*
CLKSEL[9:5]	I	PLL frequency division control signal of DDR2 controller clock, see *Table 10*
PCI_CLK	I	Clock for PCI and local bus interface.

Table 9. Processor internal/external frequency configuration

CLKSEL[4:0]	Multi. factor	Input frequency range (MHz)	CLKSEL[4:0]	Multi. factor	Input frequency range (MHz)
11xxx	1	-			
10000	2.25	88.9~177.8	01100	6.5	61.5~123.1
10001	2.5	80.0~160.0	01101	7	57.1~114.3
10010	2.75	72.7~145.5	01110	7.5	53.3~106.7
10011	3	66.7~133.3	01111	8	50.0~100.0
10100	3.25	61.5~123.1	00000	9	88.9~177.8
10101	3.5	57.1~114.3	00001	10	80.0~160.0
10110	3.75	53.3~106.7	00010	11	72.7~145.5
10111	4	50.0~100.0	00011	12	66.7~133.3
01000	4.5	88.9~177.8	00100	13	61.5~123.1
01001	5	80.0~160.0	00101	14	57.1~114.3
01010	5.5	72.7~145.5	00110	15	53.3~106.7
01011	6	66.7~133.3	00111	16	50.0~100.0

Table 10. DDR internal/external frequency division factor

CLKSEL[9:5]	Multi. factor	Input frequency range (MHz)	CLKSEL[9:5]	Multi. factor	Input frequency range (MHz)
11000	1.125	88.9~177.8	10100	3.25	61.5~123.1
11001	1.25	80.0~160.0	10101	3.5	57.1~114.3
11010	1.375	72.7~145.5	10110	3.75	53.3~106.7
11011	1.5	66.7~133.3	10111	4	50.0~100.0
11100	1.625	61.5~123.1	01000	4.5	88.9~177.8
11101	1.75	57.1~114.3	01001	5	80.0~160.0
11110	1.875	53.3~106.7	01010	5.5	72.7~145.5
11111	2	50.0~100.0	01011	6	66.7~133.3
10000	2.25	88.9~177.8	01100	6.5	61.5~123.1
10001	2.5	80.0~160.0	01101	7	57.1~114.3
10010	2.75	72.7~145.5	01110	7.5	53.3~106.7
10011	3	66.7~133.3	01111	8	50.0~100.0
-	-	-	00xxx	1	-

2.10 Supply and ground

See *Table 11* for supply and ground signals of the STLS2F02.

Table 11. Supply and ground signals

Name	Input/output	Description
Vdd	PWR	1.2 V CPU core voltage
Gnd	GND	1.2 V CPU core ground
Vdde1v8	PWR	1.8 V DDR2 power supply
Gnde	GND	1.8 V DDR2 and 3.3V IO ground
Vdde3v3	PWR	3.3 V IO power supply
DDR2_VREF	I	0.9 V DDR reference voltage input
Pll_vdd_1	PWR	1.0 V PLL 1 digital power supply
Pll_gnd_1	GND	1.0 V PLL 1 digital ground
Pll_vdd_0	PWR	1.0 V PLL 0 digital power supply
Pll_gnd_0	GND	1.0 V PLL 0 digital ground
Pllio_vdde1v8	PWR	1.8 V PLL IO power supply
Pllio_gnde	GND	1.8 V PLL IO ground
Pllio_vdd	PWR	1.2 V PLL IO power supply
Pllio_gnd	GND	1.2 V PLL IO ground
Pll_vdde1v8_1	PWR	1.8 V PLL 1 analog power supply
Pll_gnde_1	GND	1.8 V PLL 1 analog ground
Pll_vdde1v8_0	PWR	1.8 V PLL 0 analog power supply
Pll_gnde_0	GND	1.8 V PLL 0 analog ground
Comp1v8_gnd	GND	Compensation reference current ground
Comp1v8_resistor	I	Compensation external resistor input

3 IO bus interface description

The STLS2F02 processor IO interface consists of the PCI bus and a local bus. The PCI bus is used to for generic peripheral device interface, while the local bus a simple interface for processor boot or debug.

3.1 PCI interface characteristic

The PCI interface features are as follows:

- PCI 2.3 and PCIX 1.0 compatible
- Support PCI 66 MHz and PCIX133 MHz
- Support dual address cycle for 64-bit addressing
- Support 8 outstanding master request in PCIX mode
- Support 4 delay-split read request in PCIX mode

3.2 Host and agent mode

The STLS2F02 PCI interface can work in host mode or agent mode, depending on the initial value of signal PCI_CONFIG.

When the processor works in host mode, the interface initializes the bus device according to the value of PCI_CONFIG[6:4]. In this case, PCI_IDSEL can be connected directly to GND.

When the processor works in agent mode, the initial value of the PCI bus defines the working-mode of the interface. In host mode, on the system main board, the value of PCI_CONFIG[6:4] should be set according to the ability of bus device. (Refer also to the PCIX 1.0 standard)

3.3 PCI bus arbitrator

The PCI/PCIX bus arbitrator built into the STLS2F02 supports up t o 7 external masters. The arbitration rules are two-level round robin scheduling. The level of each request is determined by software configuration. The bus is granted to insert a dummy cycle during switching. Bus parking can be configured as the last master or any specified master.

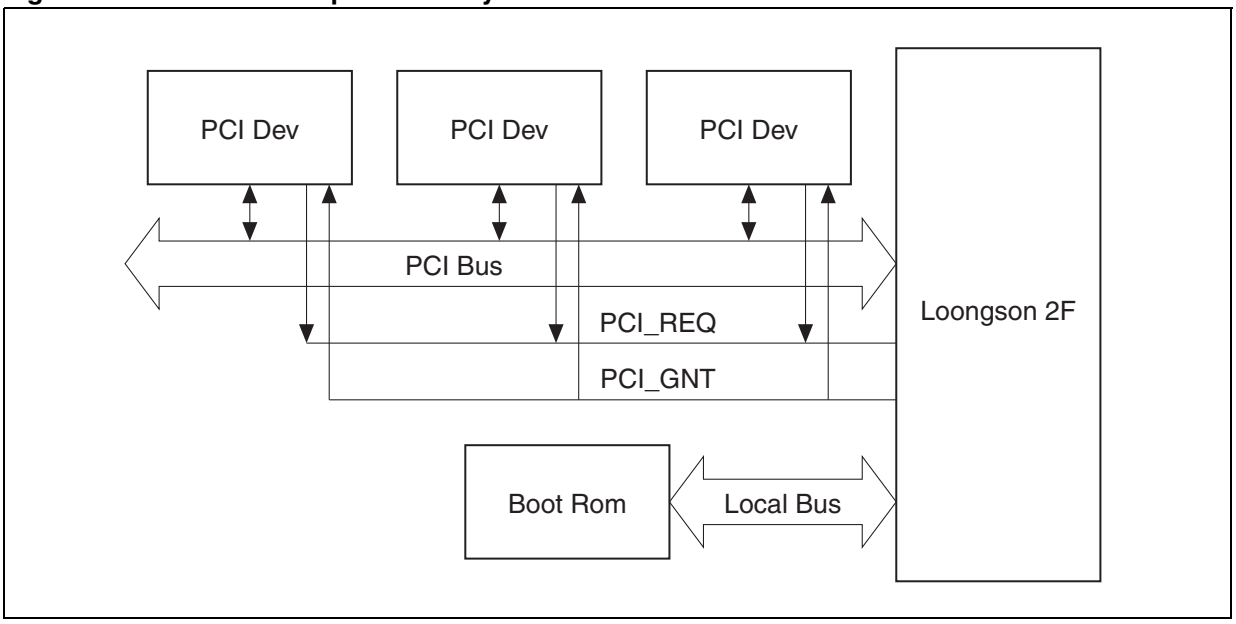
The internal request/grant wire of the interface can be set to connect to the number 0 request/grant wire by PCI_CONFIG [1] so that the external bus arbitrator can be used.

3.4 System interface connection

The STLS2F02 processor can be easily implemented in uniprocessor system. Since no multi-processor cache coherence protocol is supported in the PCI interface, the cache coherence should be managed by software in a multiprocessor system.

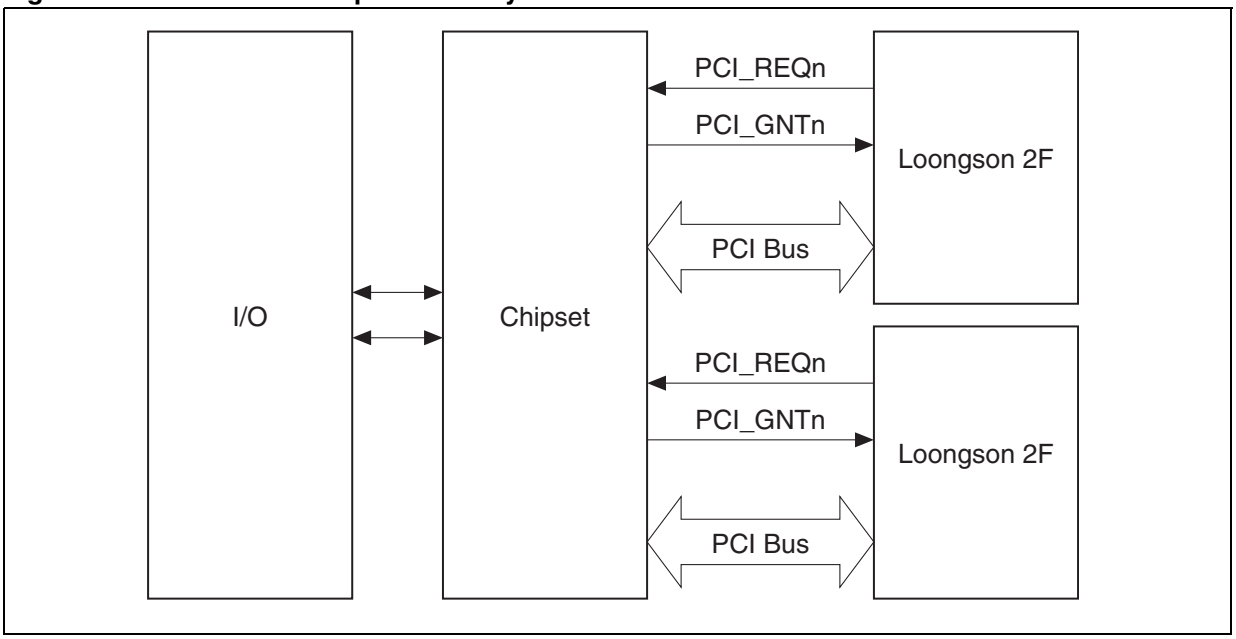
3.4.1 Single processor system connection

Figure 3. STLS2F02 uniprocessor system connection



3.4.2 Multiprocessor system connections

Figure 4. STLS2F02 multiprocessor system connections



3.5 Local bus description

The local bus is a simple peripheral interface. It is mainly used to connect to boot ROM. There are two chip select signals, and a corresponding configurable data width and access delay. The read and writing timings are shown in *Figure 5* and *Figure 6*. When the data width is 16-bits, the output address can be generated by shifting the physical address right one bit.

Figure 5. Local bus read timing

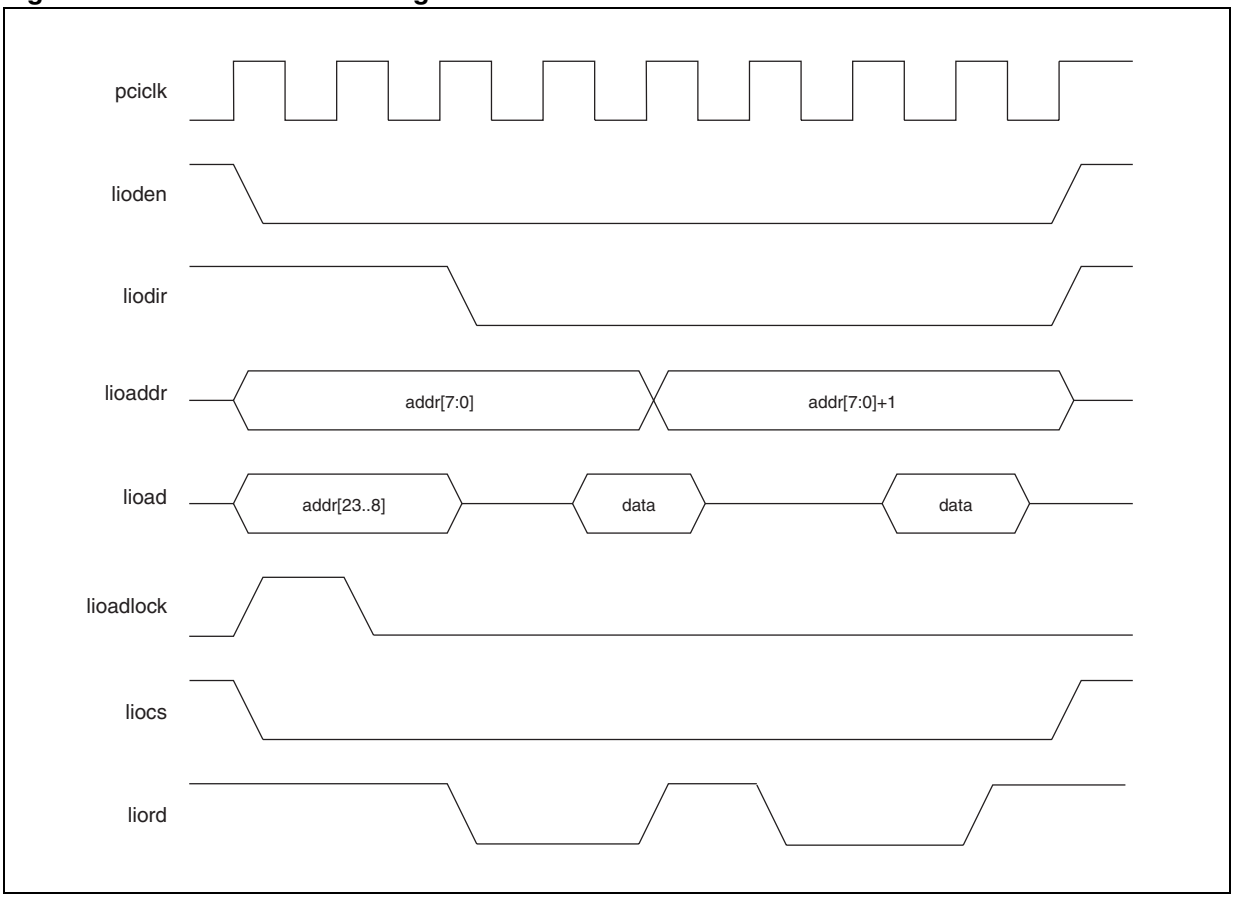
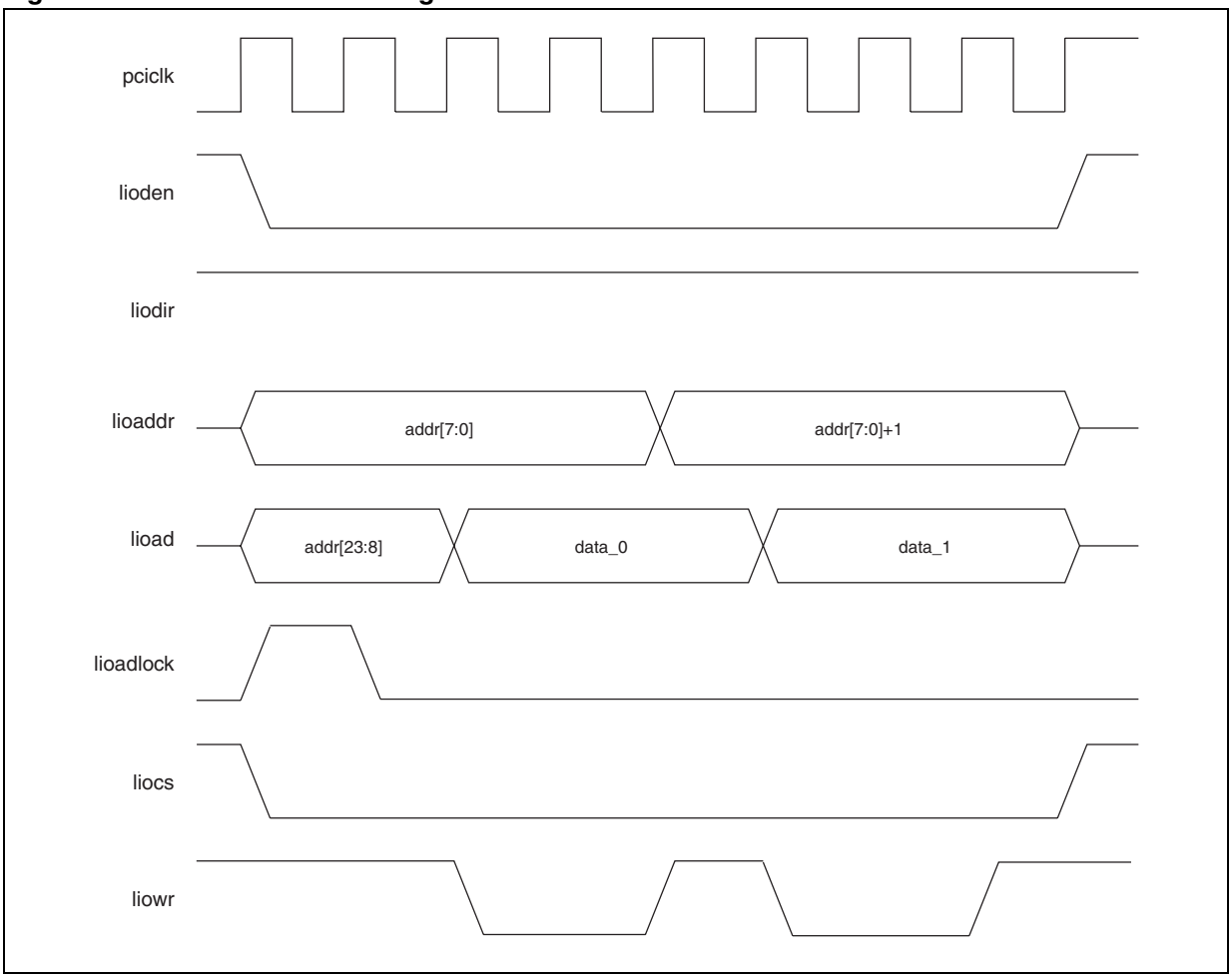


Figure 6. Local bus write timing



3.6 Interrupt handling

An interrupt controller is built into the STLS2F02 processor to handle internal and external interrupt. The 4 most significant bits of the interrupt INTn[5:0] in L2E are still used as interrupts in the STLS2F02, while the other two bits are used for new interrupts, such as PCI_IRQ and GPIO.

Interrupt between processors is handled as follows:

1. The interrupt initiator writes the dedicated interrupt register in the chipset.
2. Upon receiving the request for interrupt transmission, the chipset requests the target processor for an interrupt.
3. The processor handles the request in the same way as the previous L2E.

4 DDR2 SDRAM controller interface description

The STLS2F02 integrates a built-in memory controller compliant with DDR2 SDRAM standard (JESD79-2B). The STLS2F02 provides JESD79-2B-compliant read/write memory operations.

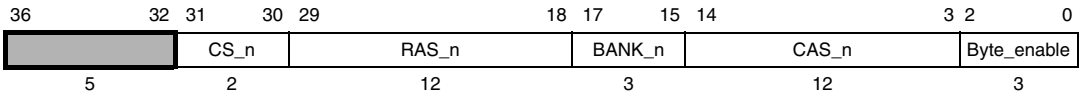
4.1 DDR2 SDRAM controller features

The STLS2F01 CPU supports up to 4 physical memories by using two DDR SDRAM chip select signals, with an 18-bit address bus (15-bit row/column address and 3-bit logic bank bus). The maximum address space is 128 Gbytes (2^{37} bytes).

This device supports all the JESD79-2B-compatible memory chips. The DDR2 controller parameters can be set to support specific memory chip type. The maximum number of chip selection (CS_n) is 2-bit. The maximum width of row address (RAS_n) is 15-bit, and the maximum width of column address (CAS_n) is 14-bit. And there is 3-bit logic bank bus (BANK_n).

For example, in the 4 Gbyte address space configuration of 2-bit CS_n, 3-bit BANK_n, 12-bit RAS_n and 12-bit CAS_n, the physical memory address CPU required can be translated into row/column address as shown in *Figure 7: DDR2 SDRAM row/column address translation*.

Figure 7. DDR2 SDRAM row/column address translation



The built-in memory controller IC receives only memory read/write requests from a processor or external device. The controller IC is in slave state whenever memory are read or written.

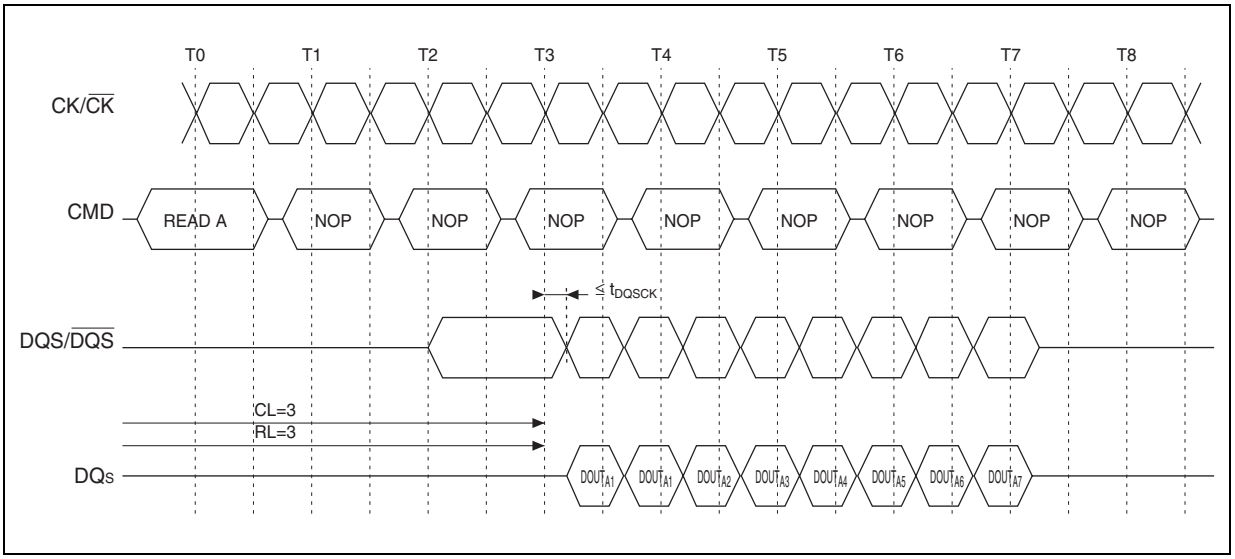
A dynamic page management policy is implemented on the integrated memory controller. For one access to memory, the controller selects open page/close page strategies on a hardware circuit, without software designers' intervention. The memory controller features:

- Full pipelining support to command and read/write data of interface
- Increasing bandwidth by merging and sorting memory command
- Modify fundamental parameters through the configuration of register read/write ports
- Built-in delay compensation circuit (DCC), it is used to send/receive data reliably
- 1-bit and 2-bit error detection, 1-bit error correction by error correcting-code (ECC)
- Frequency: 133 MHz to 333 MHz.

4.2 DDR2 SDRAM read protocol

As shown in *Figure 8* DDR2 SDRAM read protocol, the command (CMD) includes RAS_n, CAS_n and WE_n. When a read request happens, RAS_n=1,CAS_n=0,and WE_n=1.

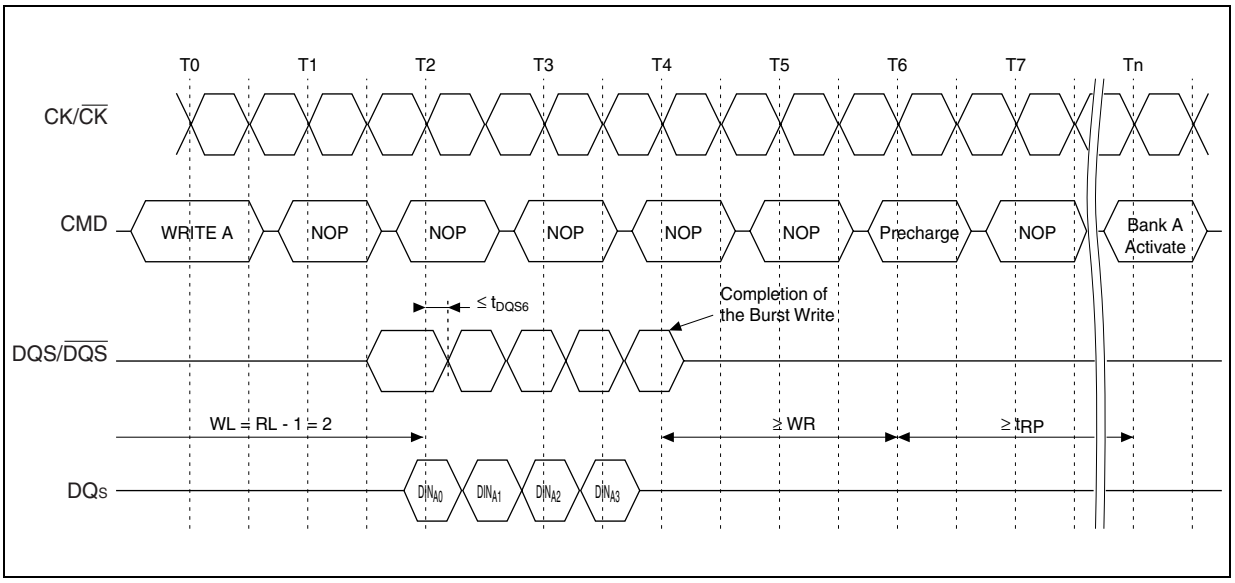
Figure 8. DDR2 SDRAM read protocol
CAS latency = 3, read latency = 3, burst length = 8



4.3 DDR2 SDRAM write protocol

As shown in *Figure 9* DDR2 SDRAM write protocol, the command (CMD) includes RAS_n, CAS_n and WE_n. When a write request happens, RAS_n=1, CAS_n=0,and WE_n=0. Unlike a read transaction, DQM is used to identify the write mask. In other words, the number of written bytes is needed. DQM is synchronous with DQS.

Figure 9. DDR2 SDRAM write protocol
CAS latency = 3, write latency = read latency = 2, burst length = 4



4.4 DDR2 SDRAM parameters

Since different DDR2 SDRAMs may be used in a system, DDR2 SDRAM needs configuration after power-on reset. The JESD79-2B standard defines the configuration operations and procedure in detail. DDR2 is not available before the memory is initialized. In STLS2F02-based systems, after the system motherboard is initialized, the DDR2 SDRAM controller must configure the memory type before the memory is used. The configuration parameters are written into the 29 64-bit registers corresponding to the physical address 0x0000 0000 0FFF FE00. In one register, single, multiple or partial parameter data can be included. The configuration register and its parameters are shown in *Table 12: DDR SDRAM configuration parameter register format*

Note: Unused bits are reserved.

4.4.1 Memory initialization sequence

The memory initialization sequence is as follows:

1. System reset, aresetn signal is set to 0, all register content is set to its initial value
2. System reset release, aresetn signal is set to 1
3. Issue 64-bit write command to configuration register, all 29 registers are configured. If register CTRL_03 is written in this step, the parameter of start should be set 0.
4. Issue 64-bit write command to register CTRL_03. Set the parameter of start to 1. The memory controller then sends the initial instruction to memory automatically.

4.4.2 Parameter descriptions

CONF_CTL_00 AP

The parameter determines whether the auto pre-charge function is enabled. If the function is enabled, memory closes the page after each write/read instruction. If mass continuous address operation happens, setting this parameter causes performance degradation.

CONF_CTL_00 CONCURRENTAP

This parameter determines whether the concurrent auto pre-charge function is enabled. Most SDRAM vendors do not support this feature.

CONF_CTL_03 SREFRESH

This parameter sets the self refresh style. It must be set to 0 when returning from self refresh.

CONF_CTL_07 CASLAT_LIN_GATE

This parameter controls the data sample of the memory controller when a read operation returns. In general, It is equal to or less than half period of ACALAT_LIN. The value of CASLAT_LIN is twice that of CAS.

CONF_CTL_15 DLL_INCREMENT

This parameter should not be set 0.

CONF_CTL_15 DLL_START_POINT

This parameter should not be set to 0 or 1 and should be less than 1.5 times the DLL_LOCK_VALUE.

CONF_CTL_28 UB_DIMM

This parameter should be set to 1, when unbuffered DIMM(s) are used. It should be set 0 when SDRAM(s) are used.

4.4.3 Parameter formats

Table 12. DDR SDRAM configuration parameter register format

Parameters	Bits	Default value	Range	Description
CONF_CTL_00[31:0] Offset: 0x00		**DDR2 667:0x00000101**		
AREFRESH	24:24	0x0	0x0-0x1	Initiate auto-refresh when specified by AUOT_REFRESH_MODE. WRITE-ONLY
AP	16:16	0x0	0x0-0x1	Enable auto pre-charge mode of controller
ADDR_CMP_EN	8:8	0x0	0x0-0x1	Enable address collision detection for command queue placement logic
ACTIVE_AGING	0:0	0x0	0x0-0x1	Enable command aging in the command queue, avoiding low priority command hungry
CONF_CTL_00[63:32] Offset: 0x00		**DDR2 667:0x01000100**		
DDR2_SDRAM_MODE	56:56	0x0	0x0-0x1	DDRI or DDRII mode
CONCURRENTAP	48:48	0x0	0x0-0x1	Allow controller to issue cmds to other banks while a bank is in auto pre-charge. Note: most DDR2 DIMM vendor do not support this feature
BANK_SPLIT_EN	40:40	0x0	0x0-0x1	Enable bank splitting for cmd queue placement logic
AUTO_REFRESH_MODE	32:32	0x0	0x0-0x1	Sets if auto-refresh occurs be at next burst or next cmd boundary
CONF_CTL_01[31:0] Offset: 0x10		**DDR2 667:0x00010000**		
ECC_DISBALE_W_UC_ERR	24:24	0x0	0x0-0x1	Disable auto-corruption of ECC when un-correctable errors occur in R/M/W operations.
DQS_N_EN	16:16	0x0	0x0-0x1	Single-ended or differential dqs pins.
DLL_BYPASS_MODE	8:8	0x0	0x0-0x1	Enable the DLL bypass feature of the controller.
DLLLOCKREG	0:0	0x0	0x0-0x1	Status of DLL lock coming out of master delay. READ-ONLY
CONF_CTL_01[63:32] Offset: 0x10		**DDR2 667:0x00100000**		
FWC	56:56	0x0	0x0-0x1	Force a write checks. Xor XOR_CHECK_BITS with ecc code and write to memory. WRITE_ONLY
FAST_WRITE	48:48	0x0	0x0-0x1	Sets when write cmds are issued to DRAM device.
ENABLE_QUICK_SREFRESH	40:40	0x0	0x0-0x1	Allows user to interrupt memory initialization to enter self-refresh mode.
EIGHT_BANK_MODE	32:32	0x0	0x0-0x1	Number of banks on the DRAM(s).

Table 12. DDR SDRAM configuration parameter register format (continued)

Parameters	Bits	Default value	Range	Description
CONF_CTL_02[31:0] Offset: 0x20		**DDR2 667:0x00000000**		
NO_CMD_INIT	24:24	0x0	0x0-0x1	Disable DRAM cmds until TDLL has expired during initialization.
INTRPTWRITENA	16:16	0x0	0x0-0x1	Allow the controller to interrupt a combined write cmd with auto pre-charge with another write cmd.
INTRPTREADA	8:8	0x0	0x0-0x1	Allow the controller to interrupt a combined read with auto pre-charge cmd with another read cmd.
INTRPTAPBURST	0:0	0x0	0x0-0x1	Allow the controller to interrupt an auto pre-charge cmd with another cmd.
CONF_CTL_02[63:32] Offset: 0x20		**DDR2 667:0x01000101**		
PRIORITY_EN	56:56	0x0	0x0-0x1	Enable priority for cmd queue placement logic.
POWER_DOWN	48:48	0x0	0x0-0x1	Disable clock enable and set DRAMs in power-down state.
PLACEMENT_EN	40:40	0x0	0x0-0x1	Enable placement logic for cmd queue.
ODT_ADD_TURN_CLK_EN	32:32	0x0	0x0-0x1	Enable extra turn-around clock between back-to-back reads/writes to different chip selects.
CONF_CTL_03[31:0] Offset: 0x30		**DDR2 667:0x01000000**		
RW_SAME_EN	24:24	0x0	0x0-0x1	Enable read/write grouping for cmd queue placement logic.
REG_DIMM_EN	16:16	0x0	0x0-0x1	Enable registered DIMM operation of the controller.
REDUC	8:8	0x0	0x0-0x1	Enable the half datapath (32-bit) feature of the controller.
PWRUP_SREFRESH_EXIT	0:0	0x0	0x0-0x1	Powerup via self-refresh instead of full memory initialization.
CONF_CTL_03[63:32] Offset: 0x30		**DDR2 667:0x01010000**		
SWAP_PORT_RW_SAME_EN	56:56	0x0	0x0-0x1	Enable command swapping logic between commands of the same type from the same port in execution unit.
SWAP_EN	48:48	0x0	0x0-0x1	Enable command swapping logic in execution unit.
START	40:40	0x0	0x0-0x1	Initiate cmd processing in the controller.
SREFRESH	32:32	0x0	0x0-0x1	Place DRAMs in self-refresh mode.
CONF_CTL_04[31:0] Offset: 0x40		**DDR2 667:0x00010101**		
WRITE_MODEREG	24:24	0x0	0x0-0x1	Write EMRS data to the DRAMs. WRITE-ONLY

Table 12. DDR SDRAM configuration parameter register format (continued)

Parameters	Bits	Default value	Range	Description
WRITEINTERP	16:16	0x0	0x0-0x1	Allow controller to interrupt write bursts to the DRAMs with a read cmd.
TREF_ENABLE	8:8	0x0	0x0-0x1	Issue self-refresh cmds to the DRAMs every TREF cycle.
TRAS_LOCKOUT	0:0	0x0	0x0-0x1	Allow the controller to execute auto pre-charge cmds before TRAS_MIN expires.
CONF_CTL_04[63:32] Offset: 0x40			**DDR2 667:0x01000202**	
RTT_0	57:56	0x0	0x0-0x3	On-Die termination resistance setting for all DRAM devices.
CTRL_RAW	49:48	0x0	0x0-0x3	ECC error checking and correcting control. 2'b00 – no ECC 2'b01 – report error only, not corrected 2'b10 – no ECC device used 2'b11 – report and correct ECC error
AXI0_W_PRIORITY	41:40	0x0	0x0-0x3	Priority of write cmds from port 0.
AXI0_R_PRIORITY	33:32	0x0	0x0-0x3	Priority of read cmds from port 0.
CONF_CTL_05[31:0] Offset: 0x50			**DDR2 667:0x04050202**	
COLUMN_SIZE	26:24	0x0	0x0-0x7	Difference between number of column pins available and number being used.
CASLAT	18:16	0x0	0x0-0x7	Encoded CAS latency sent to DRAMs during initialization.
ADDR_PINS	10:8	0x0	0x0-0x7	Difference between number of addr pins available and number being used.
RTT_PAD_TERMINATION	1:0	0x0	0x0-0x3	Set termination resistance in controller pads.
CONF_CTL_05[63:32] Offset: 0x50			**DDR2 667:0x00000000**	
Q_FULLNESS	58:56	0x0	0x0-0x7	Quantity that determines cmd queue full.
PORT_DATA				
_ERROR_TYPE	50:48	0x0	0x0-0x7	Type of error and access type that caused the PORT data error. READ-ONLY bit 0 – Data Overflow. The wirte data quantity exceeded the Maximum_Byte_Request configured option. bit 1 – Write data interleaved beyond supported interleaving depth. bit 2 – ECC 2-bit error.

Table 12. DDR SDRAM configuration parameter register format (continued)

Parameters	Bits	Default value	Range	Description
OUT_OF_RANGE_TYPE	42:40	0x0	0x0-0x7	Type of cmd that caused and Out-of-Range interrupt. READ-ONLY
MAX_CS_REG	34:32	0x4	0x0-0x4	Maximum number of chip selects available. READ-ONLY
CONF_CTL_06[31:0] Offset: 0x60		**DDR2 667:0x03040203**		
TRTP	26:24	0x0	0x0-0x7	DRAM TRTP parameter in cycles.
TRRD	18:16	0x0	0x0-0x7	DRAM TRRD parameter in cycles.
TEMRS	10:8	0x0	0x0-0x7	DRAM TEMRS parameter in cycles.
TCKE	2:0	0x0	0x0-0x7	Minimum CKE pulse width.
CONF_CTL_06[63:32] Offset: 0x60		**DDR2 667:0x0a040305**		
APREBIT	59:56	0x0	0x0-0xF	Location of the auto pre-charge bit in the DRAM address.
WRLAT	50:48	0x0	0x0-0x7	DRAM WRLAT parameter in cycles.
TWTR	42:40	0x0	0x0-0x7	DRAM TWTR parameter in cycles.
TWR_INT	34:32	0x0	0x0-0x7	DRAM TWR parameter in cycles.
CONF_CTL_07[31:0] Offset: 0x70		**DDR2 667:0x000F090A**		
ECC_C_ID	27:24	0x0	0x0-0xF	Source ID associated with correctable ECC event. READ-ONLY
CS_MAP	19:16	0x0	0x0-0xF	Number of active chip selects used in address decoding.
CASLAT_LIN_GATE	11:8	0x0	0x0-0xF	Adjusts data capture gate open by half cycles.
CASLAT_LIN	3:0	0x0	0x0-0xF	Sets latency from read cmd send to data receive from/to controller.
CONF_CTL_07[63:32] Offset: 0x70		**DDR2 667:0x00000400**		
MAX_ROW_REG	59:56	0xF	0x0-0xF	Maximum width of memory address bus. READ-ONLY
MAX_COL_REG	51:48	0xE	0x0-0xe	Maximum width of column address in DRAMs. READ-ONLY
INITAREF	43:40	0x0	0x0-0xF	Number of auto-refresh cmds to execute during DRAM initialization.
ECC_U_ID	35:32	0x0	0x0-0xF	Source ID associated with the uncorrectable ECC even. READ-ONLY
CONF_CTL_08[31:0] Offset: 0x80		**DDR2 667:0x01020408**		
ODT_RD_MAP_CS3	27:24	0x0	0x0-0xF	ODT chip select 3 map for reads. Determines which chip(s) have termination when a read occurs on chip 3.

Table 12. DDR SDRAM configuration parameter register format (continued)

Parameters	Bits	Default value	Range	Description
ODT_RD_MAP_CS2	19:16	0x0	0x0-0xF	ODT chip select 2 map for reads. Determines which chip(s) have termination when a read occurs on chip 2.
ODT_RD_MAP_CS1	11:8	0x0	0x0-0xF	ODT chip select 1 map for reads. Determines which chip(s) have termination when a read occurs on chip 1.
ODT_RD_MAP_CS0	3:0	0x0	0x0-0xF	ODT chip select 0 map for reads. Determines which chip(s) have termination when a read occurs on chip 0.
CONF_CTL_08[63:32] Offset: 0x80 DDR2 667:0x01020408				
ODT_WR_MAP_CS3	59:56	0x0	0x0-0xF	ODT chip select 3 map for writes. Determines which chip(s) have termination when a write occurs on chip 3.
ODT_WR_MAP_CS2	51:48	0x0	0x0-0xF	ODT chip select 2 map for writes. Determines which chip(s) have termination when a write occurs on chip 2.
ODT_WR_MAP_CS1	43:40	0x0	0x0-0xF	ODT chip select 1 map for writes. Determines which chip(s) have termination when a write occurs on chip 1.
ODT_WR_MAP_CS0	35:32	0x0	0x0-0xF	ODT chip select 0 map for writes. Determines which chip(s) have termination when a write occurs on chip 0.
CONF_CTL_09[31:0] Offset: 0x90 DDR2 667:0x00000000				
PORT_DATA_ERROR_ID	27:24	0x0	0x0-0xF	Port number of cmd that caused the PORT data error. READ-ONLY
PORT_CMD_ERROR_TYPE	19:16	0x0	0x0-0xF	Type of error and access type that caused the PORT cmd error. READ-ONLY)
PORT_CMD_ERROR_ID	11:8	0x0	0x0-0xF	Port number of cmd that caused the PORT cmd error. READ-ONLY
OUT_OF_RANGE_SOURCE_ID	3:0	0x0	0x0-0xF	Source ID of cmd that caused an Out-of-Range interrupt. READ-ONLY
CONF_CTL_09[63:32] Offset: 0x90 DDR2 667:0x0000050b				
OCD_ADJUST_PUP_CS0	60:56	0x0	0x0-0x1F	OCD pull-up adjust setting for DRAMs for chip select 0.
OCD_ADJUST_PDN_CS0	52:48	0x0	0x0-0x1F	OCD pull-down adjust setting for DRAMs for chip select 0.

Table 12. DDR SDRAM configuration parameter register format (continued)

Parameters	Bits	Default value	Range	Description
TRP	43:40	0x0	0x0-0xF	DRAM TRP parameter in cycles.
TDAL	35:32	0x0	0x0-0xF	DRAM TDAL parameter in cycles.
CONF_CTL_10[31:0] Offset: 0xA0			**DDR2 667:0x3F130200**	
AGE_COUNT	29:24	0x0	0x0-0x3F	Initial value of master aging-rate counter for cmd aging.
TRC	20:16	0x0	0x0-0x1F	DRAM TRC parameter in cycles.
TMRD	12:8	0x0	0x0-0x1F	DRAM TMRD parameter in cycles.
TFAW	4:0	0x0	0x0-0x1F	DRAM TFAW parameter in cycles.
CONF_CTL_10[63:32] Offset: 0xA0			**DDR2 667:0x1D1D1D3F**	
DLL_DQS_DELAY_2	62:56	0x0	0x0-0x7F	Fraction of a cycle to delay the dqs signal from the DRAMs for dll_rd_dqs_slice 2 during reads.
DLL_DQS_DELAY_1	54:48	0x0	0x0-0x7F	Fraction of a cycle to delay the dqs signal from the DRAMs for dll_rd_dqs_slice 1 during reads.
DLL_DQS_DELAY_0	46:40	0x0	0x0-0x7F	Fraction of a cycle to delay the dqs signal from the DRAMs for dll_rd_dqs_slice 0 during reads.
COMMAND_AGE_COUNT	37:32	0x0	0x0-0x3F	Initial value of individual cmd aging counters for cmd aging.
CONF_CTL_11[31:0] Offset: 0xB0			**DDR2 667:0x1D1D1D1D**	
DLL_DQS_DELAY_6	30:24	0x0	0x0-0x7F	Fraction of a cycle to delay the dqs signal from the DRAMs for dll_rd_dqs_slice 6 during reads.
DLL_DQS_DELAY_5	22:16	0x0	0x0-0x7F	Fraction of a cycle to delay the dqs signal from the DRAMs for dll_rd_dqs_slice 5 during reads.
DLL_DQS_DELAY_4	14:8	0x0	0x0-0x7F	Fraction of a cycle to delay the dqs signal from the DRAMs for dll_rd_dqs_slice 4 during reads.
DLL_DQS_DELAY_3	6:0	0x0	0x0-0x7F	Fraction of a cycle to delay the dqs signal from the DRAMs for dll_rd_dqs_slice 3 during reads.
CONF_CTL_11[63:32] Offset: 0xB0			**DDR2 667:0x507F1D1D**	
WR_DQS_SHIFT	62:56	0x0	0x0-0x7F	Fraction of a cycle to delay the clk_wr signal in the controller.
DQS_OUT_SHIFT	54:48	0x0	0x0-0x7F	Fraction of a cycle to delay the write dqs signal to the DRAMs during writes.
DLL_DQS_DELAY_8	46:40	0x0	0x0-0x7F	Fraction of a cycle to delay the dqs signal from the DRAMs for dll_rd_dqs_slice 8 during reads.

Table 12. DDR SDRAM configuration parameter register format (continued)

Parameters	Bits	Default value	Range	Description
DLL_DQS_DELAY_7	38:32	0x0	0x0-0x7F	Fraction of a cycle to delay the dqs signal from the DRAMs for dll_rd_dqs_slice 7 during reads.
CONF_CTL_12[31:0] Offset: 0xC0 DDR2 667:0x0E000000				
TRAS_MIN	31:24	0x0	0x0-0xFF	DRAM TRAS_MIN parameter in cycles.
OUT_OF_RANGE_LENGTH	23:16	0x0	0x0-0xFF	Length f cmd that caused an Out-of-Range interrupt. READ-ONLY
ECC_U_SYND	15:8	0x0	0x0-0xFF	Syndrome for uncorrectable ECC event. READ-ONLY
ECC_C_SYND	7:0	0x0	0x0-0xFF	Syndrome for correctable ECC event. READ-ONLY
CONF_CTL_12[63:32] Offset: 0xC0 DDR2 667:0x002A3305				
DLL_DQS_DELAY_BYPASS_0	56:48	0x0	0x0-0x1FF	Number of delay elements to include in the dqs signal from the DRAMs for dll_rd_dqs_slice 0 during reads when DLL is being bypassed.
TRFC	47:40	0x0	0x0-0xFF	DRAM TRFC parameter in cycles.
TRCD_INT	39:32	0x0	0x0-0xFF	DRAM TRCD parameter in cycles.
CONF_CTL_13[31:0] Offset: 0xD0 DDR2 667:0x002A002A				
DLL_DQS_DELAY_BYPASS_2	24:16	0x0	0x0-0x1	Number of delay elements to include in the dqs signal from the DRAMs for dll_rd_dqs_slice 2 during reads when DLL is being bypassed.
DLL_DQS_DELAY_BYPASS_1	8:0	0x0	0x0-0x1	Number of delay elements to include in the dqs signal from the DRAMs for dll_rd_dqs_slice 1 during reads when DLL is being bypassed.
CONF_CTL_13[63:32] Offset: 0xD0 DDR2 667:0x002A002A				
DLL_DQS_DELAY_BYPASS_4	56:48	0x0	0x0-0x1FF	Number of delay elements to include in the dqs signal from the DRAMs for dll_rd_dqs_slice 4 during reads when DLL is being bypassed.
DLL_DQS_DELAY_BYPASS_3	40:32	0x0	0x0-0x1FF	Number of delay elements to include in the dqs signal from the DRAMs for dll_rd_dqs_slice 3 during reads when DLL is being bypassed.
CONF_CTL_14[31:0] Offset: 0xE0 DDR2 667:0x002A002A				
DLL_DQS_DELAY_BYPASS_6	24:16	0x0	0x0-0x1FF	Number of delay elements to include in the dqs signal from the DRAMs for dll_rd_dqs_slice 6 during reads when DLL is being bypassed.

Table 12. DDR SDRAM configuration parameter register format (continued)

Parameters	Bits	Default value	Range	Description
DLL_DQS_DELAY_BYPASS_5	8:0	0x0	0x0-0x1FF	Number of delay elements to include in the dqs signal from the DRAMs for dll_rd_dqs_slice 7 during reads when DLL is being bypassed.
CONF_CTL_14[63:32] Offset: 0xE0 DDR2 667:0x002A002A				
DLL_DQS_DELAY_BYPASS_8	56:48	0x0	0x0-0x1FF	Number of delay elements to include in the dqs signal from the DRAMs for dll_rd_dqs_slice 8 during reads when DLL is being bypassed.
DLL_DQS_DELAY_BYPASS_7	40:32	0x0	0x0-0x1FF	Number of delay elements to include in the dqs signal from the DRAMs for dll_rd_dqs_slice 7 during reads when DLL is being bypassed.
CONF_CTL_15[31:0] Offset: 0xF0 DDR2 667:0x00000004				
DLL_LOCK	24:16	0x0	0x0-0x1FF	Number of delay elements in master DLL lock. READ-ONLY
DLL_INCREMENT	8:0	0x0	0x0-0x1FF	Number of elements to add to DLL_START_POINT when searching for lock.
CONF_CTL_15[63:32] Offset: 0xF0 DDR2 667:0x00B4000A				
DQS_OUT_SHIFT_BYPASS	56:48	0x0	0x0-0x1FF	Number of delay elements to include in the write dqs signal to the DRAMs during writes when DLL is being bypassed.
DLL_START_POINT	40:32	0x0	0x0-0x1FF	Initial delay count when searching for lock in master DLL.
CONF_CTL_16[31:0] Offset: 0x100 DDR2 667:0x00000087				
INT_ACK	25:16	0x0	0x0-0x3FF	Clear mask of the INT_STATUS parameter. WRITE-ONLY
WR_DQS_SHIFT_BYPASS	8:0	0x0	0x0-0x1FF	Number of delay elements to include in the clk_wr signal in the controller when DLL is being bypassed.
CONF_CTL_16[63:32] Offset: 0x100 DDR2 667:0x00000000				
INT_STATUS	58:48	0x0	0x0-0x7FF	Status of interrupt features in the controller. READ-ONLY
INT_MASK	42:32	0x0	0x0-0x7FF	Mask for controller_int signals from the INT_STATUS parameter.
CONF_CTL_17[31:0] Offset: 0x110 DDR2 667:0X0000181B				
EMRS1_DATA	30:16	0x0	0x0-0x7FF	EMRS1 data.
TREF	13:0	0x0	0x0-0x3FF	DRAM TREF parameter in cycles.
CONF_CTL_17[63:32] Offset: 0x110 DDR2 667:0x00000000				

Table 12. DDR SDRAM configuration parameter register format (continued)

Parameters	Bits	Default value	Range	Description
EMRS2_DATA_1	62:48	0x0000	0x0-0x7FFF	EMRS2 data for chip select 1.
EMRS2_DATA_0	46:32	0x0000	0x0-0x7FFF	EMRS2 data for chip select 0.
CONF_CTL_18[31:0] Offset: 0x120 DDR2 667:0x00000000				
EMRS2_DATA_3	30:16	0x0000	0x0-0x7FFF	EMRS2 data for chip select 3.
EMRS2_DATA_2	14:0	0x0000	0x0-0x7FFF	EMRS2 data for chip select 2.
CONF_CTL_18[63:32] Offset: 0x120 DDR2 667:0x001C0000				
AXI0_EN_SIZE_LT_WIDTH_INSTR	63:48	0x0000	0x0-0xFFFF	Allow narrow instructions from port 0 requestors with bit enabled.
EMRS3_DATA	46:32	0x0000	0x0-0x7FFF	EMRS3 data.
CONF_CTL_19[31:0] Offset: 0x130 DDR2 667:0x00C8006B				
TDLL	31:16	0x0000	0x0-0xFFFF	DRAM TDLL parameter in cycles.
TCPD	15:0	0x0000	0x0-0xFFFF	DRAM TCPD parameter in cycles.
CONF_CTL_19[63:32] Offset: 0x130 DDR2 667:0x48E10002				
TRAS_MAX	63:48	0x0000	0x0-0xFFFF	DRAM TRAS_MAX parameter in cycles.
TPDEX	47:32	0x0000	0x0-0xFFFF	DRAM TPDEX parameter in cycles.
CONF_CTL_20[31:0] Offset: 0x140 DDR2 667:0x00C8002F				
TXSR	31:16	0x0000	0x0-0xFFFF	DRAM TXSR parameter in cycles.
TXSNR	15:0	0x0000	0x0-0xFFFF	DRAM TXSNR parameter in cycles.
CONF_CTL_20[63:32] Offset: 0x140 DDR2 667:0x00000000				
XOR_CHECK_BITS	63:48	0x0000	0x0-0xFFFF	Value to Xor with generated ECC codes for forced write check.
VERSION	47:32	0x2041	0x2041	Controller version number. READ-ONLY

Table 12. DDR SDRAM configuration parameter register format (continued)

Parameters	Bits	Default value	Range	Description
CONF_CTL_21[31:0] Offset: 0x150 DDR2 667:0x00000036				
ECC_C_ADDR[7:0]	31:24	0x0000	0x0-0x1FFFFFFFF	Address of correctable ECC event. READ-ONLY
TINIT	23:0	0x0000	0x0-0xFFFFF	DRAM TINIT parameter in cycles.
CONF_CTL_21[63:32] Offset: 0x150 DDR2 667:0x00000000				
ECC_C_ADDR[36:8]	60:32	0x0	0x0-0x1FFFFFFFF	Address of correctable ECC event. READ-ONLY
CONF_CTL_22[31:0] Offset: 0x160 DDR2 667:0x00000000				
ECC_U_ADDR[31:0]	31:0	0x0	0x0-0x1FFFFFFFF	Address of uncorrectable ECC event. READ-ONLY
CONF_CTL_22[63:32] Offset: 0x160 DDR2 667:0x00000000				
ECC_U_ADDR[36:32]	36:32	0x0	0x0-0x1FFFFFFFF	Address of uncorrectable ECC event. rEAD-ONLY
CONF_CTL_23[31:0] Offset: 0x170 DDR2 667:0x00000000				
OUT_OF_RANGE_ADDR[31:0]	31:0	0x0	0x0-0x1FFFFFFFF	Address of cmd that caused an Out-of-Range interrupt. READ-ONLY
CONF_CTL_23[63:32] Offset: 0x170 DDR2 667:0x00000000				
OUT_OF_RANGE_ADDR[36:32]	36:32	0x0	0x0-0x1FFFFFFFF	Address of cmd that caused an Out-of-Range interrupt. READE-ONLY
CONF_CTL_24[31:0] Offset: 0x180 DDR2 667:0x00000000				
PORT_CMD_ERROR_ADDR[31:0]	31:0	0x0	0x0-0x1FFFFFFFF	Address of port that caused the PORT cmd error. READ-ONLY
CONF_CTL_24[63:32] Offset: 0x180 DDR2 667:0x00000000				
PORT_CMD_ERROR_ADDR[36:32]	36:32	0x0	0x0-0x1FFFFFFFF	Address of port that caused the PORT cmd error. READ-ONLY
CONF_CTL_25[31:0] Offset: 0x190 DDR2 667:0x00000000				
ECC_C_DATA[31:0]	31:0	0x0	0x0-0x1FFFFFFFF	Data associated with correctable ECC event. READ-ONLY
CONF_CTL_25[63:32] Offset: 0x190 DDR2 667:0x00000000				
ECC_C_DATA[63:32]	63:32	0x0	0x0-0x1FFFFFFFF	Data associated with correctable ECC event. READ-ONLY
CONF_CTL_26[31:0] Offset: 0x1A0 DDR2 667:0x00000000				
ECC_U_DATA[31:0]	31:0	0x0	0x0-0x1FFFFFFFF	Data associated with uncorrectable ECC event. READ-ONLY
CONF_CTL_26[63:32] Offset: 0x1A0 DDR2 667:0x00000000				
ECC_U_DATA[63:32]	63:32	0x0	0x0-0x1FFFFFFFF	Data associated with uncorrectable ECC event. READ-ONLY

Table 12. DDR SDRAM configuration parameter register format (continued)

Parameters	Bits	Default value	Range	Description
CONF_CTL_27[63:32] Offset: 0x1B0 DDR2 667:0x00000000				
CKE_DELAY	2:0	0x0	0x0-0x7	Additional cycles to delay CKE for status reporting
CONF_CTL_28[63:32] Offset: 0x1C0 DDR2 667:0x00000001				
UB_DIMM	0:0	0x0	0x0-0x1	Enable unbuffered DIMM

4.5 DDR2 SDRAM sample mode configuration

A DDR2 SDRAM controller is integrated in the STLS2F02. A delay compensation circuit (using a DLL) samples return data on DQS. Since there is a data return path delay between the memory controller and the SDRAM module, it is necessary to introduce a set of control signals to measure the delay.

The control signals of DDR2_GATE_I[3:0] and DDR2_GATE_O[3:0] are used for the delay measurement. On the PCB the signals DDR2_GATE_I and DDR2_GAT_O are connected together to imitate the wiring delay on the PCB. The sampling accuracy is thus guaranteed.

5 Initialization process

The initialization of STLS2F02 is divided into core and interface parts.

When the STLS2F02 PCI interface is configured as main bridge, interface initialization is finished internally and PCI_RESETn is output signal. When the processor works as a PCI/PCIX device, PCI_RESETn acts as an input to reset the STLS2F02 PCI interface.

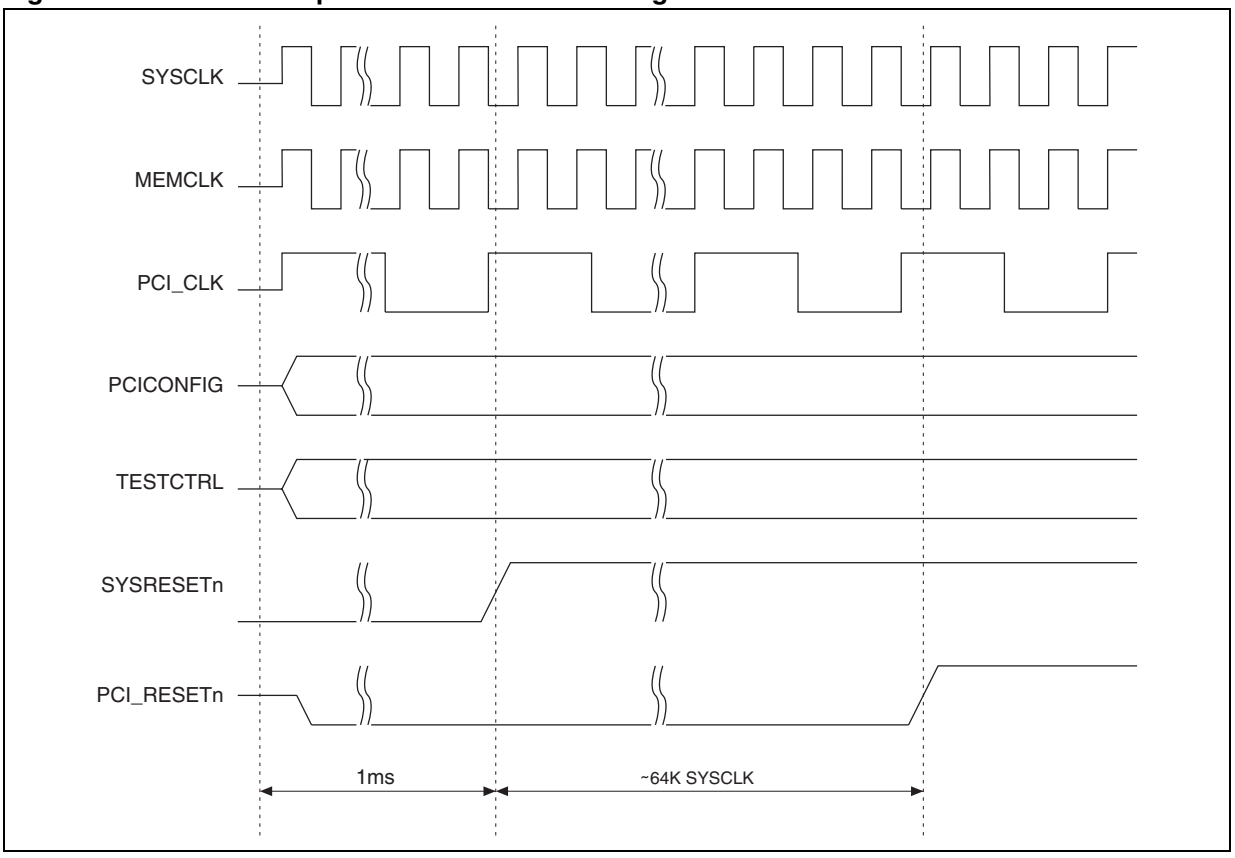
When the processor reset signal SYSRESETn is low, the related clock, test, and initial signals must be valid.

- SYSCLK, MEMCLK, CLKSEL and PCI_CLK must be stable
- Initial signal PCI_CONFIG should set to the appropriate value
- TEST_CTRL[7:0] are all high

When SYSRESETn is invalid, the processor internal reset logic begins to work to initialize the chip. The SYSRESETn signal should be valid for at least one clock cycle to ensure that it is sampled by the reset logic.

The work mode of the PCI bus is determined by the main bridge during the reset period. The PCI_RESETn output generated by the processor when it works as the main bridge is used to ensure that all devices working at the same mode. When not in main bridge mode, the PCI_RESETn input receives the bus configuration.

Figure 10. Initialization process when in main bridge mode



6 Electrical characteristics

6.1 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 13* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended period may affect device reliability.

Table 13. Absolute maximum rating

Parameter	Description	Min	Max	Unit
Vdd	CPU core voltage	-0.3	1.32	V
Vdde1v8	DDR2 voltage	-0.3	2.0	V
Vdde3v3	IO voltage	-0.3	4.0	V
DDR2_VREF	DDR2 voltage reference	-0.3	2.0	V
Pll_vdd_1	1.0 V PLL1 digital voltage	-0.3	1.32	V
Pll_vdd_0	1.0 V PLL0 digital voltage	-0.3	1.32	V
Pllio_vdde1v8	1.8 V PLL IO voltage	-0.3	2.0	V
Pll_vdde1v8_1	1.8 V PLL1 analog voltage	-0.3	2.0	V
Pll_vdde1v8_0	1.8 V PLL0 analog voltage	-0.3	2.0	V
Pllio_vdd	1.2 V PLL IO voltage	-0.3	1.32	V
T_S	Storage temperature	-55	150	°C
ESD	ESD susceptibility (CDM)		350	V

6.2 Recommended operation environment

Table 14. Recommended operating temperature, voltage and frequency

Parameter	Description	Min	Typ	Max	Unit
T_A	Ambient temperature	-40		85	°C
Vdd	CPU core voltage	1.20	1.26	1.32	V
Vdde1v8	DDR2 voltage	1.7	1.8	1.9	V
Vdde3v3	IO voltage	3.0	3.3	3.6	V
DDR2_VREF	DDR2 voltage reference	0.83	0.9	0.97	V
Pll_vdd_1	1.0 V PLL1 digital voltage	1.08	1.2	1.26	V
Pll_vdd_0	1.0 V PLL0 digital voltage	1.08	1.2	1.26	V
Pllio_vdde1v8	1.8 V PLL IO voltage	1.7	1.8	1.9	V
Pll_vdde1v8_1	1.8 V PLL1 analog voltage	1.7	1.8	1.9	V
Pll_vdde1v8_0	1.8 V PLL0 analog voltage	1.7	1.8	1.9	V

Table 14. Recommended operating temperature, voltage and frequency (continued)

Parameter	Description	Min	Typ	Max	Unit
Pllio_vdd	1.2 V PLL IO voltage	1.08	1.2	1.26	V
TJ	Junction temperature	-40		125	°C

6.3 DC parameters

Table 15. DC parameters

Parameter	Description	Min	Typ	Max	Unit	Note
V_{IH}	Input high level voltage	2			V	(1)
V_{IL}	input low level voltage			0.8	V	(1)
V_{OH}	output high level voltage	vdde3v3-0.3			V	(2)
V_{OL}	output low level voltage			0.3	V	(2)
I_{IH}	input high level leakage current	0.002		0.4	µA	(3)
I_{IL}	input low level leakage current	-67.3		-65	µA	(3)
I_{OL}	output low level current		8		mA	(4)
I_{OH}	output high level current		8		mA	(4)
C_{IN}	Input pin capacitor	4.4	7	7.5	pF	
C_{OUT}	Output pin capacitor	23	25	27	pF	
R_{PH}	Pull-up resistance	32	50	81	KΩ	(5)

1. Input pin level (including tri-state pin).
2. Individual output pin (including output state tri-state pin) level.
3. For tri-state input pin (excluding input).
4. Individual output pin (including output state tri-state pin) driving capability.
5. For input pin (excluding tri-state pin).

Table 16. DC parameters (JTAG)

Parameter	Description	Min	Typ	Max	Unit	Note
C_{TIN}	Test input capacitance	4.4	7	7.5	pF	(1)
C_{TOUT}	Test output capacitance	23	25	27	pF	(2)
C_{TCK}	TCK capacitance	4.4	7	7.5	pF	

1. For TDI, TMS and TRST in JTAG.
2. For TDO in JTAG.

6.4 AC parameters

Table 17. Clock parameters

(Test conditions:SYSCLK=100 MHz, PCICLK=133 MHz, MEMCLK=333 MHz, CoreClk=1000 MHz)

Parameter	Min	Typ	Max	Unit
SYSCLK high level time	2	5	8	ns
SYSCLK low level time	2		8	ns
SYSCLK rising time	1		1	ns
SYSCLK falling time	1		1	ns
SYSCLK cycle variation			±300	ps
PCI_CLK high level time	3			ns
PCI_CLK low level time	3			ns
PCI_CLK rising slew	1.5			V/ns
PCI_CLK falling slew	1.5			V/ns
PCI_CLK cycle variation			±500	ps
MEMCLK high level time	1.41		1.59	ns
MEMCLK low level time	1.41		1.59	ns
MEMCLK rising slew	1			V/ns
MEMCLK falling slew	1			V/ns
MEMCLK cycle variation			±225	ps
DQS high level time	1.35		1.65	ns
DQS low level time	1.35		1.65	ns
DQS rising slew	1			V/ns
DQS falling slew	1			V/ns
DQS cycle variation			±225	ps

Table 18. Input setup and hold time

(Test conditions:SYSCLK=100 MHz, PCICLK=133 MHz, MEMCLK=333 MHz, CoreClk=1000 MHz)

Parameter	Min	Typ	Max	Unit
PCI_* signals setup time	1.2			ns
PCI_* signals hold time	0.5			ns
LIO_* signals setup time	1.2			ns
LIO_* signals hold time	0.5			ns
DDR2_DQ*/CB* signals setup time	0.1			ns
DDR2_DQ*/CB* signals hold time	0.175			ns

Table 19. Input setup and hold time

(Test conditions:SYSCLK=100 MHz, PCICLK=66 MHz, CoreClk=1000 MHz)

Parameter	Min	Typ	Max	Unit
PCI_* signals setup time	3.0			ns
PCI_* signals hold time	0.0			ns
LIO_* signals setup time	3.0			ns
LIO_* signals hold time	0.0			ns

Table 20. Output delay time

(Test conditions:SYSCLK=100 MHz, PCICLK=133 MHz, CoreClk=1000 MHz)

Parameter	Min	Typ	Max	Unit
PCI_* signals effective delay	0.7		3.8	ns
LIO_* signals effective delay	1.5		6.0	ns
DDDR2_A*/RAS*/CAS*/WE*/CS*/CKE*/ODT* signals effective delay		1.5		ns
DDR2_DQ*/DQM* effective delay		0.75		ns

Table 21. JTAG parameters

(Test condition:TCK=100 MHz)

Parameter	Min	Typ	Max	Unit
TCK high level time	2	5	8	ns
TCK low level time	2		8	ns
TCK rising time	1		1	ns
TCK falling time	1		1	ns
TRST pulse width	10			ns
TDI,TMS setup time	3.5		4.4	ns
TDI,TMS hold time	2.5		5.5	ns
TDO output effective delay			1.28	ns
TDO output disable delay			1.28	ns

7 Thermal characteristics

7.1 Thermal resistivity

Heat spreader optimized with the following assumptions

- Ambient temperature 40 °C
- Package assembled on PCB as per JEDEC EIA/JESD51-9
- Maximum power 7.45 W

Customer should implement power extraction from the top of the package so that package case to ambient R_{th} is below 16 °C/W.

Without air flow, this can be achieved with a 40x40x15 heat spreader or 27x27x25 HS or 35x35x18 HS. This should guarantee 120 °C max junction temperature (low margin).

The preferred configuration is to use a 27x27x10 HS with 0.5m/sec. air flow. A single fan in PC case should be enough. In such case, max Junction temp should be around 112 °C.

7.2 Reflow temperature to time curve

TheSTLS2F02 processor uses a flip chip eutectic packaging technology. It can endure maximum reflow temperature ranging from 235 °C to 245 °C. The reflow temperature curve and parameters are shown in *Figure 11* and *Table 22*.

Figure 11. Reflow temperature to time curve

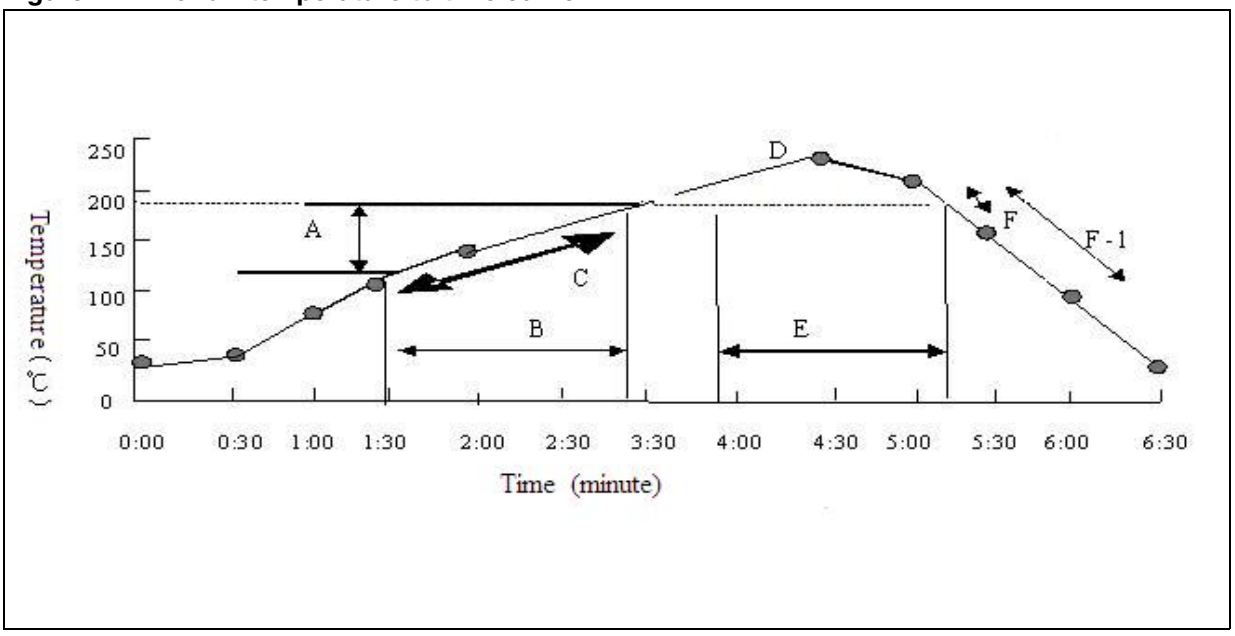


Table 22. Reflow temperature parameters

Parameter	Reference value
A	120 ~ 180 °C
B	90 ~ 120 seconds
C	0.3 ~ 2.0 °C/second
D	235 ~ 245 °C
E	85 ~ 105 seconds
F	< 1.2 °C/second
F-1	< 1.0 °C/second

8 Pin arrangement and package information

8.1 Pin arrangement

The STLS2F02 processor is packaged in HSFCBGA452. The pin arrangement is shown in *Figure 12: Pin arrangement (left-hand side)*, and *Figure 14: Pin arrangement (right-hand side)*,

Figure 12. Pin arrangement (left-hand side)

	1	2	3	4	5	6	7	8	9
A	gnde	vdd	TEST_CTRL7	LIO_AD01	LIO_AD04	LIO_AD12	LIO_A3	LIO_A5	LIO_A7
B	vdd	gnde	TEST_CTRL5	TEST_CTRL6	LIO_AD05	LIO_AD08	LIO_A1	LIO_A4	sysclk
C	vdd	TEST_CTRL3	gnde	memclk	SYSRESETN	LIO_AD06	LIO_AD14	LIO_A0	testclk
D	TEST_CTRL0	TEST_CTRL1	TEST_CTRL2	gnde	pllclock1	LIO_AD02	LIO_AD10	LIO_AD09	pllclock0
E	pll_vdd_1	gpio0	gpio2	gpio3					
F	pllio_vdde1v8	pll_gnd_1	pll_vdde1v8_1	pll_gnde_1					
G	gpio1	pllio_gnd	pllio_vdd	pllio_gnde					
H	vdd	pll_gnde_0	gnde	gnde					9
J	vdd	gnde	pll_gnd_0	pll_vdde1v8_0				J	gnde
K	CLKSEL7	pll_vdd_0	gnde	gnde				K	gnde
L	CLKSEL6	CLKSEL5	CLKSEL8	CLKSEL9				L	vdd
M	CLKSEL3	CLKSEL4	CLKSEL0	CLKSEL2				M	vdd
N	vdd	CLKSEL1	PCI_CONFIG7	PCI_CONFIG6				N	vdd
P	vdd	PCI_CONFIG5	PCI_CONFIG4	vdde3v3				P	vdd
R	PCI_CONFIG3	PCI_CONFIG0	PCI_CONFIG1	vdde3v3				R	vdd
T	PCI_CONFIG2	PCI_IDSEL	PCI_AD00	PCI_AD02				T	vdd
U	PCI_AD01	PCI_AD03	PCI_AD05	PCI_AD04				U	gnde
V	PCI_CBEn0	PCI_AD06	PCI_AD07	PCI_AD08				V	gnde
W	PCI_AD10	PCI_AD09	PCI_AD12	PCI_AD14					9
Y	GND	PCI_AD11	PCI_AD13	PCI_CBEn1					
AA	PCI_AD15	PCI_PAR	PCI_SERR	PCI_FRAMEn					
AB	PCI_PERR	PCI_STOPn	PCI_IRDYn	VDD					
AC	PCI_TRDYn	PCI_DEVSELn	vdd	gnde	PCI_AD19	PCI_AD22	PCI_AD28	PCI_AD30	PCI_GNTn5
AD	vdd	PCI_CBEn2	gnde	PCI_AD17	PCI_AD23	PCI_AD24	PCI_AD27	PCI_GNTn6	PCI_REQn5
AE	vdd	gnde	PCI_AD16	PCI_AD18	PCI_AD21	PCI_AD26	PCI_AD31	PCI_REQn6	PCI_GNTn3
AF	gnde	vdd	vdd	PCI_AD20	PCI_CBEn3	PCI_AD25	PCI_AD29	PCI_REQn4	PCI_GNTn4
	1	2	3	4	5	6	7	8	9

Color legend

Core power balls — Core and I/O ground balls — 3.3 V I/O power balls — PLL power and ground balls

Figure 13. Pin arrangement (middle)

10	11	12	13	14	15	16	17	18	
TEST_CTRL4	LIO_AD07	LIO_A2	LIO_ADLOCK	DDR2_VREF	DDR2_DQSn0	DDR2_DQ03	DDR2_DQ12	DDR2_DQM1	A
LIO_AD00	LIO_AD15	LIO_A6	LIO_DIR	DDR2_DQ00	DDR2_DQSp0	DDR2_DQ02	DDR2_DQ09	DDR2_DQSp1	B
LIO_AD03	LIO_AD13	LIO_RDn	LIO_DEN	DDR2_DQ04	DDR2_DQ05	DDR2_DQ06	DDR2_DQ08	DDR2_DQSn1	C
LIO_AD11	LIO_CSn	LIO_WRn	LIO_ROMCSn	DDR2_DQ01	DDR2_DQM0	DDR2_DQ07	DDR2_DQ13	DDR2_GATEI0	D
									E
									F
									G
10	11	12	13	14	15	16	17	18	H
vdd	vdd	vdd	gnde	gnde	gnde	vdde1v8	vdde1v8	gnde	J
gnde	vdde3v3	vdde3v3	vdde3v3	vdde1v8	vdde1v8	vdde1v8	vdde1v8	gnde	K
vdde3v3	vdde3v3	vdde3v3	gnd	gnd	vdde1v8	vdde1v8	vdde1v8	vdde1v8	L
vdde3v3	gnd	gnd	gnd	gnd	gnd	gnd	vdde1v8	gnde	M
vdde3v3	gnd	gnd	gnd	gnd	gnd	gnd	vdde1v8	gnde	N
vdde3v3	gnd	gnd	gnd	gnd	gnd	gnd	vdde1v8	gnde	P
vdde3v3	gnd	gnd	gnd	gnd	gnd	gnd	vdde1v8	gnde	R
vdde3v3	vdde3v3	vdde3v3	gnd	gnd	vdde1v8	vdde1v8	vdde1v8	vdde1v8	T
vdde3v3	vdde3v3	vdde3v3	vdde3v3	vdde1v8	vdde1v8	vdde1v8	vdde1v8	gnde	U
gnde	vdd	vdd	vdde3v3	gnde	gnde	vdde1v8	vdde1v8	gnde	V
10	11	12	13	14	15	16	17	18	W
									Y
									AA
									AB
PCI_REQn3	PCI_GNTn1	PCI_IRQnA	INTN1	tck	comp1v8_resistor	DDR2_SCSn1	DDR2_A00	DDR2_ODT0	AC
PCI_REQn2	PCI_REQn0	PCI_IRQnC	INTN2	tdo	PCI_CLK	DDR2_ODT3	DDR2_SCSn3	DDR2_ODT2	AD
PCI_GNTn2	PCI_GNTn0	PCI_IRQnB	INTN3	trst	tms	DDR2_ODT1	DDR2_A01	DDR2_CASn	AE
PCI_REQn1	PCI_RESETn	PCI_IRQnD	NMIN	INTN0	tdi	comp1v8_gnd	DDR2_A02	DDR2_A13	AF
10	11	12	13	14	15	16	17	18	

Color legend

Core power balls — Core and I/O ground balls — 3.3 V I/O power balls — 1.8 V I/O power balls

Figure 14. Pin arrangement (right-hand side)

19	20	21	22	23	24	25	26	
DDR2_GATEO0	DDR2_DQM2	DDR2_DQ20	DDR2_DQ22	DDR2_CKE3	vdde1v8	vdde1v8	gnde	A
DDR2_DQ14	DDR2_DQ16	DDR2_DQ17	DDR2_DQ23	DDR2_CKn4	DDR2_CKE1	gnde	vdde1v8	B
DDR2_DQ15	DDR2_DQ10	DDR2_DQSp2	DDR2_DQ18	DDR2_CKp4	gnde	DDR2_CKE2	DDR2_A12	C
DDR2_DQ11	DDR2_DQ21	DDR2_DQSn2	DDR2_DQ19	gnde	DDR2_CKn1	DDR2_CKp1	DDR2_BA2	D
				DDR2_A14	DDR2_A07	DDR2_A11	DDR2_A06	E
				DDR2_A08	DDR2_CKE0	DDR2_A05	DDR2_A04	F
				DDR2_A09	DDR2_A03	DDR2_DQ29	DDR2_DQ28	G
				DDR2_DQM3	DDR2_DQ25	DDR2_DQ24	DDR2_DQ31	H
J				DDR2_DQ30	DDR2_DQ36	DDR2_DQSn3	DDR2_DQSp3	J
K				DDR2_DQ27	DDR2_DQ26	DDR2_GATEO1	DDR2_GATEI1	K
L				DDR2_DQ37	DDR2_DQ33	DDR2_DQ32	DDR2_DQM4	L
M				DDR2_DQ39	DDR2_DQ38	DDR2_DQSn4	DDR2_DQSp4	M
N				DDR2_DQ34	DDR2_DQ35	DDR2_CKp3	DDR2_CKn3	N
P				DDR2_BA1	DDR2_A10	DDR2_CKn0	DDR2_CKp0	P
R				DDR2_SCSn2	DDR2_SCSn0	DDR2_BA0	DDR2_RASn	R
T				DDR2_DQ44	DDR2_DQ40	DDR2_DQ45	DDR2_DQ41	T
U				DDR2_DQ43	DDR2_DQSn5	DDR2_DQSp5	DDR2_DQM5	U
V				DDR2_DQ48	DDR2_DQ47	DDR2_DQ42	DDR2_DQ46	V
				DDR2_DQ52	DDR2_DQ49	DDR2_GATEI2	DDR2_GATEO2	W
				DDR2_DQ55	DDR2_DQ51	DDR2_DQSp6	DDR2_DQSn6	Y
				DDR2_DQM6	DDR2_DQ53	DDR2_DQ54	DDR2_DQ50	AA
				DDR2_DQ61	DDR2_DQ60	DDR2_DQM7	DDR2_DQ56	AB
DDR2_WEn	DDR2_CB2	DDR2_DQM8	DDR2_GATEI3	gnde	DDR2_DQSp7	DDR2_DQSn7	DDR2_DQ57	AC
DDR2_CKp2	DDR2_CB3	DDR2_CB6	DDR2_GATEO3	DDR2_DQ59	gnde	DDR2_DQ62	DDR2_DQ58	AD
DDR2_CKn2	DDR2_CB7	DDR2_DQSp8	DDR2_CB5	DDR2_CB4	DDR2_DQ63	gnde	vdde1v8	AE
DDR2_CKn5	DDR2_CKp5	DDR2_DQSn8	DDR2_CB1	DDR2_CB0	vdde1v8	vdde1v8	gnde	AF
19	20	21	22	23	24	25	26	

Color legend

Core and I/O ground balls

1.8 V I/O power balls

9 Package information

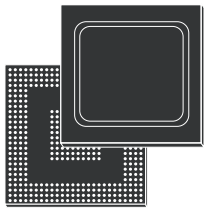
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

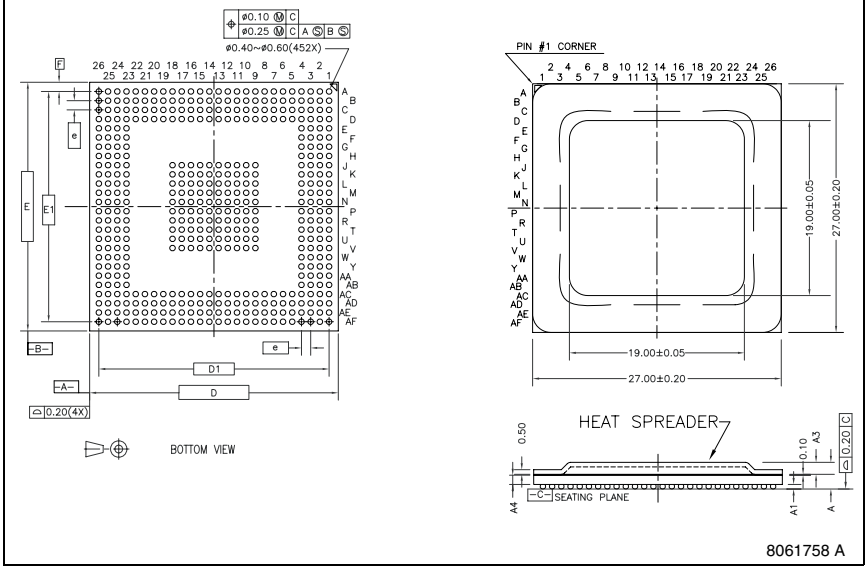
Figure 15. HFCBGA452 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.150			0.1240
A1	0.250			0.0098		
A3		1.300			0.0512	
A4		1.000			0.0394	
b	0.450	0.500	0.550	0.0177	0.0197	0.0217
D	26.800	27.000	27.200	1.0551	1.0630	1.0709
D1		25.000			0.9843	
E	26.800	27.000	27.200	1.0551	1.0630	1.0709
E1		25.000			0.9843	
e		1.000			0.0394	
F		1.000			0.0394	
aaa			0.200			0.0079
ddd			0.200			0.0079
eee			0.250			0.0098
fff			0.100			0.0039

OUTLINE AND MECHANICAL DATA



HFCBGA452 (27x27x2.9mm)
Heat **S**preader **F**lip **C**hip **B**all **G**rid **A**rray



10 Revision history

Table 23. Document revision history

Date	Revision	Changes
28-Jul-2008	1	Initial relase.

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