Ordering number : EN*A1476

Preliminary

SANYO Semiconductors
DATA SHEET

Thick-Film Hybrid IC

STK433-760-E — 2-channel class AB audio power IC, 50W+50W

Overview

The STK433-760-E is a hybrid IC designed to be used in 50W × 50W (2-channel) class AB audio power amplifiers.

Applications

- Audio power amplifiers.

Features

- Miniature package (47.0mm × 25.6mm × 9.0mm)
- Output load impedance: R_L = 6Ω to 4Ω supported
- Built-in stand-by circuit, output limiting circuit for substrate overheating, and load short-circuit protection circuit constituted by monolithic ICs

Series Models

	STK433-730-E	STK433-760-E
Output 1 (10%/1kHz)	30W×2 channels	50W×2 channels
Output 2 (0.4%/20Hz to 20kHz)	15W×2 channels	35W×2 channels
Max. rated V_{CC} (quiescent)	±30V	±50V
Max. rated V_{CC} (6Ω)	±28V	±40V
Max. rated V_{CC} (4Ω)	±25V	±33V
Recommended operating V_{CC} (4Ω)	±18V	±23V
Dimensions (excluding pin height)	47.0mm×25.6mm×9.0mm	

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Specifications

Absolute Maximum Ratings at Ta = 25°C, Tc=25°C unless otherwise specified

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max (0)	Stand-by ON or When no signal (Stand-by OFF)	±50	V
	V_{CC} max (1)	When signals are present, $R_L \geq 6\Omega$ (*1)	±40	V
	V_{CC} max (2)	When signals are present, $R_L \geq 4\Omega$ (*1)	±33	V
Minimum operating supply voltage	V_{CC} min		±10	V
Stand-by pin maximum voltage	VST max		-0.3 to +5.5	V
Output current	I_O (peak)	1ch, ton=25ms	5.0	A
Thermal resistance	θj-c	Per power transistor	3.5	°C/W
		Per package	0.88	
Junction temperature	Tj max	Both the Tj max and Tc max conditions must be met.	150	°C
IC substrate operating temperature	Tc max		125	°C
Storage temperature	Tstg		-30 to +125	°C

Operating Characteristics at Tc=25°C, R_L=4Ω, Rg=600Ω, VG=30dB, non-inductive load R_L, using constant-voltage power supply and specification test circuit, unless otherwise specified

Parameter	Symbol	Conditions *2					Ratings			unit
		V_{CC} (V)	f (Hz)	P_O (W)	THD (%)		min	typ	max	
Output power *2	P_O (1)	±23	20 to 20k		0.4		33	35		W
	P_O (2)	±23	1k		0.4			40		
	P_O (3)	±23	1k		10			50		
Total harmonic distortion *2	THD (1)	±23	20 to 20k	5.0		VG=30dB			0.4	%
	THD (2)	±23	1k					0.04		
Output power transistor saturation voltage	Vsat	±23	1k	50	10			5.0		V
Frequency characteristics *2	f_L, f_H	±23		1.0		+0 -3dB	20 to 50k			Hz
Input impedance	ri	±23	1k	1.0				55		kΩ
Output noise voltage *10	V_{NO}	±28				Rg=2.2kΩ			1.0	mVrms
Quiescent current	I_{CCO}	±28				No loading	15	30	60	mA
Output neutral voltage	V_N	±28					-70	0	+70	mV
Pin 13 voltage when standby ON *5	VST ON	±23				Standby			0.6	V
Pin 13 voltage when standby OFF *5	VST OFF	±23				Operating	2.5	3.6	5.5	V
Pin 10 (latch operation detection pin) voltage *7	IM ON					In short-circuit protection mode		5.5		V
Substrate thermal protection *8	TD	±23	1k			R_L=∞		130		°C
Overcurrent protection *8,*10	I_O (peak)	±23	1k					6.0		A

[Remarks]

*1: Maximum ratings are limits beyond which damage to the device may occur.
Exceeding the maximum ratings, even momentarily, may cause damage to the hybrid IC.
In SANYO Semiconductor's test processes, operation at the maximum supply voltage is checked.
(Test conditions) V_{CC} max (2)=±33V, R_L=4Ω, f=1kHz, Po=35W, 1ch Drive, ton=25ms, Tc=25°C

*2: For 1-channel operation

*3: -Pre V_{CC} (pin 7) must be connected to the lowest stable potential to prevent the current flowing into the pin 1 due to reverse bias, etc.

*4: Thermal design must be implemented based on the conditions under which the customer's end products are expected to operate on the market.

*5: Use the hybrid IC so that the voltage applied to the stand-by pin (pin 13) never exceeds the maximum rating. The power amplifier is turned on by applying +2.5V to +5.5V to the stand-by pin (pin 13).

*6: An output limiting circuit for H-IC overheating is incorporated to protect the hybrid IC from the heat generation exceeding the maximum rating. Thermal design must be implemented from the maximum loss Pd max and "Pd-Tc" derating curve based on the conditions under which the customer's end products are expected to operate on the market. When deviating from the "Pd-Tc" derating curve, the desired output is not obtained, but the prescribed output is generated again by reducing H-IC temperature to within the recommended operating region.

*7: The load short-circuit protection is designed based on the specification test condition.
The load short-circuit protection circuit is activated when it has detected an overcurrent in the output transistors. So if any deviation from the "Pd-Tc" derating curve occurs, the protection circuit is activated and the circuit shuts down in order to protect the output transistors. When the load short-circuit protection circuit has been activated and the circuit shuts down, approximately +5.5V of voltage will be placed at the MONITOR pin (pin 10) (normally 0V).
The protection circuit operation is released by establishing the stand-by mode (pin 13: 0V).

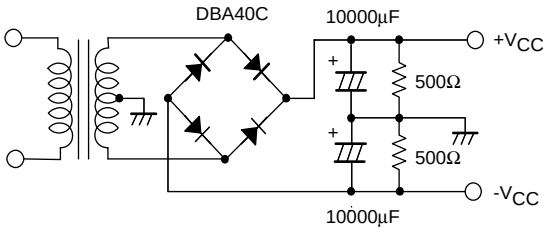
*8: The substrate temperature protection rating is the design guarantee value using the specification test circuit of SANYO Semiconductor.
The output limiting circuit for H-IC overheating (*6) and the load short-circuit protection circuit (*7) are the only protection functions incorporated.
The thermal design and overcurrent protection level must be verified based on the conditions under which the customer's end products are expected to operate on the market.

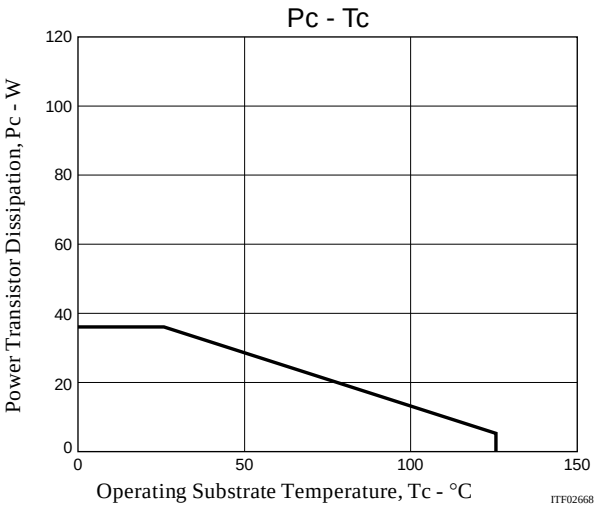
*9: A thermoplastic adhesive resin is used to secure the case and aluminum substrate. For this reason, the hybrid IC must be fixed to the heat sink before soldering and mounted. The heat sink must be installed or removed at room temperature.

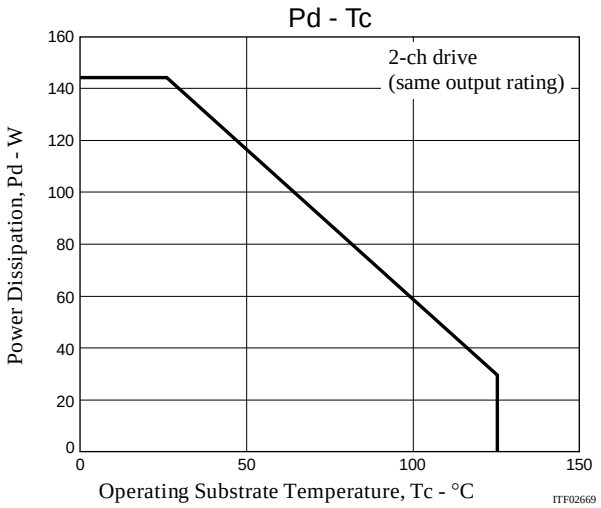
*10: Use the designated transformer power supply circuit shown in the figure below for the measurement of allowable load shorted time and output noise voltage level.

*11: Weight of independent hybrid IC: 12.2g
Outer box dimensions: 452(D) × 325(W) × 192(H) mm

Designated transformer power supply
(MG-200 equivalent)

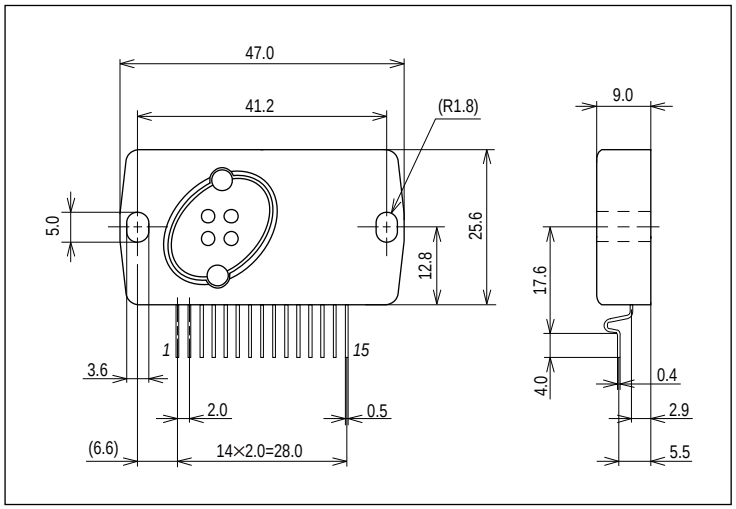




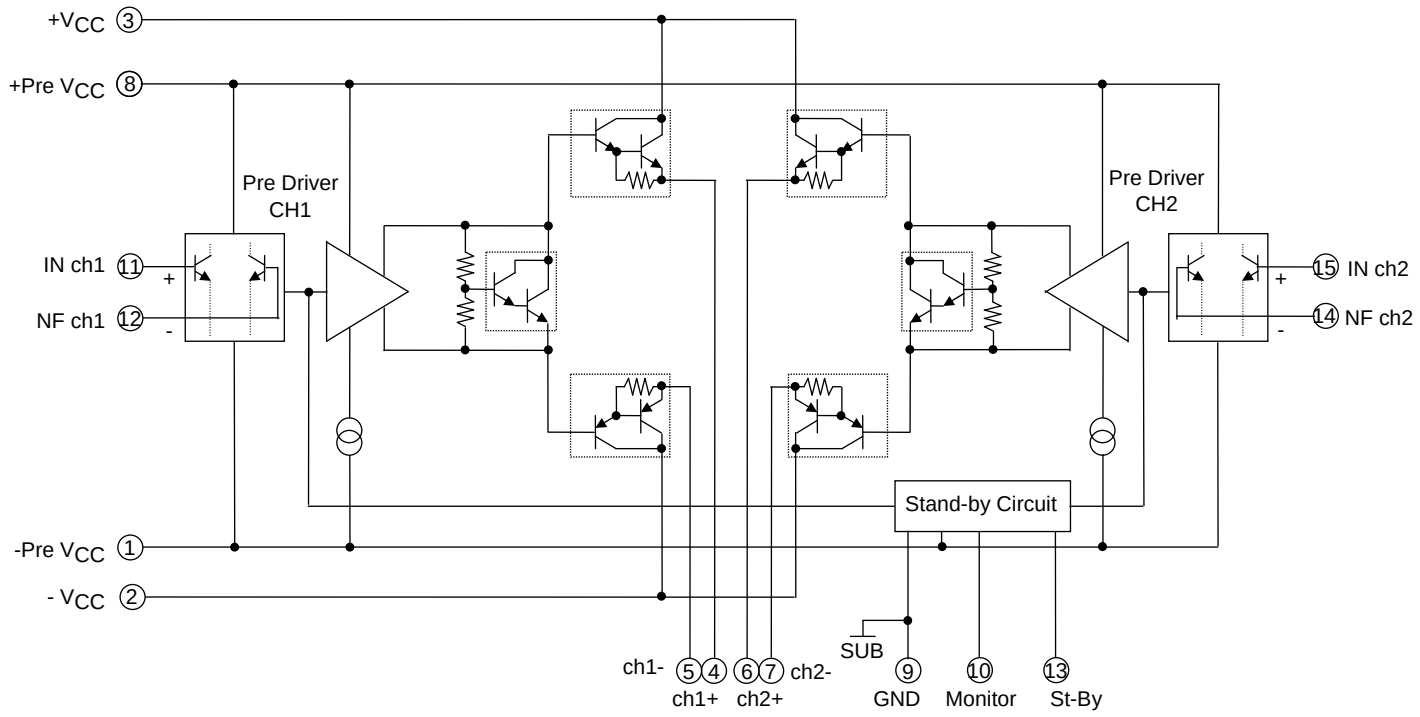


Package Dimensions

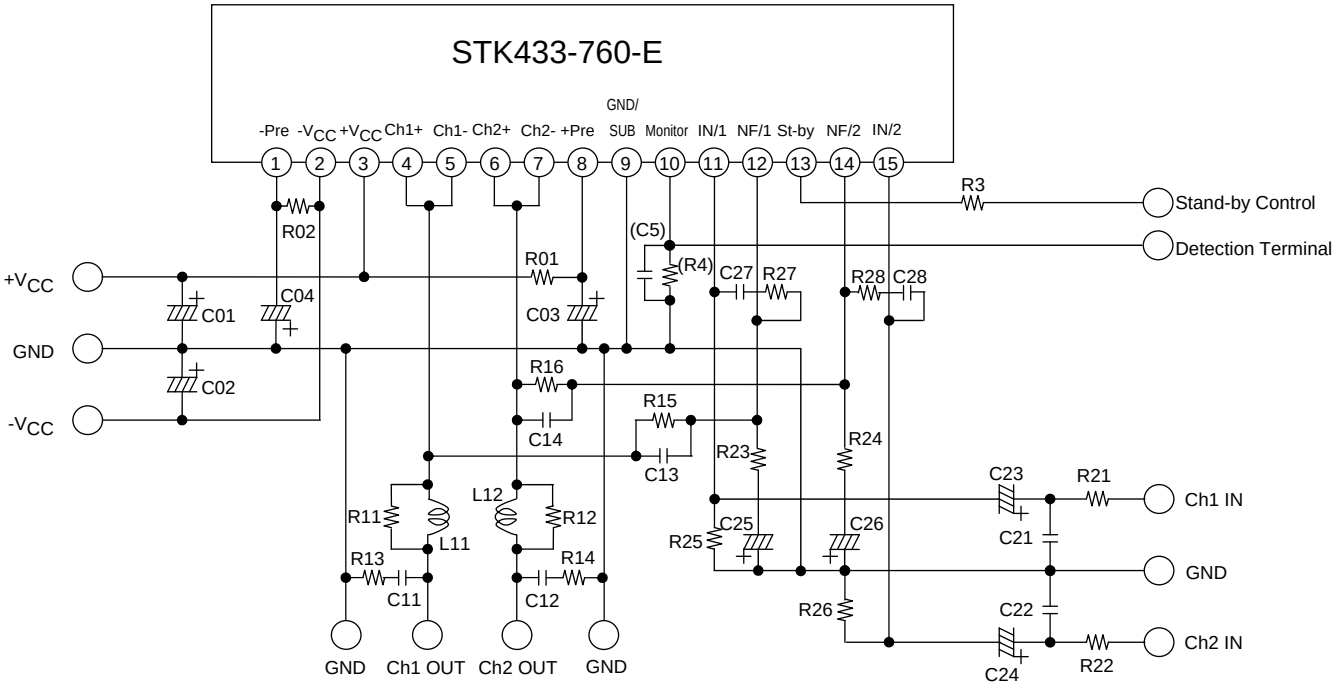
unit:mm (typ)



Internal Equivalent Circuit



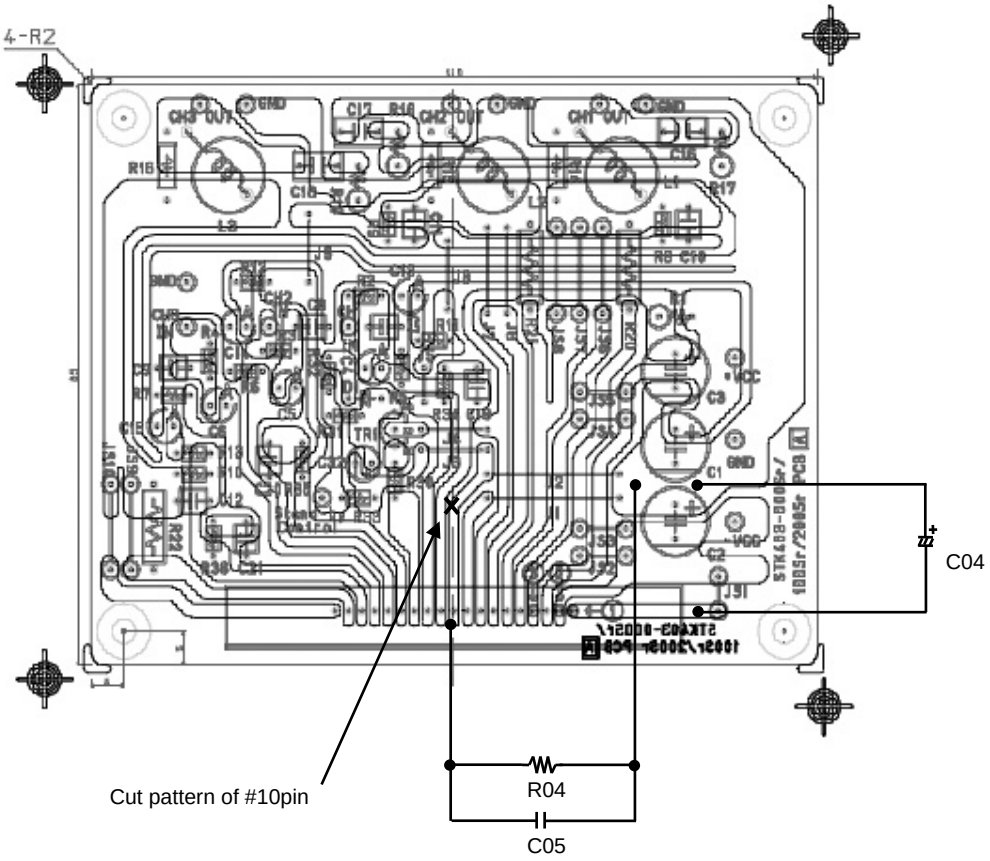
Application Circuit Example



Recommended Values for Application Parts (for the test circuit)

Symbol	Recommended Value	Description	Larger than Recommended Value	Smaller than Recommended Value
R01, R02	100Ω	Ripple filtering resistors (Fusible resistors are desirable) (Used with C03, C04 to form a ripple filter.)	Decreased pass-through current at high frequencies.	Increased pass-through current at high frequencies.
R03	-	Use a limiting resistor according to the stand-by control voltage in order to control the stand-by pin voltage VST within the rating.		
(R04)	about 10kΩ	Pull down resistance (at detection terminal use).	-	(min) 5.1kΩ
R11, 12	4.7Ω	Noise-absorbing resistors	-	-
R13, 14	4.7Ω/1W	Oscillation prevention	-	-
R15, 16	56kΩ	Used with R23 and R24 to determine the voltage gain VG.	VN offset (Ensure R15=R25, R16=R26 when changing.)	
R21, 22	1kΩ	Input filtering resistor	-	-
R23, 24	1.8kΩ	Used with R15 and R16 to determine the voltage gain VG. (VG should desirably be determined by the R23 and R24 value.)	Likely to oscillate (VG<30dB)	None (VG≤42dB)
R25, 26	56kΩ	Input bias resistors (Virtually determine the input impedance.)	-	-
R27, 28	560Ω	Oscillation prevention	Likely to oscillate	
C01, 02	100μF	Oscillation prevention • Insert the capacitors as close to the IC as possible to decrease the power impedance for reliable IC operation (use of electrolytic capacitors are desirable).	-	-
C03, C04	100μF	Decoupling capacitors. • Eliminate ripple components that pass into the input side from the power line. (Used with R01, R02 to form a filter.)	Increase in ripple components that pass into the input side from the power line.	
(C05)	About 0.1μF	A constant is adjusted when detection voltage appears at the time of latch rise (at detection terminal use).		
C11, 12	0.1μF	Oscillation prevention (Mylar capacitors are recommended.)	Likely to oscillate	
C13, 14	15pF	Oscillation prevention	Likely to oscillate	
C21, 22	470pF	Input filter capacitor (Used with R21 and R22 to form a filter that suppresses high-frequency noises.)	-	-
C23, 24	2.2μF	Input coupling capacitor (block DC current)	-	-
C25, 26	10μF	NF capacitor (Changes the low cutoff frequency; $f_L=1/(2\pi \bullet C25 \bullet R23)$	Increase in low-frequency voltage gain, with higher pop noise at power-on.	Decrease in low-frequency voltage gain
C27, 28	120pF	Oscillation prevention	Likely to oscillate	
L11, 12	1μH	Oscillation prevention	None	Likely to oscillate

Sample PCB Trace Pattern



* Additional parts are indicated by CIRCUIT Location No.

STK433-760-E TEST Board PARTS LIST

STK403-000sr/100sr/200sr PCB

PCB Location No.		CIRCUIT Location No.	PARTS	RATING	STK433-760-E
R01		R01	ERG1SJ101	100Ω,1W	
R02,R03		R21, R22	RN16S102FK	1kΩ, 1/6W	
R05, R06, R08, R09		R15, R16, R25, R26	RN16S563FK	56kΩ, 1/6W	
R11, R12		R23, R24	RN16S182FK	1.8kΩ, 1/6W	
R14, R15		R11, R12	RN14S4R7FK	4.7Ω, 1/4W	
R17, R18		R13, R14	ERX1SJ4R7	4.7Ω, 1W	
R20, R21		-	-	-	short
R34, R35		R27, R28	RN16S561FK	560Ω, 1/6W	
-		R04	RN16S103FK	10kΩ, 1/6W	
-		C05	ECQ-V1H104JZ	0.1μF, 50V	
C01, C02, C03		C01, C02, C03, C04	100MV100HC	100μF, 100V	
C05, C06		C23, C24	50MV2R2HC	2.2μF, 50V	(*)
C07, C08		C21, C22	DD104-63B471K50	470pF, 50V	
C10, C11		C13, C14	DD104-63CJ150C50	15pF, 50V	
C13, C14		C25, C26	10MV10HC	10μF, 10V	(*)
C16, C17		C11, C12	ECQ-V1H104JZ	0.1μF, 50V	
C19, C20		C27, C28	DD104-63B121K50	120pF, 50V	
L01, L02		L11, L12	-	1μH	
Stand-By Control Circuit	Tr1		2SC2274 (Reference)	VCE≥50V, IC≥10mA	
	D1		-	-	
	R03		RN16S133FK	13kΩ, 1/6W	
	R31		RN16S333FK	33kΩ, 1/6W	
	R32		-	-	
	R33		RN16S202FK	2kΩ, 1/6W	
	C32		10MV33HC	33μF, 10V	
J1, J2, J3, J4, J5, J6, J8, J9		-	-	-	Jumper
JS6		-	-	-	Jumper
JS1		R02	ERG1SJ101	100Ω, 1W	-

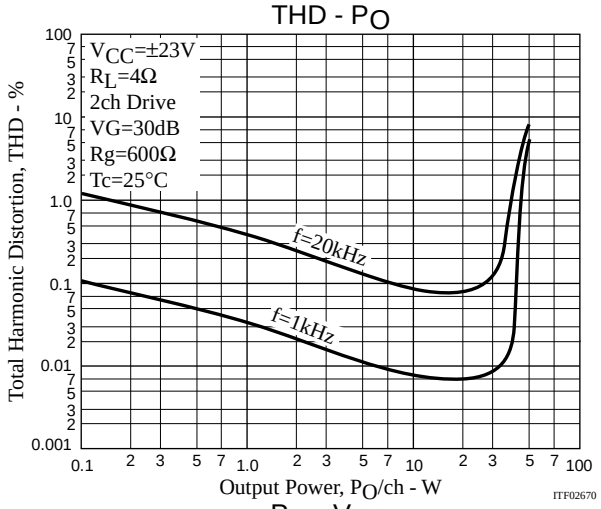
- (*) Capacitor mark “A” side is “-” (negative).
- R04, C04 and C05 does not have a location number on the PCB so the component must be mounted on the reverse side of the board.

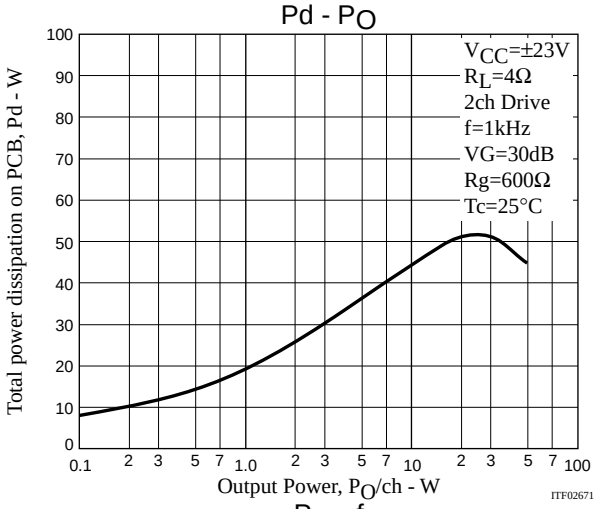
Pin Assignments

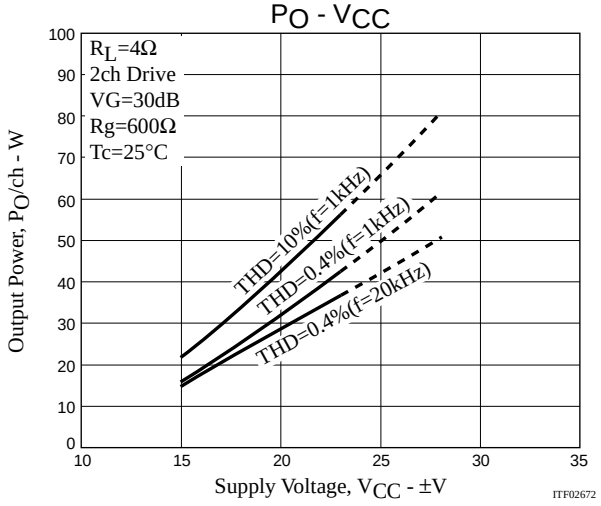
[STK433-730-E/-760-E Pin Layout]

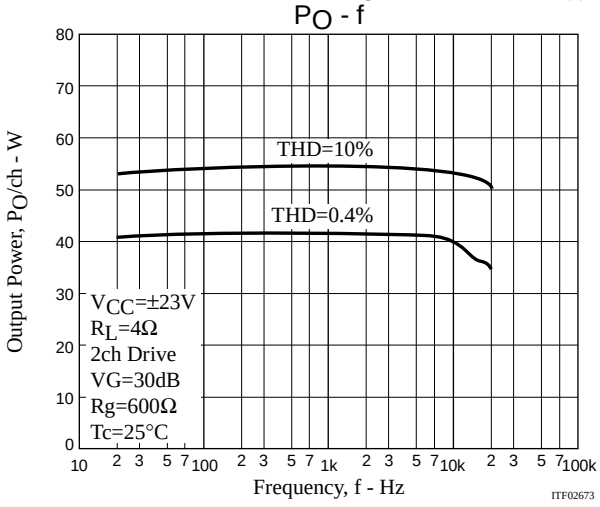
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
(Size) 47.0mm×25.6mm×9.0mm	2ch classAB/2.00mm																		
STK433-730-E 30W×2ch/JEITA STK433-760-E 50W×2ch/JEITA	-PRE	-VCC	+VCC	OUT/CH1+	OUT/CH1-	OUT/CH2+	OUT/CH2-	+PRE	SUB/GND	MONITOR	IN/CH1	NF/CH1	STAND|BY	NF/CH2	IN/CH2				

Evaluation Board Characteristics









[Thermal Design Example for STK433-760-E (R_L = 4Ω)]

The thermal resistance, θc-a, of the heat sink for total power dissipation, Pd, within the hybrid IC is determined as follows.

Condition 1: The hybrid IC substrate temperature, Tc, must not exceed 125°C.

$Pd \times \theta c\text{-}a + Ta < 125°C$ ..... (1)

Ta: Guaranteed ambient temperature for the end product

Condition 2: The junction temperature, Tj, of each power transistor must not exceed 150°C.

$Pd \times \theta c\text{-}a + Pd/N \times \theta j\text{-}c + Ta < 150°C$ ..... (2)

N: Number of power transistors

θj-c: Thermal resistance per power transistor

However, the power dissipation, Pd, for the power transistors shall be allocated equally among the number of power transistors.

The following inequalities result from solving equations (1) and (2) for θc-a.

$\theta c\text{-}a < (125 - Ta)/Pd$ ..... (1)'

$\theta c\text{-}a < (150 - Ta)/Pd - \theta j\text{-}c/N$ ..... (2)'

Values that satisfy these two inequalities at the same time represent the required heat sink thermal resistance.

When the following specifications have been stipulated, the required heat sink thermal resistance can be determined from formulas (1)' and (2)' .

- Supply voltage V_{CC}
- Load resistance R_L
- Guaranteed ambient temperature Ta

[Example]

When the IC supply voltage, V_{CC}, is ±23V and R_L is 4Ω, the total power dissipation, Pd, within the hybrid IC, will be a maximum of 52W at 1kHz for a continuous sine wave signal according to the Pd-P_O characteristics.

For the music signals normally handled by audio amplifiers, a value of 1/8P_O max is generally used for Pd as an estimate of the power dissipation based on the type of continuous signal. (Note that the factor used may differ depending on the safety standard used.)

This is:

Pd = 38.0W (when 1/8P_O max. = 6.25W).

The number of power transistors in audio amplifier block of these hybrid ICs, N, is 4, and the thermal resistance per transistor, θj-c, is 3.5°C/W. Therefore, the required heat sink thermal resistance for a guranteed ambient temperature, Ta, of 50°C will be as follows.

From formula (1)' $\theta c\text{-}a < (125 - 50)/38.0$

< 1.92

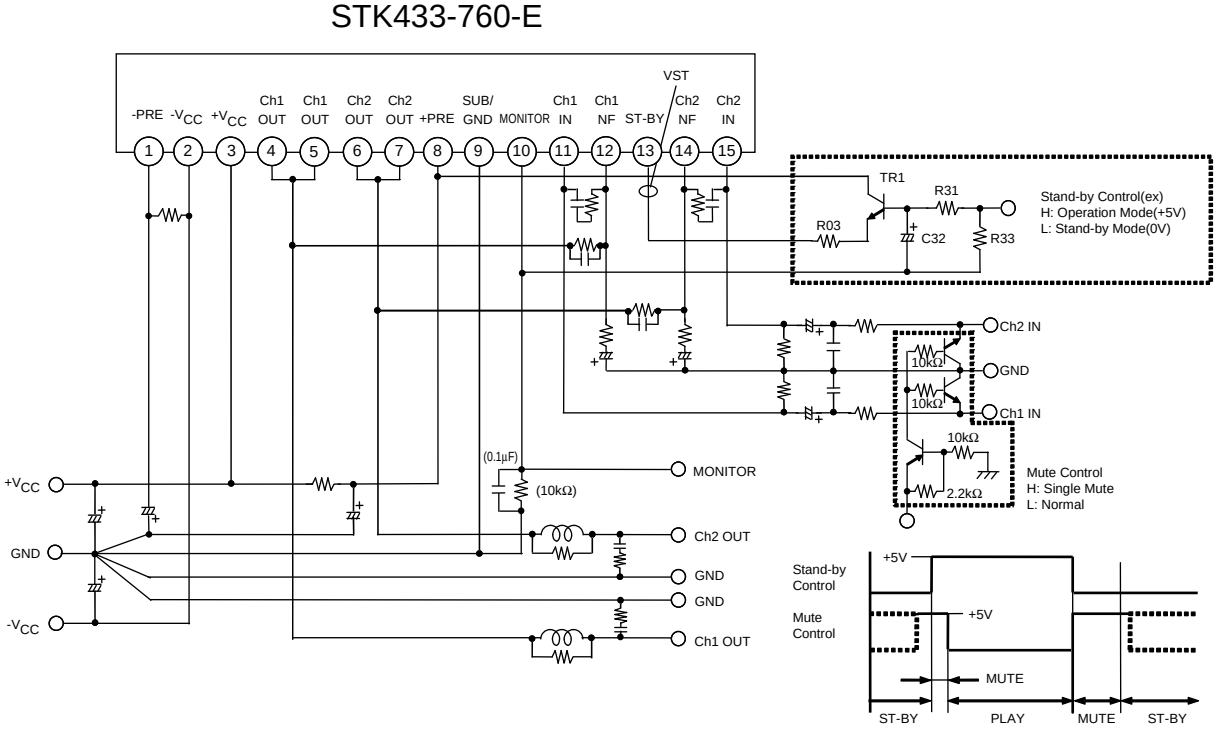
From formula (2)' $\theta c\text{-}a < (150 - 50)38.0 - 3.5/4$

< 1.75

Therefore, the value of 1.75°C/W, which satisfies both of these formulae, is the required thermal resistance of the heat sink.

Note that this thermal design example assumes the use of a constant-voltage power supply, and is therefore not a verified design for any particular user’s end product.

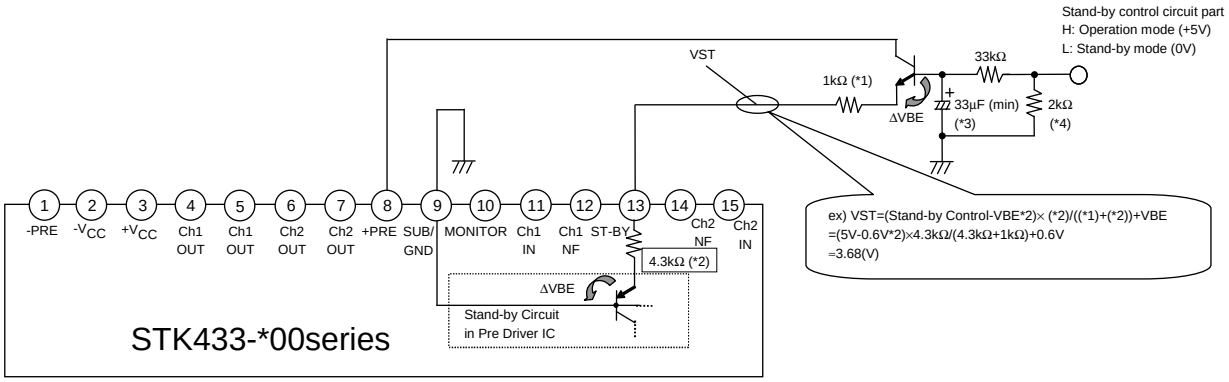
STK433-760-E Stand-by Control & Mute Control Application



[The example of use STK433-*00series Stand-by control circuit]

Features

- By using the recommended stand-by control application, the pop noise level when the power is turned on/off can be significantly reduced.
- By adjusting the limiting resistance (*2) in accordance with the voltages of the microcontroller and other components used, it is possible to perform stand-by control, facilitating the finished product design effort.
  (ex) STK433-*00series test circuit. When impressed by Stand-by control control [+5V].



Operation Explanation

1) About VST (#13pin Stand-by Threshold)

<1> Operation Mode

When pin 13 reference voltage VST is equal to or greater than 2.5V, the stand-by circuit is set off, and the amplifier is set to the operation mode.

<2> Stand-by Mode

When pin 13 reference voltage VST is equal to or less than 0.6V, the stand-by circuit is set off, and the amplifier is set to the stand-by mode.

(*3) The pop noise that occurs when the power is turned ON is reduced by providing a time constant using a capacitor during operation.

(*4) The pop noise level is reduced by discharging the capacitor with a resistor in the stand-by mode.

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