

SANYO

STK401-270

Preliminary

Package Dimensions

unit: mm

4134

Technical drawing of the STK401-270 component, showing front and side views with dimensions.

Front View Dimensions:

- Overall width: 66
- Inner width: 55.6
- Overall height: 36.5
- Bottom flange height: 18.7
- Pin diameter: $\phi 3.8$
- Pin spacing: 15 x 2.54 = 38.1
- Pin pitch: 2.54
- Pin width: 0.5
- Pin height: 18
- Pin offset: 2
- Pin hole offset: (8.75)

Side View Dimensions:

- Top flange width: 8.5
- Top flange height: 23.5
- Pin height: 4
- Pin offset: 2.9
- Pin width: 0.4
- Pin pitch: 5.5

- Pin compatible with the 3-channel output devices (STK400-×00 series) and 2-channel output devices (STK401-×00 series)
- Output load impedance $R_L = 6/3\Omega$ supported
- Pin configuration grouped into individual blocks of inputs, outputs and supply lines to minimize the adverse effects of pattern layout on operating characteristics.
- Few external components

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC \text{ max}}$		± 44	V
Thermal resistance	θ_{j-c}	Per power transistor	1.7	$^\circ\text{C/W}$
Junction temperature	T_j		150	$^\circ\text{C}$
Operating substrate temperature	T_c		125	$^\circ\text{C}$
Storage temperature	T_{stg}		-30 to $+125$	$^\circ\text{C}$
Available time for load short-circuit	t_s	$V_{CC} = \pm 30\text{V}$, $R_L = 6\Omega$, $f = 50\text{Hz}$, $P_O = 40\text{W}$	1	s

Operating Characteristics at $T_a = 25^\circ\text{C}$, $R_L = 6\Omega$ (noninductive load), $R_g = 600\Omega$, $V_G = 40\text{dB}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Output power	$P_{O(1)}$	$V_{CC} = \pm 30\text{V}$, $f = 20\text{Hz}$ to 20kHz , $\text{THD} = 0.08\%$	40	45	—	W
	$P_{O(2)}$	$V_{CC} = \pm 24\text{V}$, $f = 1\text{kHz}$, $\text{THD} = 0.2\%$, $R_L = 3\Omega$	40	45	—	W
Total harmonic distortion	$\text{THD}(1)$	$V_{CC} = \pm 30\text{V}$, $f = 20\text{Hz}$ to 20kHz , $P_O = 1.0\text{W}$	—	—	0.08	%
	$\text{THD}(2)$	$V_{CC} = \pm 30\text{V}$, $f = 1\text{kHz}$, $P_O = 5.0\text{W}$	—	0.007	—	%
Frequency response	f_L, f_H	$V_{CC} = \pm 30\text{V}$, $P_O = 1.0\text{W}$, $+0_{-3}\text{dB}$	—	20 to 50k	—	Hz
Input impedance	r_i	$V_{CC} = \pm 30\text{V}$, $f = 1\text{kHz}$, $P_O = 1.0\text{W}$	—	55	—	$\text{k}\Omega$
Output noise voltage	V_{NO}	$V_{CC} = \pm 36\text{V}$, $R_g = 10\text{k}\Omega$	—	—	1.2	mVrms
Quiescent current	I_{CCO}	$V_{CC} = \pm 36\text{V}$	20	60	100	mA
Neutral voltage	V_N	$V_{CC} = \pm 36\text{V}$	-70	0	$+70$	mV

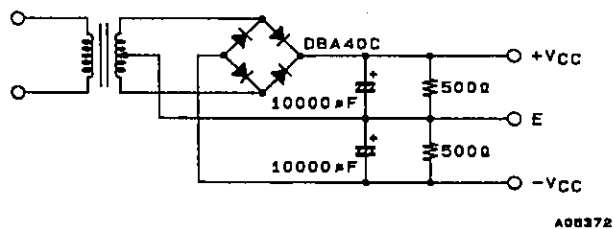
Notes.

All tests are measured using a constant-voltage supply unless otherwise specified.

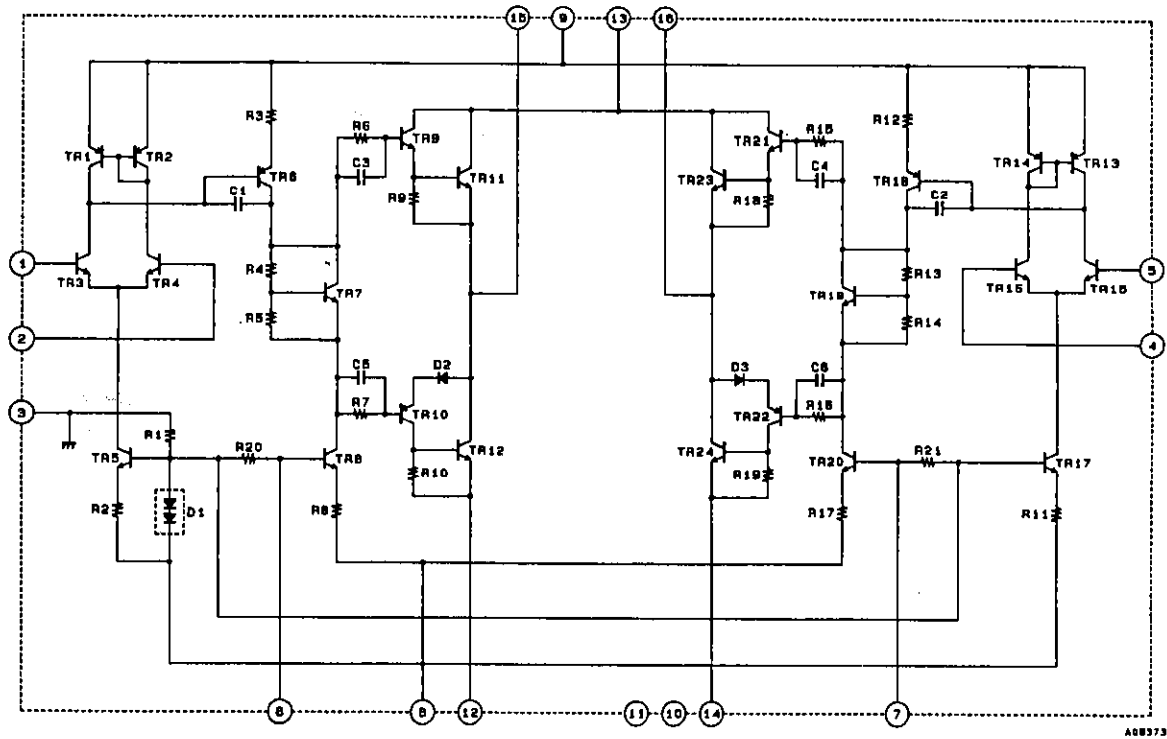
Available time for load short-circuit and output noise voltage are measured using the transformer supply specified below.

The output noise voltage is the peak value of an average-reading meter with an rms value scale (VTVM). A regulated AC supply (50Hz) should be used to eliminate the effects of AC primary line flicker noise.

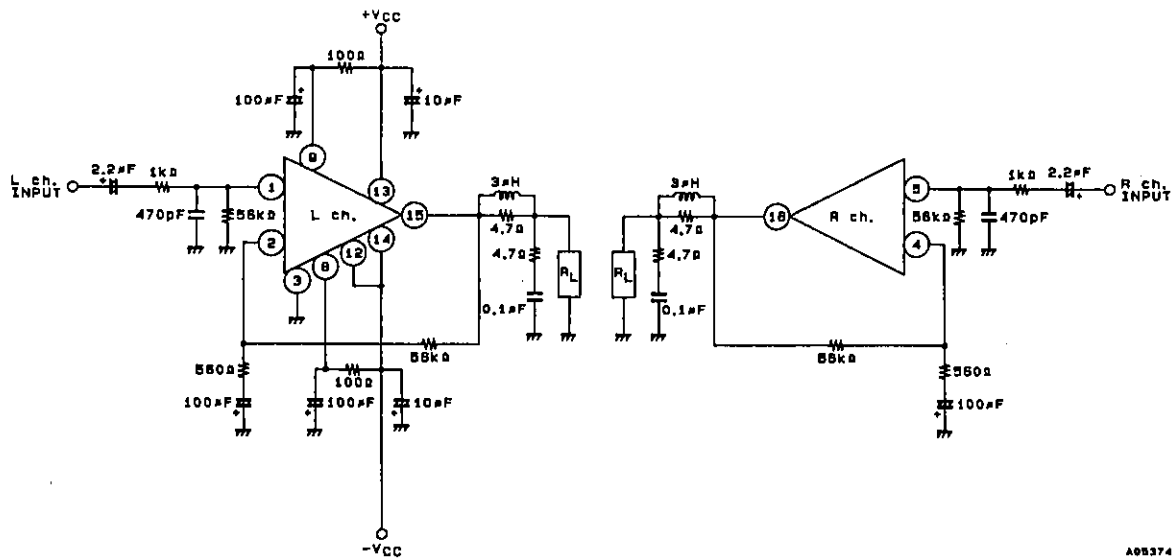
Specified Transformer Supply (MG-200 or Equivalent)



Equivalent Circuit



Sample Application Circuit



Series Configuration

These devices form a series of pin-compatible devices with different number of output channels, output ratings and total harmonic distortion. Some of these devices are under development. Contact your Sanyo sales representative if you require more detailed information.

STK400-000, STK400-200 series (3-channel, same output rating)					STK401-000, STK401-200 series (2-channel)					Supply voltage [V] ¹			
Type No.	THD [%]	Type No.	THD [%]	Rated output	Type No.	THD [%]	Type No.	THD [%]	Rated output	V _{CC} max1	V _{CC} max2	V _{CC} 1	V _{CC} 2
STK400-010	0.4	STK400-210	0.08	10W × 3	STK401-010	0.4	STK401-210	0.08	10W × 2	–	±26.0	±17.5	±14.0
STK400-020		STK400-220		15W × 3	STK401-020		STK401-220		15W × 2	–	±29.0	±20.0	±16.0
STK400-030		STK400-230		20W × 3	STK401-030		STK401-230		20W × 2	–	±34.0	±23.0	±19.0
STK400-040		STK400-240		25W × 3	STK401-040		STK401-240		25W × 2	–	±36.0	±25.0	±21.0
STK400-050		STK400-250		30W × 3	STK401-050		STK401-250		30W × 2	–	±39.0	±26.0	±22.0
STK400-060		STK400-260		35W × 3	STK401-060		STK401-260		35W × 2	–	±41.0	±28.0	±23.0
STK400-070		STK400-270		40W × 3	STK401-070		STK401-270		40W × 2	–	±44.0	±30.0	±24.0
STK400-080		STK400-280		45W × 3	STK401-080		STK401-280		45W × 2	–	±45.0	±31.0	±25.0
STK400-090		STK400-290		50W × 3	STK401-090		STK401-290		50W × 2	–	±47.0	±32.0	±26.0
STK400-100		STK400-300		60W × 3	STK401-100		STK401-300		60W × 2	–	±51.0	±35.0	±27.0
STK400-110		STK400-310		70W × 3	STK401-110		STK401-310		70W × 2	±56.0	–	±38.0	–
					STK401-120		STK401-320		80W × 2	±61.0	–	±42.0	–
					STK401-130		STK401-330		100W × 2	±65.0	–	±45.0	–
					STK401-140		STK401-340		120W × 2	±74.0	–	±51.0	–

STK400-400, STK400-600 series (3-channel, different output ratings)					Supply voltage [V] ¹				
Type No.	THD [%]	Type No.	THD [%]	Rated output		V _{cc} max1	V _{cc} max2	V _{cc} 1	V _{cc} 2
STK400-450	0.4	STK400-650	0.08	Cch	30W	–	±39.0	±26.0	±22.0
				Lch, Rch	15W	–	±29.0	±20.0	±16.0
STK400-460		STK400-660		Cch	35W	–	±41.0	±28.0	±23.0
				Lch, Rch	15W	–	±29.0	±20.0	±16.0
STK400-470		STK400-670		Cch	40W	–	±44.0	±30.0	±24.0
				Lch, Rch	20W	–	±34.0	±23.0	±19.0
STK400-480		STK400-680		Cch	45W	–	±45.0	±31.0	±25.0
				Lch, Rch	20W	–	±34.0	±23.0	±19.0
STK400-490		STK400-690		Cch	50W	–	±47.0	±32.0	±26.0
				Lch, Rch	25W	–	±36.0	±25.0	±21.0
STK400-500		STK400-700		Cch	60W	–	±51.0	±35.0	±27.0
				Lch, Rch	30W	–	±39.0	±26.0	±22.0
STK400-510		STK400-710		Cch	70W	±56.0	–	±38.0	–
				Lch, Rch	35W	–	±41.0	±28.0	±23.0
STK400-520		STK400-720		Cch	80W	±61.0	–	±42.0	–
				Lch, Rch	40W	–	±44.0	±30.0	±24.0
STK400-530		STK400-730		Cch	100W	±65.0	–	±45.0	–
				Lch, Rch	50W	–	±47.0	±32.0	±26.0

1. V_{CC} max1 (R_L = 6Ω), V_{CC} max2 (R_L = 3 to 6Ω), V_{CC}1 (R_L = 6Ω), V_{CC}2 (R_L = 3Ω)

Heatsink Design Considerations

The heatsink thermal resistance, θ_{c-a} , required to dissipate the STK401-270 device total power dissipation, P_d , is determined as follows:

Condition 1: IC substrate temperature not to exceed 125°C.

$$P_d \times \theta_{c-a} + T_a < 125^\circ\text{C} \dots\dots\dots (1)$$

where T_a is the guaranteed maximum ambient temperature.

Condition 2: Power transistor junction temperature, T_j , not to exceed 150°C.

$$P_d \times \theta_{c-a} + P_d/N \times \theta_{j-c} + T_a < 150^\circ\text{C} \dots\dots\dots (2)$$

where N is the number of power transistors and θ_{j-c} is the power transistor thermal resistance per transistor. Note that the power dissipated per transistor is the total, P_d , divided evenly among the N power transistors.

Expressions (1) and (2) can be rewritten making θ_{c-a} the subject.

$$\theta_{c-a} < (125 - T_a)/P_d \dots\dots\dots (1)'$$

$$\theta_{c-a} < (150 - T_a)/P_d - \theta_{j-c}/N \dots\dots\dots (2)'$$

The heatsink required must have a thermal resistance that simultaneously satisfies both expressions.

The heatsink thermal resistance can be determined from (1)' and (2)' once the following parameters have been defined.

- Supply voltage: V_{CC}
- Load resistance: R_L
- Guaranteed maximum ambient temperature: T_a

The total device power dissipation when STK401-270 $V_{CC} = \pm 30\text{V}$ and $R_L = 6\Omega$, for a continuous sine wave signal, is a maximum of 62.5W, as shown in the $P_d - P_O$ graphs.

When estimating the power dissipation for an actual audio signal input, the rule of thumb is to select P_d corresponding to $(1/10) \times P_O \text{ max}$ (within safe limits) for a continuous sine wave input. For example,

$$P_d = 38\text{W [for } (1/10) \times P_O \text{ max} = 4\text{W]}$$

The STK401-270 has 4 power transistors, and the thermal resistance per transistor, θ_{j-c} , is 1.7°C/W. If the guaranteed maximum ambient temperature, T_a , is 50°C, then the required heatsink thermal resistance, θ_{c-a} , is:

$$\text{From expression (1)': } \theta_{c-a} < (125 - 50)/38 \\ < 1.97$$

$$\text{From expression (2)': } \theta_{c-a} < (150 - 50)/38 - 1.7/4 \\ < 2.20$$

Therefore, to satisfy both expressions, the required heatsink must have a thermal resistance less than 1.97°C/W.

Similarly, when STK401-270 $V_{CC} = \pm 24\text{V}$ and $R_L = 3\Omega$,

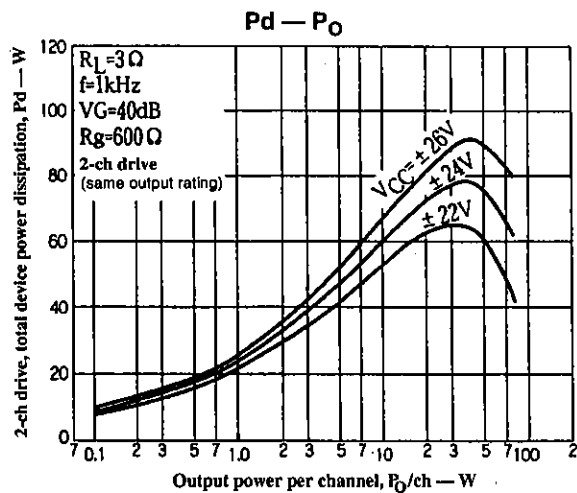
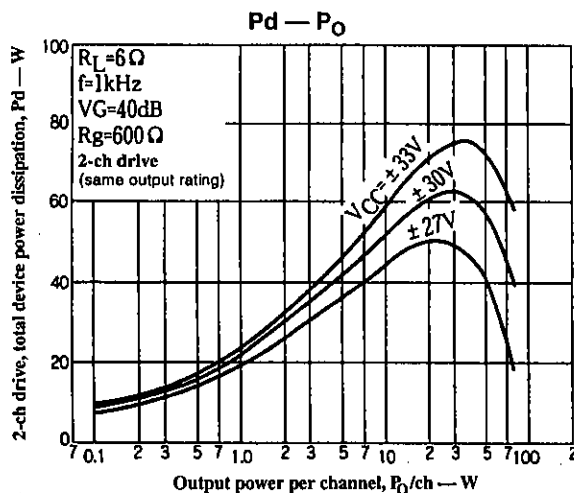
$$P_d = 43\text{W [for } (1/10) \times P_O \text{ max} = 4\text{W]}$$

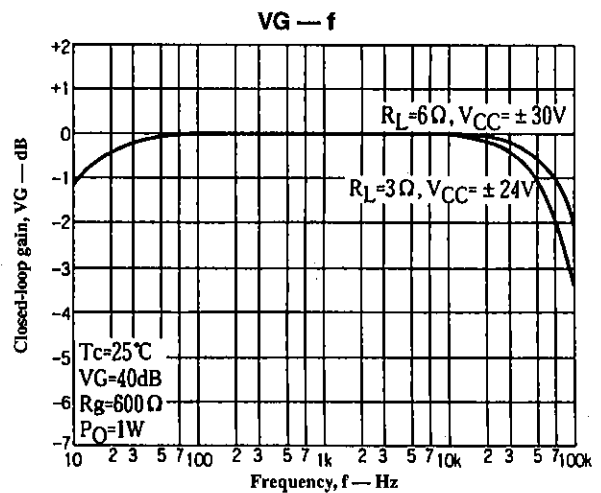
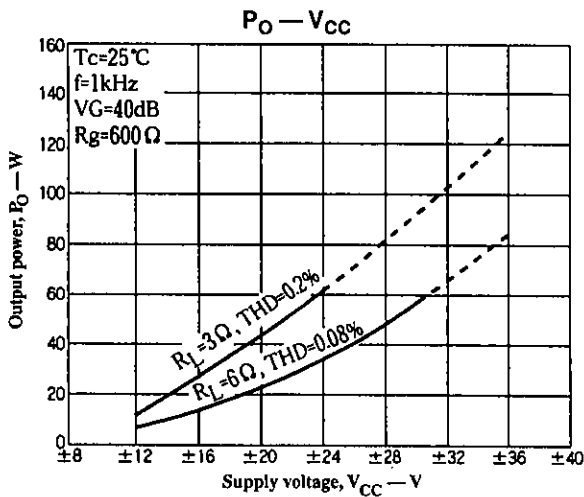
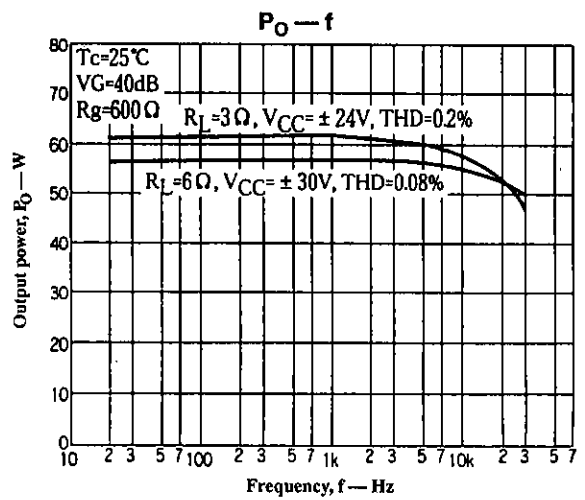
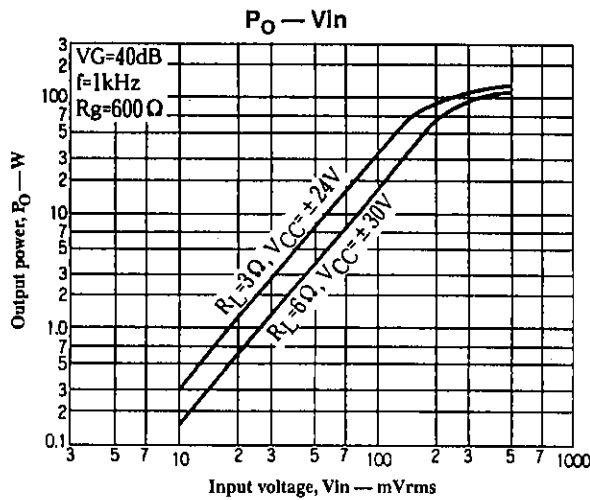
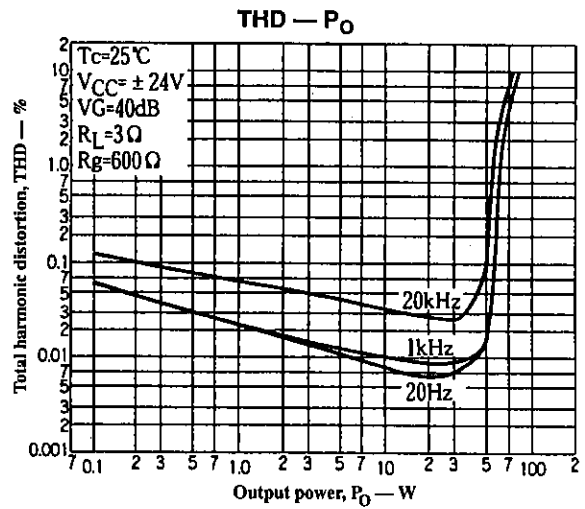
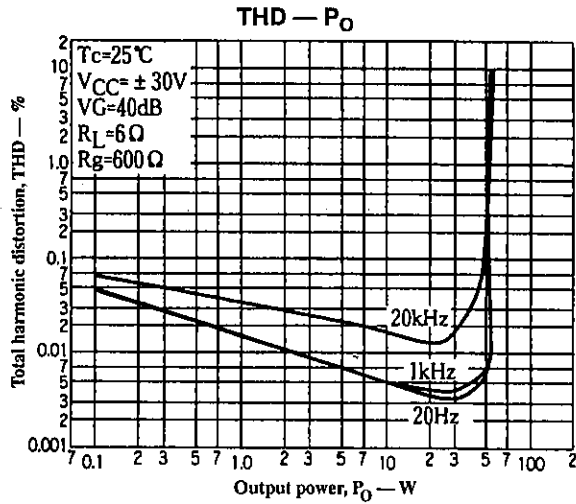
$$\text{From expression (1)': } \theta_{c-a} < (125 - 50)/43 \\ < 1.74$$

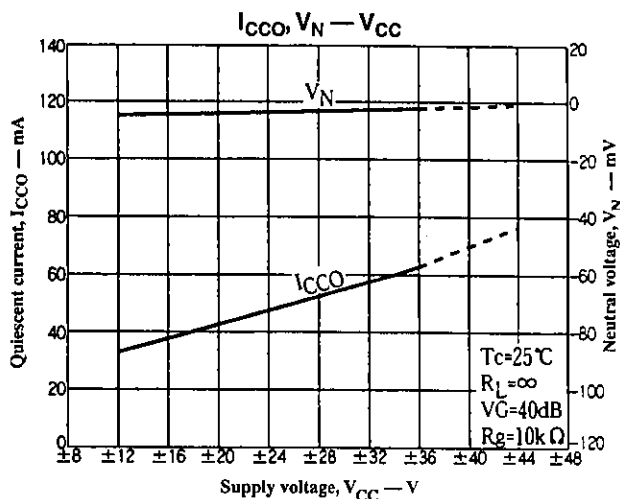
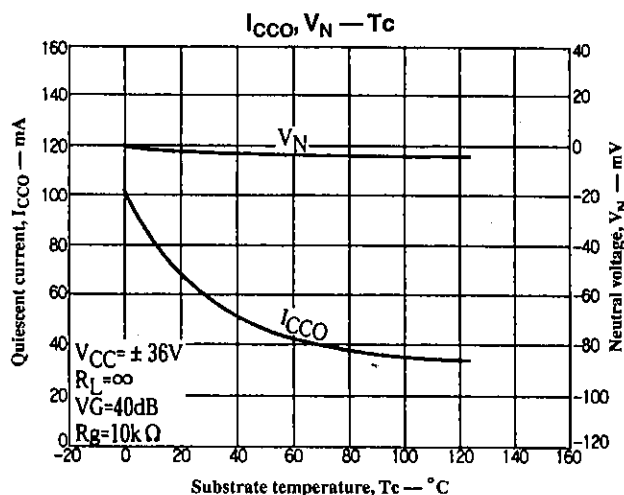
$$\text{From expression (2)': } \theta_{c-a} < (150 - 50)/43 - 1.7/4 \\ < 1.90$$

Therefore, to satisfy both expressions, the required heatsink must have a thermal resistance less than 1.74°C/W.

This heatsink design example is based on a constant-voltage supply, and should be verified within your specific set environment.







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