

## FEATURES

- 35, 45 ns Read Access & R/W Cycle Time
- Unlimited Read/Write Endurance
- Automatic Non-volatile STORE on Power Loss
- Non-Volatile STORE Under Hardware or Software Control
- Automatic RECALL to SRAM on Power Up
- Unlimited RECALL Cycles
- 1 Million STORE Cycles
- 100-Year Non-volatile Data Retention
- Single 3.3V  $\pm$  10% Power Supply
- Commercial and Industrial Temperatures
- 32-Pin 300 mil SOIC and 600 mil PDIP Packages (RoHS-Compliant)

## DESCRIPTION

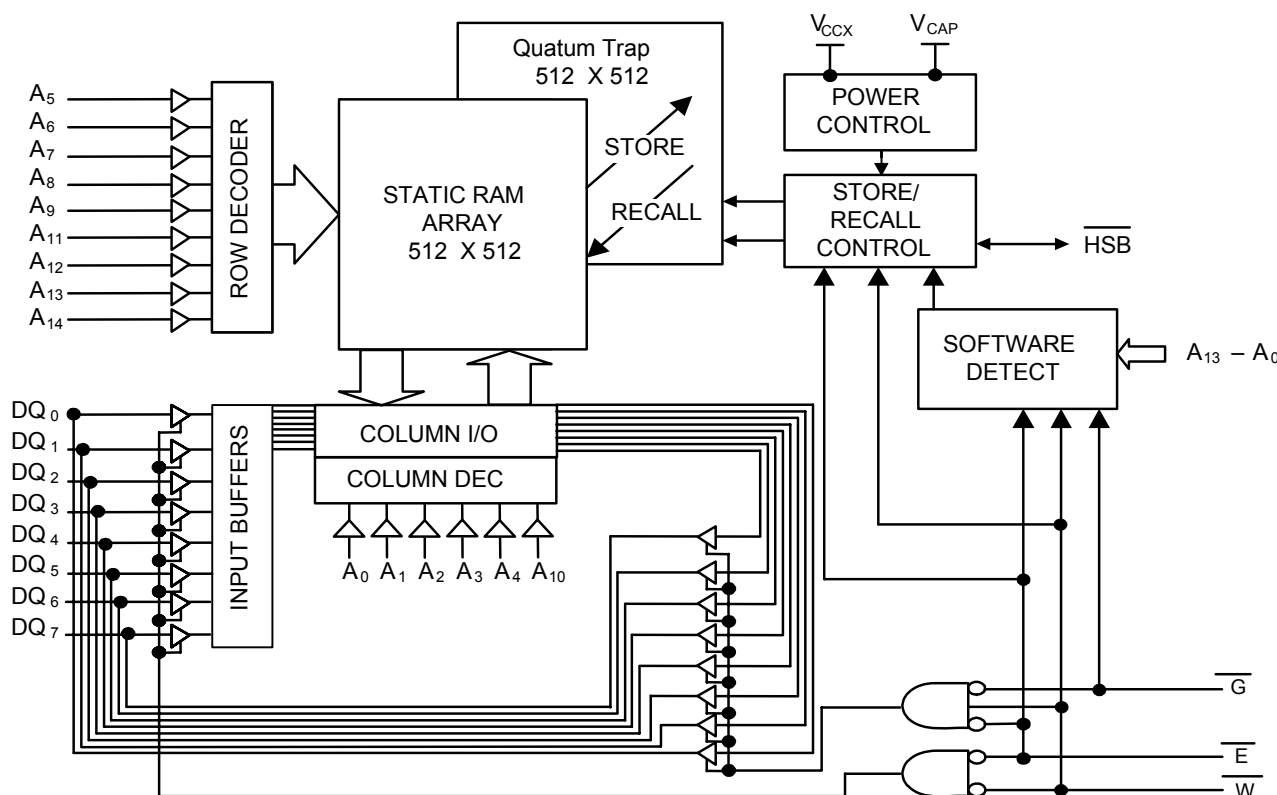
The Simtek STK14C88-3 is a 256Kb fast static RAM with a non-volatile Quantum Trap storage element included with each memory cell.

The SRAM provides the fast access & cycle times, ease of use and unlimited read & write endurance of a normal SRAM.

Data transfers automatically to the non-volatile storage cells when power loss is detected (the STORE operation). On power up, data is automatically restored to the SRAM (the RECALL operation). Both STORE and RECALL operations are also available under software control.

The Simtek nvSRAM is the first monolithic non-volatile memory to offer unlimited writes and reads. It is the highest performance, most reliable non-volatile memory available.

## BLOCK DIAGRAM



|      |    |    |                         |
|------|----|----|-------------------------|
| VCAP | 1  | 32 | VCCX                    |
| A14  | 2  | 31 | $\overline{\text{HSB}}$ |
| A12  | 3  | 30 | $\overline{\text{W}}$   |
| A7   | 4  | 29 | A13                     |
| A6   | 5  | 28 | A8                      |
| A5   | 6  | 27 | A9                      |
| A4   | 7  | 26 | A11                     |
| A3   | 8  | 25 | $\overline{\text{G}}$   |
| NC   | 9  | 24 | NC                      |
| A2   | 10 | 23 | A10                     |
| A1   | 11 | 22 | $\overline{\text{E}}$   |
| A0   | 12 | 21 | DQ7                     |
| DQ0  | 13 | 20 | DQ6                     |
| DQ1  | 14 | 19 | DQ5                     |
| DQ2  | 15 | 18 | DQ4                     |
| VSS  | 16 | 17 | DQ3                     |

**32-Pin SOIC**

**32-Pin PDIP**

## PIN DESCRIPTIONS

| Pin Name                         | I/O          | Description                                                                                                                                                                                                                                            |
|----------------------------------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A <sub>14</sub> -A <sub>0</sub>  | Input        | Address: The 15 address inputs select one of 32,768 bytes in the nvSRAM array                                                                                                                                                                          |
| DQ <sub>7</sub> -DQ <sub>0</sub> | I/O          | Data: Bi-directional 8-bit data bus for accessing the nvSRAM                                                                                                                                                                                           |
| $\overline{\text{E}}$            | Input        | Chip Enable: The active low $\overline{\text{E}}$ input selects the device                                                                                                                                                                             |
| $\overline{\text{W}}$            | Input        | Write Enable: The active low $\overline{\text{W}}$ enables data on the DQ pins to be written to the address location latched by the falling edge of $\overline{\text{E}}$                                                                              |
| $\overline{\text{G}}$            | Input        | Output Enable: The active low $\overline{\text{G}}$ input enables the data output buffers during read cycles. De-asserting $\overline{\text{G}}$ high caused the DQ pins to tri-state.                                                                 |
| V <sub>CCX</sub>                 | Power Supply | Power: 3.3V, $\pm 10\%$                                                                                                                                                                                                                                |
| $\overline{\text{HSB}}$          | I/O          | Hardware Store Busy: When low this output indicates a Store is in progress. When pulled low external to the chip, it will initiate a nonvolatile STORE operation. A weak pull up resistor keeps this pin high if not connected. (Connection Optional). |
| V <sub>CAP</sub>                 | Power Supply | AutoStore Capacitor: Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile storage elements.                                                                                                                               |
| V <sub>SS</sub>                  | Power Supply | Ground                                                                                                                                                                                                                                                 |

## ABSOLUTE MAXIMUM RATINGS<sup>a</sup>

Voltage on Input Relative to Ground . . . . . -0.5V to 7.0V  
 Voltage on Input Relative to  $V_{SS}$  . . . . . -0.6V to ( $V_{CC} + 0.5V$ )  
 Voltage on  $DQ_{0-7}$  or  $\overline{HSB}$  . . . . . -0.5V to ( $V_{CC} + 0.5V$ )  
 Temperature under Bias . . . . . -55°C to 125°C  
 Storage Temperature . . . . . -65°C to 150°C  
 Power Dissipation . . . . . 1W  
 DC Output Current (1 output at a time, 1s duration) . . . . . 15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC CHARACTERISTICS

( $V_{CC} = 3 - 3.6V$ )<sup>e</sup>

| SYMBOL      | PARAMETER                                                           | COMMERCIAL    |               | INDUSTRIAL    |               | UNITS    | NOTES                                                                                           |
|-------------|---------------------------------------------------------------------|---------------|---------------|---------------|---------------|----------|-------------------------------------------------------------------------------------------------|
|             |                                                                     | MIN           | MAX           | MIN           | MAX           |          |                                                                                                 |
| $I_{CC1}^b$ | Average $V_{CC}$ Current                                            |               | 50<br>42      |               | 52<br>44      | mA<br>mA | $t_{AVAV} = 35ns$<br>$t_{AVAV} = 45ns$                                                          |
| $I_{CC2}^c$ | Average $V_{CC}$ Current during <i>STORE</i>                        |               | 3             |               | 3             | mA       | All Inputs Don't Care, $V_{CC} = \max$                                                          |
| $I_{CC3}^b$ | Average $V_{CC}$ Current at $t_{AVAV} = 200ns$<br>5V, 25°C, Typical |               | 9             |               | 9             | mA       | $\overline{W} \geq (V_{CC} - 0.2V)$<br>All Others Cycling, CMOS Levels                          |
| $I_{CC4}^c$ | Average $V_{CAP}$ Current during AutoStore<br>Cycle                 |               | 2             |               | 2             | mA       | All Inputs Don't Care                                                                           |
| $I_{SB1}^d$ | Average $V_{CC}$ Current<br>(Standby, Cycling TTL Input Levels)     |               | 18<br>16      |               | 19<br>17      | mA<br>mA | $t_{AVAV} = 35ns, \overline{E} \geq V_{IH}$<br>$t_{AVAV} = 45ns, \overline{E} \geq V_{IH}$      |
| $I_{SB2}^d$ | $V_{CC}$ Standby Current<br>(Standby, Stable CMOS Input Levels)     |               | 1             |               | 1             | mA       | $\overline{E} \geq (V_{CC} - 0.2V)$<br>All Others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$  |
| $I_{ILK}$   | Input Leakage Current                                               |               | $\pm 1$       |               | $\pm 1$       | $\mu A$  | $V_{CC} = \max$<br>$V_{IN} = V_{SS}$ to $V_{CC}$                                                |
| $I_{OLK}$   | Off-State Output Leakage Current                                    |               | $\pm 1$       |               | $\pm 1$       | $\mu A$  | $V_{CC} = \max$<br>$V_{IN} = V_{SS}$ to $V_{CC}$ , $\overline{E}$ or $\overline{G} \geq V_{IH}$ |
| $V_{IH}$    | Input Logic "1" Voltage                                             | 2.2           | $V_{CC} + .5$ | 2.2           | $V_{CC} + .5$ | V        | All Inputs                                                                                      |
| $V_{IL}$    | Input Logic "0" Voltage                                             | $V_{SS} - .5$ | 0.8           | $V_{SS} - .5$ | 0.8           | V        | All Inputs                                                                                      |
| $V_{OH}$    | Output Logic "1" Voltage                                            | 2.4           |               | 2.4           |               | V        | $I_{OUT} = -4mA$ except $\overline{HSB}$                                                        |
| $V_{OL}$    | Output Logic "0" Voltage                                            |               | 0.4           |               | 0.4           | V        | $I_{OUT} = 8mA$ except $\overline{HSB}$                                                         |
| $V_{BL}$    | Logic "0" Voltage on $\overline{HSB}$ Output                        |               | 0.4           |               | 0.4           | V        | $I_{OUT} = 3mA$                                                                                 |
| $T_A$       | Operating Temperature                                               | 0             | 70            | -40           | 85            | °C       |                                                                                                 |
| $V_{CC}$    | Operating Voltage                                                   | 3.0           | 3.6           | 3.0           | 3.6           | V        | $3.3V \pm 0.3V$                                                                                 |
| $V_{CAP}$   | Storage Capacitor                                                   | 54            | 264           | 54            | 264           | $\mu F$  | 68 to 220 $\mu F \pm 20\%$ , 4.7v Rated                                                         |
| $NV_C$      | Nonvolatile <i>STORE</i> operations                                 | 1,000         |               | 1,000         |               | K        |                                                                                                 |
| $DATA_R$    | Data Retention                                                      | 100           |               | 100           |               | Years    | @55 °C                                                                                          |

Note b:  $I_{CC1}$  and  $I_{CC3}$  are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note c:  $I_{CC2}$  and  $I_{CC4}$  are the average currents required for the duration of the respective *STORE* cycles ( $t_{STORE}$ ).

Note d:  $\overline{E} \geq V_{IH}$  will not produce standby current levels until any nonvolatile cycle in progress has timed out.

Note e:  $V_{CC}$  reference levels throughout this datasheet refer to  $V_{CCX}$  if that is where the power supply connection is made, or  $V_{CAP}$  if  $V_{CCX}$  is connected to ground.

AC TEST CONDITIONS

|                                                |              |
|------------------------------------------------|--------------|
| Input Pulse Levels .....                       | 0V to 3V     |
| Input Rise and Fall Times .....                | ≤ 5ns        |
| Input and Output Timing Reference Levels ..... | 1.5V         |
| Output Load .....                              | See Figure 1 |

CAPACITANCE<sup>f</sup> (T<sub>A</sub> = 25°C, f = 1.0MHz)

| SYMBOL           | PARAMETER          | MAX | UNITS | CONDITIONS   |
|------------------|--------------------|-----|-------|--------------|
| C <sub>IN</sub>  | Input Capacitance  | 5   | pF    | ΔV = 0 to 3V |
| C <sub>OUT</sub> | Output Capacitance | 7   | pF    | ΔV = 0 to 3V |

Note f: These parameters are guaranteed but not tested.

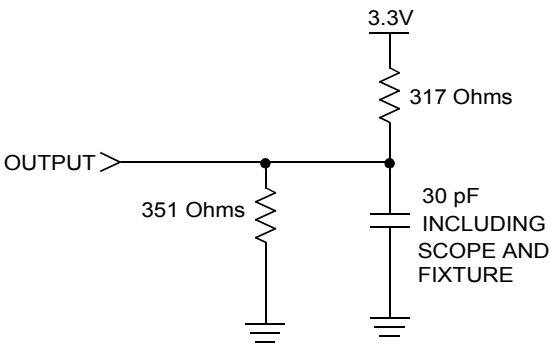


Figure 1. AC Output Loading

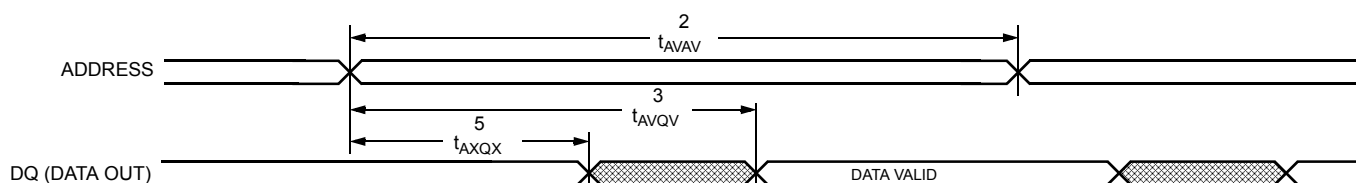
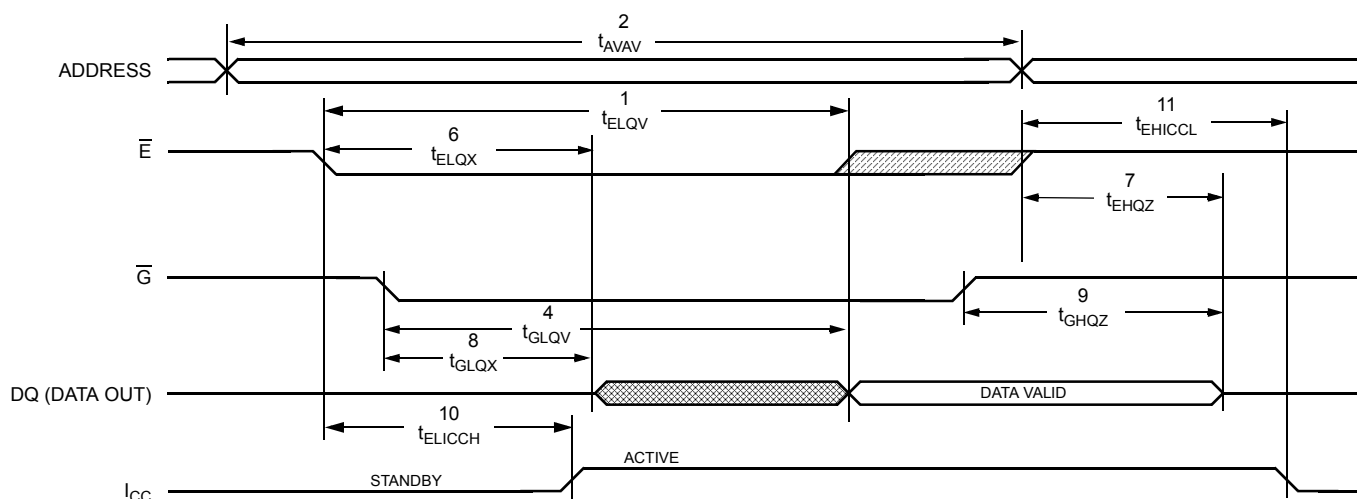
**SRAM READ CYCLES #1 & #2**
 $(V_{CC} = 3V - 3.6V)^e$ 

| NO. | SYMBOLS        |           | PARAMETER                         | STK14C88-3-35 |     | STK14C88-3-45 |     | UNITS |
|-----|----------------|-----------|-----------------------------------|---------------|-----|---------------|-----|-------|
|     | #1, #2         | Alt.      |                                   | MIN           | MAX | MIN           | MAX |       |
| 1   | $t_{ELQV}$     | $t_{ACS}$ | Chip Enable Access Time           |               | 35  |               | 45  | ns    |
| 2   | $t_{AVAV}^g$   | $t_{RC}$  | Read Cycle Time                   | 35            |     | 45            |     | ns    |
| 3   | $t_{AVQV}^h$   | $t_{AA}$  | Address Access Time               |               | 35  |               | 45  | ns    |
| 4   | $t_{GLQV}$     | $t_{OE}$  | Output Enable to Data Valid       |               | 15  |               | 20  | ns    |
| 5   | $t_{AXQX}^h$   | $t_{OH}$  | Output Hold after Address Change  | 5             |     | 5             |     | ns    |
| 6   | $t_{ELQX}$     | $t_{LZ}$  | Chip Enable to Output Active      | 5             |     | 5             |     | ns    |
| 7   | $t_{EHQZ}^i$   | $t_{HZ}$  | Chip Disable to Output Inactive   |               | 13  |               | 15  | ns    |
| 8   | $t_{GLQX}$     | $t_{OLZ}$ | Output Enable to Output Active    | 0             |     | 0             |     | ns    |
| 9   | $t_{GHQZ}^i$   | $t_{OHZ}$ | Output Disable to Output Inactive |               | 13  |               | 15  | ns    |
| 10  | $t_{ELICCH}^f$ | $t_{PA}$  | Chip Enable to Power Active       | 0             |     | 0             |     | ns    |
| 11  | $t_{EHICCL}^f$ | $t_{PS}$  | Chip Disable to Power Standby     |               | 35  |               | 45  | ns    |

Note g:  $\overline{W}$  and  $\overline{HSB}$  must be high during SRAM READ cycles and low during SRAM WRITE cycles.

Note h: /O state assumes  $\overline{E}$  and  $\overline{G} \leq V_{IL}$  and  $\overline{W} \geq V_{IH}$ ; device is continuously selected.

Note i: Measured  $\pm 200mV$  from steady state output voltage.

**SRAM READ CYCLE #1: Address Controlled<sup>g, h</sup>**

**SRAM READ CYCLE #2:  $\overline{E}$  Controlled<sup>g</sup>**


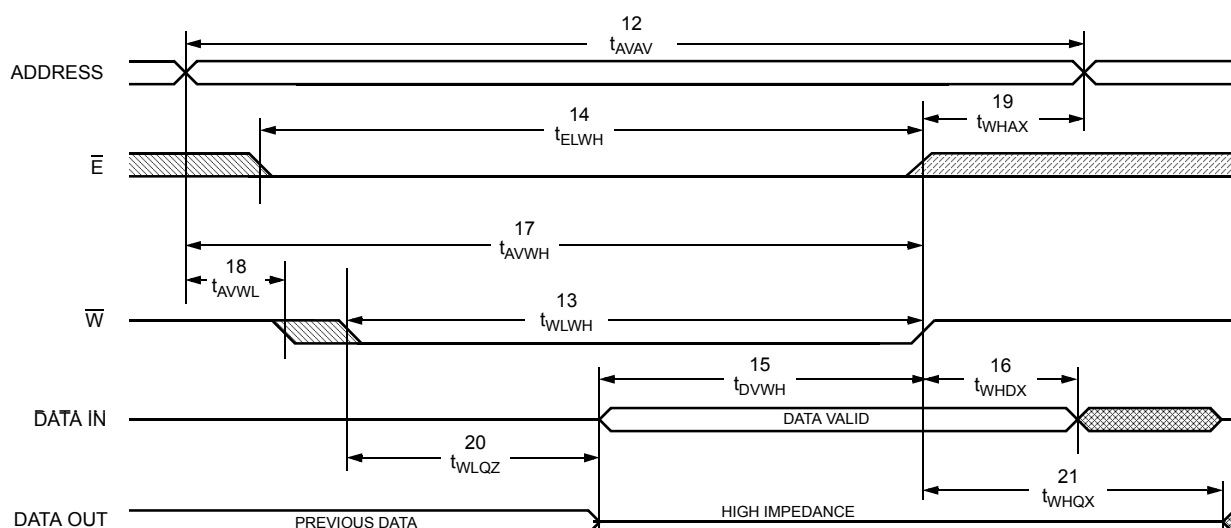
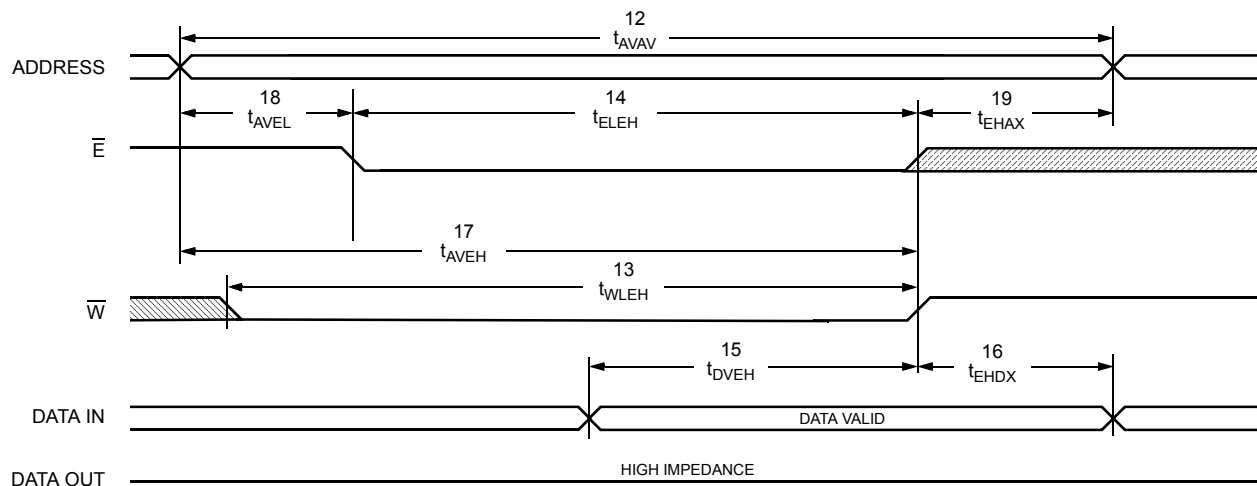
**SRAM WRITE CYCLES #1 & #2**
 $(V_{CC} = 3V - 3.6V)^e$ 

| NO. | SYMBOLS          |            |          | PARAMETER                        | STK14C88-3-35 |     | STK14C88-3-45 |     | UNITS |
|-----|------------------|------------|----------|----------------------------------|---------------|-----|---------------|-----|-------|
|     | #1               | #2         | Alt.     |                                  | MIN           | MAX | MIN           | MAX |       |
| 12  | $t_{AVAV}$       | $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time                 | 35            |     | 45            |     | ns    |
| 13  | $t_{WLWH}$       | $t_{WLEH}$ | $t_{WP}$ | Write Pulse Width                | 25            |     | 30            |     | ns    |
| 14  | $t_{ELWH}$       | $t_{ELEH}$ | $t_{CW}$ | Chip Enable to End of Write      | 25            |     | 30            |     | ns    |
| 15  | $t_{DVWH}$       | $t_{DVEH}$ | $t_{DW}$ | Data Set-up to End of Write      | 12            |     | 15            |     | ns    |
| 16  | $t_{WHDX}$       | $t_{EHDX}$ | $t_{DH}$ | Data Hold after End of Write     | 0             |     | 0             |     | ns    |
| 17  | $t_{AVWH}$       | $t_{AVEH}$ | $t_{AW}$ | Address Set-up to End of Write   | 25            |     | 30            |     | ns    |
| 18  | $t_{AVWL}$       | $t_{AVEL}$ | $t_{AS}$ | Address Set-up to Start of Write | 0             |     | 0             |     | ns    |
| 19  | $t_{WHAX}$       | $t_{EHAX}$ | $t_{WR}$ | Address Hold after End of Write  | 0             |     | 0             |     | ns    |
| 20  | $t_{WLQZ}^{i,j}$ |            | $t_{WZ}$ | Write Enable to Output Disable   |               | 13  |               | 15  | ns    |
| 21  | $t_{WHQX}$       |            | $t_{OW}$ | Output Active after End of Write | 5             |     | 5             |     | ns    |

Note j:  $\overline{W}$  is low when  $\overline{E}$  goes low, the outputs remain in the high-impedance state.

Note k:  $\overline{E}$  or  $\overline{W}$  must be  $\geq V_{IH}$  during address transitions.

Note l: HSB must be high during SRAM WRITE cycles.

**SRAM WRITE CYCLE #1:  $\overline{W}$  Controlled<sup>k, l</sup>**

**SRAM WRITE CYCLE #2:  $\overline{E}$  Controlled<sup>k, l</sup>**


## HARDWARE MODE SELECTION

| $\overline{E}$ | $\overline{W}$ | $\overline{HSB}$ | A <sub>13</sub> - A <sub>0</sub> (hex) | MODE              | I/O           | POWER            | NOTES |
|----------------|----------------|------------------|----------------------------------------|-------------------|---------------|------------------|-------|
| H              | X              | H                | X                                      | Not Selected      | Output High Z | Standby          |       |
| L              | H              | H                | X                                      | Read SRAM         | Output Data   | Active           | t     |
| L              | L              | H                | X                                      | Write SRAM        | Input Data    | Active           |       |
| X              | X              | L                | X                                      | Nonvolatile STORE | Output High Z | I <sub>CC2</sub> | m     |

Note m:  $\overline{HSB}$  STORE operation occurs only if an SRAM WRITE has been done since the last nonvolatile cycle. After the STORE (if any) completes, the part will go into standby mode, inhibiting all operations until  $\overline{HSB}$  rises.

## HARDWARE STORE CYCLE

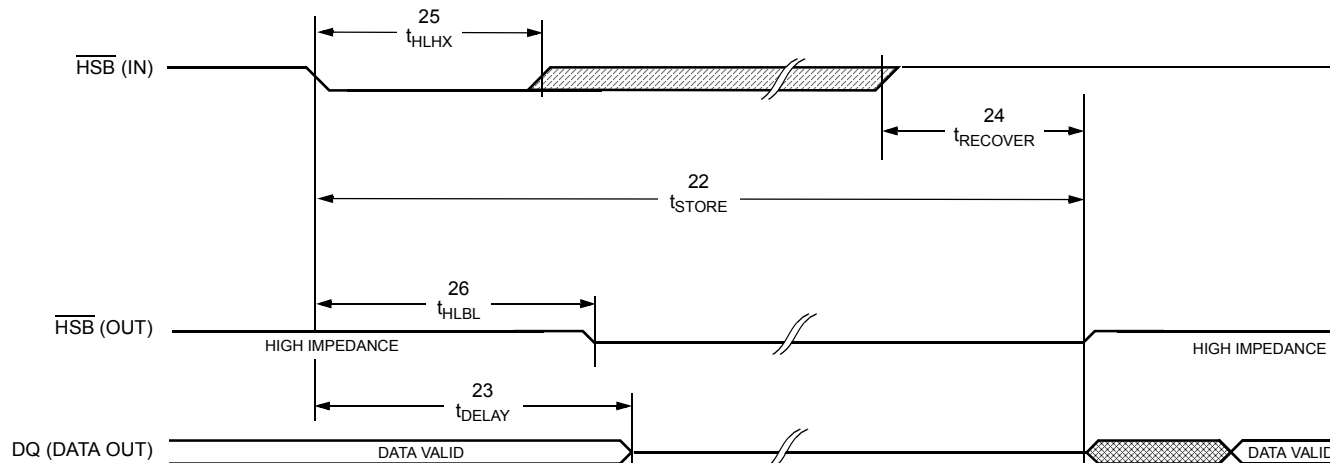
(V<sub>CC</sub> = 3V - 3.6V)<sup>e</sup>

| NO. | SYMBOLS              |                   | PARAMETER                           | STK14C88-3 |     | UNITS | NOTES |
|-----|----------------------|-------------------|-------------------------------------|------------|-----|-------|-------|
|     | Standard             | Alternate         |                                     | MIN        | MAX |       |       |
| 22  | t <sub>STORE</sub>   | t <sub>HLHZ</sub> | STORE Cycle Duration                |            | 10  | ms    | i, n  |
| 23  | t <sub>DELAY</sub>   | t <sub>HLQZ</sub> | Time Allowed to Complete SRAM Cycle | 1          |     | μs    | i, n  |
| 24  | t <sub>RECOVER</sub> | t <sub>HHQX</sub> | Hardware STORE High to Inhibit Off  |            | 700 | ns    | n, o  |
| 25  | t <sub>HLHX</sub>    |                   | Hardware STORE Pulse Width          | 15         |     | ns    |       |
| 26  | t <sub>HLBL</sub>    |                   | Hardware STORE Low to STORE Busy    |            | 300 | ns    |       |

Note n:  $\overline{E}$  and  $\overline{G}$  low and  $\overline{W}$  high for output behavior.

Note o: t<sub>RECOVER</sub> is only applicable after t<sub>STORE</sub> is complete.

## HARDWARE STORE CYCLE



## AutoStore/POWER-UP RECALL

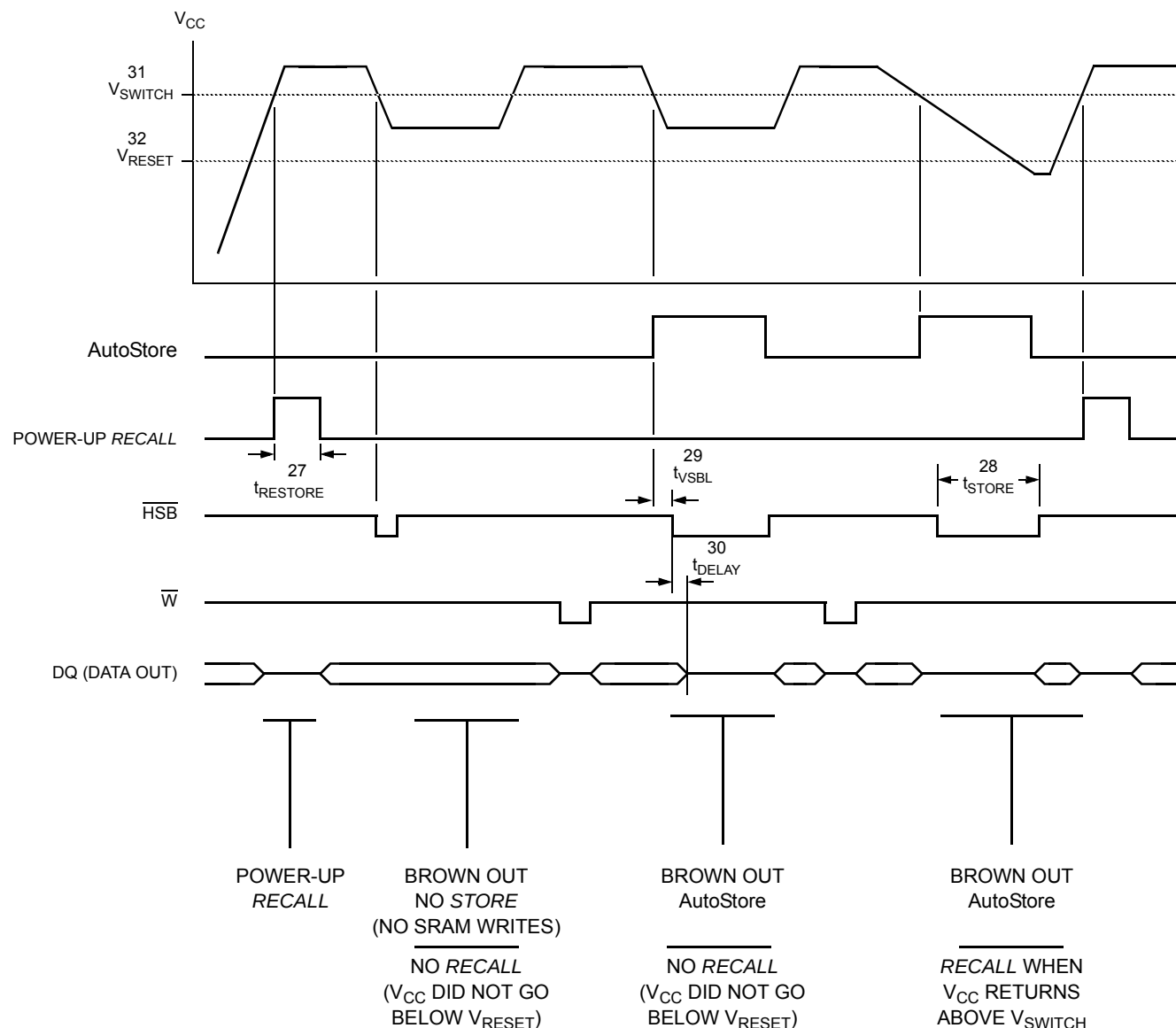
( $V_{CC} = 3V - 3.6V$ )<sup>e</sup>

| NO. | SYMBOLS       |            | PARAMETER                                                    | STK14C88-3 |      | UNITS   | NOTES |
|-----|---------------|------------|--------------------------------------------------------------|------------|------|---------|-------|
|     | Standard      | Alternate  |                                                              | MIN        | MAX  |         |       |
| 27  | $t_{RESTORE}$ |            | Power-up <i>RECALL</i> Duration                              |            | 550  | $\mu s$ | p     |
| 28  | $t_{STORE}$   | $t_{HLHZ}$ | <i>STORE</i> Cycle Duration                                  |            | 10   | ms      | n, q  |
| 29  | $t_{VSBL}$    |            | Low Voltage Trigger ( $V_{SWITCH}$ ) to $\overline{HSB}$ Low |            | 300  | ns      | l     |
| 30  | $t_{DELAY}$   | $t_{BLQZ}$ | Time Allowed to Complete SRAM Cycle                          | 1          |      | $\mu s$ | n     |
| 31  | $V_{SWITCH}$  |            | Low Voltage Trigger Level                                    | 2.7        | 2.95 | V       |       |
| 32  | $V_{RESET}$   |            | Low Voltage Reset Level                                      |            | 2.4  | V       |       |

Note p:  $t_{RESTORE}$  starts from the time  $V_{CC}$  rises above  $V_{SWITCH}$ .

Note q:  $\overline{HSB}$  is asserted low for  $1\mu s$  when  $V_{CAP}$  drops through  $V_{SWITCH}$ . If an SRAM WRITE has not taken place since the last nonvolatile cycle,  $\overline{HSB}$  will be released and no *STORE* will take place.

## AutoStore/POWER-UP RECALL



**SOFTWARE-CONTROLLED *STORE/RECALL* CYCLE<sup>v</sup>** ( $V_{CC} = 3V - 3.6V$ )<sup>e</sup>

Note v: The six consecutive addresses must be in the order listed in the Hardware Mode Selection Table: (0E38, 31C7, 03E0, 3C1F, 303F, 0FC0) for a *STORE* cycle or (0E38, 31C7, 03E0, 3C1F, 303F, 0C63) for a *RECALL* cycle.  $\overline{W}$  must be high during all six consecutive cycles.

### SOFTWARE STORE/RECALL CYCLE: $\bar{E}$ CONTROLLED<sup>v</sup>



## nvSRAM OPERATION

The STK14C88-3 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to nonvolatile elements (the *STORE* operation) or from nonvolatile elements to SRAM (the *RECALL* operation). In this mode SRAM functions are disabled.

### NOISE CONSIDERATIONS

The STK14C88-3 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1 $\mu$ F connected between  $V_{CAP}$  and  $V_{SS}$ , using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

### SRAM READ

The STK14C88-3 performs a *READ* cycle whenever  $\overline{E}$  and  $\overline{G}$  are low and  $\overline{W}$  and  $\overline{HSB}$  are high. The address specified on pins  $A_{0-14}$  determines which of the 32,768 data byte will be accessed. When the *READ* is initiated by an address transition, the outputs will be valid after a delay of  $t_{AVQV}$  (*READ* cycle #1). If the *READ* is initiated by  $\overline{E}$  or  $\overline{G}$ , the outputs will be valid at  $t_{ELQV}$  or at  $t_{GLQV}$ , whichever is later (*READ* cycle #2). The data outputs will repeatedly respond to address changes within the  $t_{AVQV}$  access time without the need for transitions on any control input pins, and will remain valid until another address change or until  $\overline{E}$  or  $\overline{G}$  is brought high, or  $\overline{W}$  or  $\overline{HSB}$  is brought low.

### SRAM WRITE

A *WRITE* cycle is performed whenever  $\overline{E}$  and  $\overline{W}$  are low and  $\overline{HSB}$  is high. The address inputs must be stable prior to entering the *WRITE* cycle and must remain stable until either  $\overline{E}$  or  $\overline{W}$  goes high at the end of the cycle. The data on the common I/O pins  $DQ_{0-7}$  will be written into the memory if it is valid  $t_{DVWH}$  before the end of a  $\overline{W}$  controlled *WRITE* or  $t_{DVEH}$  before the end of an  $\overline{E}$  controlled *WRITE*.

It is recommended that  $\overline{G}$  be kept high during the entire *WRITE* cycle to avoid data bus contention on common I/O lines. If  $\overline{G}$  is left low, internal circuitry will turn off the output buffers  $t_{WLQZ}$  after  $\overline{W}$  goes low.

### POWER-UP RECALL

During power up, or after any low-power condition ( $V_{CAP} < V_{RESET}$ ), an internal *RECALL* request will be latched. When  $V_{CAP}$  once again exceeds the sense voltage of  $V_{SWITCH}$ , a *RECALL* cycle will automatically be initiated and will take  $t_{RESTORE}$  to complete.

If the STK14C88-3 is in a *WRITE* state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected either between  $\overline{W}$  and system  $V_{CC}$  or between  $\overline{E}$  and system  $V_{CC}$ .

### SOFTWARE NONVOLATILE STORE

The STK14C88-3 software *STORE* cycle is initiated by executing sequential  $\overline{E}$  controlled *READ* cycles from six specific address locations. During the *STORE* cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of *READ*s from specific addresses is used for *STORE* initiation, it is important that no other *READ* or *WRITE* accesses intervene in the sequence, or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To initiate the software *STORE* cycle, the following *READ* sequence must be performed:

- |                 |            |                             |
|-----------------|------------|-----------------------------|
| 1. Read address | 0E38 (hex) | Valid <i>READ</i>           |
| 2. Read address | 31C7 (hex) | Valid <i>READ</i>           |
| 3. Read address | 03E0 (hex) | Valid <i>READ</i>           |
| 4. Read address | 3C1F (hex) | Valid <i>READ</i>           |
| 5. Read address | 303F (hex) | Valid <i>READ</i>           |
| 6. Read address | 0FC0 (hex) | Initiate <i>STORE</i> cycle |

The software sequence must be clocked with  $\overline{E}$  controlled *READ*s.

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that *READ* cycles and not *WRITE* cycles be used in the sequence, although it is not necessary that  $\overline{G}$  be low for the sequence to be valid. After the  $t_{STORE}$  cycle time has been fulfilled, the SRAM will again be activated for *READ* and *WRITE* operation.

## SOFTWARE NONVOLATILE RECALL

A software *RECALL* cycle is initiated with a sequence of READ operations in a manner similar to the software *STORE* initiation. To initiate the *RECALL* cycle, the following sequence of  $\overline{E}$  controlled READ operations must be performed:

|                 |            |                              |
|-----------------|------------|------------------------------|
| 1. Read address | 0E38 (hex) | Valid READ                   |
| 2. Read address | 31C7 (hex) | Valid READ                   |
| 3. Read address | 03E0 (hex) | Valid READ                   |
| 4. Read address | 3C1F (hex) | Valid READ                   |
| 5. Read address | 303F (hex) | Valid READ                   |
| 6. Read address | 0C63 (hex) | Initiate <i>RECALL</i> cycle |

Internally, *RECALL* is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the  $t_{\text{RECALL}}$  cycle time the SRAM will once again be ready for READ and WRITE operations. The *RECALL* operation in no way alters the data in the nonvolatile elements. The nonvolatile data can be recalled an unlimited number of times.

## AutoStore OPERATION

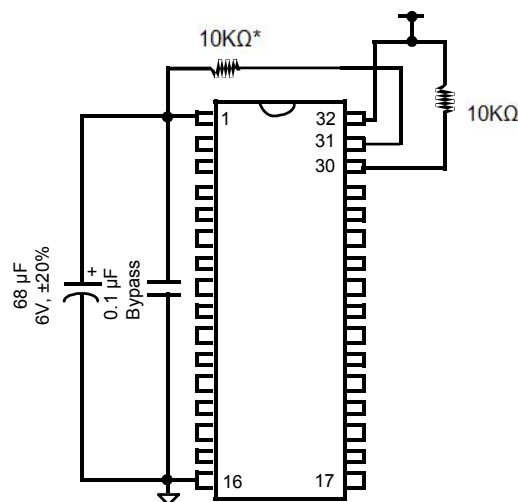
The STK14C88-3 can be powered in one of three modes.

During normal AutoStore operation, the STK14C88-3 will draw current from  $V_{\text{CCX}}$  to charge a capacitor connected to the  $V_{\text{CAP}}$  pin. This stored charge will be used by the chip to perform a single *STORE* operation. After power up, when the voltage on the  $V_{\text{CAP}}$  pin drops below  $V_{\text{SWITCH}}$ , the part will automatically disconnect the  $V_{\text{CAP}}$  pin from  $V_{\text{CCX}}$  and initiate a *STORE* operation.

Figure 2 shows the proper connection of capacitors for automatic store operation. A charge storage capacitor having a capacity of between 68 $\mu\text{F}$  and 220 $\mu\text{F}$  ( $\pm 20\%$ ) rated at 4.7V should be provided.

In order to prevent unneeded *STORE* operations, automatic *STORES* as well as those initiated by externally driving  $\overline{\text{HSB}}$  low will be ignored unless at least one WRITE operation has taken place since the most recent *STORE* or *RECALL* cycle. Software-initiated *STORE* cycles are performed regardless of whether a WRITE operation has taken place.

If the power supply drops faster than 20  $\mu\text{s/volt}$  before  $V_{\text{CCX}}$  reaches  $V_{\text{SWITCH}}$ , then a 1 ohm resistor should be inserted between  $V_{\text{CCX}}$  and the system supply to avoid momentary excess of current between  $V_{\text{CCX}}$  and  $V_{\text{CAP}}$ .



**Figure 2: AutoStore Mode**

\*If  $\overline{\text{HSB}}$  is not used, it should be left unconnected.

## HSB OPERATION

The STK14C88-3 provides the  $\overline{\text{HSB}}$  pin for controlling and acknowledging the *STORE* operations. The  $\overline{\text{HSB}}$  pin can be used to request a hardware *STORE* cycle. When the  $\overline{\text{HSB}}$  pin is driven low, the STK14C88-3 will conditionally initiate a *STORE* operation after  $t_{\text{DELAY}}$ ; an actual *STORE* cycle will only begin if a WRITE to the SRAM took place since the last *STORE* or *RECALL* cycle. The  $\overline{\text{HSB}}$  pin also acts as an open drain driver that is internally driven low to indicate a busy condition while the *STORE* (initiated by any means) is in progress. Pull up this pin with an external 10K ohm resistor to  $V_{\text{CAP}}$  if  $\overline{\text{HSB}}$  is used as a driver.

SRAM READ and WRITE operations that are in progress when  $\overline{\text{HSB}}$  is driven low by any means are given time to complete before the *STORE* operation is initiated. After  $\overline{\text{HSB}}$  goes low, the STK14C88-3 will continue SRAM operations for  $t_{\text{DELAY}}$ . During  $t_{\text{DELAY}}$ , multiple SRAM READ operations may take place. If a WRITE is in progress when  $\overline{\text{HSB}}$  is pulled low it will be allowed a time,  $t_{\text{DELAY}}$ , to complete. However, any SRAM WRITE cycles requested after  $\overline{\text{HSB}}$  goes low will be inhibited until  $\overline{\text{HSB}}$  returns high.

The  $\overline{\text{HSB}}$  pin can be used to synchronize multiple STK14C88-3s while using a single larger capacitor. To operate in this mode the  $\overline{\text{HSB}}$  pin should be connected together to the  $\overline{\text{HSB}}$  pins from the other STK14C88-3s. An external pull-up resistor to +3.3V is required since  $\overline{\text{HSB}}$  acts as an open drain pull-down. The  $V_{\text{CAP}}$  pins from the other STK14C88-3

parts can be tied together and share a single capacitor. The capacitor size must be scaled by the number of devices connected to it. When any one of the STK14C88-3s detects a power loss and asserts  $\overline{\text{HSB}}$ , the common  $\overline{\text{HSB}}$  pin will cause all parts to request a *STORE* cycle (a *STORE* will take place in those STK14C88-3s that have been written since the last nonvolatile cycle).

During any *STORE* operation, regardless of how it was initiated, the STK14C88-3 will continue to drive the  $\overline{\text{HSB}}$  pin low, releasing it only when the *STORE* is complete. Upon completion of the *STORE* operation the STK14C88-3 will remain disabled until the  $\overline{\text{HSB}}$  pin returns high.

If  $\overline{\text{HSB}}$  is not used, it should be left unconnected.

## PREVENTING STORES

The *STORE* function can be disabled on the fly by holding  $\overline{\text{HSB}}$  high with a driver capable of sourcing 30mA at a  $V_{\text{OH}}$  of at least 2.2V, as it will have to overpower the internal pull-down device that drives  $\overline{\text{HSB}}$  low for 20 $\mu\text{s}$  at the onset of a *STORE*. When the STK14C88-3 is connected for AutoStore operation (system  $V_{\text{CC}}$  connected to  $V_{\text{CCX}}$  and a 68 $\mu\text{F}$  capacitor on  $V_{\text{CAP}}$ ) and  $V_{\text{CC}}$  crosses  $V_{\text{SWITCH}}$  on the way down, the STK14C88-3 will attempt to pull  $\overline{\text{HSB}}$  low; if  $\overline{\text{HSB}}$  doesn't actually get below  $V_{\text{IL}}$ , the part will stop trying to pull  $\overline{\text{HSB}}$  low and abort the *STORE* attempt.

## HARDWARE PROTECT

The STK14C88-3 offers hardware protection against inadvertent *STORE* operation and SRAM WRITES during low-voltage conditions. When  $V_{\text{CAP}} < V_{\text{SWITCH}}$ , all externally initiated *STORE* operations and SRAM WRITES will be inhibited.

## LOW AVERAGE ACTIVE POWER

The STK14C88-3 draws significantly less current when it is cycled at times longer than 50ns. Figure 5 shows the relationship between  $I_{\text{CC}}$  and READ cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range,  $V_{\text{CC}} = 3.6\text{V}$ , 100% duty cycle on chip enable). Figure 6 shows the same relationship for WRITE cycles.

If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK14C88-3 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READs to WRITES; 5) the operating temperature; 6) the  $V_{\text{CC}}$  level; and 7) I/O loading.

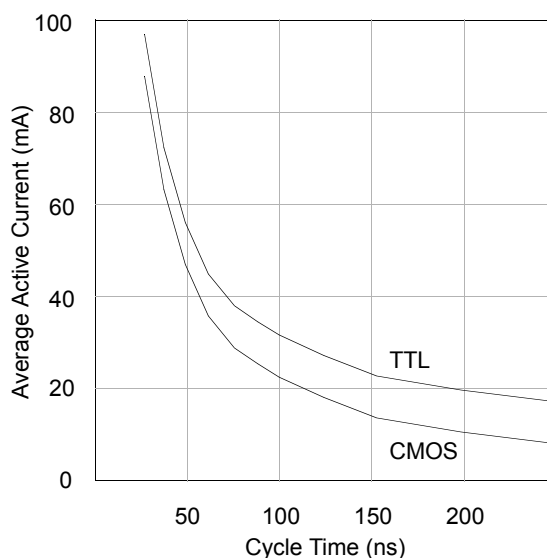


Figure 5:  $I_{\text{CC}}$  (max) Reads

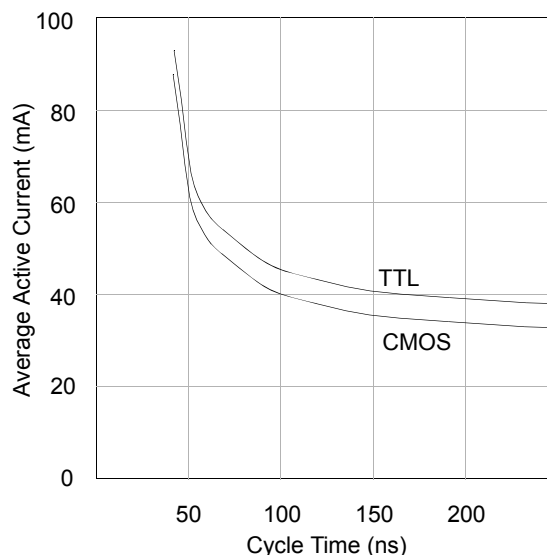
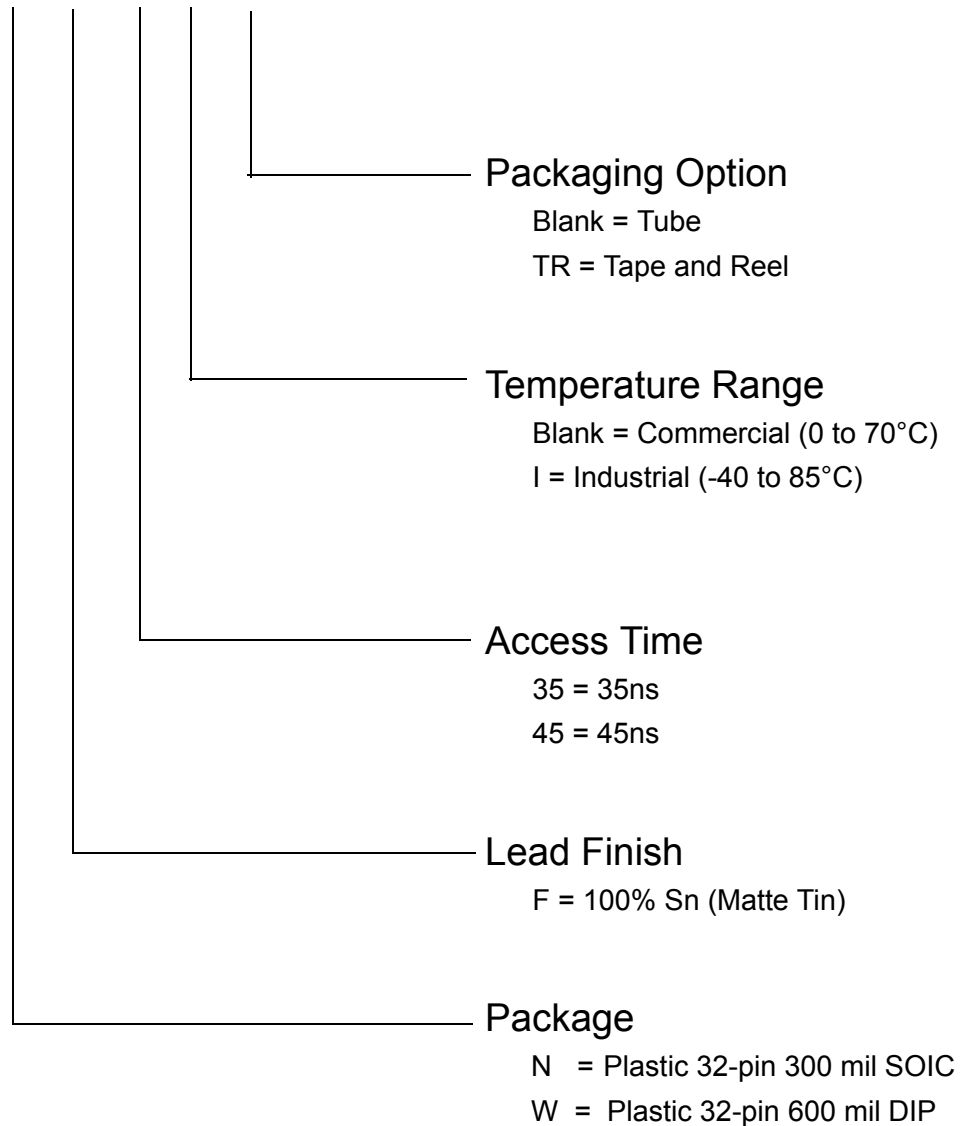


Figure 6:  $I_{\text{CC}}$  (max) Writes

**Commercial and Industrial Ordering Information**

**STK14C88-3 N F 45 I TR**

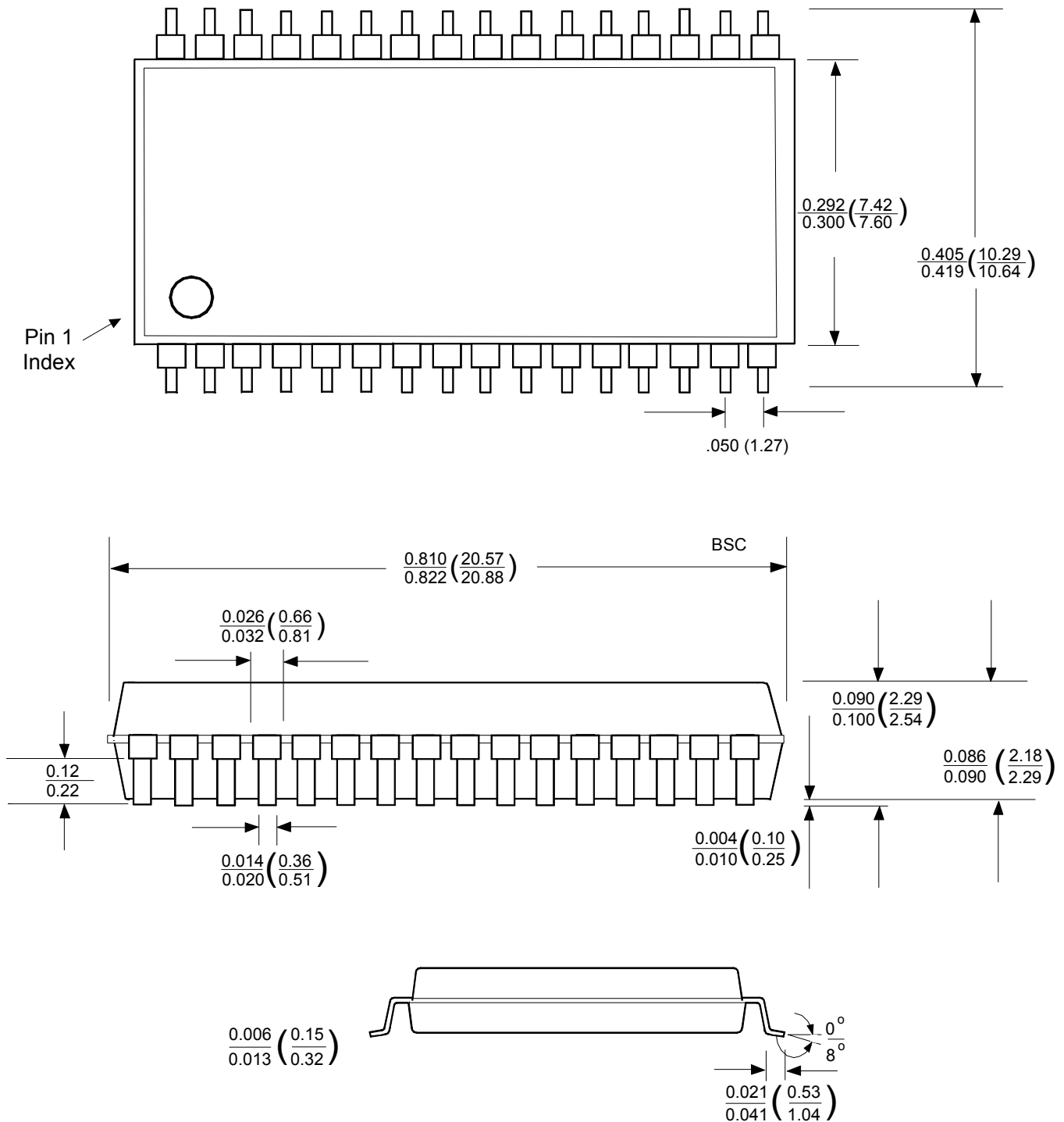


## ORDERING INFORMATION

| Part Number       | Description                            | Temperature |
|-------------------|----------------------------------------|-------------|
| STK14C88-3WF35    | 3.3V 32Kx8 AutoStore nvSRAM PDIP32-600 | Commercial  |
| STK14C88-3WF45    | 3.3V 32Kx8 AutoStore nvSRAM PDIP32-600 | Commercial  |
| STK14C88-3NF35    | 3.3V 32Kx8 AutoStore nvSRAM SOP32-300  | Commercial  |
| STK14C88-3NF45    | 3.3V 32Kx8 AutoStore nvSRAM SOP32-300  | Commercial  |
| STK14C88-3NF35TR  | 3.3V 32Kx8 AutoStore nvSRAM SOP32-300  | Commercial  |
| STK14C88-3NF45TR  | 3.3V 32Kx8 AutoStore nvSRAM SOP32-300  | Commercial  |
| STK14C88-3WF35I   | 3.3V 32Kx8 AutoStore nvSRAM PDIP32-600 | Industrial  |
| STK14C88-3WF45I   | 3.3V 32Kx8 AutoStore nvSRAM PDIP32-600 | Industrial  |
| STK14C88-3NF35I   | 3.3V 32Kx8 AutoStore nvSRAM SOP32-300  | Industrial  |
| STK14C88-3NF45I   | 3.3V 32Kx8 AutoStore nvSRAM SOP32-300  | Industrial  |
| STK14C88-3NF35ITR | 3.3V 32Kx8 AutoStore nvSRAM SOP32-300  | Industrial  |
| STK14C88-3NF45ITR | 3.3V 32Kx8 AutoStore nvSRAM SOP32-300  | Industrial  |

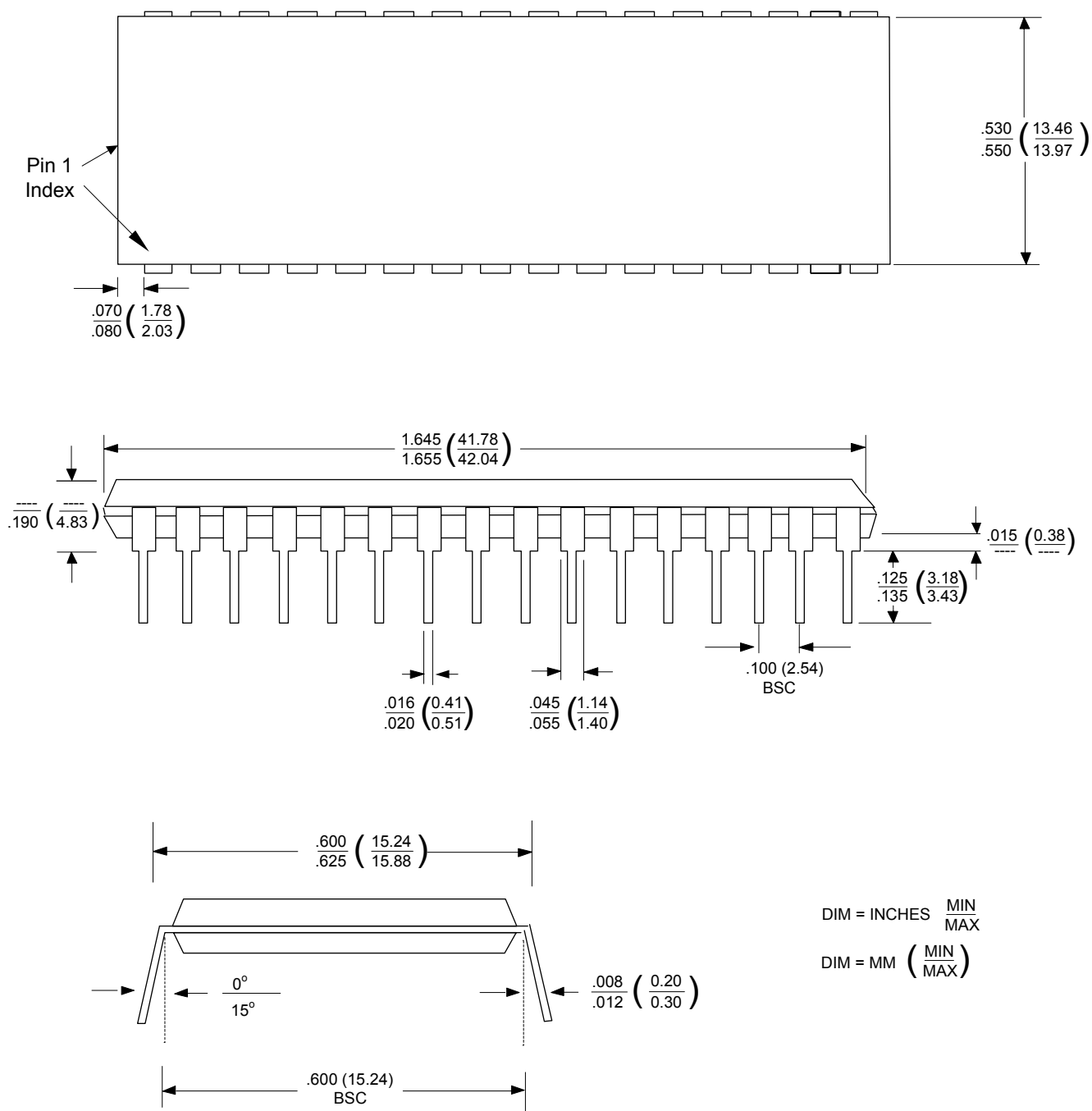
# Package Diagrams

## 32-pin 300 mil SOIC Gull Wing



DIM = INCHES  $\frac{\text{MIN}}{\text{MAX}}$   
 DIM = mm  $\left( \frac{\text{MIN}}{\text{MAX}} \right)$

## 32-pin 600 mil PDIP



**Document Revision History**

| Revision | Date           | Summary                                                                                                                                                                     |
|----------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0.0      | January 2003   | Added 35 nsec device; added HSB operation; current limiting resistor added to Vccx for extreme power-off slew rate                                                          |
| 0.1      | February 2003  | Added 48 SSOP package                                                                                                                                                       |
| 0.2      | September 2003 | Added lead-free lead finish                                                                                                                                                 |
| 0.3      | November 2003  | Modified pin assignments on 48 SSOP package                                                                                                                                 |
| 0.4      | January 2006   | Removed 48 pin SSOP package.<br>Removed 55 ns product offering.<br>Added previously unspecified NV <sub>C</sub> and DATA <sub>R</sub> specifications to DC Characteristics. |
| 0.5      | March 2006     | Removed Leaded Lead Finish                                                                                                                                                  |
| 0.6      | February 2007  | Add Tape Reel Ordering Options<br>Add Product Ordering Code Listing<br>Add Package Drawings<br>Reformat Entire Document                                                     |

SIMTEK STK14C88-3 Datasheet, February 2007

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