AN2713
Application note

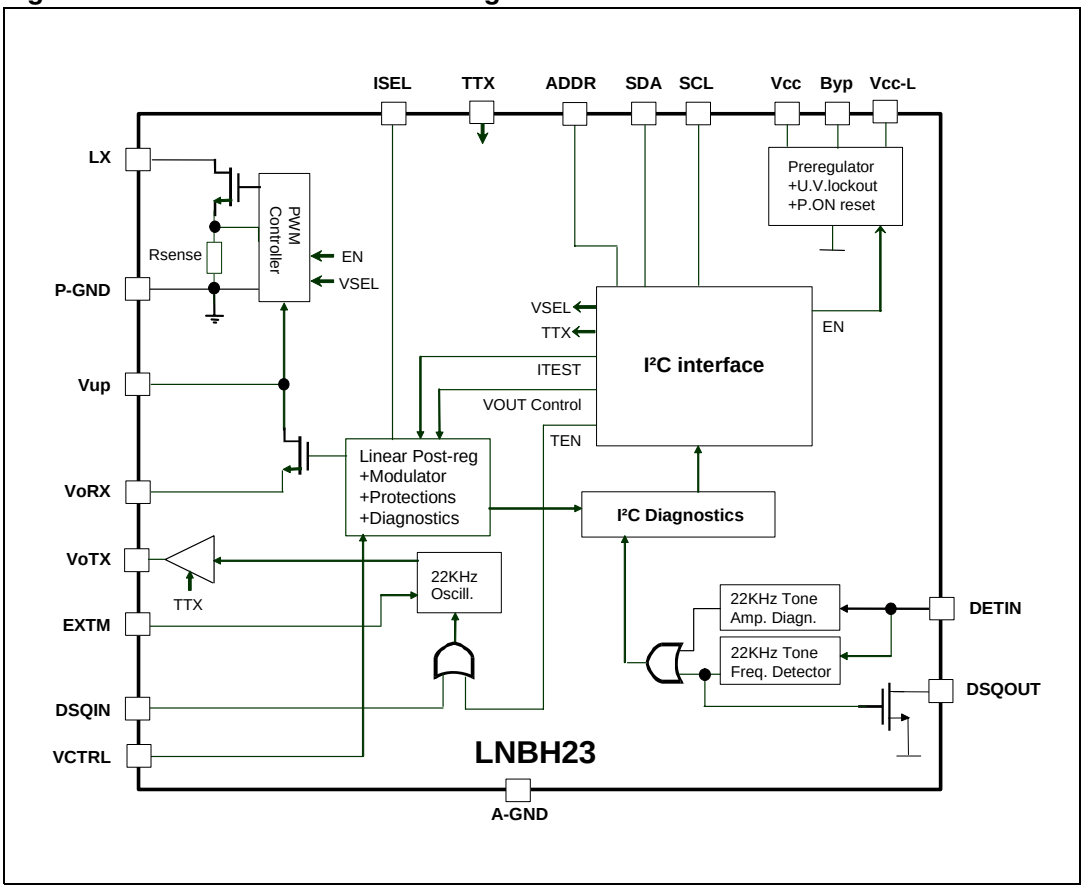
LNB power supply based on the LNBH23 supply and control IC with step-up and I²C interface

Introduction

This application note is intended to provide additional information and suggestions for the correct use of the LNBH23 device. All waveforms shown are based on the demonstration board (order code STEVAL-CBL003V1) described in *Section 5*.

The LNBH23 is an integrated solution for supplying/interfacing satellite LNB modules. It provides good performance in a simply and cheaply way, with minimum external components necessary. It includes all functions needed for LNB supply and interfacing, in accordance with international standards. Moreover, it includes an I^2C bus interface and, thanks to a fully integrated step-up DC-DC converter, it functions with a single input voltage supply ranging from 8 V to 15 V.

Figure 1. LNBH23 internal block diagram



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1 Block diagram description

The internal blocks of the LNBH23 are described in the paragraphs that follow.

1.1 Step-up controller

The LNBH23 features a built-in step-up DC-DC converter that, from a single supply source ranging from 8 V to 15 V, generates the voltages that allow the linear post-regulator to work with minimum power dissipation. The external components of the DC-DC converter are connected to the Lx and VUP pins (see *Figure 5*). No external power MOSFET is needed.

1.2 Pre-regulator block

This block includes a voltage reference connected to the BYP pin, an undervoltage lockout circuit, intended to disable the whole circuit when the supplied Vcc drops below a fixed threshold (6.7 V typ) and a power-on reset that sets all the I^2C registers to zero when the Vcc is turned on and rises from zero above the on threshold (7.3 V typ).

1.3 I^2C interface and diagnostics

The main functions of the device are controlled via I^2C bus by writing 5 bits on the system register (SR bits in write mode). In the same register there are 5 bits that can be read back (SR bits in read mode) and provide 5 diagnostic functions.

Five bits report the diagnostic status of five internal monitoring functions:

- VMON: output voltage diagnostic. If the output voltage level is below the guaranteed limit (refer to the device datasheet) the VMON I^2C bit is set to "1".
- TMON: 22 kHz tone diagnostic. If the 22 kHz tone amplitude and/or the tone frequency is outside of the guaranteed limits (refer to the device datasheet.), the TMON I^2C bit is set to "1".
- IMON: minimum output current diagnostic to detect if no LNB is connected on the bus or a cable not connected to the IRD. The LNBH23 is provided with a minimum output current flag by the IMON I^2C bit in read mode, which is set to "1" if the output current is lower than 12 mA (typ) with ITEST=1 and 6 mA with ITEST=0.
- OTF: overtemperature flag. If overheating occurs (junction temperature exceeds 150 °C), the OTF I^2C bit is set to "1".
- OLF: overload flag. If the output current required exceeds the current limit threshold or a short-circuit occurs, the OLF I^2C bit is set to "1".

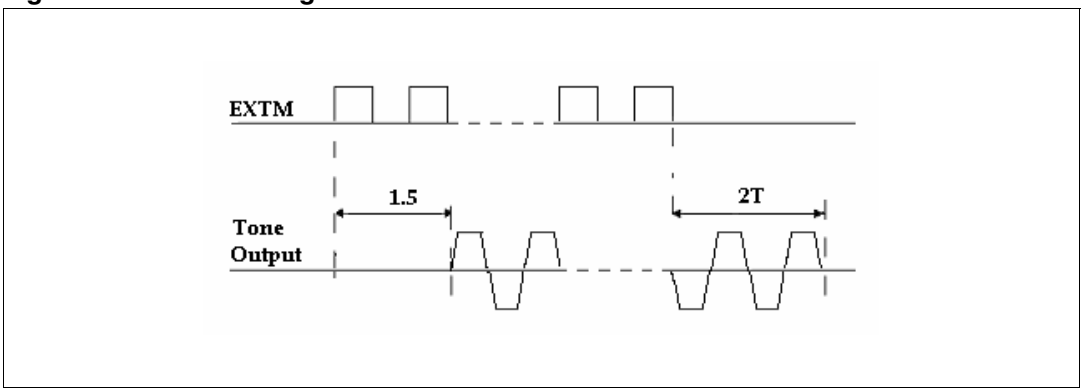
Moreover, three bits will report the last output voltage register status (EN, VSEL, LLC) received by the IC. The LNBH23 I^2C interface address can be selected among two different addresses by setting the voltage level of the dedicated ADDR pin.

1.4 22 kHz oscillator and EXTM function

The internal 22 kHz tone generator is factory-trimmed in accordance with current standards and can be controlled by the DSQIN pin (TTL-compatible), which allows immediate DiSEqC™ data encoding. The rising and falling edges are kept within the 5 µs to 15 µs range, 8 µs (typ) for 22 kHz. The duty cycle is 50% (typ), and modulates the DC output with a 0.650 Vpp (typ) amplitude as well as the DSQIN pin.

The EXTM is a logic input to allow the activation of the 22 kHz tone output, on the V_{oTx} pin, by using the device's integrated tone generator. If the EXTM pin is used, the internal 22 kHz generator must be kept ON (TTX pin or TTX bit set HIGH). When a TTL-compatible 22 kHz signal is applied (for example, a 22 kHz square wave from the demodulator), the EXTM internal circuit detects the 22 kHz TTL signal code and activates the internal 22 kHz tone on the V_{oTx} output. The 22 kHz tone on the output is activated after a delay from the TTL signal presence on the EXTM pin. The tone output starts with about a 1.5 T delay after the 1st cycle of the TTL signal and stops after about a 2 T delay after the TTL signal on the EXTM has expired (see *Figure 2* below). The tone output can also be activated via the DSQIN pin. It starts with a 1.5 T ± 25 µs maximum delay and stops after 2 T ± 25 µs maximum delay with 20~24 kHz tolerance for EXTM input pin.

Figure 2. EXTM timing control



1.5 Tone detector

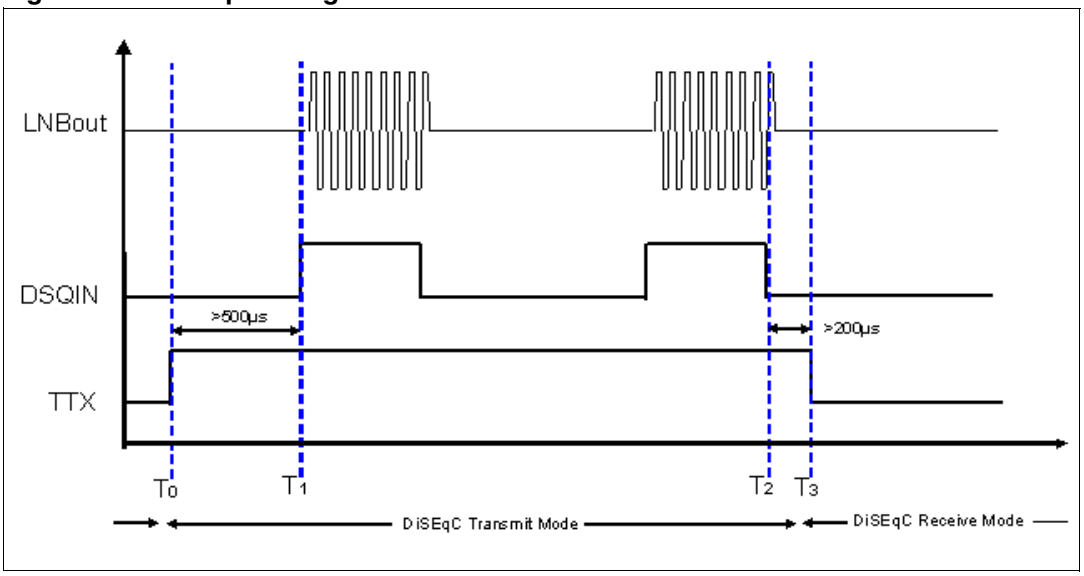
This block provides a complete circuit to decode the 22 kHz burst code present on the DETIN pin in a digital signal by the DSQOUT pin where an open drain MOSFET is connected. The tone is also monitored and a dedicated bit (TMON) provides the diagnostic function described in the *Section 1.3*.

1.6 DiSEqC communication

The following steps must be taken to ensure the correct implementation of the DiSEqC 2.0 communication:

- T0: before starting the DiSEqC transmission, the TTX function must be activated (through the TTX pin or TTX I^2C bit).
- T1: after a 500 µs minimum, the IC is ready to receive the DiSEqC code through the DSQIN pin (or, alternatively, the TEN I^2C bit can be set to HIGH to activate the 22 kHz burst).
- T2: when the transmission has elapsed, the TTX function must be set to LOW (through the TTX pin or TTX I^2C bit) not earlier than 200 µs after the last falling edge of the DiSEqC code.

Figure 3. DiSEqC timing control



1.7 Linear post-regulator, modulator and protection

The output voltage selection and the current selection commands join this block, which manages all the LNB output function. This block gives feedback to the I^2C interface, from the diagnostic block, regarding the status of the thermal protection, overcurrent protection and output settings.

2 Pin description

The LNBH23 is available in exposed pad PowerSSO-24 or QFN32 packages for surface mount assembly. *Figure 4* shows the device pinouts for each package. *Table 1* briefly summarizes the pin functionality.

Figure 4. LNBH23 pin configuration

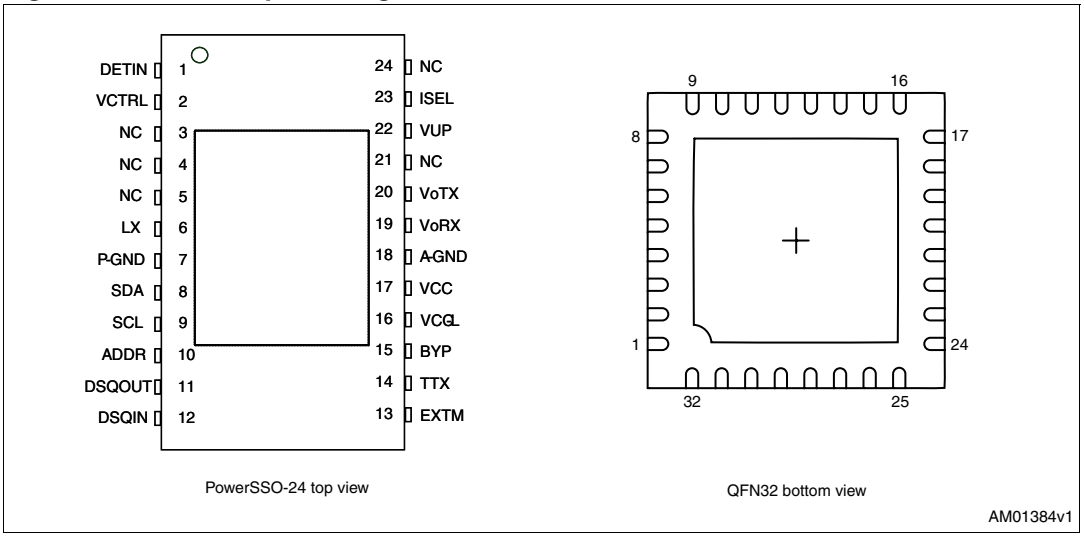


Table 1. LNBH23 pin description

Pin n° QFN32	Pin n° PSSO-24	Symbol	Name	Pin Function
19	17	V_{CC}	Supply input	8 to 15 V IC DC-DC power supply
18	16	V_{CC}–L	Supply input	8 to 15 V analog power supply
4	6	Lx	NMOS drain	Integrated N-channel power MOSFET drain
27	22	V_{UP}	Step-up voltage	Input of the linear post-regulator. The voltage on this pin is monitored by the internal step-up controller to keep a minimum dropout across the linear pass transistor
21	19	V_{oRX}	LDO output port	Output of the integrated linear post-regulator
22	20	V_{oTX}	Output port for 22 kHz tone TX	TX output to the LNB
6	8	SDA	Serial data	Bi-directional data from/to I^2C bus
9	9	SCL	Serial clock	Clock from I^2C bus
12	12	DSQIN	DiSEqC input	This pin accepts the DiSEqC code from the main microcontroller. The LNBH23 uses this code to modulate the internally-generated 22 kHz carrier. Set this pin to ground if not used

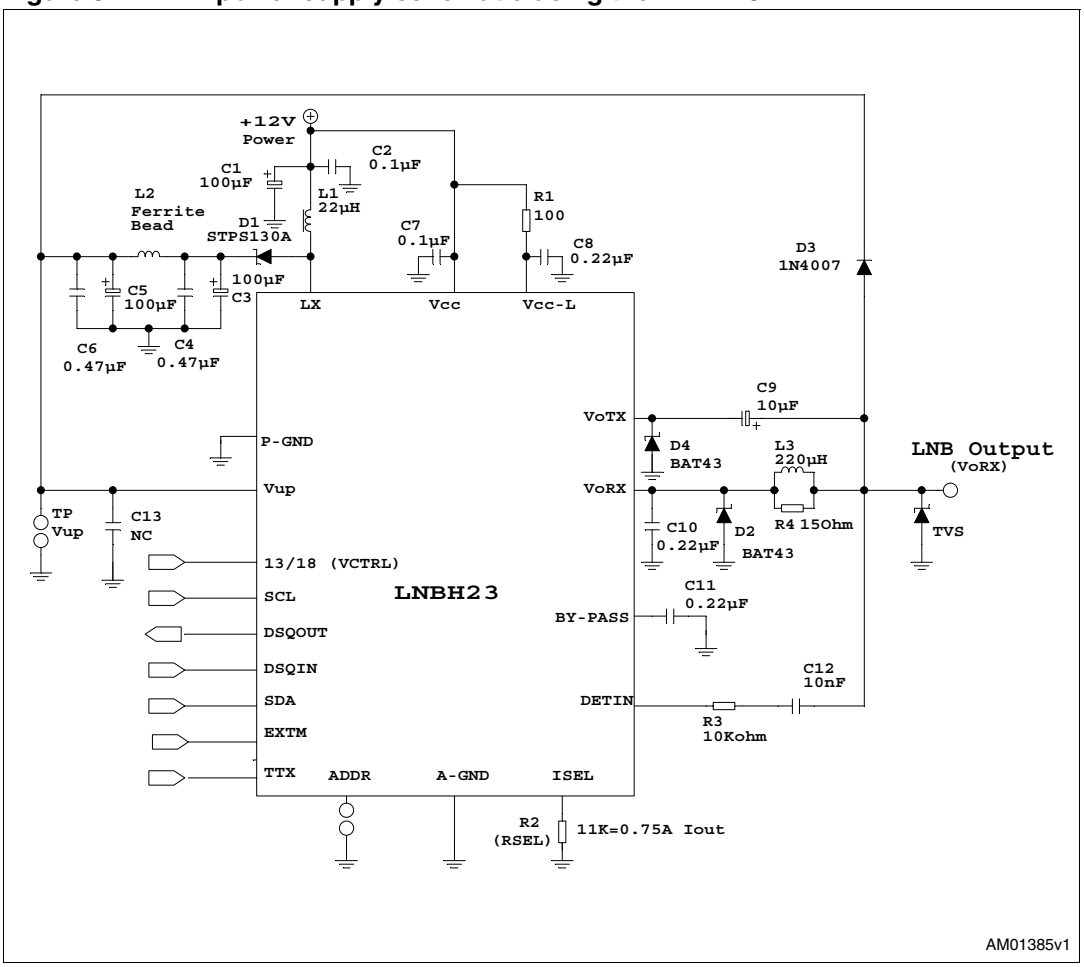
Table 1. LNBH23 pin description (continued)

Pin n° QFN32	Pin n° PSSO-24	Symbol	Name	Pin Function
14	14	TTX	TTX enable	This pin, as well as the TTX I^2C bit of the system register, is used to control the TTX function enable before starting the 22 kHz tone transmission. Set this pin to ground if not used
29	1	DETIN	Tone decoder input	22 kHz tone decoder input, must be AC coupled to the DiSEqC 2.0 bus
11	11	DSQOUT	DiSEqC output	Open drain output of the tone detector to the main microcontroller for DiSEqC 2.0 data decoding. It is low when a tone is detected on the DETIN pin
13	13	EXTM	External modulation	External modulation logic input pin which activates the 22 kHz tone output on the VoTX pin. Set to ground if not used
5	7	P-GND	Power ground	DC-DC converter power ground
20	18	A-GND	Analog ground	Analog circuits ground
15	15	BYP	Bypass capacitor	Needed for internal preregulator filtering. The BYP pin is intended only to connect an external ceramic capacitor. Any connection of this pin to external current or voltage sources may cause permanent damage to the device
10	10	ADDR	Address setting	Two I^2C bus addresses available by setting the address pin level voltage
28	23	ISEL	Current selection	The resistor "R_{SEL}" connected between I_{SEL} and GND defines the linear regulator current limit threshold with the equation: Imax(typ.)=10000/R_{SEL}
30	2	VCTRL	Output voltage control	13 V - 18 V linear regulator V_{oRX} switch control. To be used only with V_{SEL}=1. If VCTRL=1 or floating V_{oRX}=18.5 V (or 19.5 V if LLC=1). If VCTRL=0 then V_{oRX}=13.4 V (LLC=either 0 or 1)
ePad	ePad	ePad	ePad	On the bottom side of the PowerSSO-24 package. Must be connected with power ground and to the ground layer through vias to dissipate heat

3 Component selection guidelines

The LNBH23 application schematic in *Figure 5* shows the typical configuration for a single LNB power supply.

Figure 5. LNB power supply schematic using the LNBH23



Note: TVS diode to be used if surge protection is required (see Section 3.9).

Table 2. LNBH23 demonstration board BOM list

Component	Notes
IC1	LNBH23 PSSO-24 ePad for STEVAL-CBL003V1 LNBH23 QFN32 ePad for STEVAL-CBL005V1
C1	100 µF 35 V electrolytic capacitor, higher value is suitable
C3, C5	100 µF 25 V electrolytic capacitor, ESR in the 150 mΩ to 350 mΩ range (see *Section 3.3*)
C9	10 µF 35 V electrolytic capacitor
C2, C7	0.1 µF 35 V ceramic capacitors
C4, C6	0.47 µF 35 V ceramic capacitors

Table 2. LNBH23 demonstration board BOM list (continued)

Component	Notes
C8, C10, C11	0.22 µF 35 V ceramic capacitors
C12	0.01 µF 35 V ceramic capacitor
R1	100 Ω 1/4 W resistor
R2 (R_{SEL})	11 kΩ 1/16 W resistor (see *Section 3.6*)
R3	10 kΩ 1/4 W resistor
R4	15 Ω 1/4 W resistor
D1	STPS130A or similar Schottky diode (see *Section 3.4*)
D2, D4	BAT43 BAT43 (or Schottky diode with $I_{F(AV)}$>0.2 A, V_{RRM}>25 V) or BAT30, BAT54, TMM BAT43, 1N5818
D3	1N4007
L1	22 µH Inductor with Isat>I_{PEAK} (see *Section 3.5*)
L2	Ferrite bead filter; recommended part numbers: Panasonic EXCELS A35, Murata BL01RN1-A62 or equivalent with similar or higher impedance and current rating higher than 2 A (see *Section 3.2*)
L3	220 µH inductor with current rating higher than rated output current
TVS	LNBTVS22-XX TVS protection diode is recommended. Other solutions can be used depending on the level of surge protection required (see *Section 3.9*)

3.1 Input capacitors

An electrolytic bypass capacitor (C1 in *Figure 5*) between 100 µF and 470 µF located close to the LNBH23 is needed for stable operation. In any case, a ceramic capacitor between 100 nF and 470 nF is recommended to reduce the switching noise at the input voltage pin.

3.2 Ferrite bead

The most important parameter when selecting the ferrite bead is the rated current. Ensure that the ferrite has a current rating of at least 2 A and impedance higher than 60 Ω at 100 MHz.

3.3 DC-DC converter output capacitors

Two low-cost electrolytic capacitors are needed on the DC-DC converter output stage (C3 and C5 in *Figure 5*). Moreover, two ceramic capacitors are recommended to reduce high frequency switching noise. The switching noise is due to the voltage spikes of the fast switching action of the output switch, and to the parasitic inductance of the output capacitors. To minimize these voltage spikes, special low-inductance ceramic capacitors can be used, and their lead lengths must be kept short and as close as possible to the IC pins (C4 and C6 in *Figure 5*). To further reduce switching noise, a ferrite bead is recommended between the capacitors (see *Section 3.2* for required rating and impedance).

The most important parameter for the output capacitors is the effective series resistance (ESR). The DC-DC converter control loop circuit has been designed to work properly with low-cost electrolytic capacitors which have ESR in the range of 200 mΩ. A 100 µF output filter capacitor with ESR between 150 mΩ and 350 mΩ is a good choice in most application conditions. It is also possible to use electrolytic capacitors up to 220 µF with ESR between 100 mΩ and 300 mΩ. The capacitor voltage rating must be at least 25 V, but if the highest voltage selection condition is used (AUX=1), 35 V or higher voltage capacitors are suggested.

3.4 DC-DC converter Schottky diode

In typical application conditions it is beneficial to use a 1 A Schottky diode which is suitable for the LNBH23 DC-DC converter. Taking into consideration that the DC-DC converter Schottky diode must be selected depending on the application conditions (V_{RRM} > 25 V), an N-channel Schottky diode like the STPS130A is recommended.

The average current flowing through the Schottky diode is lower than I_{PEAK} and can be calculated using *Equation 1*. In worst-case conditions, such as low input voltage and higher output current, a Schottky diode capable of supporting the I_{PEAK} should be selected. I_{PEAK} can be calculated using *Equation 2*.

Equation 1

$$Id = Iout \cdot \frac{Vout}{Vin}$$

Table 3. Recommended Schottky diode

Vendor	Part number	I_F(av)	V_F(max)
STMicroelectronics	1N5818	1 A	0.50 V
	1N5819	1 A	0.55 V
	STPS130A	1 A	0.46 V
	STPS1L30A	1 A	0.30 V
	STPS2L30A	2 A	0.45 V
	1N5822	3 A	0.52 V
	STPS340	3 A	0.63 V
	STPS3L40A	3 A	0.5 V

3.5 DC-DC converter inductor

The LNBH23 operates with a standard 22 µH inductor for the entire range of supply voltages and load current. The inductor saturation current rating (where inductance is approximately 70% of zero current inductance) must be greater than the switch peak current (I_{PEAK}) calculated at:

- maximum load ($Iout_{max}$)
- minimum input voltage (Vin_{min})
- maximum DC-DC output voltage (VUP_{max} =$Vout_{max}$ +0.75 V)

In this condition the switch peak current is calculated using the formula in *Equation 2*.

Equation 2

$$Ipeak = \frac{VUP_{max} \cdot Iout_{max}}{Eff \cdot Vin_{min}} + \frac{Vin_{min}}{2LF}\left(1 - \frac{Vin_{min}}{VUP_{max}}\right)$$

where

- Eff is the efficiency of the DC-DC converter (93% typ. at highest load)
- L is the inductance (22 µH typ.)
- F is the PWM frequency (220 kHz typ.).

Example:

Application conditions:

- $Vout_{max}$= 19.2 V (supposing EN=VSEL=1, LLC=0)
- Vin_{min}= 11 V
- Vup_{max}=$Vout_{max}$+V_{drop}= 19.2 V+0.75 V= 19.95 V
- $Iout_{max}$= 500 mA
- Eff=90%

Based on *Equation 2* and the preceding application conditions, I_{PEAK} is:

Equation 3

$$Ipeak = \frac{19.95 \cdot 0.5}{0.9 \cdot 11} + \frac{11}{2 \cdot 22 \cdot 10^{-6} \cdot 220 \cdot 10^{3}}\left(1 - \frac{11}{19.95}\right) = 1.52\ A$$

Several inductors suitable for the LNBH23 are listed in the *Table 4*, although there are many other manufacturers and devices that can be used. Consult each manufacturer for more detailed information and for their entire selection of related parts, since many different shapes and sizes are available. Ferrite core inductors should be used to obtain the best efficiency. Choose an inductor that can handle at least the I_{PEAK} current without saturating, and ensure that the inductor has a low DCR (copper wire resistance) to minimize power losses and, consequently, to maximize total efficiency.

Table 4. Recommended inductors

Vendor	Part number	Isat(A)	DRC (mΩ)	Mounting type
Sumida	CD104-220MC	1.6	67	SMD
	RHC110-220M	2.4	88	Through-hole
Toko	822LY-220K	1.3	70	Through-hole
	824LY-220K	1.72	76	Through-hole
	A671HN-220L	2.44	21	Through-hole
	A814LY-220M	2.0	75	SMD

Table 4. Recommended inductors (continued)

Vendor	Part number	Isat(A)	DRC (mΩ)	Mounting type
Panasonic	ELC08D220E	1.8	51	Through-hole
	ELC10D220E	3.2	40	Through-hole
Coilcraft	DC1012-223	2.5	46	Through-hole
	PVC-0-223-03	3	35	Through-hole
	DO3316P-223	2.6	85	SMD

3.6 Output current limit-R_{SEL} selection

The linear regulator current limit threshold can be set through an external resistor connected to ISEL pin. The resistor value defines the output current limit using the equation:

Equation 4

$$Imax(A) = \frac{10000}{R_{SEL}}$$

where R_{SEL} is the resistor connected between the ISEL pin and GND. The highest selectable current limit threshold is 1.0 A (typ) with R_{SEL}=10 kΩ.

3.7 Undervoltage diode protection

During a short-circuit removal on the LNB output, negative voltage spikes may occur on the V_{oTx} and V_{oRx} pins. To prevent reliability problems, two low-cost Schottky diodes are used between those pins and GND (see D2 and D4 in *Figure 5*).

3.8 DiSEqC implementation and inductor selection

To comply with DiSEqC 2.x requirements, an output R-L filter is needed. The 22 kHz tone transmission occurs through the V_{oTX} pin, whereas the DC voltage is provided from the V_{oRx} pin. The V_{oTX} function must be activated only during the tone transmission while the V_{oRX} provides the 13/18 V output voltage. This solution allows the 22 kHz tone to pass without any losses due to the R-L filter impedance. But to respect the minimum DC voltage requirement, it is recommended to use an inductor with a current rating higher than the rated output current and a low DRC to minimize the voltage drop.

For example, supposing:

- Iout = 500 mA
- DRC=51 mΩ (Panasonic inductor ELC08D221E)

Equation 5

$$Vdrop(V) = DCR(\Omega) \cdot Iout(A) = 0.051 \cdot 0.5 = 0.025\ V$$

Several inductors suitable for the LNBH23 are listed in the *Table 5*.

Table 5. Recommended inductors for output R-L filter

Vendor	Part number	Isat(A)	DRC(mΩ)	Mounting type
Sumida	CD104-221MC RHC110-221M	1.6 2.4	67 88	SMD Through-hole
Toko	822LY-221K 824LY-221K A671HN-221L A814LY-221M	1.3 1.72 2.44 2.0	70 76 21 75	Through-hole Through-hole Through-hole SMD
Panasonic	ELC08D221E ELC10D221E	1.8 3.2	51 40	Through-hole Through-hole
Coilcraft	DC1012-223 PVC-0-223-03 DO3316P-223	2.5 3 2.6	46 35 85	Through-hole Through-hole SMD

3.9 TVS diode

The LNBH23 device is directly connected to the antenna cable in a set-top box. Atmospheric phenomenon can cause high voltage discharges on the antenna cable causing damage to the attached devices. Surge pulses occur due to direct or indirect lightning strikes to an external (outdoor) circuit. This leads to currents or electromagnetic fields causing high voltage or current transients. LNBH23 devices are not able to withstand such high energy discharges, so transient voltage suppressor (TVS) devices are used to protect the LNBH23 and other devices electrically connected to the antenna cable.

The LNBTVS developed by STMicroelectronics is a dedicated lightning and electrical overstress surge protection device for LNB voltage regulators. These protection devices are designed to comply with the stringent IEC 61000-4-5 standards and to withstand surges of up to 500 A. ST offers a broad selection of these products for cost/performance optimization.

The selection of the TVS diode must be made based on the maximum peak power dissipation that the diode is capable of supporting.

Table 6. Recommended LNBTVS

Vendor	Part number	VBR_{TYP}(V)	Ppp(W)10/100µs
STMicroelectronics	LNBTVS4-220	23.1	1800
	LNBTVS4-221	23.1	2000
	LNBTVS4-222S	23.1	2000
	LNBTVS6-221S	21.3	3000

Select the TVS diode which is capable of supporting the required Ppp(W) value indicated in *Table 6*.

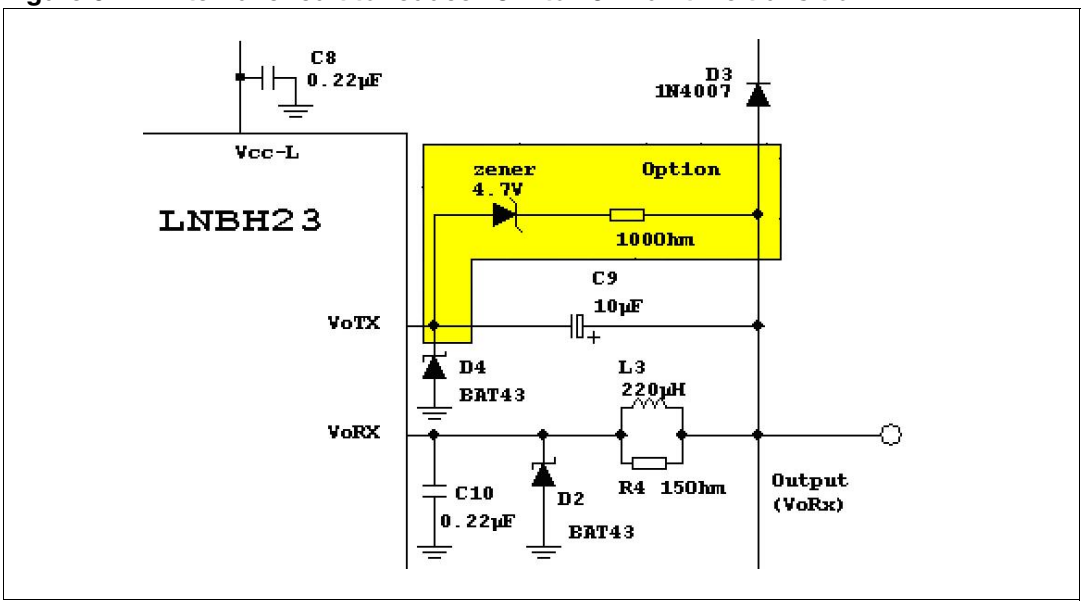
4 Other application circuits

The following paragraphs present two particular application solutions: the first can be used to reduce the 18 V to 13 V transition time, while the second is designed to improve lightning surge protection.

4.1 18 V to 13 V fast transition with high bus capacitance

In cases of very high bus capacitance (Cbus>10 µF) and very low output current, an external circuit (with a 4.7 V Zener diode and a 100 Ω series resistor) can be added to reduce 18 V to 13 V transition fall time, as shown in *Figure 6*.

Figure 6. External circuit to reduce 18 V to 13 V fall time transition



The TTX bit (or pin) must be set high only during the transition from 18 V to 13 V. The TTX function activates only the push-pull circuit, but not the tone output. The 22 kHz tone is activated only when the TEN bit (or DSQIN pin) is also set high and injected into the LNB bus through the 10 µF capacitor.

When the TTX function is activated, the V_{oTx} voltage is internally set at 5 V (typ). below the Vout (for example, if Vout=18 V then V_{oTx}=18-5=13 V) and, at the same time, the P-channel is enabled to sink current (note: the P-channel is internally current-limited).

With a 4.7 V Zener diode, when TTX=high, the current through the Zener is: Iz=(5-4.7)/100=3 mA. If TTX=low, the current through the Zener is negligible.

If there is a high output capacitance present, during the transition from 18 V to 13 V (with TTX=high), the voltage drop (Vout-V_{oTx}) is increased because the V_{oTx} goes quickly to low level (at 13 V-5 V=8 V) and, consequently, the Zener current is also increased until the output capacitance is discharged to 13 V. For example, with 100 µF on the output, the 18 V to 13 V fall time is about 25 ms.

The following steps must be taken to ensure the correct implementation of 18 to 13 V transition with the V_{oTx} addition circuit shown in *Figure 6*:

- T0: to start the 18 V to 13 V transition the TTX function must be activated at least 0.5 ms before setting the VSEL I^2C bit (set HIGH TTX I^2C bit or TTX pin).
- T1: set LOW VSEL I^2C bit.
- T2: after 30 ms, 18 V to 13 V LNB transition time is elapsed at T2. The 30 ms delay is valid to ensure 18 V to 13 V complete transition in case of Cbus=100 µF and Iout=0 mA. The delay time can be modified with different Cbus capacitance and output current value.

Figure 7. Fast transition timing sequence

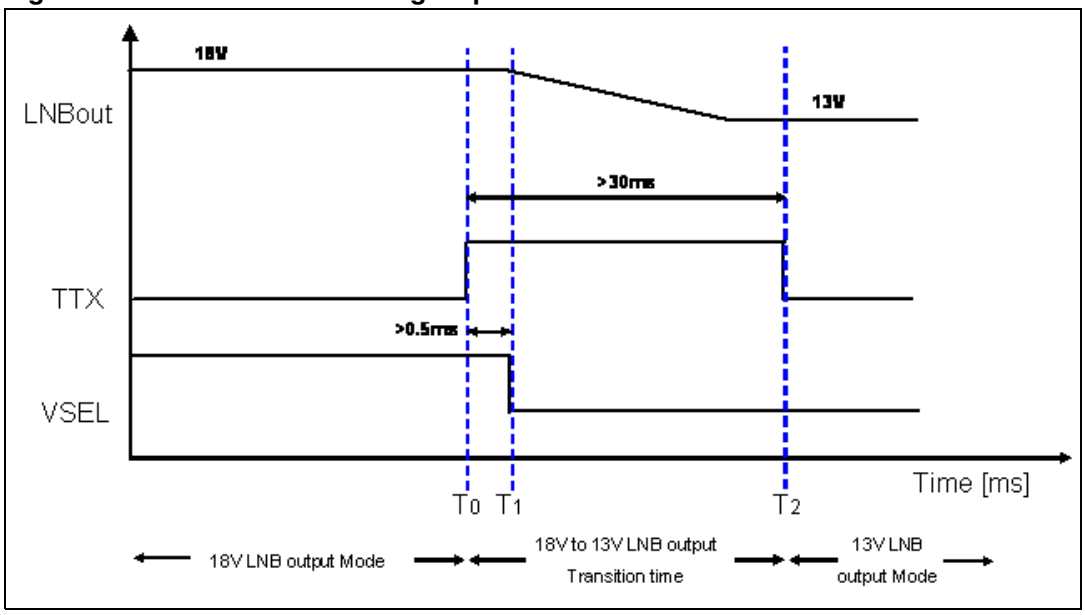
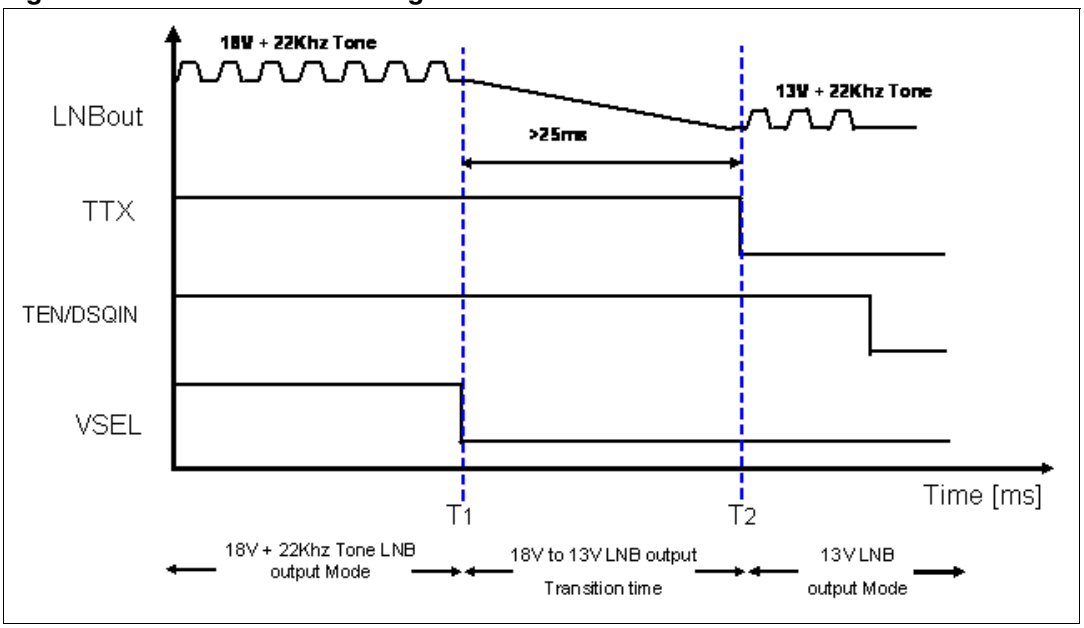


Figure 8. Fast transition timing control with 22 kHz tone



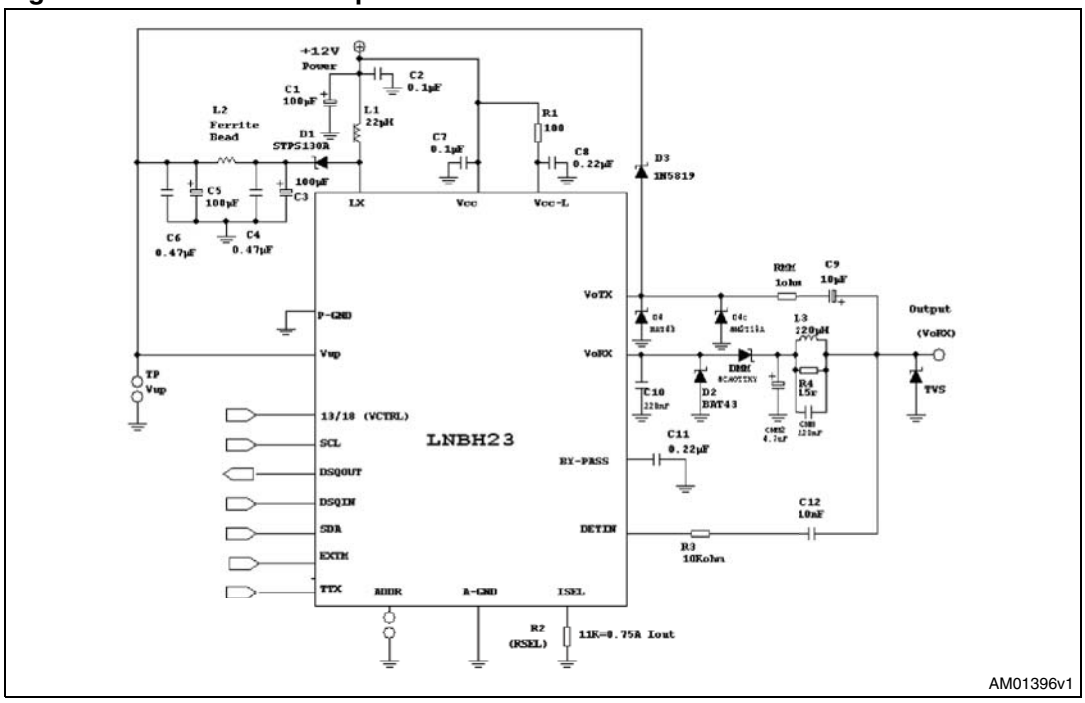
If the internal 22 kHz tone generator is activated (TEN I^2C bit or DSQIN pin is set high), at T1 set low the VSEL I^2C bit or VCTRL pin and after 25 ms, 18 V to 13 V LNB transition time is elapsed at T2.

4.2 Reverse voltage and lightning surge protection

Figure 9 shows a suggested schematic to improve output circuit protection in applications where:

- TVS diode with Vclamp voltage of 25 V is required
- an external power supply source could force a reverse DC voltage of 25 V on the LNB bus

Figure 9. External circuit protection schematic



The Schottky diode prevents the reverse voltage from flowing into the V_{oRx} pin (internally connected to the linear regulator). In applications where a reverse DC voltage (up to 60 V) is forced and low Vout tolerance is required, the recommended part number is STPS3L60U. In any case, it is possible to use a different part based to the DC reverse voltage. D3 shields the V_{oTx} pin because it discharges the reverse voltage into the Vup capacitor and D4c (suggested part number SM2T18A) is mandatory for DC reverse voltage ≥ 25 V.

5 Layout guidelines

Due to high current levels and fast switching waveforms, which radiate noise, a proper printed circuit board (PCB) layout is essential. Sensitive analog grounds can be protected by using a star ground configuration. Also, lead lengths should be minimized to reduce stray capacitance, trace resistance, and radiated noise. Ground noise can be minimized by connecting GND, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a single point (star ground configuration). Place input bypass capacitors (C1, C2, C7 and C8) as close as possible to Vcc and GND, and the DC-DC output capacitors (C3, C4, C5 and C6) as close as possible to VUP. Excessive noise at the Vcc input may falsely trigger the undervoltage circuitry, resetting the I^2C internal registers. If this occurs, the registers are set to zero and the LNBH23 is put into shutdown mode.

LNB power supply demonstration boards are available for each package option through order codes STEVAL-CBL003V1 (*Figure 10*) and STEVAL-CBL005V1 (*Figure 11*).

Figure 10. STEVAL-CBL003V1 demonstration board photo (PowerSSO-24 package)

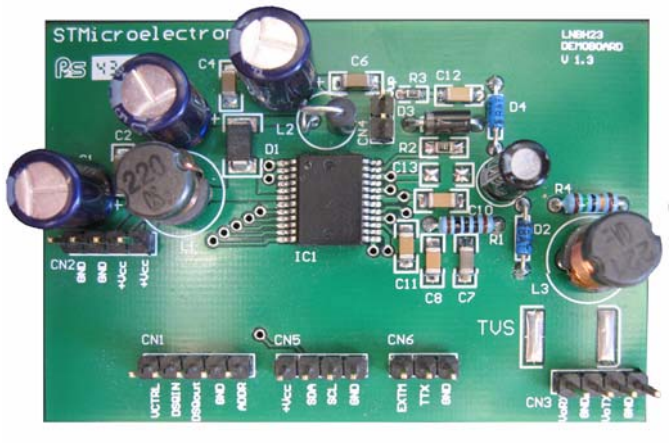
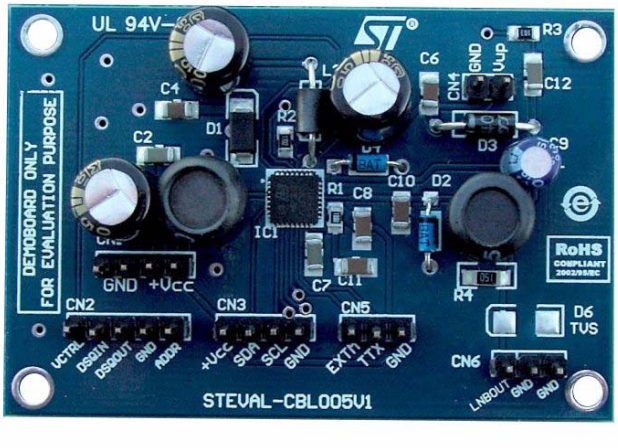


Figure 11. STEVAL-CBL005V1 demonstration board photo (QFN32 package)



5.1 PCB layout

Any switch mode power supply requires a good PCB layout in order to achieve maximum performance. Component placement, and GND trace routing and width are the major issues. Basic rules commonly used for DC-DC converters for good PCB layout should be followed.

All traces carrying current should be drawn on the PCB as short and as thick as possible. This should be done to minimize resistive and inductive parasitic effects, and increase system efficiency.

White arrows indicate the suggested PCB (ring) ground plane to avoid spikes on the output voltage (this is related to the switching side of the LNBH23). Good soldering of the ePad helps on this issue.

Figure 12. STEVAL-CBL003V1 PCB top layer

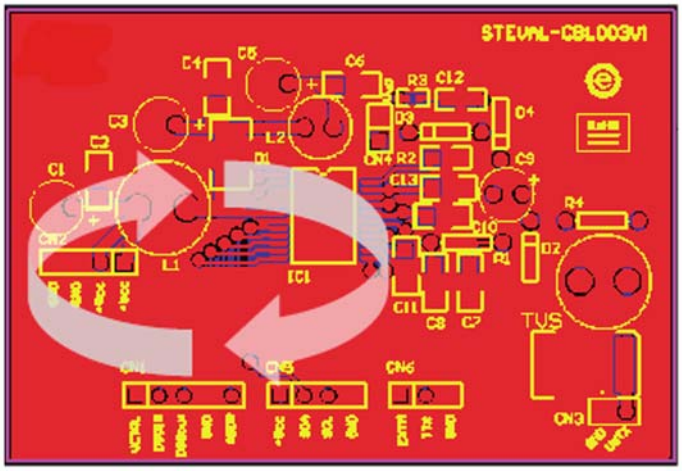


Figure 13. STEVAL-CBL003V1 PCB bottom layer

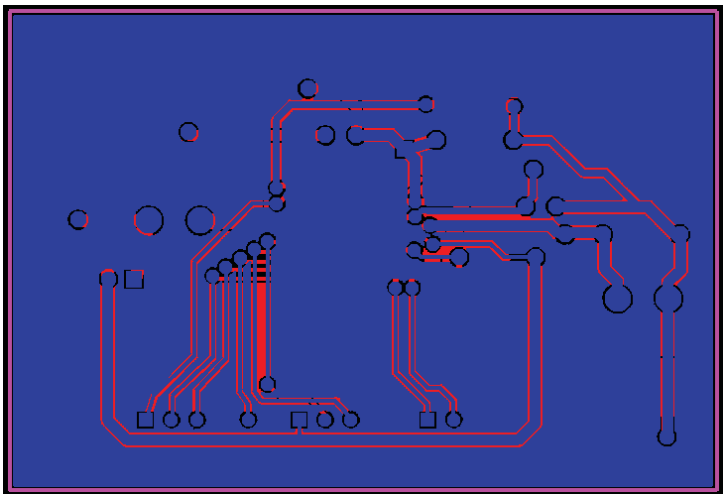


Figure 14. STEVAL-CBL003V1 component layout

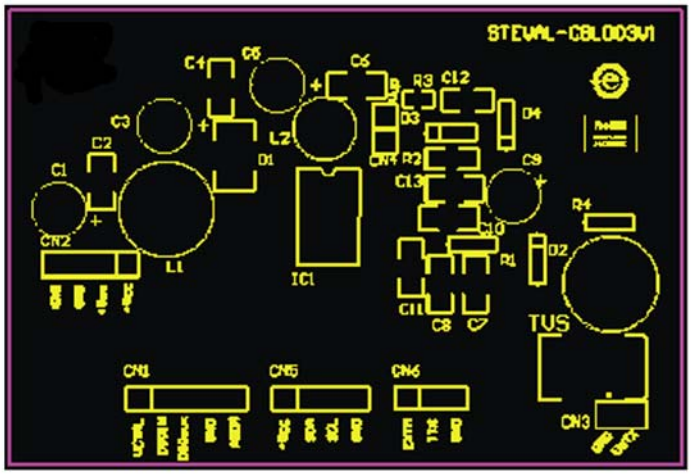


Figure 15. STEVAL-CBL005V1 PCB top layer

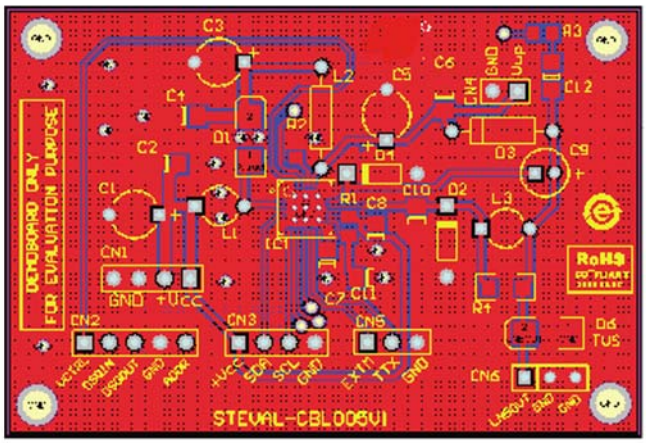


Figure 16. STEVAL-CBL005V1 PCB bottom layer

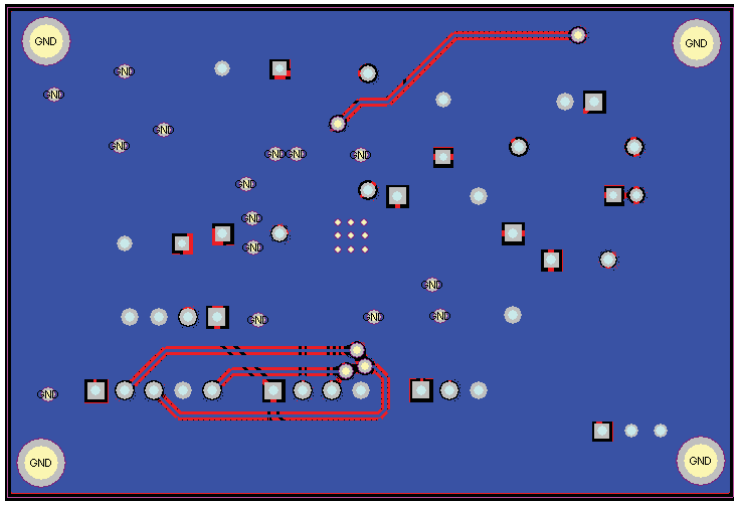
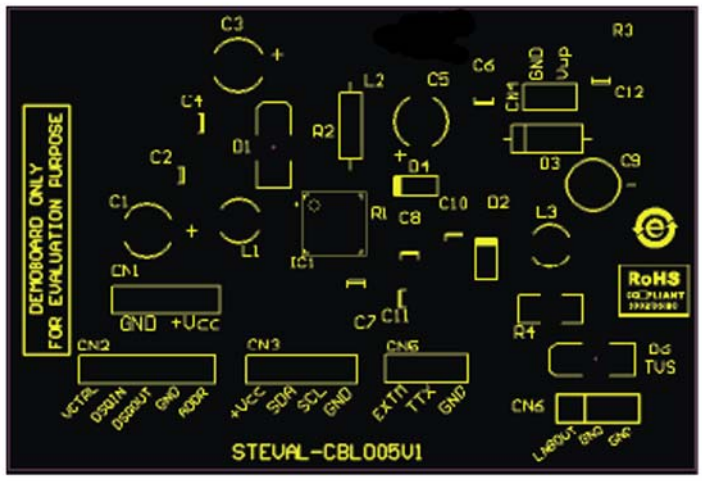


Figure 17. STEVAL-CBL005V1 component layout



5.2 Startup procedure

Testing the demonstration board requires a PC with a parallel port (ECP printer port), an I^2C bus interface, software (LNBxxx control suite), a dual-output power supply (3 A clamp current or higher) and an electronic load.

- Step 1: Install the LNBXXX control suite software (see *Section 6*).
- Step 2: Plug the I^2C connector into CN5.
- Step 3: Supply the demonstration board through CN2.
- Step 4: Refer to *Section 6.1* of software installation guide to use the software.

Figure 18. STEVAL-CBL003V1 connectors

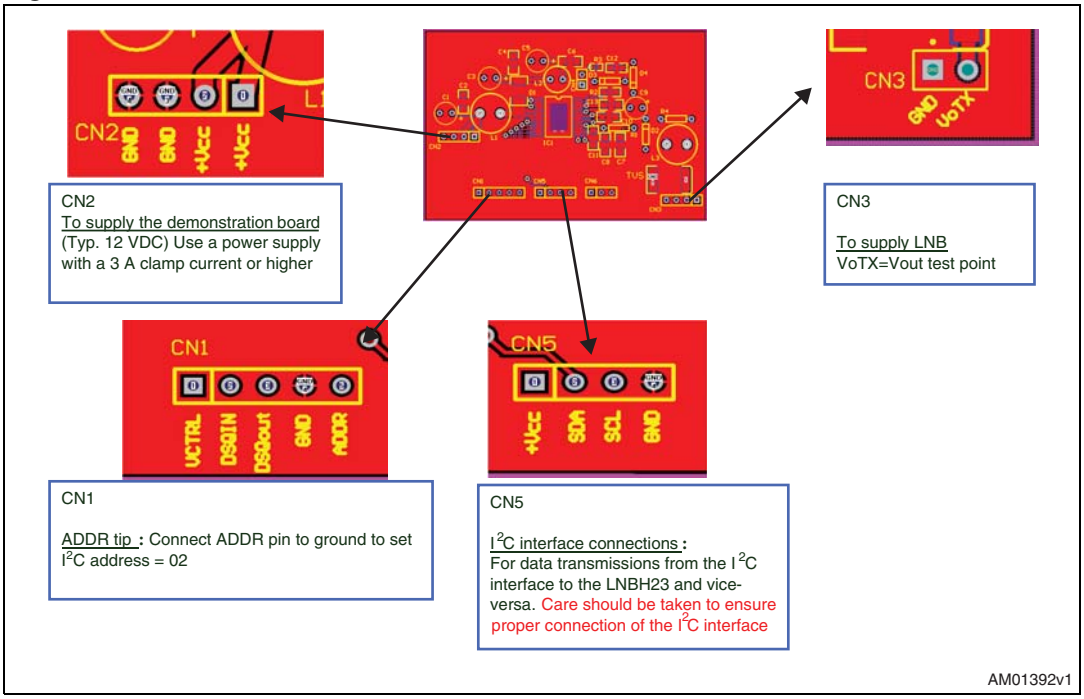


Figure 19. STEVAL-CBL005V1 connectors

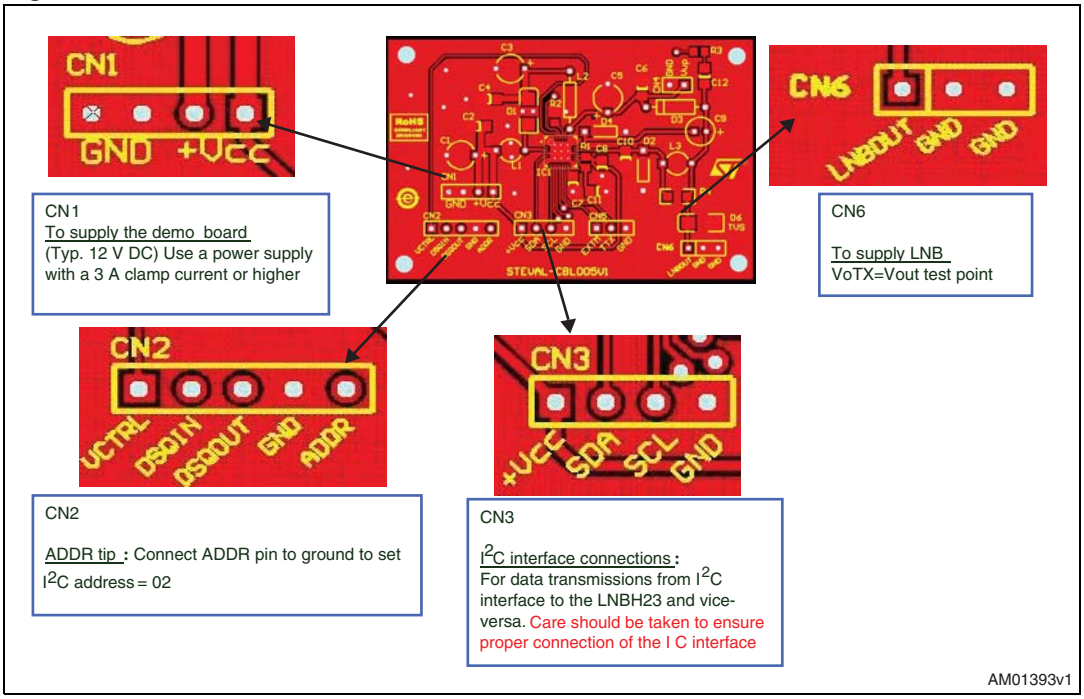


Figure 20. STEVAL-CBL003V1 bench test

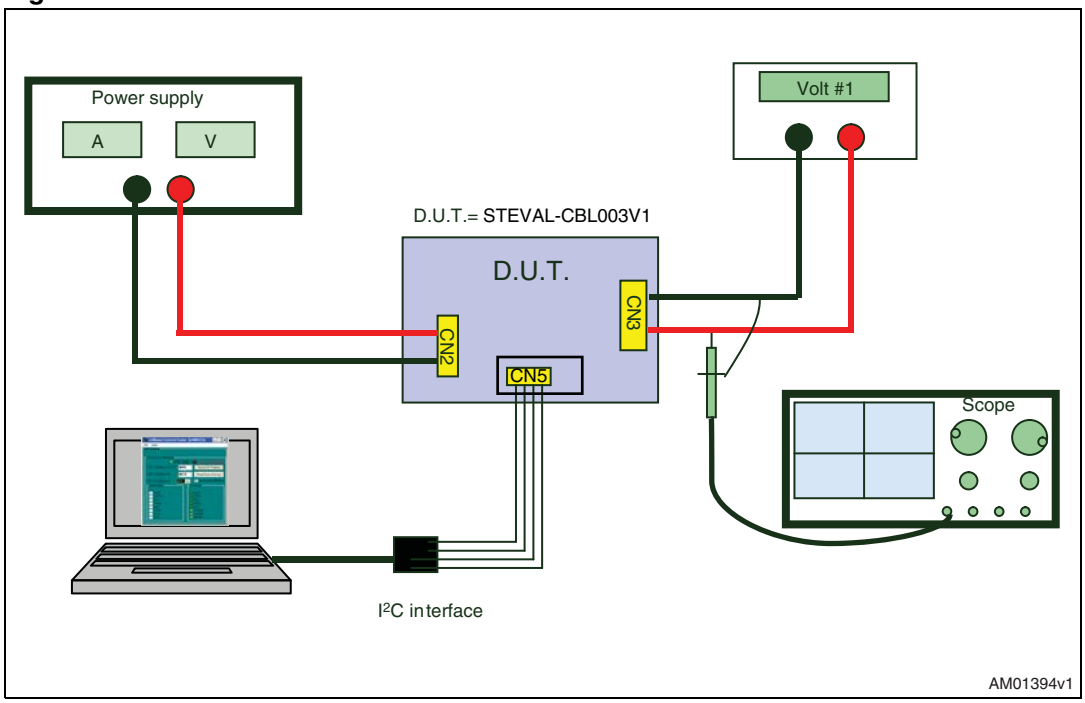
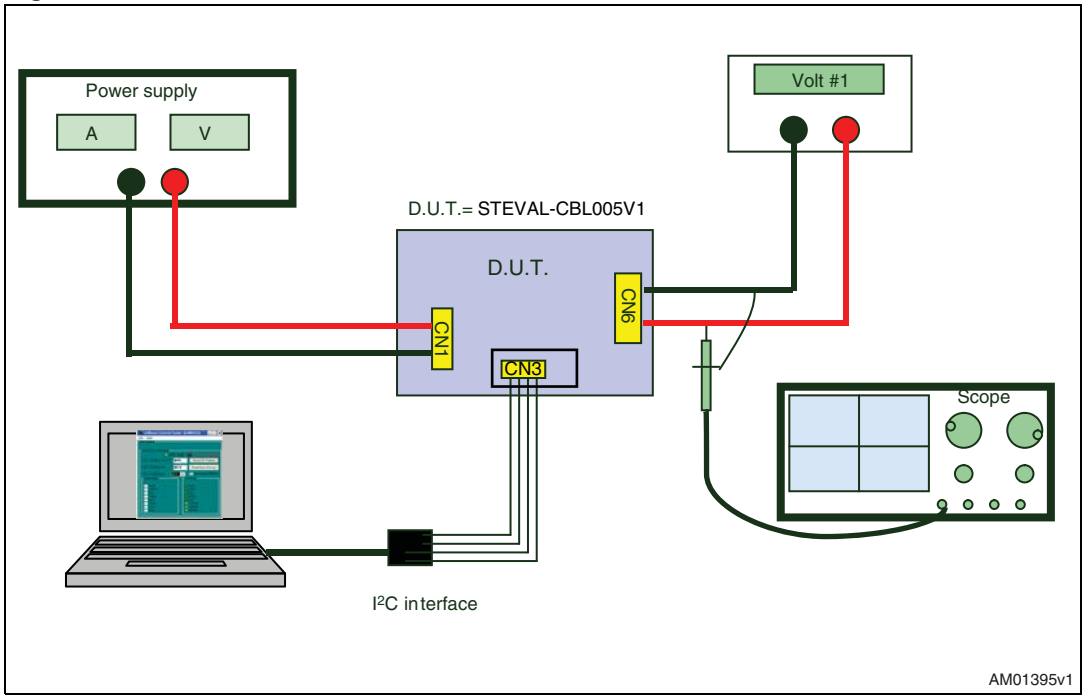


Figure 21. STEVAL-CBL005V1 bench test

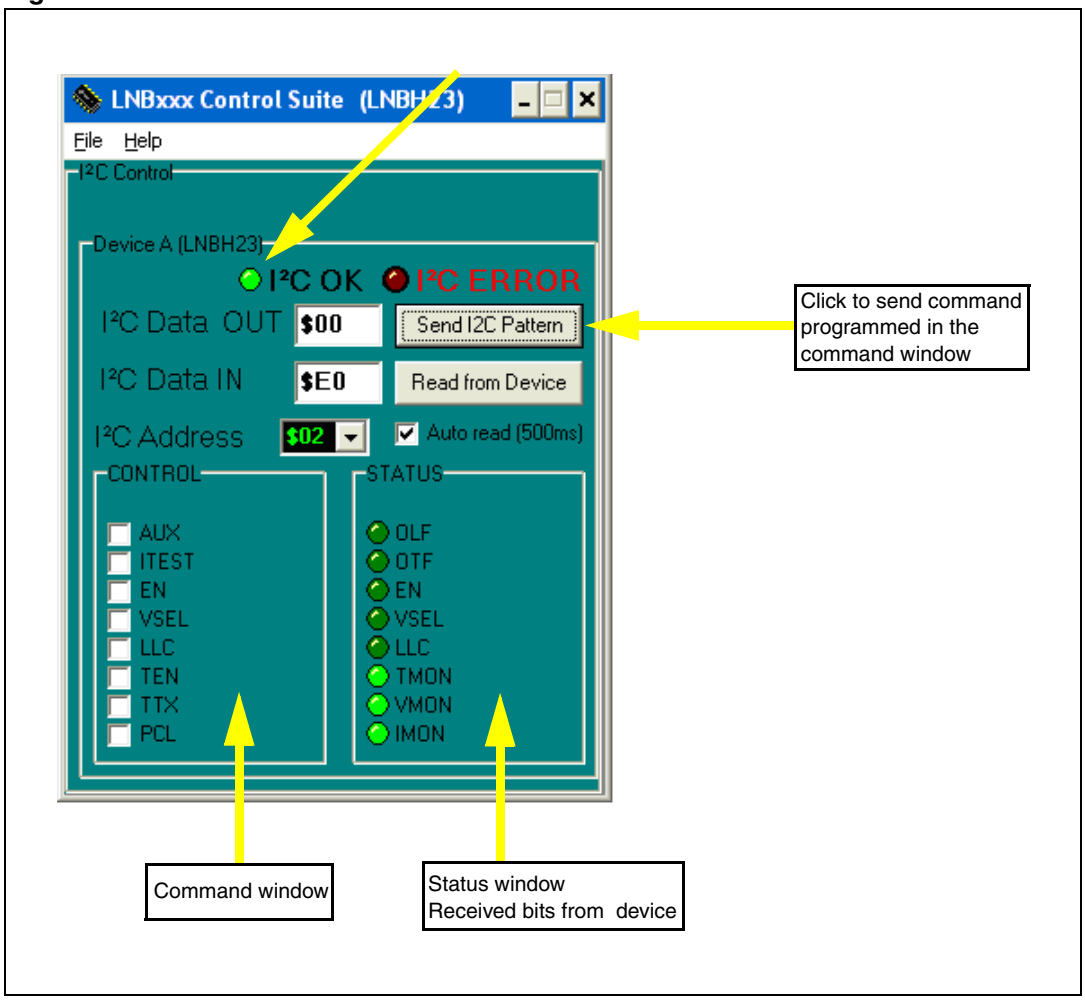


6 Software installation

Unzip the compressed file and perform the installation by clicking on the SETUP.exe file.

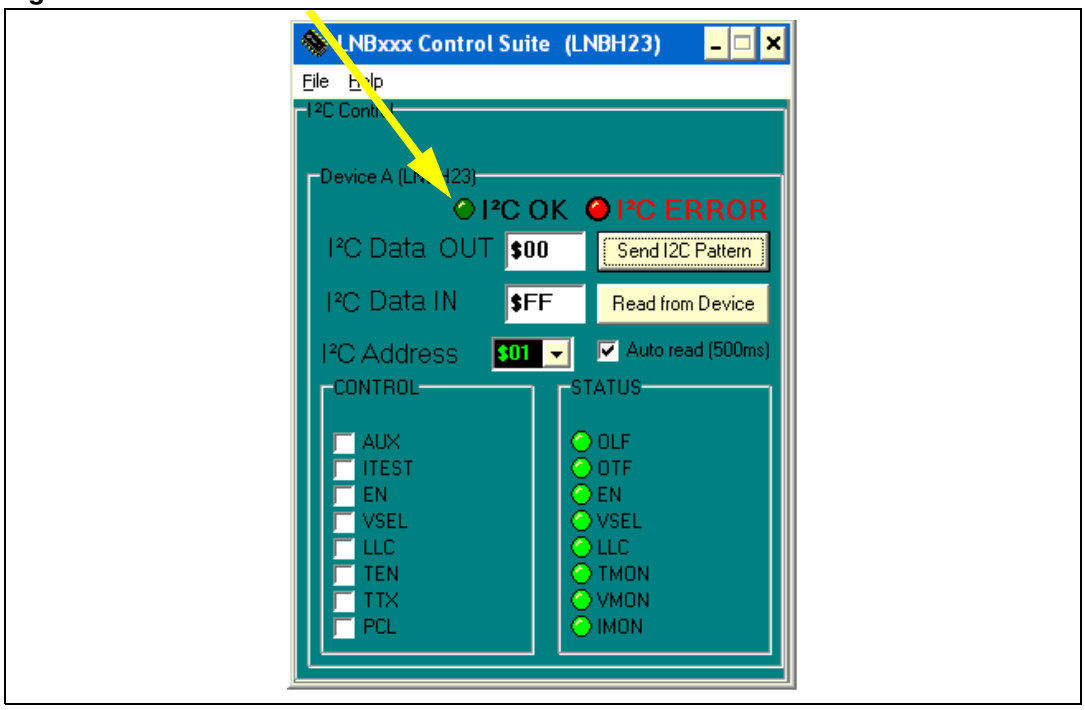
Click on: Windows® “start” menu -> Program -> STMicroelectronics -> LNBxxx control suite. The screen shown in *Figure 22* appears, with a green light indicating that the hardware and software are ready to work.

Figure 22. PC to I²C main window



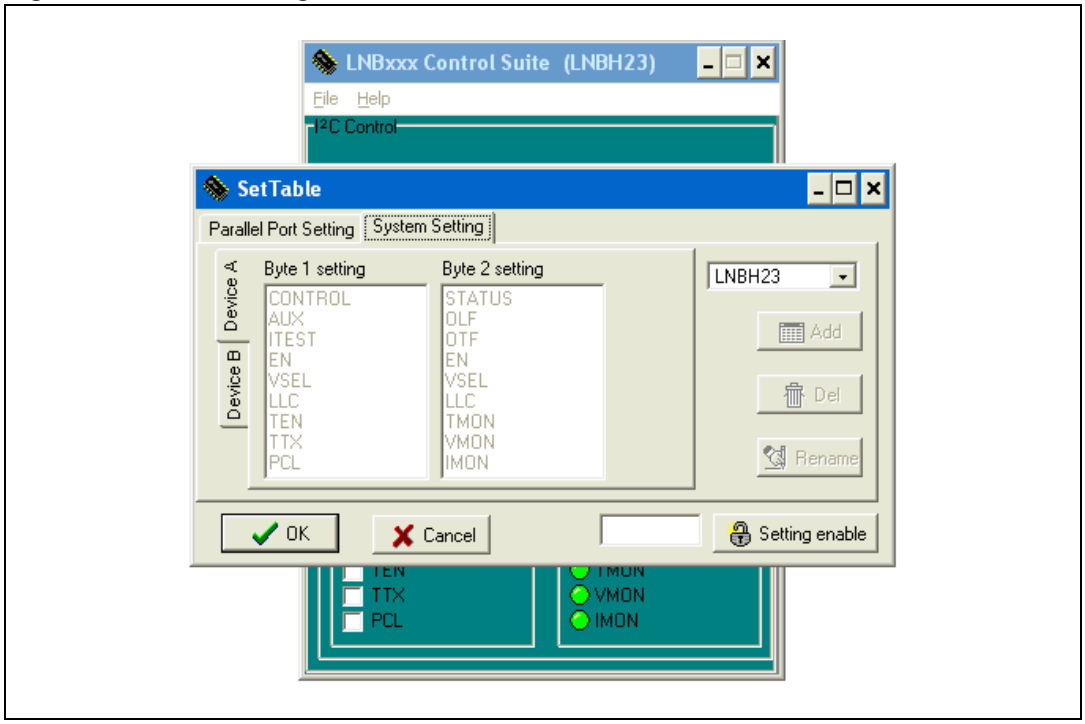
The red "I²C ERROR" indicator signals that the LPT port needs to be configured, and/or the I²C cable (swap the SCL and SDA, if needed) and power supply need to be checked.

Figure 23. I²C bus communication error



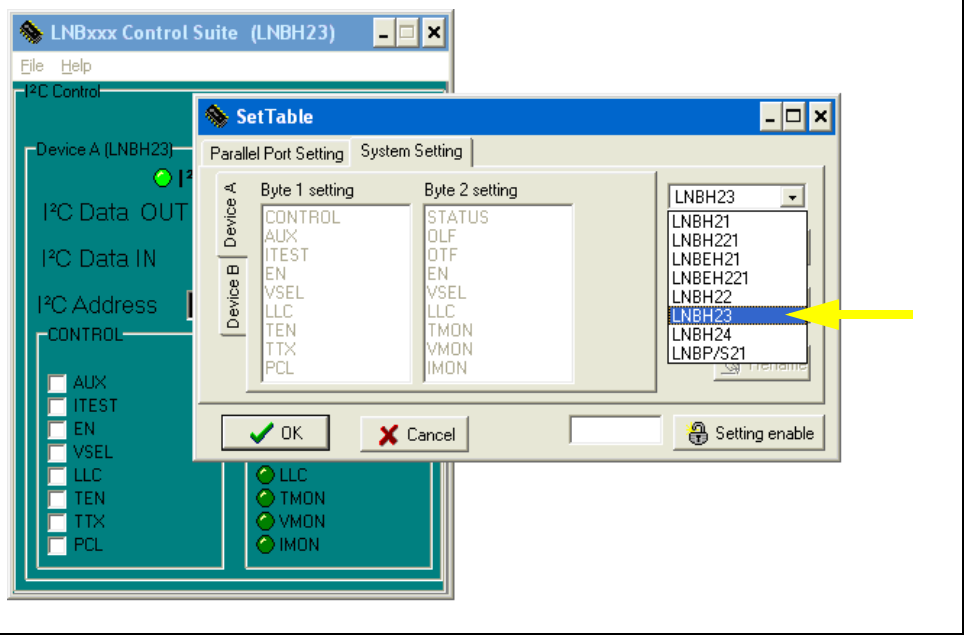
The user can choose the device, printer port address for the PC and correct settings of the SCL and SDA bits to customize the I²C hardware interface.

Figure 24. Main settings window



In the system setting menu, the device to be tested can be changed.

Figure 25. Device selection window



From the parallel port setting menu, the LPT parameters can be set.

Figure 26. Parallel port setting

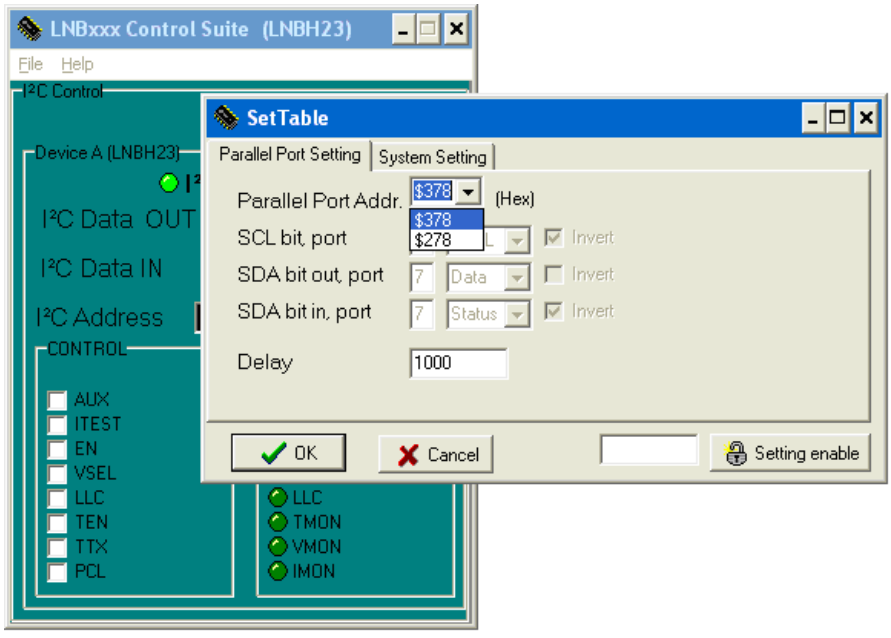


Figure 27. LPT1 setting

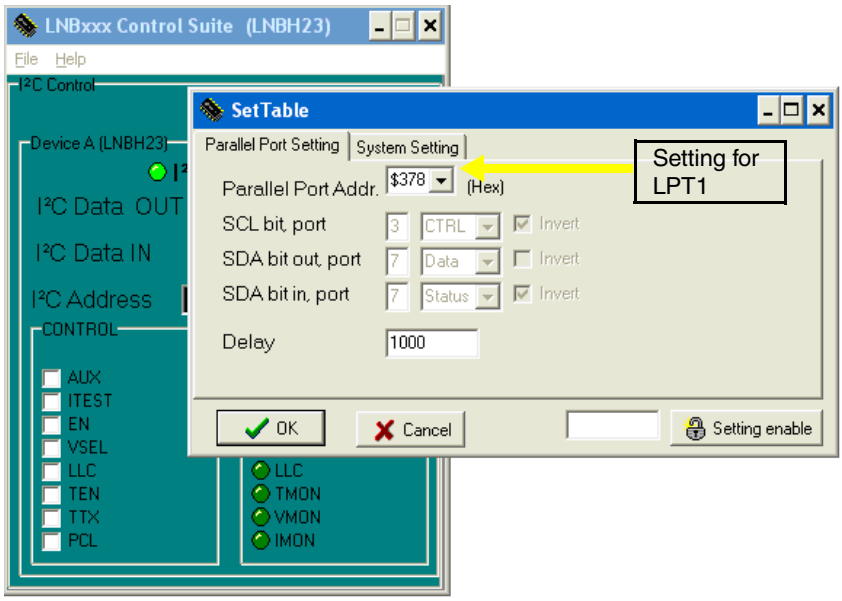
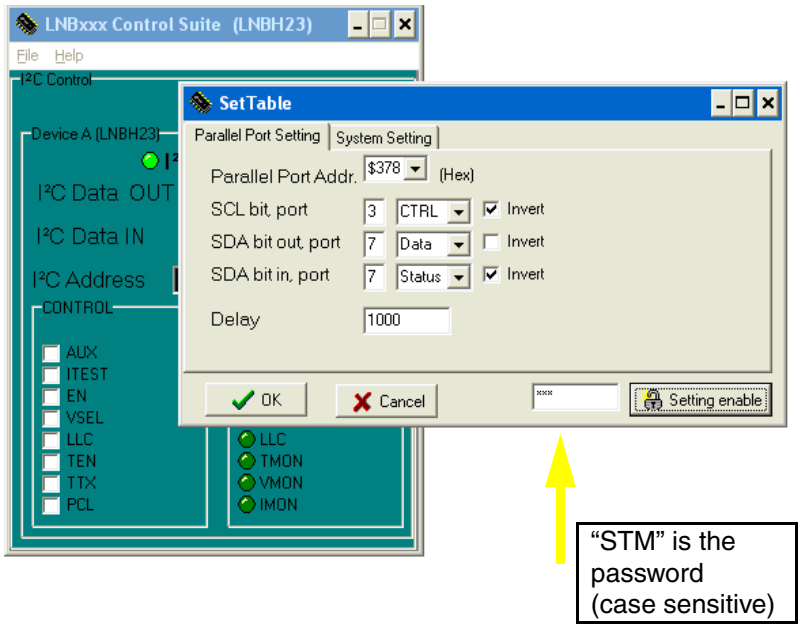
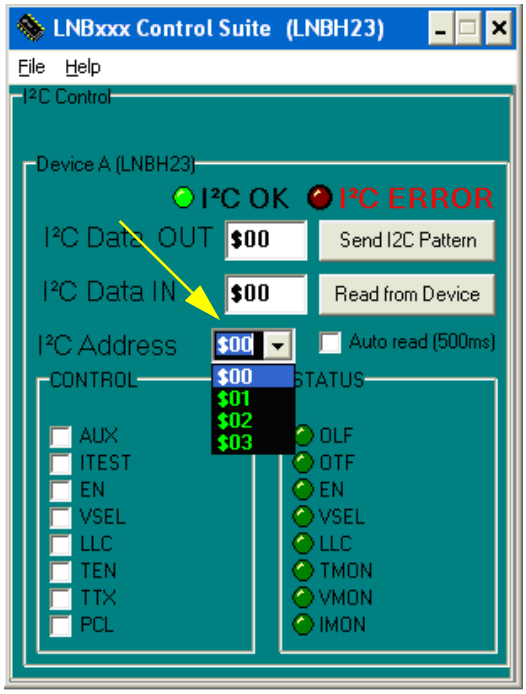


Figure 28. Password setting



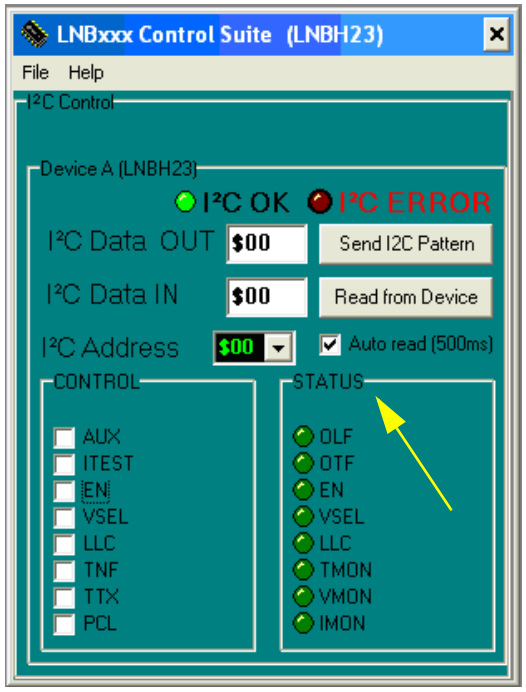
At this point, the device address can be chosen. For the LNBH23, only $02= ADDR pin force to GND or $03= ADDR pin force to +5 V can be selected.

Figure 29. I²C device address setting



To obtain the status of the received bits in real-time, the "Auto read" checkbox must be checked.

Figure 30. Autoread setting



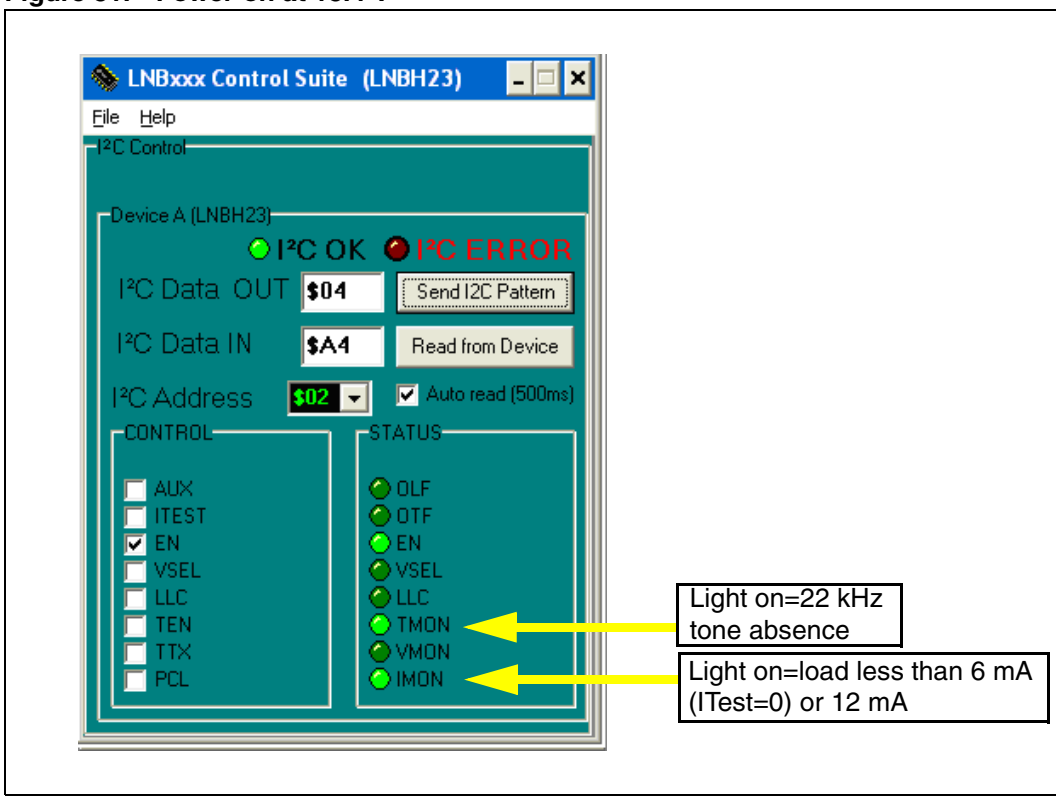
6.1 How to use the LNBH23 demonstration board with the LNBxxx control suite software

To power the IC, place a check in the EN checkbox and click the "Send I²C Pattern" button. If the device accepts the command string, the green indicator turns on. If there is no powerup after sending the command, it may be that the 12 V power supply is not sufficient to start the application, and more current capability is needed.

The screenshot in *Figure 31* shows the following conditions:

- EN=1=ON
- Vout=13.4 V_{typ}

Figure 31. Power-on at 13.4 V

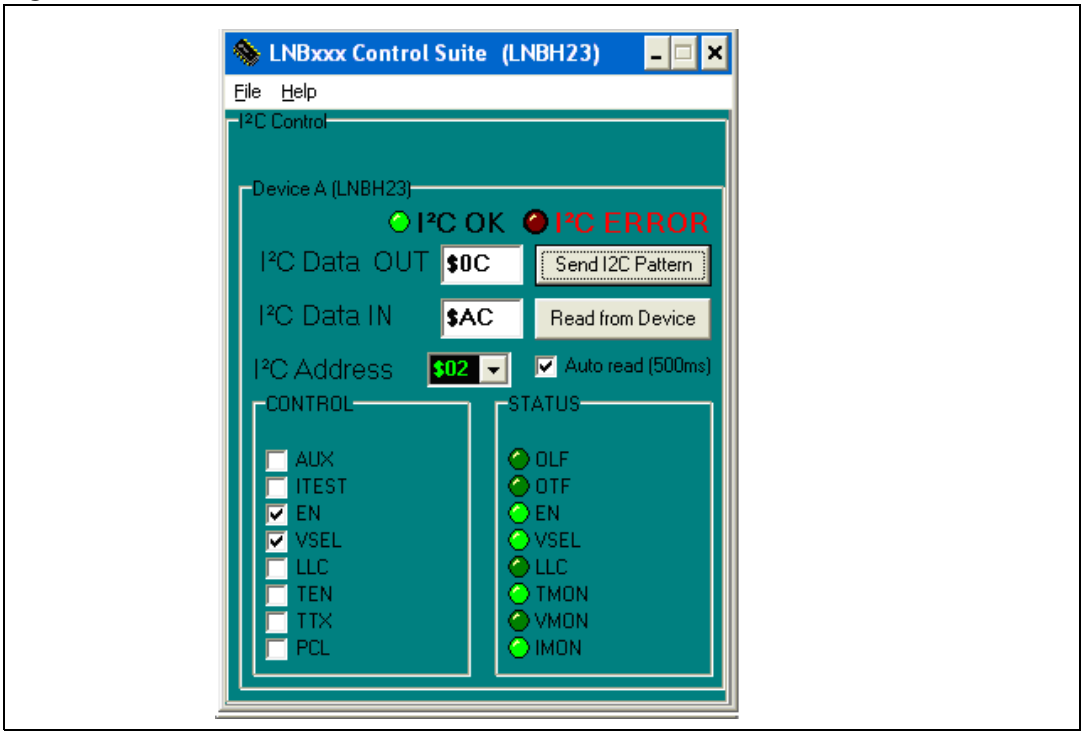


A status light “on” for OLF, OTF, TMON, VMON and IMON indicates that an error has occurred.

The screenshot in *Figure 32* shows the following conditions:

- EN=1, VSEL=1
- Vout=18.5 V_{typ}

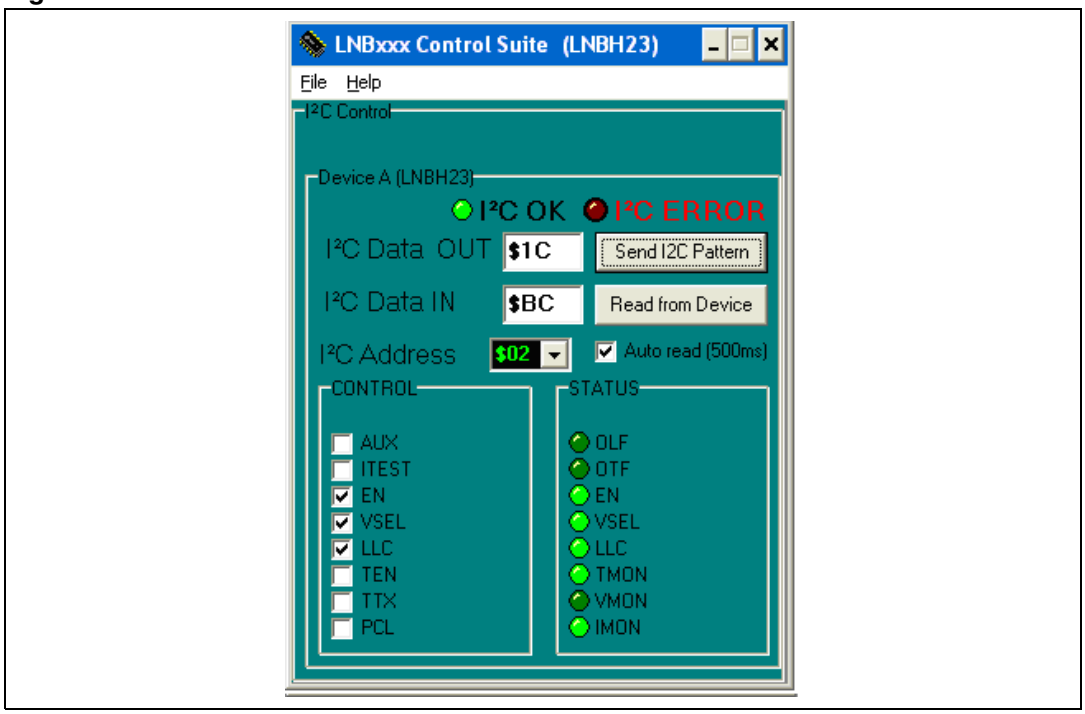
Figure 32. Power-on at 18.5 V



The screenshot in *Figure 33* shows the following conditions:

- EN=1, VSEL=1, LLC=1
- Vout=19.5 V_{typ}

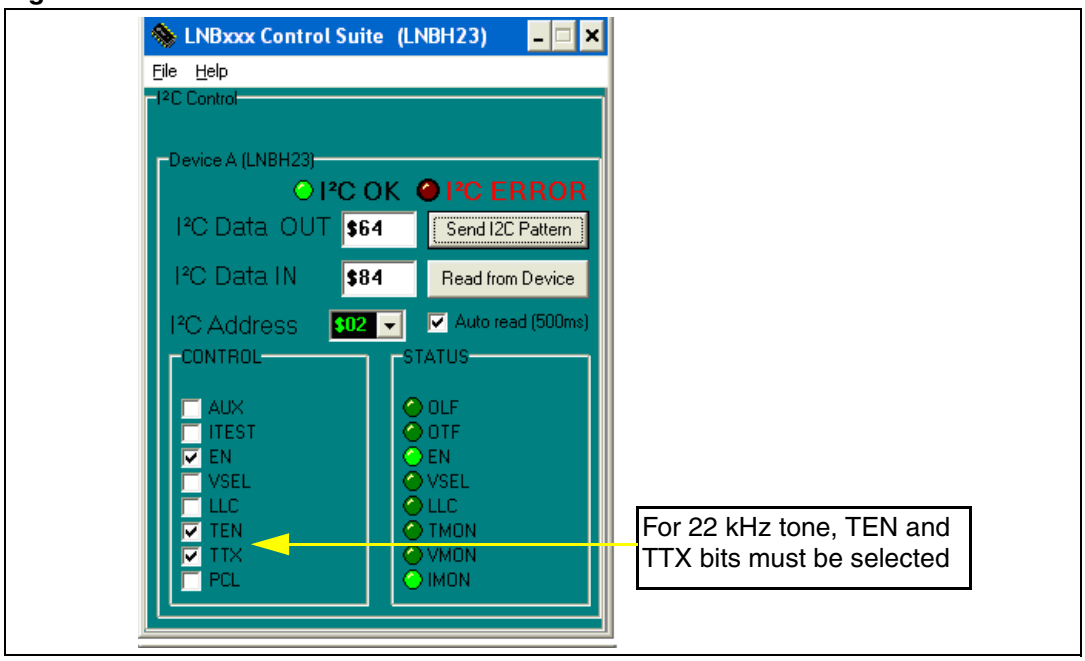
Figure 33. LLC activation



The screenshot in *Figure 34* shows the following conditions:

- EN=1, TEN=TTX=1
- Vout=13.4 V_{typ} + 22 kHz tone

Figure 34. Tone activation

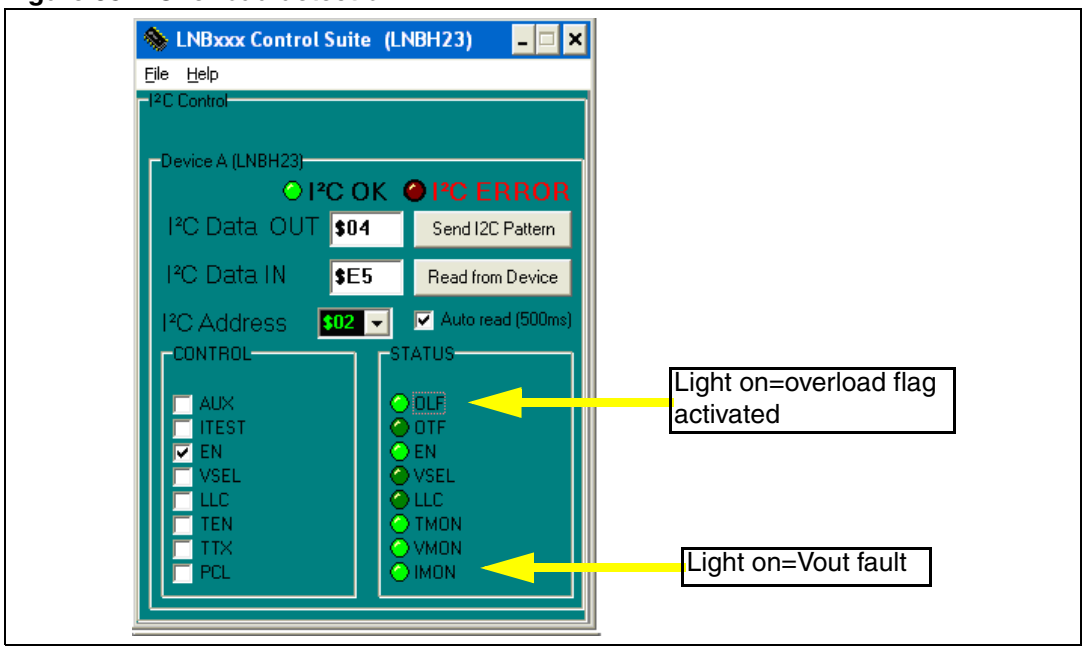


Overload condition

If the OLF (overload flag) indicator is on, a fault condition on the output has been detected and the status of this bit is changed. It turns off when the fault condition is removed.

- EN=1
- Vout=fault, OLF=1

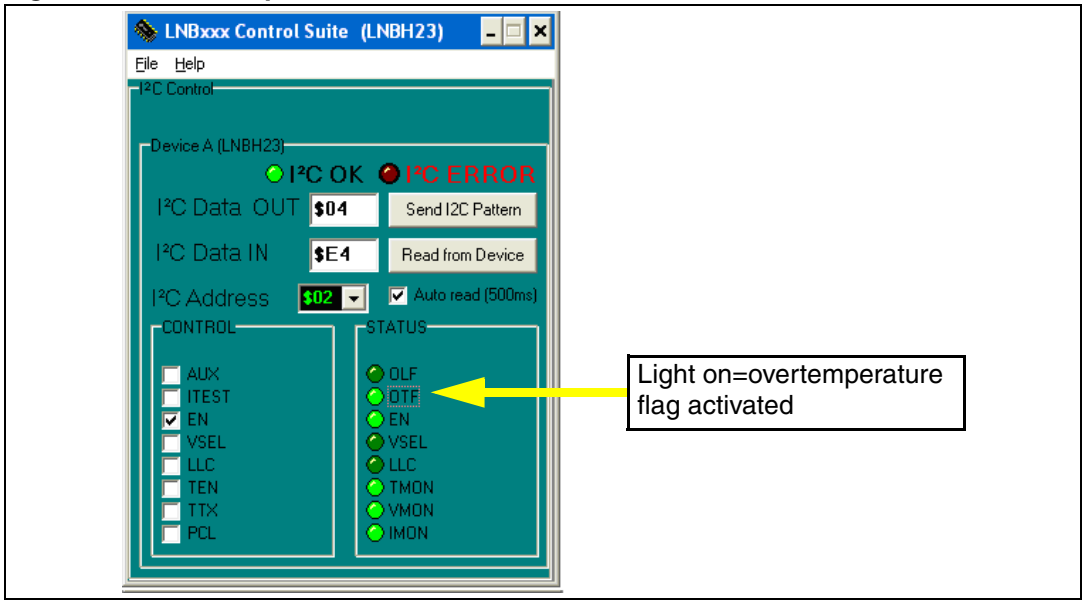
Figure 35. Overload detection



The screenshot in *Figure 36* shows the following conditions:

- EN=1
- Vout=fault, OTF=1

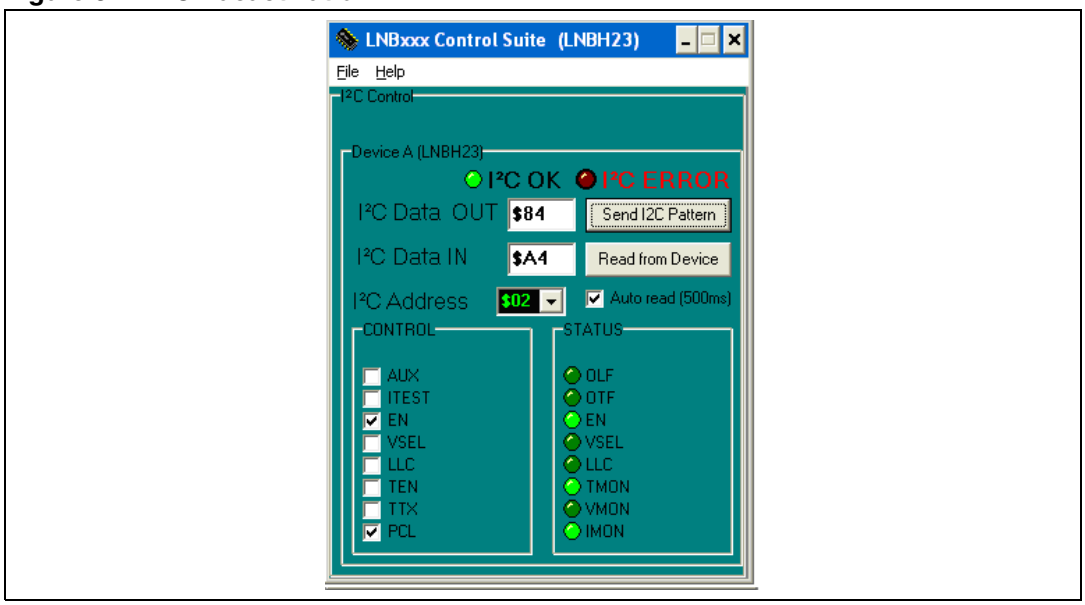
Figure 36. Overtemperature detection



If the PCL checkbox is checked, a simple output short-circuit current clamp is set. If not, the overcurrent protection circuit works dynamically: as soon as an overload is detected, the output current is provided for 90 ms (typ.), after which the output is set in shutdown for a time TOFF of 900 ms (typ). Simultaneously, the diagnostic OLF I²C bit of the system register is set high. This feature allows the reduction of the total power dissipation during an overload or a short-circuit condition:

- EN=1, PCL=1
- Vout=13.4 V_{typ}

Figure 37. PCL deactivation



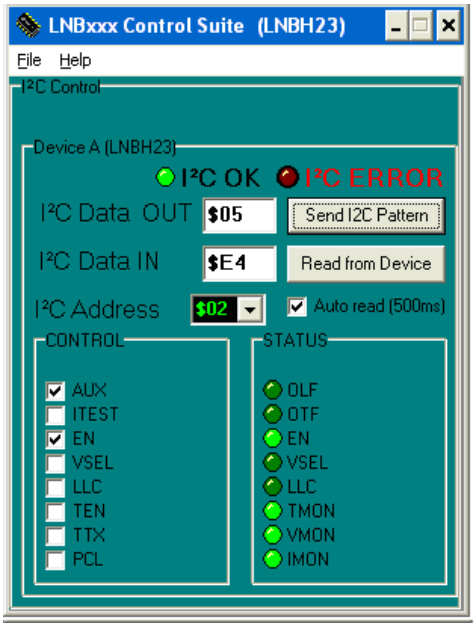
The AUX bit can be set high to force the LNBH23 output voltage to the highest voltage on the line (22 V typ.) during the minimum current diagnostic phase, in order to detect the output load and check the dish status or any optional devices inserted on the line.

The maximum current detected at ITEST=0 is 6 mA, while at ITEST=1 it is 12 mA.

During the minimum diagnostic current test, setting only EN=ITEST=AUX=1 is recommended. The screenshot in *Figure 38* shows the following conditions:

- EN=1, AUX=1
- Vout=22 V (for testing multiswitch-box dish connection)

Figure 38. AUX activation



7 Revision history

Table 7. Document revision history

Date	Revision	Changes
13-Nov-2009	1	Initial release.