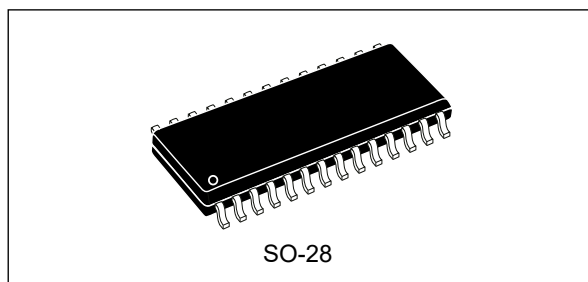


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**Triple half-bridge high-voltage gate driver**

---

**Features**

- High voltage rail up to 600 V
- Driver current capability:
  - STDRIVE601:
    - 200 mA source current @ 25 °C
    - 350 mA sink current @ 25 °C
- dV/dt transient immunity  $\pm 50$  V/ns
- Gate driving voltage range from 9 V to 20 V
- Overall input-output propagation delay: 85 ns
- Matched propagation delay for all channels
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Integrated bootstrap diodes
- Comparator for fast overcurrent protection
- Smart shutdown function
- Interlocking and deadtime function
- Dedicated Enable pin
- UVLO function on low-side and high-sides

**Applications**

- 3-phase motor drives
- Inverters

**Description**

The STDRIVE601 is a high voltage device manufactured with BCD6s offline technology. It is a single-chip with three half-bridge gate drivers for N-channel power MOSFETs or IGBTs suitable for 3-phase applications.

All device outputs can sink and source 350 mA and 200 mA respectively. Prevention from cross conduction is ensured by interlocking and deadtime function.

The device has dedicated input pins for each output and a shutdown pin. The logic inputs are CMOS/TTL compatible down to 3.3 V for easy interfacing with control devices. Matched delays between low-side and high-side sections guarantee no cycle distortion and allow high frequency operation.

The STDRIVE601 embeds a comparator featuring advanced SmartSD function also integrated in the device, ensuring fast and effective protection against fault events like overcurrent, overtemperature, etc.

Dedicated UVLO protection on the low-sides and each of the high-side driving sections allow to prevent the power switches from operating in low efficiency or dangerous conditions.

The integrated bootstrap diodes as well as all of the integrated features of this IC make the application PCB design easier, more compact and simple thus reducing the overall bill of material.

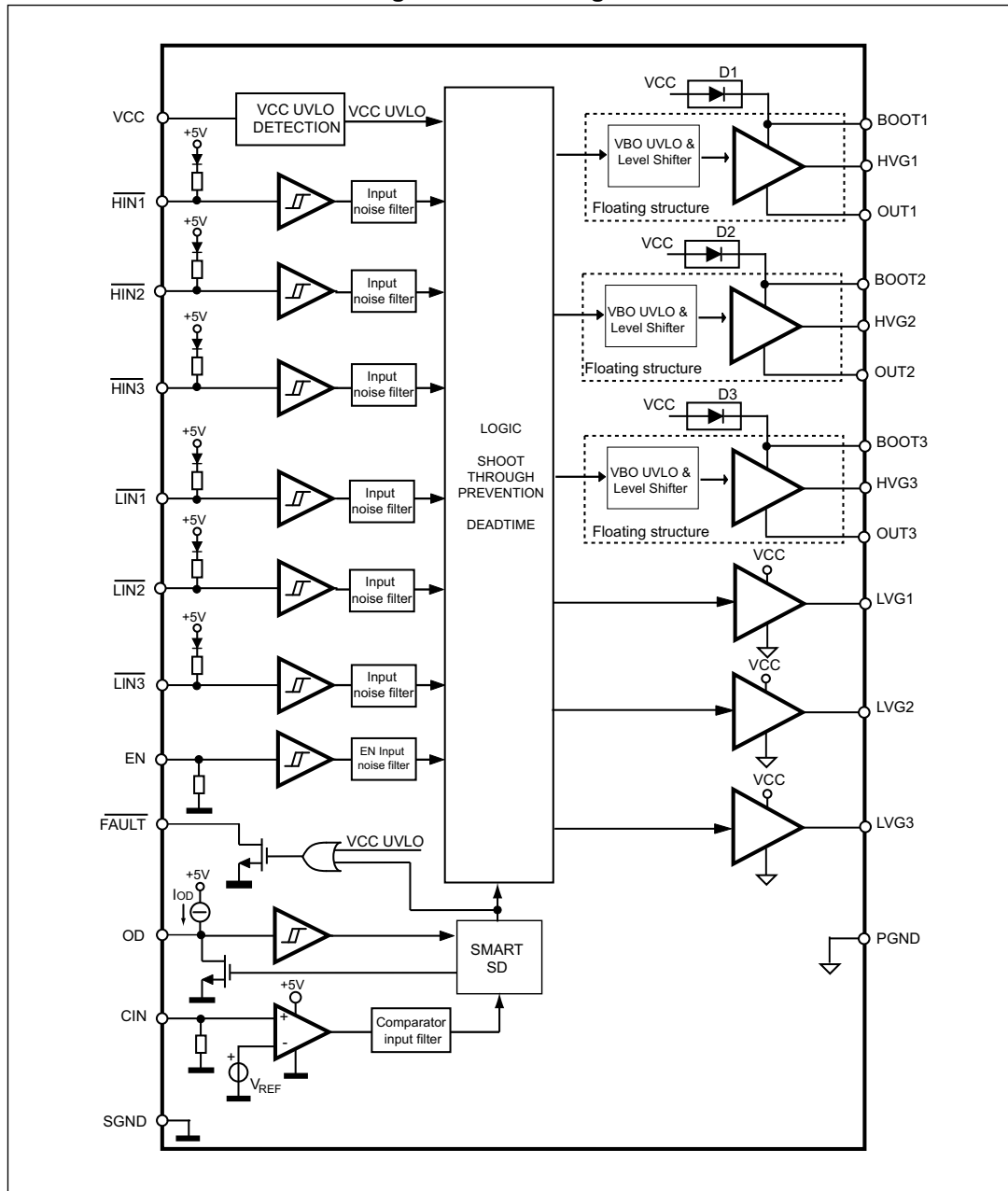
The device is available in SO-28 package.

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# 1 Block diagram

Figure 1. Block diagram



## 2 Pin description and connection diagram

Figure 2. Pin connection (top view)

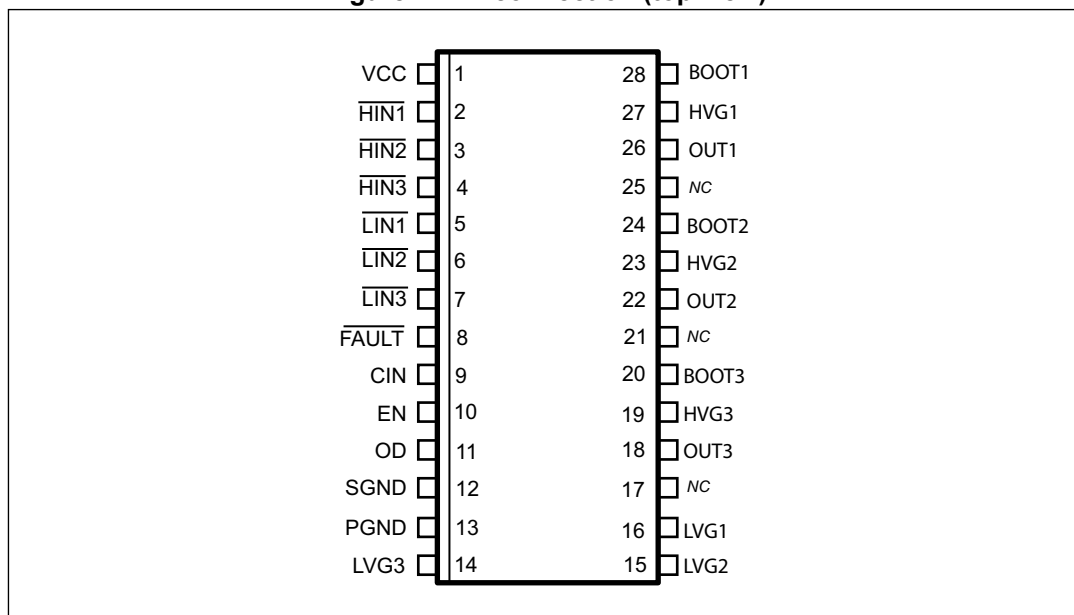


Table 1. Pin description

| Pin #     | Pin Name            | Type          | Function                                                    |
|-----------|---------------------|---------------|-------------------------------------------------------------|
| 1         | VCC                 | Power Supply  | Low-side and logic supply voltage                           |
| 2         | HIN1                | Logic Input   | High-side driver logic input 1                              |
| 3         | HIN2                | Logic Input   | High-side driver logic input 2                              |
| 4         | HIN3                | Logic Input   | High-side driver logic input 3                              |
| 5         | LIN1                | Logic Input   | Low-side driver logic input 1                               |
| 6         | LIN2                | Logic Input   | Low-side driver logic input 2                               |
| 7         | LIN3                | Logic Input   | Low-side driver logic input 3                               |
| 8         | FAULT               | OD Output     | Fault output                                                |
| 9         | CIN                 | Analog Input  | Comparator positive input                                   |
| 10        | EN                  | Logic Input   | Enable input, active high                                   |
| 11        | OD                  | OD Output     | SmartSD timing Open Drain output, unlatch and restart input |
| 12        | SGND                | Power Supply  | Signal ground                                               |
| 13        | PGND                | Power Supply  | Low-side driver ground                                      |
| 14        | LVG3 <sup>(1)</sup> | Analog Output | Low-side driver output 3                                    |
| 15        | LVG2 <sup>(1)</sup> | Analog Output | Low-side driver output 2                                    |
| 16        | LVG1 <sup>(1)</sup> | Analog Output | Low-side driver output 1                                    |
| 17, 21 25 | N.C.                | -             | Not Connected                                               |

Table 1. Pin description (continued)

| Pin # | Pin Name            | Type          | Function                                     |
|-------|---------------------|---------------|----------------------------------------------|
| 18    | OUT3                | Power Supply  | High-side (floating) common voltage driver 3 |
| 19    | HVG3 <sup>(1)</sup> | Analog Output | High-side driver output 3                    |
| 20    | BOOT3               | Power Supply  | Bootstrap supply voltage 3                   |
| 22    | OUT2                | Power Supply  | High-side (floating) common voltage driver 2 |
| 23    | HVG2 <sup>(1)</sup> | Analog Output | High-side driver output 2                    |
| 24    | BOOT2               | Power Supply  | Bootstrap supply voltage 2                   |
| 26    | OUT1                | Power Supply  | High-side (floating) common voltage driver 1 |
| 27    | HVG1 <sup>(1)</sup> | Analog Output | High-side driver output 1                    |
| 28    | BOOT1               | Power Supply  | Bootstrap supply voltage 1                   |

1. The circuit guarantees less than 1 V on the LVG and HVG pins (at  $I_{\text{sink}} = 10 \text{ mA}$ ), with  $V_{\text{CC}} > 3 \text{ V}$ . This allows omitting the "bleeder" resistor connected between the gate and the source of the external MOSFETs normally used to hold the pin low.

### 3 Electrical data

#### 3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings<sup>(1)</sup>

| Symbol                         | Parameter                          | Min.                    | Max.                    | Unit |
|--------------------------------|------------------------------------|-------------------------|-------------------------|------|
| VCC                            | Logic supply voltage               | -0.3                    | 21                      | V    |
| V <sub>PGND</sub>              | Low-side driver ground             | VCC - 21                | VCC + 0.3               | V    |
| V <sub>PS</sub> <sup>(2)</sup> | Low-side drivers ground            | -21                     | 21                      | V    |
| V <sub>OUT</sub>               | Output voltage                     | V <sub>BOOT</sub> - 21  | V <sub>BOOT</sub> + 0.3 | V    |
| V <sub>BOOT</sub>              | Bootstrap voltage                  | - 0.3                   | 620                     | V    |
| V <sub>HVG</sub>               | High-side gate output voltage      | V <sub>OUT</sub> - 0.3  | V <sub>BOOT</sub> + 0.3 | V    |
| V <sub>LVG</sub>               | Low-side gate output voltage       | V <sub>PGND</sub> - 0.3 | VCC + 0.3               | V    |
| V <sub>CIN</sub>               | Comparator input voltage           | - 0.3                   | 20                      | V    |
| V <sub>i</sub>                 | Logic input voltage <sup>(3)</sup> | - 0.3                   | 15                      | V    |
| V <sub>OD</sub>                | OD pin voltage                     | - 0.3                   | 21                      | V    |
| V <sub>FAULT</sub>             | FAULT pin voltage                  | - 0.3                   | 21                      | V    |
| dV <sub>OUT</sub> /dt          | Common mode transient Immunity     |                         | 50                      | V/ns |
| T <sub>J</sub>                 | Junction temperature               | -40                     | 150                     | °C   |
| T <sub>S</sub>                 | Storage temperature                | -50                     | 150                     | °C   |
| ESD                            | Human body model                   | 1                       |                         | kV   |

1. Each voltage referred to SGND unless otherwise specified.

2. V<sub>PS</sub> = PGND - SGND.

3. EN, LINx, HINx.

#### 3.2 Thermal data

Table 3. Thermal data

| Symbol              | Parameter                                             | Value | Unit |
|---------------------|-------------------------------------------------------|-------|------|
| R <sub>th(JA)</sub> | Thermal resistance junction to ambient <sup>(1)</sup> | 52    | °C/W |

1. JEDEC 2s2p PCB in still air.

### 3.3 Recommended operating conditions

**Table 4. Recommended operating conditions<sup>(1)</sup>**

| Symbol                         | Parameter                              | Test conditions | Min.               | Max. | Unit |
|--------------------------------|----------------------------------------|-----------------|--------------------|------|------|
| VCC                            | Logic supply voltage                   |                 | 9                  | 20   | V    |
| V <sub>LS</sub> <sup>(2)</sup> | Low-side drivers supply voltage        |                 | 4                  | 20   | V    |
| V <sub>PS</sub> <sup>(3)</sup> | Low-side drivers ground                |                 | -5                 | 5    | V    |
| V <sub>BO</sub> <sup>(4)</sup> | Floating supply voltage <sup>(4)</sup> |                 | 8.5                | 20   | V    |
| V <sub>OUT</sub>               | DC Output voltage                      |                 | -10 <sup>(5)</sup> | 580  | V    |
| V <sub>CIN</sub>               | Comparator input voltage               |                 | 0                  | 15   | V    |
| V <sub>I</sub>                 | Logic input voltage                    |                 | 0                  | 15   | V    |
| V <sub>OD</sub>                | OD pin voltage                         |                 | 0                  | 20   | V    |
| V <sub>FAULT</sub>             | FAULT pin voltage                      |                 | 0                  | 20   | V    |
| F <sub>SW</sub> <sup>(6)</sup> | Maximum switching frequency            |                 |                    | 800  | kHz  |
| PW <sup>(7)</sup>              | Minimum input pulse width              |                 | 100                |      | ns   |
| T <sub>J</sub>                 | Junction temperature                   |                 | -40                | 125  | °C   |

1. Each voltage referred to SGND unless otherwise specified.

2. V<sub>LS</sub> = VCC - PGND.

3. V<sub>PS</sub> = PGND - SGND.

4. V<sub>BO</sub> = BOOT - OUT.

5. VCC = 9 V, LVG off. Logic is operational if V<sub>BOOT</sub> > 5 V.

6. Actual maximum F<sub>SW</sub> depends on power dissipation.

7. Pulse width on LIN or HIN pins. See [Figure 3](#).

## 4 Electrical characteristics

HIN is referred to channels HIN1, HIN2, HIN3; LIN is referred to channels LIN1, LIN2, LIN3.

**Table 5. Electrical characteristics**  
(VCC = 15 V; PGND = SGND; TJ = +25 °C, unless otherwise specified)

| Symbol                                           | Pin                           | Parameter                                             | Test conditions                                                                | Min. | Typ. | Max. | Unit |
|--------------------------------------------------|-------------------------------|-------------------------------------------------------|--------------------------------------------------------------------------------|------|------|------|------|
| Low-side section supply                          |                               |                                                       |                                                                                |      |      |      |      |
| VCC <sub>THON</sub>                              |                               | VCC UVLO turn-on threshold                            |                                                                                | 8    | 8.5  | 9    | V    |
| VCC <sub>THOFF</sub>                             |                               | VCC UVLO turn-off threshold                           |                                                                                | 7.5  | 8    | 8.5  | V    |
| VCC <sub>HYS</sub>                               |                               | VCC UVLO hysteresis                                   |                                                                                | 0.4  | 0.5  | 0.6  | V    |
| I <sub>QCCU</sub>                                |                               | VCC undervoltage quiescent supply current             | VCC = 7 V;<br>EN = 5 V;<br>CIN = SGND<br>LVG & HVG: OFF                        |      | 430  | 744  | μA   |
| I <sub>QCC</sub>                                 |                               | VCC quiescent supply current                          | EN = 5 V;<br>CIN = SGND<br>LVG & HVG: OFF                                      |      | 950  | 1450 | μA   |
| High-side floating section supply <sup>(1)</sup> |                               |                                                       |                                                                                |      |      |      |      |
| V <sub>BOTHON</sub>                              | 20 - 18<br>24 - 22<br>28 - 26 | V <sub>BO</sub> UVLO turn-on threshold                |                                                                                | 7.5  | 8    | 8.5  | V    |
| V <sub>BOTHOFF</sub>                             |                               | V <sub>BO</sub> UVLO turn-off threshold               |                                                                                | 7    | 7.5  | 8    | V    |
| V <sub>BOHYS</sub>                               |                               | V <sub>BO</sub> UVLO hysteresis                       |                                                                                | 0.4  | 0.5  | 0.6  | V    |
| I <sub>QBOU</sub>                                |                               | V <sub>BO</sub> undervoltage quiescent supply current | VCC = V <sub>BO</sub> = 6.5 V;<br>EN = 5 V;<br>CIN = SGND<br>LVG OFF; HVG = ON |      | 25   | 62   | μA   |
| I <sub>QBO</sub>                                 |                               | V <sub>BO</sub> quiescent supply current              | V <sub>BO</sub> = 15 V<br>EN = 5 V;<br>CIN = SGND<br>LVG OFF; HVG = ON         |      | 84   | 150  | μA   |
| I <sub>LK</sub>                                  |                               | High voltage leakage current                          | BOOT = HVG = OUT = 620V                                                        |      |      | 15   | μA   |
| R <sub>Dboot</sub>                               |                               | Bootstrap Diode on resistance                         |                                                                                |      | 215  |      | Ω    |

**Table 5. Electrical characteristics**  
**(VCC = 15 V; PGND = SGND; TJ = +25 °C, unless otherwise specified) (continued)**

| Symbol                 | Pin                          | Parameter                                 | Test conditions                          | Min. | Typ. | Max. | Unit |
|------------------------|------------------------------|-------------------------------------------|------------------------------------------|------|------|------|------|
| Output driving buffers |                              |                                           |                                          |      |      |      |      |
| I <sub>SO</sub>        | 14, 15,<br>16, 19,<br>23, 27 | High/Low-side source<br>peak current      | TJ = 25°C                                | 160  | 200  | 300  | mA   |
|                        |                              |                                           | Full temperature<br>range <sup>(2)</sup> | 130  |      | 350  |      |
| I <sub>SI</sub>        |                              | High/Low-side sink<br>peak current        | TJ = 25°C                                | 230  | 350  | 430  | mA   |
|                        |                              |                                           | Full temperature<br>range <sup>(2)</sup> | 200  |      | 500  |      |
| R <sub>DSonON</sub>    |                              | High/Low-side source<br>R <sub>DSon</sub> | I = 10 mA                                | 24   | 35   | 46   | Ω    |
| R <sub>DSonOFF</sub>   |                              | High/Low-side sink<br>R <sub>DSon</sub>   | I = 10 mA                                | 11   | 16   | 21   | Ω    |
| Logic Inputs           |                              |                                           |                                          |      |      |      |      |
| V <sub>il</sub>        | 2, 3, 4,<br>5, 6, 7,<br>10   | Low level logic<br>threshold voltag       |                                          | 0.8  |      | 1.4  | V    |
| V <sub>ih</sub>        |                              | High level logic<br>threshold voltage     |                                          | 1.8  |      | 2.3  | V    |
| V <sub>hyst</sub>      | 2, 3, 4,<br>5, 6, 7,<br>10   | Logic input threshold<br>hysteresis       |                                          | 0.8  |      | 1.2  | V    |
| V <sub>SSDIh</sub>     | 11                           | SmartSD restart<br>threshold              |                                          | 3.5  | 3.8  | 4.1  | V    |
| V <sub>SSDI</sub>      |                              | SmartSD unlatch<br>threshold              |                                          |      | 0.56 | 0.75 | V    |
| I <sub>LINh</sub>      | 5, 6, 7                      | LIN logic “1” input bias<br>current       | V <sub>LINx</sub> = 15 V                 |      |      | 1    | μA   |
| I <sub>LINI</sub>      |                              | LIN logic “0” input bias<br>current       | V <sub>LINx</sub> = 0 V                  | 28   | 43   | 58   | μA   |
| I <sub>HINh</sub>      | 2, 3, 4                      | HIN logic “1” input<br>bias current       | V <sub>HINx</sub> = 15 V                 |      |      | 1    | μA   |
| I <sub>HINI</sub>      |                              | HIN logic “0” input<br>bias current       | V <sub>HINx</sub> = 0                    | 28   | 43   | 58   | μA   |
| R <sub>PU_IN</sub>     | 2, 3, 4,<br>5, 6, 7          | Logic input pull-up<br>resistor           |                                          | 75   | 100  | 125  | kΩ   |
| I <sub>ENh</sub>       | 10                           | EN logic “1” input bias<br>current        | V <sub>EN</sub> = 15 V                   | 110  | 150  | 200  | μA   |
| I <sub>ENI</sub>       |                              | EN logic "0" input bias<br>current        | V <sub>EN</sub> = 0 V                    |      |      | 1    | μA   |
| R <sub>PD_EN</sub>     | 10                           | EN pull-down resistor                     |                                          | 75   | 100  | 125  | kΩ   |

**Table 5. Electrical characteristics**  
**(VCC = 15 V; PGND = SGND; TJ = +25 °C, unless otherwise specified) (continued)**

| Symbol                                          | Pin | Parameter                                                       | Test conditions                                                                                                       | Min. | Typ. | Max. | Unit |
|-------------------------------------------------|-----|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| <b>Sense comparator<sup>(3)</sup> and FAULT</b> |     |                                                                 |                                                                                                                       |      |      |      |      |
| V <sub>REF</sub>                                |     | Internal voltage reference                                      |                                                                                                                       | 410  | 460  | 510  | mV   |
| C <sub>INhyst</sub>                             | 9   | Comparator input hysteresis                                     |                                                                                                                       | 40   | 70   |      | mV   |
| C <sub>IN_PD</sub>                              | 9   | Comparator input pull-down current                              | V <sub>CIN</sub> = 1 V                                                                                                | 7    | 10   | 13   | μA   |
| I <sub>OD</sub>                                 | 11  | OD internal current source                                      |                                                                                                                       | 2.5  | 5    | 7.5  | μA   |
| R <sub>ON_OD</sub>                              | 11  | OD On resistance                                                | I <sub>OD</sub> = 16 mA                                                                                               | 19   | 25   | 36   | Ω    |
| I <sub>OL_OD</sub>                              | 11  | OD low level sink current                                       | V <sub>OD</sub> = 400 mV                                                                                              | 11   | 16   | 21   | mA   |
| I <sub>SAT_OD</sub>                             | 11  | OD saturation current                                           | V <sub>OD</sub> = 5 V                                                                                                 |      | 95   |      | mA   |
| V <sub>FLOAT_OD</sub>                           | 11  | OD floating voltage level                                       | OD connected only to an external capacitance                                                                          | 4.2  | 4.7  | 5    | V    |
| R <sub>ON_F</sub>                               | 8   | FAULT ON resistance                                             | I <sub>FAULT</sub> = 8 mA                                                                                             |      | 50   | 100  | Ω    |
| I <sub>OL_F</sub>                               | 8   | FAULT low level sink current                                    | V <sub>FAULT</sub> = 400 mV                                                                                           | 4    | 8    | 12   | mA   |
| t <sub>OD</sub>                                 | 11  | Comparator propagation delay                                    | R <sub>pu</sub> = 100 kΩ to 5 V;<br>voltage step on<br>C <sub>IN</sub> = 0 to 3.3 V;<br>50% C <sub>IN</sub> to 90% OD |      | 350  | 500  | ns   |
| t <sub>CIN-F</sub>                              | 11  | Comparator triggering to FAULT                                  | voltage step on<br>C <sub>IN</sub> = 0 to 3.3 V;<br>50% C <sub>IN</sub> to 90%<br>FAULT                               |      | 350  | 500  | ns   |
| t <sub>CINoff</sub>                             | 11  | Comparator triggering to high/low-side driver propagation delay | voltage step on<br>C <sub>IN</sub> = 0 to 3.3 V;<br>50% C <sub>IN</sub> to 90%<br>LVG/HVG                             |      | 360  | 510  | ns   |
| t <sub>FCIN</sub>                               | 11  | Comparator input filter time                                    |                                                                                                                       | 200  | 300  | 400  | ns   |
| SR                                              | 11  | OD Slew rate                                                    | C <sub>L</sub> = 1 nF;<br>R <sub>pu</sub> = 33 kΩ to 5 V;<br>90% to 10% OD                                            | 20   | 60   | 100  | V/μs |

**Table 5. Electrical characteristics**  
**(VCC = 15 V; PGND = SGND; TJ = +25 °C, unless otherwise specified) (continued)**

| Symbol                         | Pin                                    | Parameter                                               | Test conditions                                                    | Min. | Typ. | Max. | Unit |
|--------------------------------|----------------------------------------|---------------------------------------------------------|--------------------------------------------------------------------|------|------|------|------|
| <b>Dynamic characteristics</b> |                                        |                                                         |                                                                    |      |      |      |      |
| $t_{on}$                       | 2 vs. 27<br>3 vs 23<br>4 vs 19         | High/Low-side driver turn-on propagation delay          | OUT = 0 V<br>BOOT = VCC<br>$C_L = 1\text{ nF}$<br>Vin = 0 to 3.3 V | 45   | 85   | 120  | ns   |
| $t_{off}$                      | 5 vs. 16<br>6 vs. 15<br>7 vs. 14       | High/Low-side driver turn-off propagation delay         |                                                                    | 45   | 85   | 120  | ns   |
| $t_{EN}$                       | 10 vs.<br>14, 15,<br>16, 19,<br>23, 27 | Enable to high/low-side driver propagation delay        |                                                                    | 245  | 385  | 520  | ns   |
| $t_{FIN}$                      | 2,3,4,<br>5,6,7                        | LIN HIN input filter time                               |                                                                    | 30   | 40   | 50   | ns   |
| $t_{FEN}$                      | 10                                     | EN input filter time                                    |                                                                    | 200  | 300  | 400  | ns   |
| $t_r$                          | 14, 15,<br>16, 19,<br>23, 27           | Rise time                                               | $C_L = 1\text{ nF}$                                                |      | 120  | 160  | ns   |
| $t_f$                          |                                        | Fall time                                               | $C_L = 1\text{ nF}$                                                |      | 50   | 75   | ns   |
| MT                             |                                        | Delay matching high/low side turn-on/off <sup>(4)</sup> |                                                                    |      | 0    | 30   | ns   |
| DT                             |                                        | Deadtime                                                | $C_L = 1\text{ nF}$                                                | 200  | 300  | 400  | ns   |
| MDT                            |                                        | Matching deadtime <sup>(5)</sup>                        | $C_L = 1\text{ nF}$                                                |      | 0    | 50   | ns   |

1.  $V_{BO} = \text{BOOT} - \text{OUT}$ .

2. Values provided by characterization, not tested.

3. Comparator is disabled when VCC is in UVLO condition.

4.  $MT = \max. (|t_{on}(LVG) - t_{off}(LVG)|, |t_{on}(HVG) - t_{off}(HVG)|, |t_{off}(LVG) - t_{on}(HVG)|, |t_{off}(HVG) - t_{on}(LVG)|)$ .

5.  $MDT = |DT_{LH} - DT_{HL}|$ , refer to [Figure 5](#).

Figure 3. Propagation delay timing definition

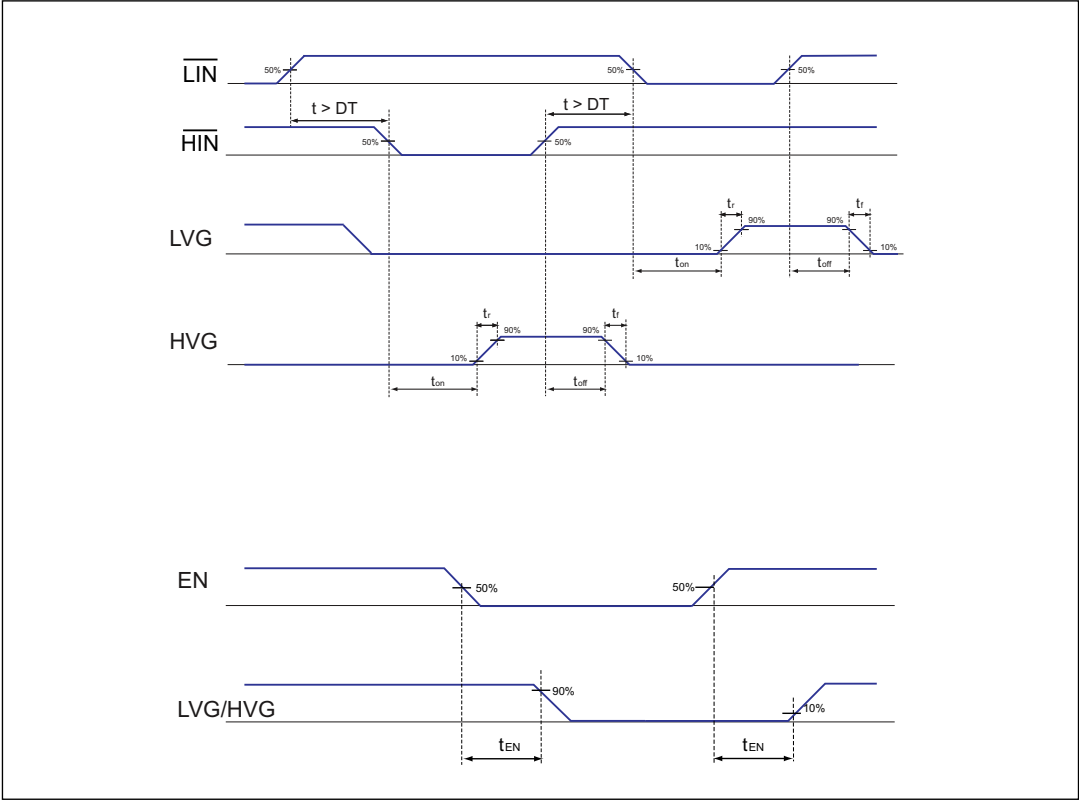


Figure 4. Deadtime timing definitions

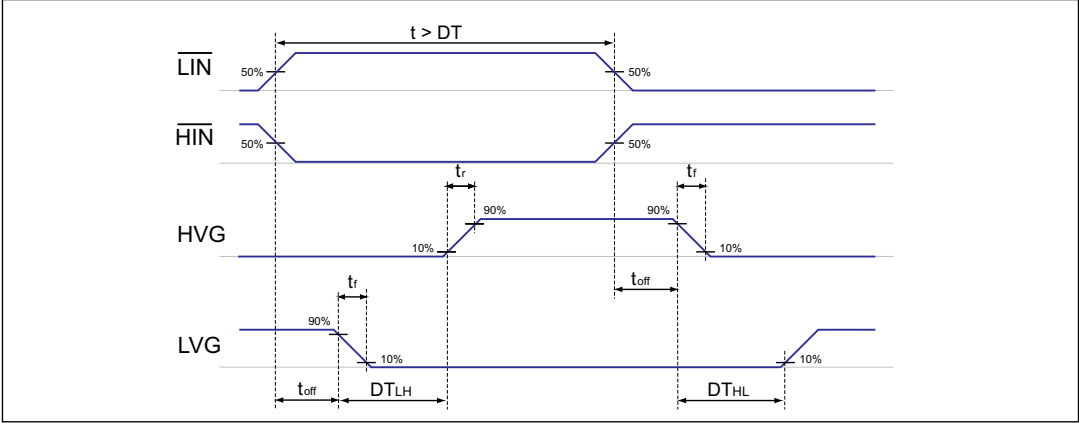
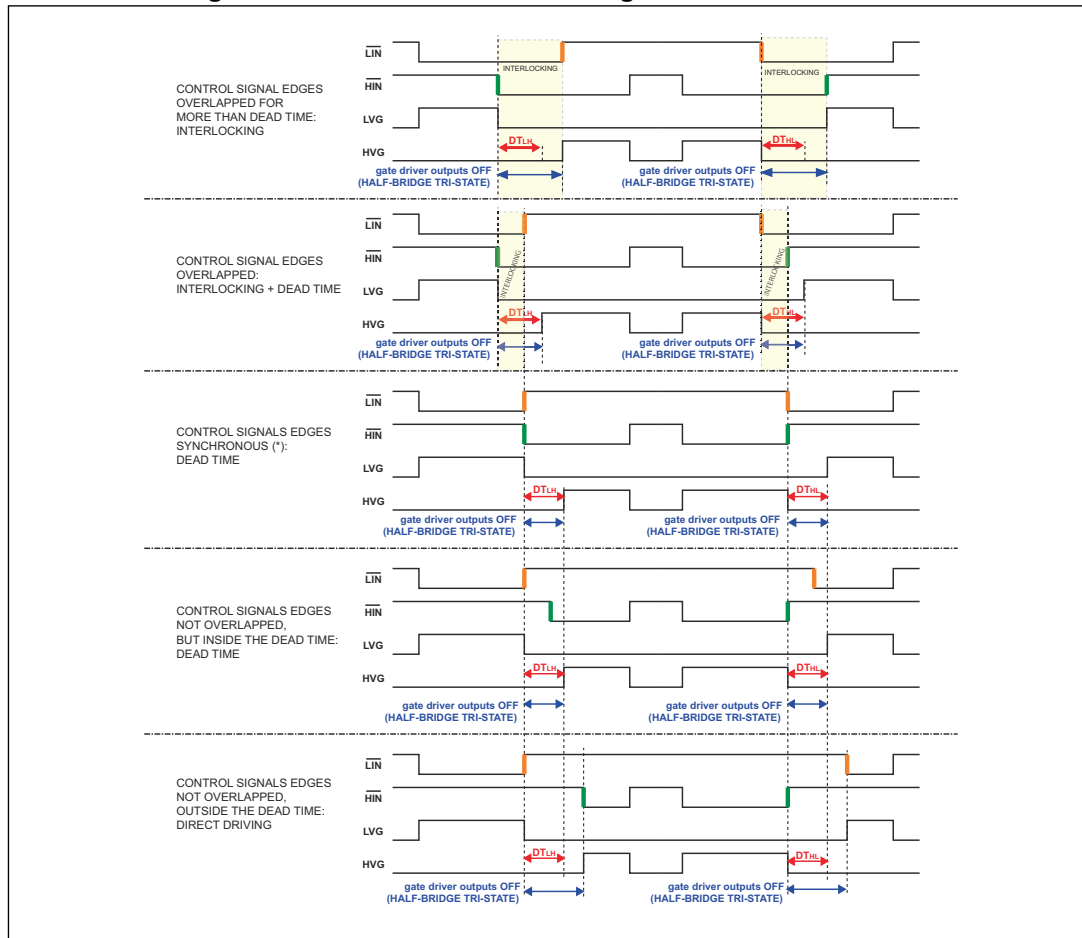


Figure 5. Deadtime and interlocking waveforms definition



## 5 Functional description

### 5.1 Inputs and outputs

The devices are controlled through the following logic inputs:

- EN: Enable input, active high;
- LIN: low-side driver inputs, active low;
- HIN: high-side driver inputs, active low.

**Table 6. Inputs truth table (applicable when device is not in UVLO or SmartSD protection)**

|                     | Input pins |                         |                         | Output pins |             |
|---------------------|------------|-------------------------|-------------------------|-------------|-------------|
|                     | EN         | $\overline{\text{LIN}}$ | $\overline{\text{HIN}}$ | LVG         | HVG         |
|                     | L          | X                       | X                       | Low         | Low         |
|                     | H          | H                       | H                       | Low         | Low         |
|                     | H          | L                       | H                       | <b>High</b> | Low         |
|                     | H          | H                       | L                       | Low         | <b>High</b> |
| <b>Interlocking</b> | H          | L                       | L                       | Low         | Low         |

The FAULT and OD pins are open-drain outputs.

The FAULT signal is set low in case VCC UVLO is detected, or in case the SmartShutDown comparator triggers an event. It is only used to signal a UVLO or SmartSD activation to external circuits, and its state does not affect the behavior of other functions or circuits inside the driver. The OD behavior is explained in [Section 5.5](#).

When EN is set low, gate driver outputs are forced low and assure low impedance.

### 5.2 Deadtime

The deadtime feature, in companion with interlocking feature, guarantees that driver outputs of the same channel are not high simultaneously and at least a DT time passes between the turn-off of one driver's output and the turn-on of the companion output of the same channel. If a deadtime longer than the internal DT is applied to LIN and HIN inputs by the external controller, the internal DT is ignored and the outputs follow the deadtime determined by the inputs.

Refer to [Figure 4](#) for the dead time and interlocking waveforms.

### 5.3 VCC UVLO protection

Undervoltage protection is available on VCC and BOOT supply pins. In order to avoid intermittent operation, a hysteresis set the turn-off threshold with respect to the turn-on threshold.

When VCC voltage goes below  $V_{CCthOFF}$  threshold all the outputs are switched off, both LVG and HVG. When VCC voltage reaches  $V_{CCthON}$  threshold the driver returns to normal operation and sets the LVG outputs according to actual input pins status; HVG is also set according to input pin status if the corresponding  $V_{BO}$  section is not in UVLO condition.

The FAULT output is kept low when VCC is in UVLO condition. The following figures show some examples of typical operation conditions.

**Figure 6. VCC power ON and UVLO, LVG timing<sup>(a)</sup>**

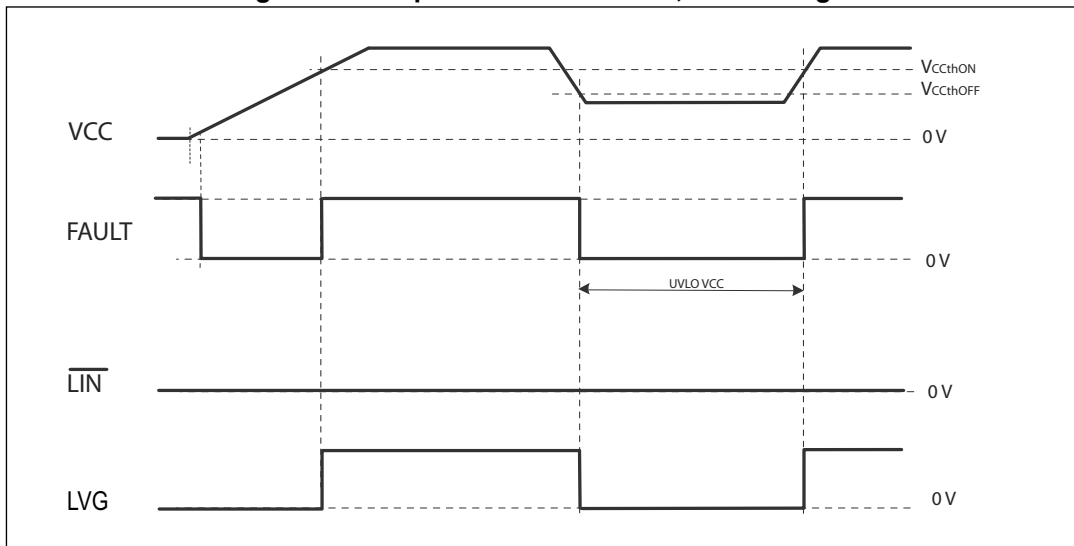
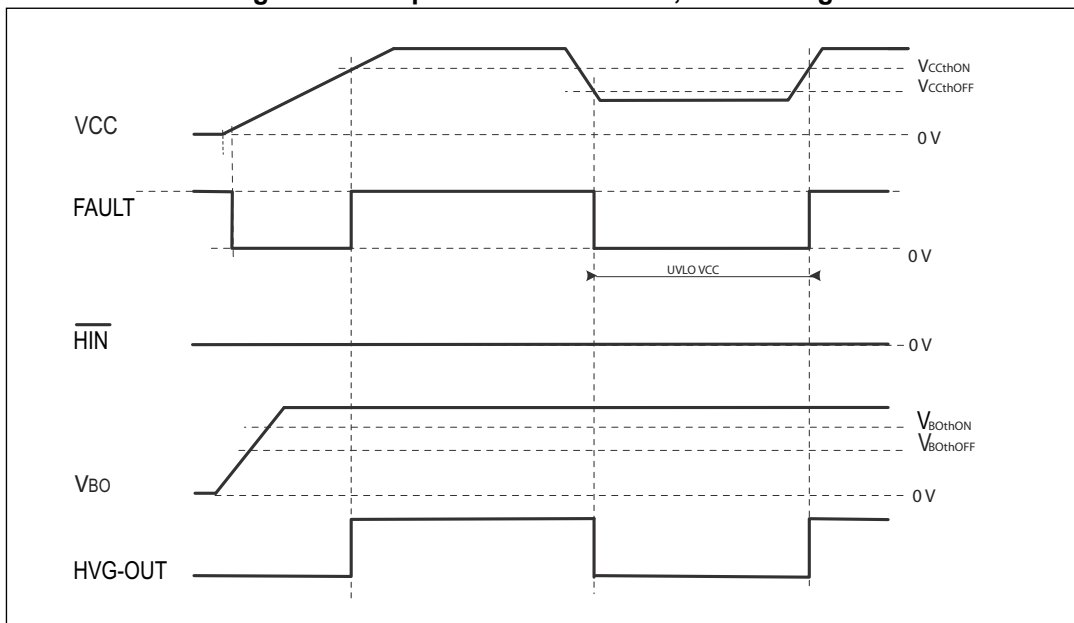


**Figure 7. VCC power ON and UVLO, HVG timing<sup>(a)</sup>**



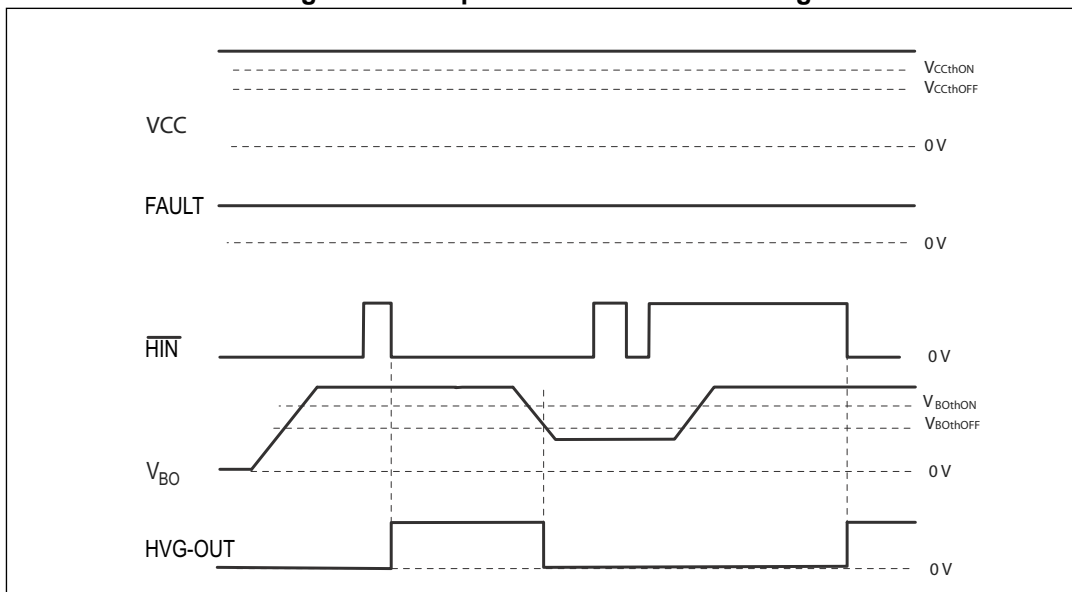
a. Fault pin connected to external pull-up.

## 5.4 VBO UVLO protection

Dedicated undervoltage protection is available on each bootstrap section between BOOTx and OUTx supply pins. In order to avoid intermittent operation, a hysteresis sets the turn-off threshold with respect to the turn-on threshold.

When  $V_{BO}$  voltage goes below  $V_{BOTHOFF}$  threshold, the HVG output of corresponding bootstrap section is switched off. When  $V_{BO}$  voltage reaches  $V_{BOTHON}$  threshold device returns to normal operation and the output remains off up to the next input pins transition that requests HVG to turn on.

Figure 8. VBO power-ON and UVLO timing



## 5.5 Comparator and smart shutdown

These devices integrate a comparator committed to the fault protection function, thanks to the SmartShutDown (SmartSD) circuit.

The SmartSD architecture allows immediate turn-off of the gate driver outputs in the case of overload or overcurrent condition, by minimizing the propagation delay between the fault detection event and the actual output switch-off. In fact, the time delay between the fault detection and the output turn-off is not dependent on the value of the external components connected to the OD pin, which are only used to set the duration of disable time after the fault.

This provides the possibility to increase the duration of the *output disable time* after the fault event up to very large values without increasing the delay time of the protection. The duration of the disable time is determined by the values of the external capacitor  $C_{OD}$  and of the optional pull-up resistor connected to OD pin.

The comparator has an internal voltage reference  $V_{REF}$  connected to the inverting input, while the non-inverting input is available on the CIN pin. The comparator's CIN input can be connected to an external shunt resistor in order to implement a fast and simple overcurrent protection function. The output signal of the comparator is filtered from glitches shorter than  $t_{FCIN}$  and then fed to the SmartSD logic.

If the impulse on CIN pin is higher than  $V_{REF}$  and wider than  $t_{FCIN}$ , the SmartSD logic is triggered and immediately sets all of the driver outputs to low-level (OFF).

At the same time, FAULT is forced low to signal the event (for example to an MCU input) and OD starts to discharge the external  $C_{OD}$  capacitor used to set the duration of the output disable time of the fault event.

The FAULT pin is released and driver outputs restart following the input pins as soon as the *output disable time* expires.

The overall disable time is composed of two phases:

- The *OD unlatch time* ( $t_1$  in [Figure 9](#)), which is the time required to discharge  $C_{OD}$  capacitor down to  $V_{SSDI}$  threshold. The discharge starts as soon as the SmartSD comparator is triggered.
- The *OD restart time* ( $t_2$  in [Figure 9](#)), which is the time required to recharge the  $C_{OD}$  capacitor up to the  $V_{SSDh}$  threshold. The recharge of  $C_{OD}$  starts when the OD internal MOSFET is turned-off, which happens when the fault condition has been removed ( $CIN < V_{REF} - C_{INhyst}$ ) and the voltage on OD reaches the  $V_{SSDI}$  threshold. This time normally covers most of the overall output disable time.

If no external pull-up is connected to OD, the external  $C_{OD}$  capacitor is discharged with a time constant defined by  $C_{OD}$  and the internal MOSFET's characteristic (Equation 1), and the *Restart time* is determined by the internal current source  $I_{OD}$  and by  $C_{OD}$  (Equation 2).

Equation 1

$$t_1 \cong R_{ON\_OD} \cdot C_{OD} \cdot \ln \left( \frac{V_{OD}}{V_{SSDI}} \right)$$

Equation 2

$$t_2 \cong \frac{C_{OD} \cdot V_{SSDh}}{I_{OD}} \cdot \ln \left( \frac{V_{SSDI} - V_{OD}}{V_{SSDh} - V_{OD}} \right)$$

In case the OD pin is connected to VCC by an external pull-up resistor  $R_{OD\_ext}$ , the OD discharge time is determined by the external network  $R_{OD\_ext}$   $C_{OD}$  and by the internal MOSFET's  $R_{ON\_OD}$  ([Equation 3](#)), while the *Restart time* is determined by current in  $R_{OD\_ext}$  ([Equation 4](#)).

Equation 3

$$t_1 \cong C_{OD} \cdot (R_{OD\_ext} // R_{ON\_OD}) \cdot \ln \left( \frac{V_{OD} - V_{on}}{V_{SSDI} - V_{on}} \right)$$

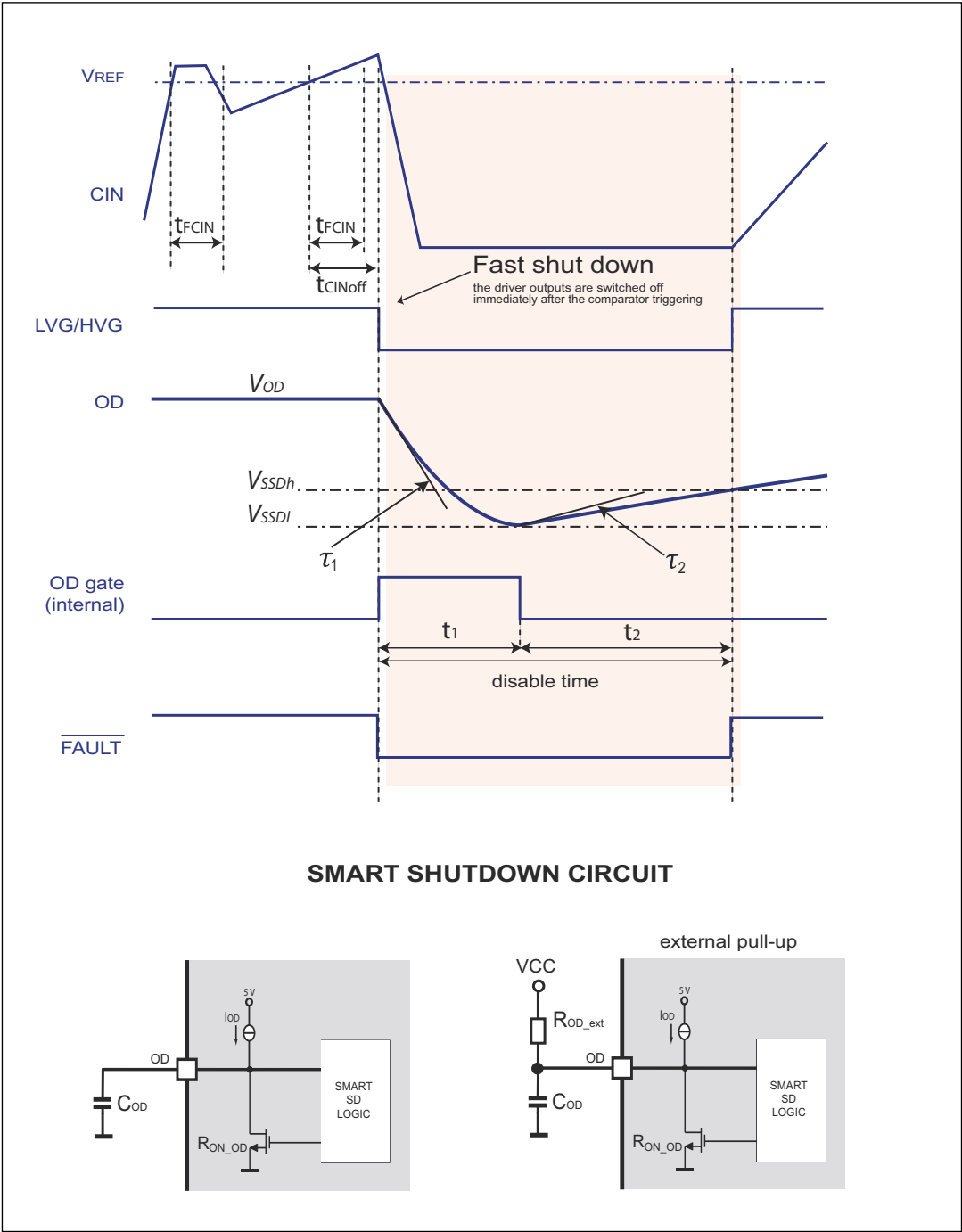
Equation 4

$$t_1 \cong C_{OD} \cdot R_{OD\_ext} \cdot \ln \left( \frac{V_{SSDI} - V_{OD}}{V_{SSDh} - V_{OD}} \right)$$

where

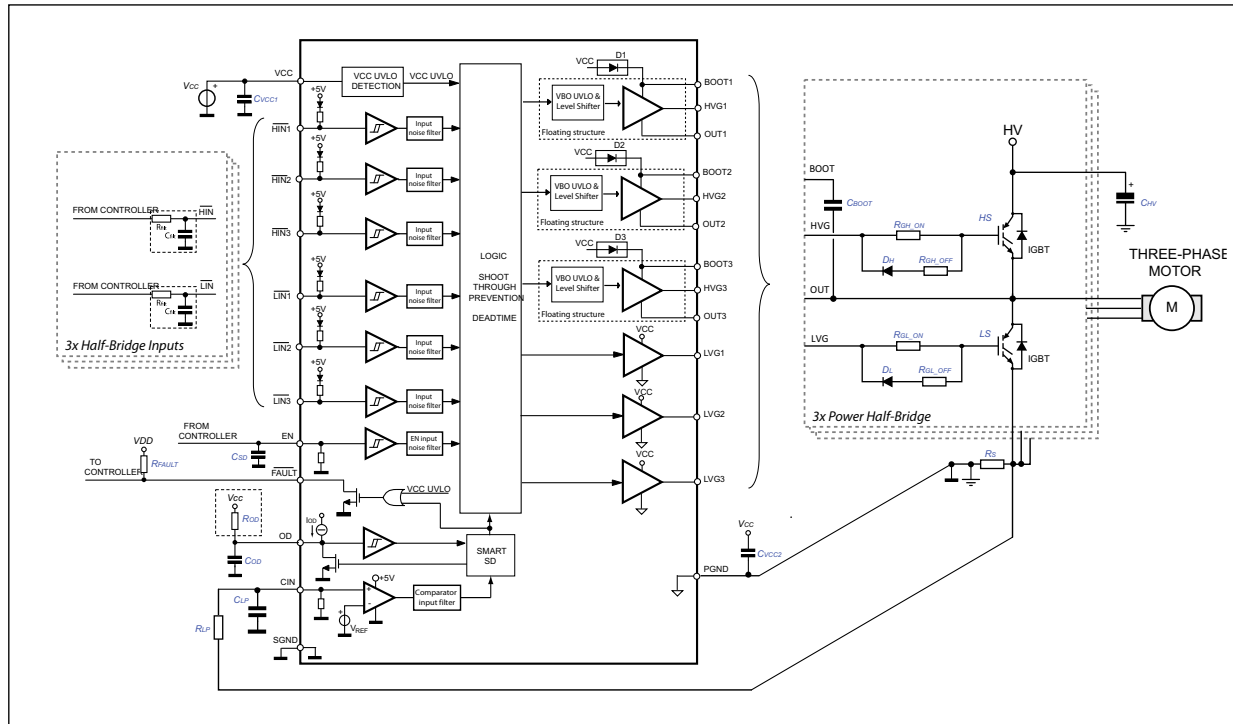
$$V_{on} = \frac{R_{ON\_OD}}{R_{OD\_ext} + R_{ON\_OD}} \cdot VCC; \quad V_{OD} = VCC$$

Figure 9. Smart shutdown timing waveforms



## 6 Typical application diagram

**Figure 10. Typical application diagram**



## 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 7.1 SO-28 package information

Table 7. SO-28 package dimensions

| Dim. | Mm    |      |       | NOTES   |
|------|-------|------|-------|---------|
|      | Min.  | Typ. | Max.  |         |
| A    | 2.35  |      | 2.65  |         |
| A1   | 0.10  |      | 0.30  |         |
| B    | 0.33  |      | 0.51  |         |
| C    | 0.23  |      | 0.32  |         |
| D    | 17.70 |      | 18.10 |         |
| E    | 7.40  |      | 7.60  |         |
| e    |       | 1.27 |       |         |
| H    | 10.00 |      | 10.65 |         |
| h    | 0.25  |      | 0.75  |         |
| L    | 0.40  |      | 1.27  |         |
| k    | 0     |      | 8     | DEGREES |
| ddd  |       |      | 0.10  |         |

Figure 11. SO-28 mechanical data

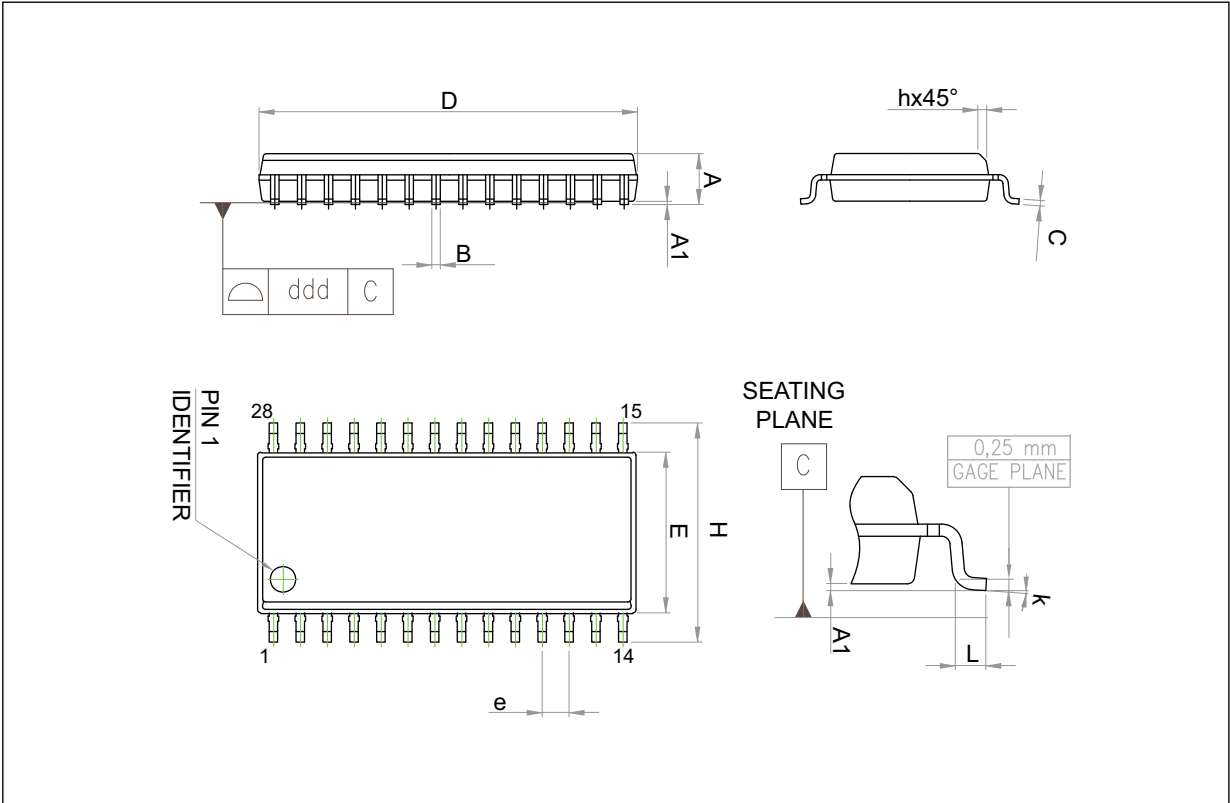
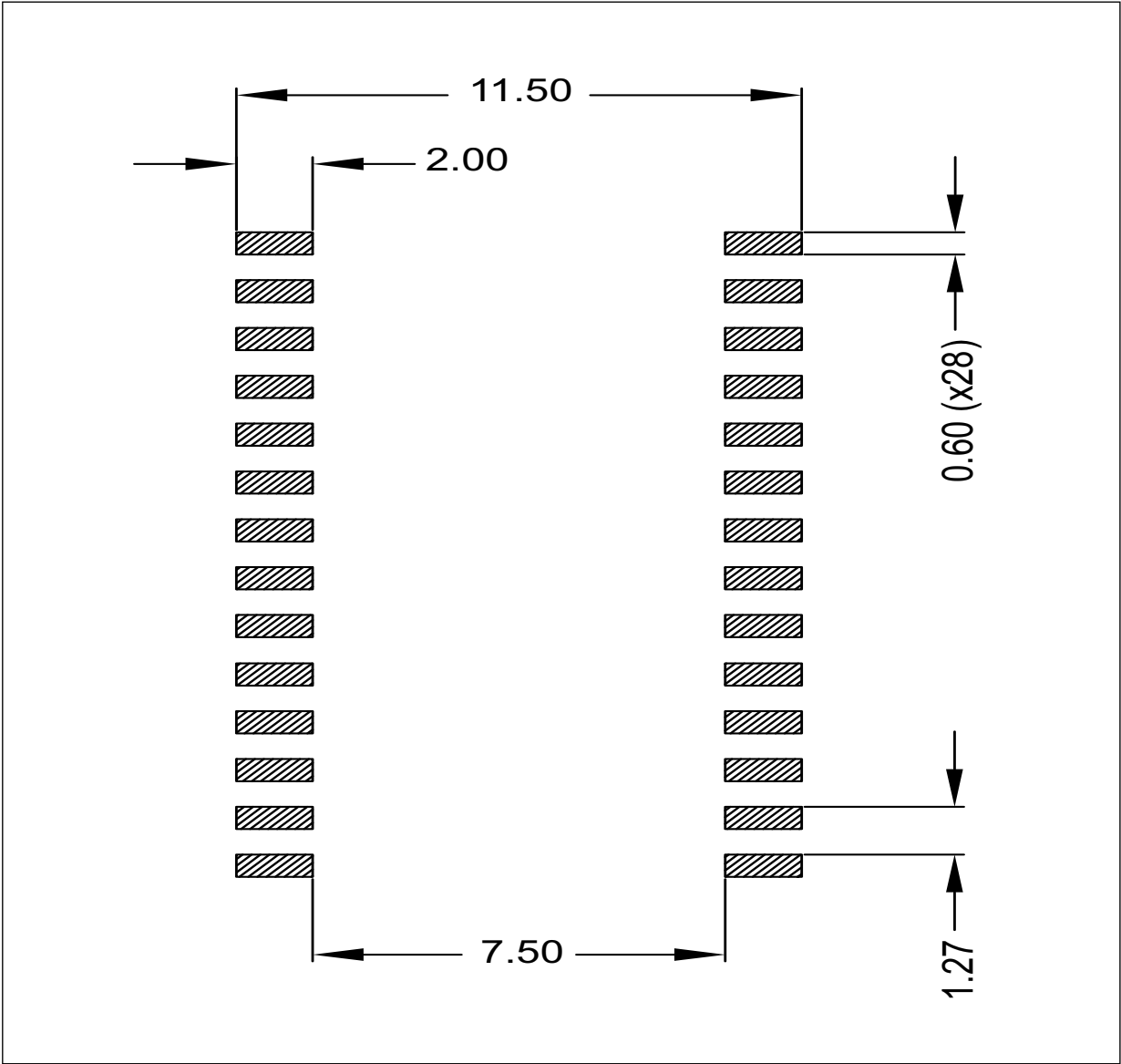


Figure 12. SO-28 suggested land pattern



## 8 Ordering information

**Table 8. Order codes**

| Order code   | Package | Marking  | Packaging     |
|--------------|---------|----------|---------------|
| STDRIVE601   | SO-28   | STDRV601 | Tube          |
| STDRIVE601TR | SO-28   | STDRV601 | Tape and reel |

## 9 Revision history

**Table 9. Document history**

| Date        | Revision | Changes          |
|-------------|----------|------------------|
| 21-May-2019 | 1        | Initial release. |

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