

N-channel 60 V, 0.07 Ω typ., 12 A, STripFET™ II Power MOSFET in an IPAK package

Datasheet - production data

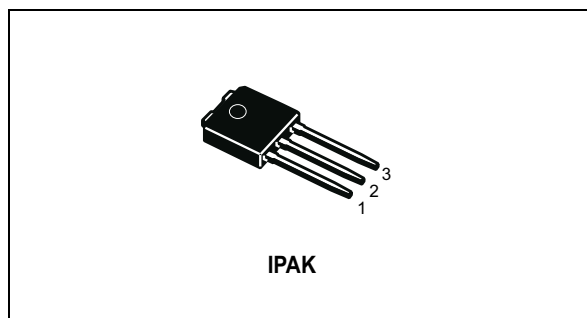
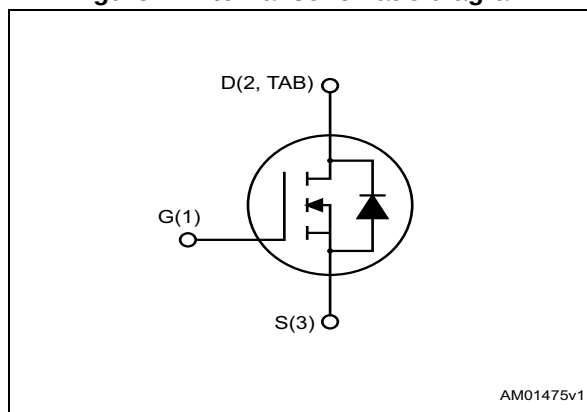


Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD12NF06L-1	60 V	0.09 Ω	12 A

- Exceptional dv/dt capability
- Low gate charge

Applications

- Switching applications

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET™ process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Table 1. Device summary

Order code	Marking	Package	Packaging
STD12NF06L-1	D12NF06L	IPAK	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 16	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	12	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	8.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	48	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	30	W
	Derating factor	0.2	W/ $^{\circ}\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	100	mJ
T_{stg}	Storage temperature	-55 to 175	$^{\circ}\text{C}$
T_J	Max. operating junction temperature		

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 12\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DS} \leq 40\text{ V}$, $T_J \leq T_{JMAX}$
3. Starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = 6\text{ A}$, $V_{DD} = 30\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	5	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max.	100	$^{\circ}\text{C}/\text{W}$

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$,	60			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 60$			1	μA
		$V_{GS} = 0, V_{DS} = 60$ $T_C = 125\text{ °C}$			10	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0$ $V_{GS} = \pm 16\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1		2	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 6\text{ A}$		0.07	0.09	Ω
		$V_{GS} = 5\text{ V}, I_D = 6\text{ A}$		0.08	0.10	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$		350		pF
C_{oss}	Output capacitance			75		pF
C_{rss}	Reverse transfer capacitance			30		pF
Q_g	Total gate charge	$V_{DD} = 48\text{ V}, I_D = 12\text{ A}$ $V_{GS} = 5\text{ V}$ (see Figure 14)		7.5	10	nC
Q_{gs}	Gate-source charge			2.5		nC
Q_{gd}	Gate-drain charge			3.0		nC

Table 6. Switching times

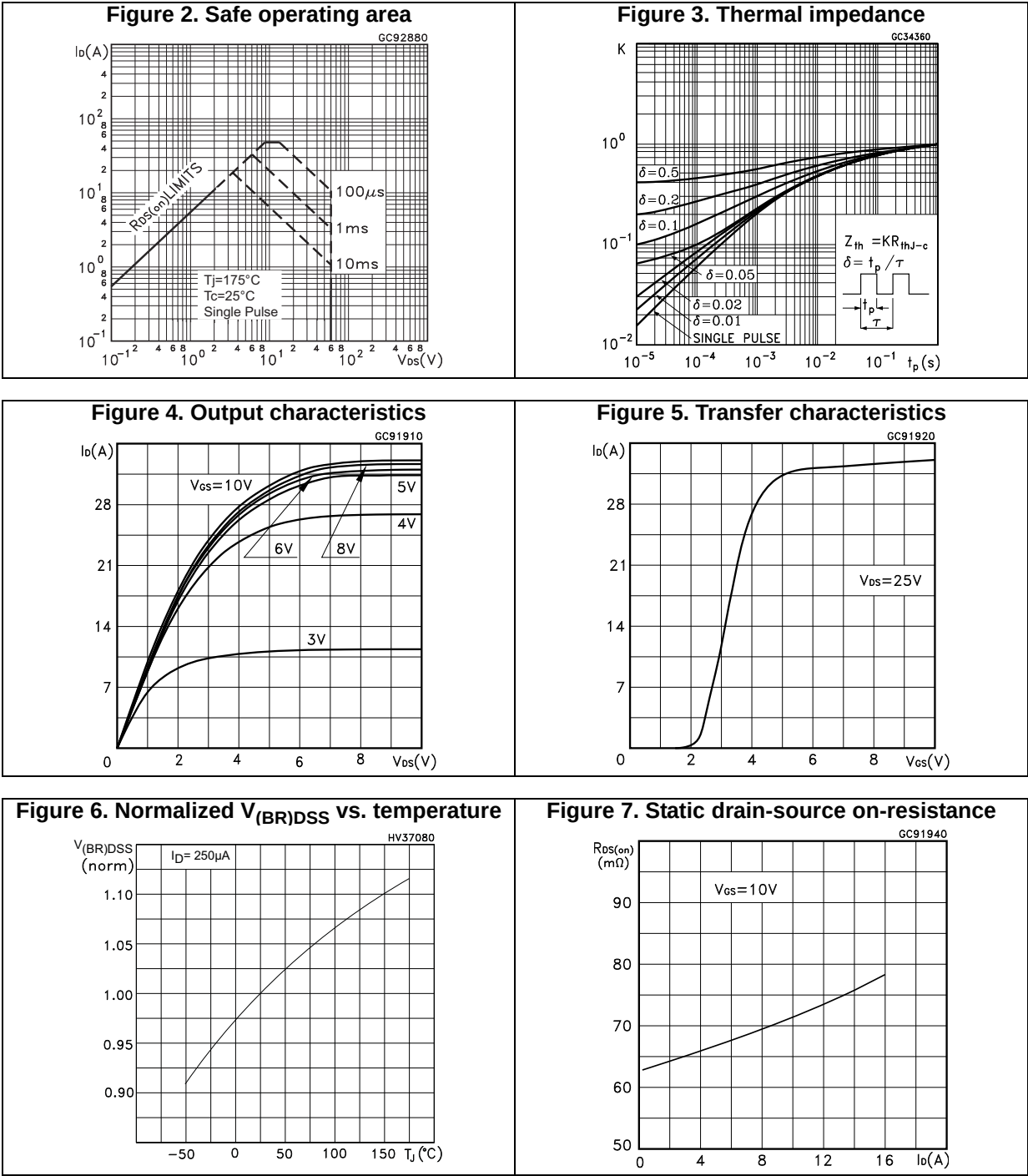
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{ V}, I_D = 6\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 4.5\text{ V}$ (see Figure 13)		10		ns
t_r	Rise time			35		ns
$t_{d(off)}$	Turn-off delay time			20		ns
t_f	Fall time			13		ns

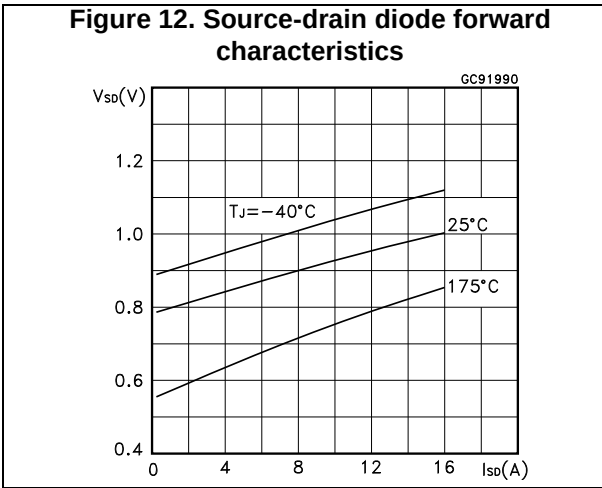
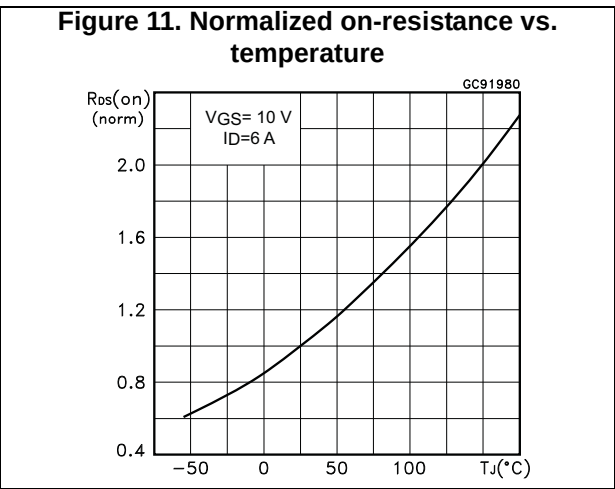
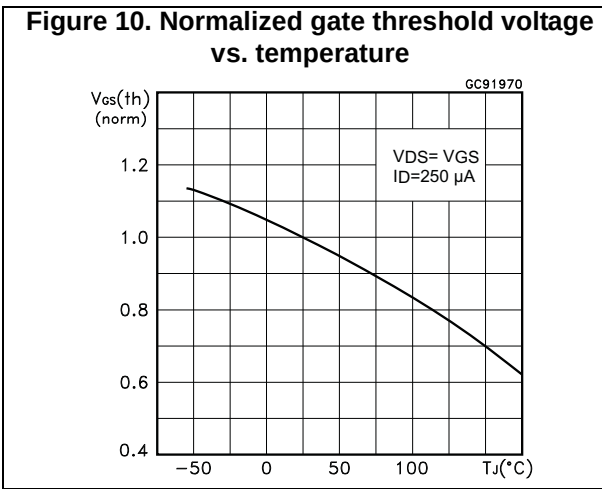
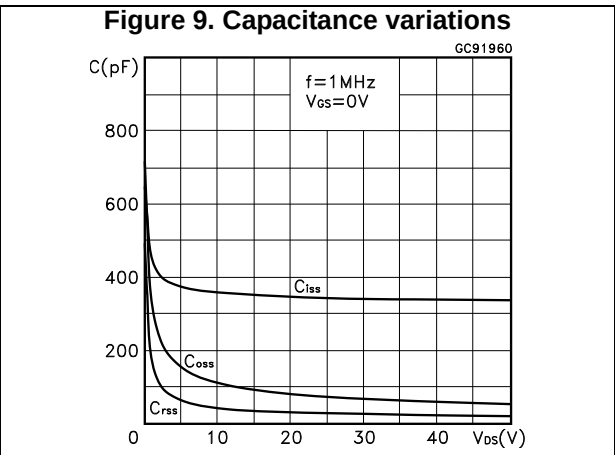
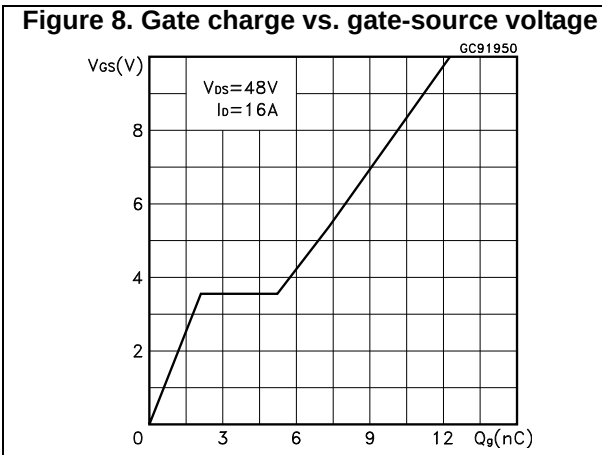
Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				12	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				48	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 12\text{ A}$, $V_{GS} = 0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 16\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 15)		50		ns
Q_{rr}	Reverse recovery charge			65		nC
I_{RRM}	Reverse recovery current			2.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

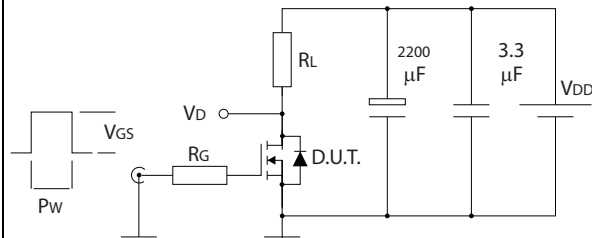
2.1 Electrical characteristics (curves)





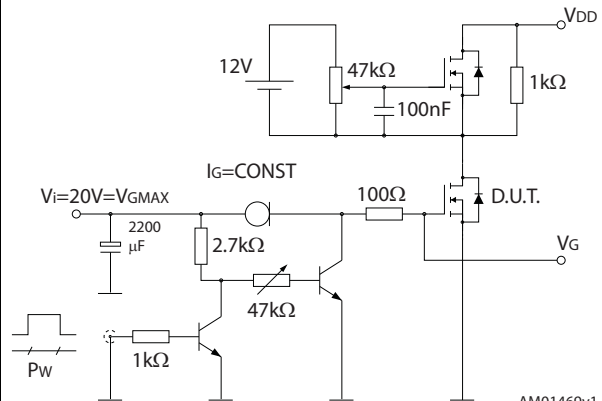
3 Test circuit

Figure 13. Switching times test circuit for resistive load



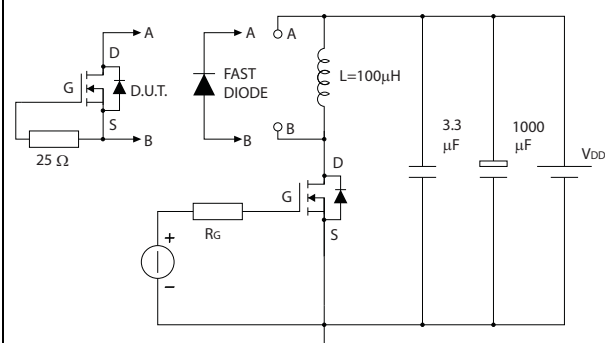
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Figure 14. Gate charge test circuit



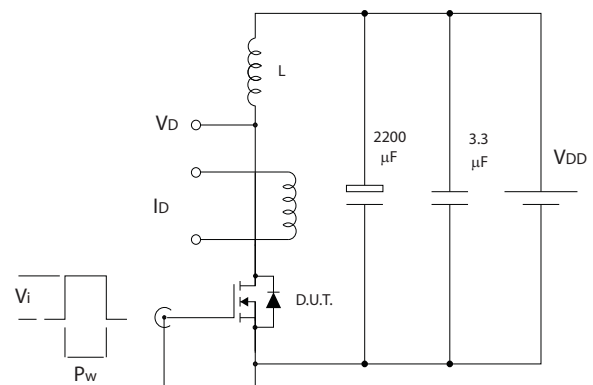
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Figure 15. Test circuit for inductive load switching and diode recovery times



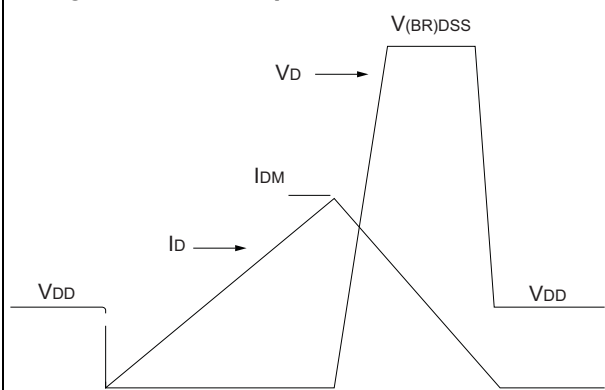
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Figure 16. Unclamped inductive load test circuit



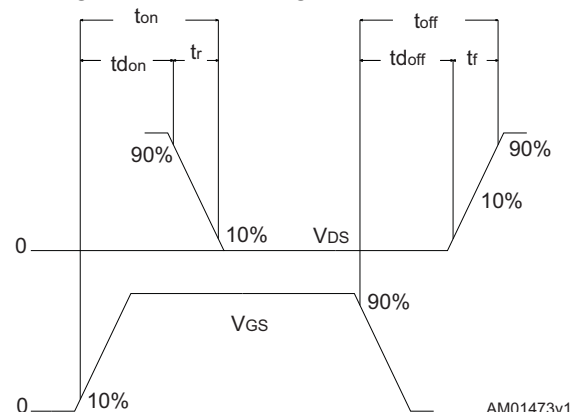
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Figure 17. Unclamped inductive waveform



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Figure 18. Switching time waveform



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4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 19. IPAK (TO-251) type A drawing

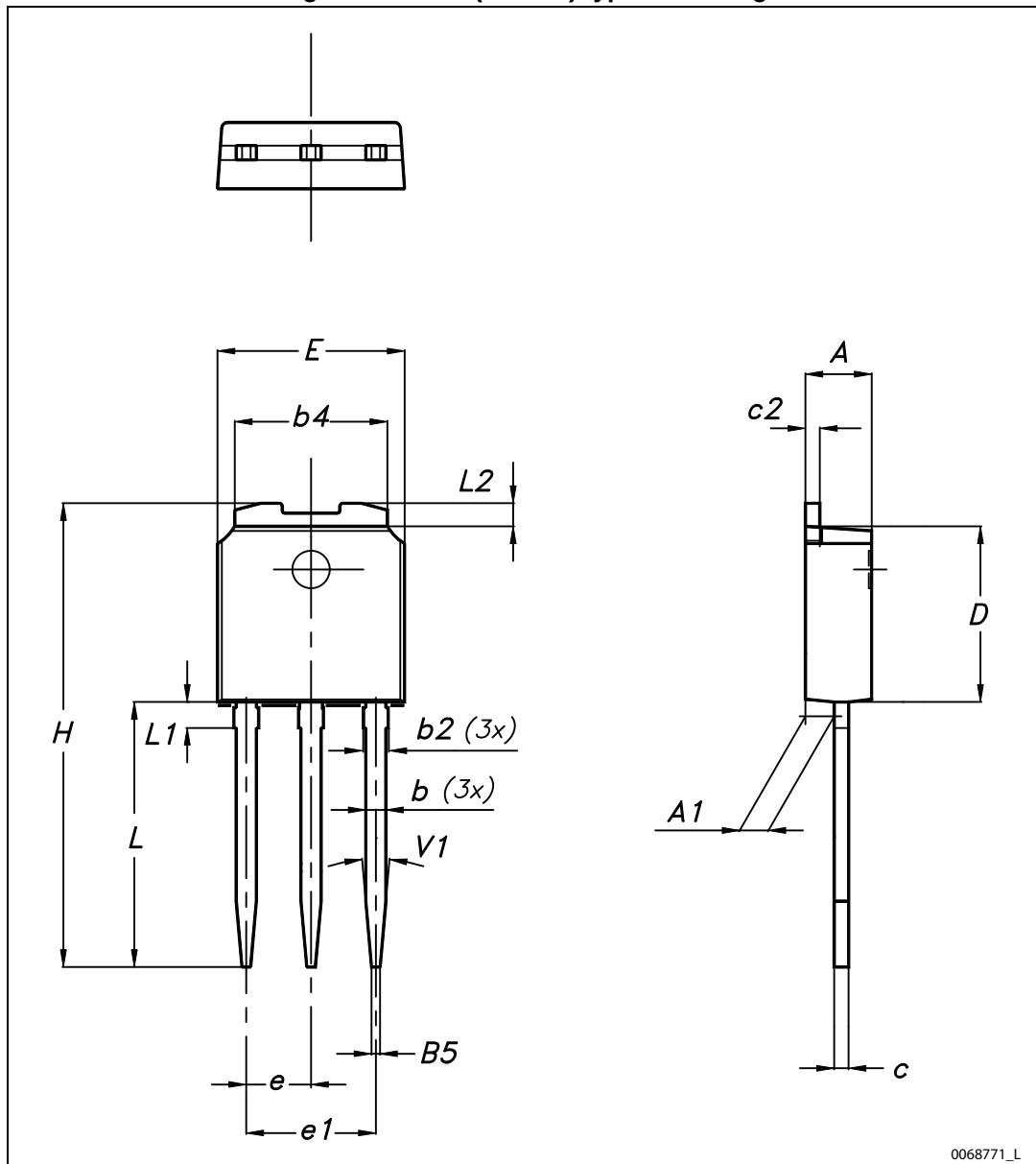


Table 8. IPAK (TO-251) type A mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

Figure 20. IPAK (TO-251) type C drawing

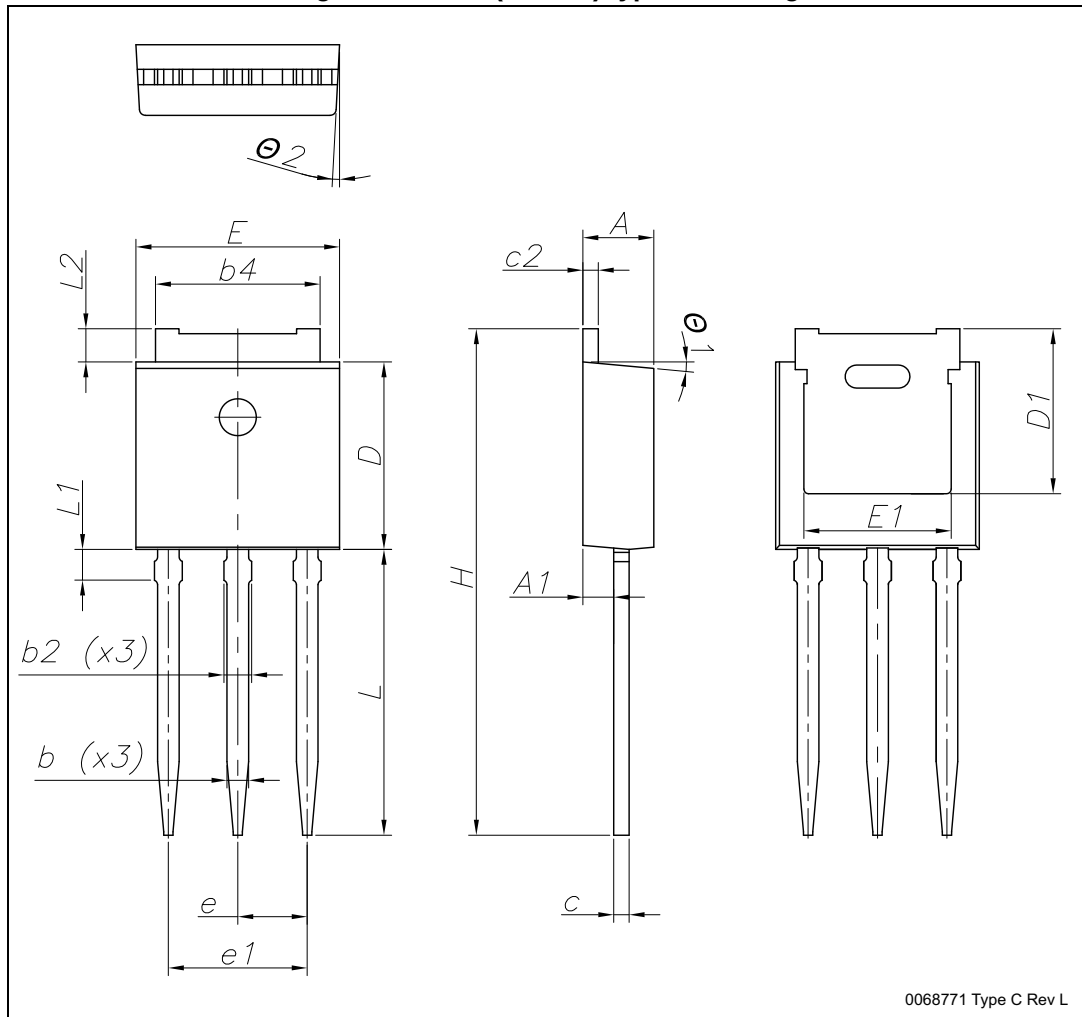


Table 9. IPAK (TO-251) type C mechanical data

Dim.	mm		
	min.	typ.	max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
03-Jul-2014	1	Initial release. The part number STD12NF06L-1 previously included in datasheet with docID8179.
15-Oct-2014	2	Updated Section 4: Package mechanical data .
14-Nov-2014	3	Updated title in cover page and Table 4: On/off states . Updated Figure 2: Safe operating area , Figure 3: Thermal impedance , Figure 10: Normalized gate threshold voltage vs. temperature and Figure 11: Normalized on-resistance vs. temperature . Minor text changes.

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