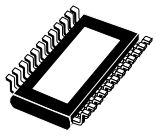
# STAP16DPS05

## Low voltage 16-bit constant current LED sink driver with output error detection and auto power-saving for automotive applications

**Datasheet - production data**



**HTSSOP24**
**(exposed pad)**

## Features

- AECQ100 qualification
- Low voltage power supply down to 3 V
- 16 constant current output channels
- Adjustable output current through external resistor
- Short and open output error detection
- Serial data IN/parallel data OUT
- 3.3 V micro driver-able
- Output current: 5-100 mA
- Auto power-saving
- Max. clock frequency: 30 MHz
- 20 V current generator rated voltage
- Power supply voltage: from 3 V to 5.5 V
- Thermal shutdown for overtemperature protection
- ESD protection 2.0 kV HBM

## Applications

- Dashboard and infotainment backlighting
- Exterior/interior lighting
- DTRLs

## Description

The STAP16DPS05 is a monolithic, low voltage, low current power 16-bit shift register designed for LED panel displays. The device contains a 16-bit serial-in, parallel-out shift register that feeds a 16-bit D-type storage register. In the output stage, sixteen regulated current sources are designed to provide 5-100 mA constant current to drive the LEDs.

The STAP16DPS05 features the open and short LED detections on the outputs.The STAP16DPS05 ensures the backward compatibility with the STP16C/L596. The detection circuit checks 3 different conditions, which can occur on the output line: short to GND, short to $V_O$ or open line. The data detection results are loaded in the shift register and shifted out via the serial line output. The detection functionality is implemented without increasing the pin number. Through a secondary function of the output enable and latch pin (DM1 and DM2 respectively), a dedicated logic sequence allows the device to enter or leave detection mode. Through an external resistor, users can adjust the output current of the STAP16DPS05, thus controlling the light intensity of the LEDs. In addition, the user can adjust the intensity of the brightness of the LEDs from 0% to 100% through the $\overline{OE}$/DM2 pin. The STAP16DPS05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 30 MHz, also satisfies the system requirement of high volume data transmission. The 3.3 V of voltage supply is very useful for applications that interface any microcontroller from 3.3 V micro. Compared with a standard TSSOP package, the TSSOP exposed pad increases the capability of heat dissipation by a factor of 2.5.

**Table 1. Device summary**

| Order code | Package | Packing |
|---|---|---|
| STAP16DPS05XTTR | HTSSOP24 (exposed pad) | 2500 parts per reel |



This is information on a product in full production. www.st.com

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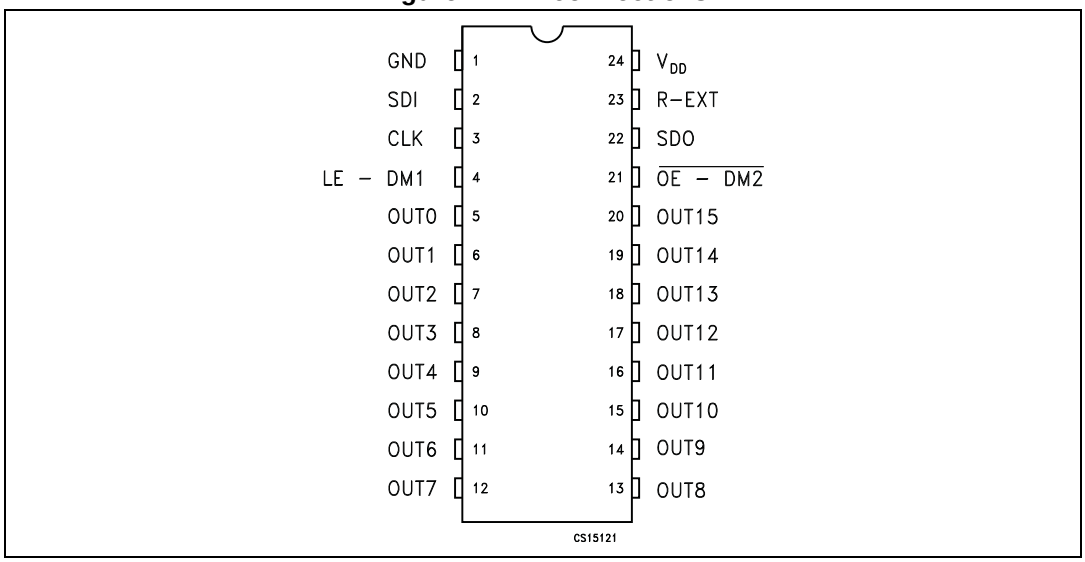
# 1 Summary description

**Table 2. Typical current accuracy**

| Output voltage | Current accuracy | | Output current | $V_{DD}$ | Temperature |
|---|---|---|---|---|---|
| | Between bits | Between ICs | | | |
| ≥ 1.3 V | ±1.5% | ±5% | 20 to 100 mA | 3.3 V to 5 V | 25 °C |

## 1.1 Pin connections and description

**Figure 1. Pin connections**




*Note: The exposed pad is electrically connected to a metal layer electrically isolated or connected to ground.*

**Table 3. Pin description**

| Pin n° | Symbol | Name and function |
|---|---|---|
| 1 | GND | Ground terminal |
| 2 | SDI | Serial data input terminal |
| 3 | CLK | Clock input terminal |
| 4 | LE/DM1 | Latch input terminal - detect mode 1 (see operation principle) |
| 5-20 | OUT-15 | Output terminal |
| 21 | $\overline{OE}$/DM2 | Input terminal of output enable (active low) - detect mode 1 (see operation principle) |
| 22 | SDO | Serial data out terminal |
| 23 | R-EXT | Input terminal of an external resistor for constant current programing |
| 24 | $V_{DD}$ | Supply voltage terminal |

# 2 Electrical ratings

## 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

.

**Table 4. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | 0 to 7 | V |
| $V_O$ | Output voltage | -0.5 to 20 | V |
| $I_O$ | Output current | 100 | mA |
| $V_I$ | Input voltage | -0.4 to $V_{DD}$ | V |
| $I_{GND}$ | GND terminal current | 1600 | mA |
| $f_{CLK}$ | Clock frequency | 50 | MHz |
| $T_{OPR}$ | Operating temperature range | -40 to +150 | °C |
| $T_{STG}$ | Storage temperature range | -55 to +150 | °C |

## 2.2 Thermal data

**Table 5. Thermal data**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $R_{th(JA)}$ | Thermal resistance junction-ambient (1) | TSSOP24 (2) exposed pad | 37.5 | °C/W |

1. According to JEDEC standard 51-7B.
2. The exposed pad should be soldered to the PCB in order to derive the thermal benefits.

## 2.3 Recommended operating conditions

**Table 6. Recommended operating conditions**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | | 3.0 | - | 5.5 | V |
| $V_O$ | Output voltage | | | - | 20 | V |
| $I_O$ | Output current | OUTn | 5 | - | 100 | mA |
| $I_{OH}$ | Output current | Serial-OUT | | - | +1 | mA |
| $I_{OL}$ | Output current | Serial-OUT | | - | -1 | mA |
| $V_{IH}$ | Input voltage | | 0.7 $V_{DD}$ | - | $V_{DD}$+0.3 | V |
| $V_{IL}$ | Input voltage | | -0.3 | - | 0.3 $V_{DD}$ | V |
| $t_{wLAT}$ | LE/DM1 pulse width | $V_{DD}$ = 3.0 V to 5.0 V | 6 | - | | ns |
| $t_{wCLK}$ | CLK pulse width | | 8 | - | | ns |
| $t_{wEN}$ | $\overline{OE}$/DM2 pulse width | | 100 | - | | ns |
| $t_{SETUP(D)}$ | Setup time for DATA | | 10 | - | | ns |
| $t_{HOLD(D)}$ | Hold time for DATA | | 5 | - | | ns |
| $t_{SETUP(L)}$ | Setup time for LATCH | | 10 | - | | ns |
| $f_{CLK}$ | Clock frequency | Cascade operation (1) | | - | 30 | MHz |

1. If the device is connected in cascade, it may not be possible to achieve the maximum data transfer. Please consider the timings carefully.

# 3 Electrical characteristics

$V_{DD}$ = 5V, $T_j$ = -40 °C to 125 °C, unless otherwise specified.

**Table 7. Electrical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input voltage high level | | $0.7 \cdot V_{DD}$ | | $V_{DD}$ | V |
| $V_{IL}$ | Input voltage low level | | GND | | $0.3 \cdot V_{DD}$ | |
| $V_{OL}$ | Serial data output voltage (SDO) | $I_{OL}$ = + 1 mA | | 0.03 | 0.4 | |
| $V_{OH}$ | | $I_{OH}$ = - 1 mA | $V_{DD}$-0.4 | | | |
| $I_{OH}$ | Output leakage current | Vo =19 V, Outn = OFF | | 0.5 | 2 | µA |
| $\Delta I_{OL1}$ | Current accuracy channel-to-channel (1) (2) | $V_{DD}$ = 3.3 V, $V_O$ = 0.4 V, $R_{ext}$ = 980 Ω | | ±1.5 | ±5 | % |
| $\Delta I_{OL2}$ | | $V_{DD}$ = 3.3 V, $V_O$ = 1.3 V, $R_{ext}$ = 200 Ω | | ±1.2 | ±4 | |
| $\Delta I_{OL3}$ | Current accuracy device-to-device (1) | $V_{DD}$ = 3.3 V, $V_O$ = 0.4 V, $R_{ext}$ = 980 Ω | | | ±6 | |
| $\Delta I_{OL4}$ | | $V_{DD}$ = 3.3 V, $V_O$ = 1.3 V, $R_{ext}$ = 200 Ω | | | ±6 | |
| $R_{IN}$(up) | Pull-up resistor for OE pin | | 150 | 300 | 600 | kΩ |
| $R_{IN}$(down) | Pull-down resistor for LE pin | | 100 | 200 | 400 | |
| IDD(AutoOff) | Supply current (OFF) | $R_{ext}$ = 980 Ω, OE = low, OUT0 to OUT7 = OFF | | 200 | 300 | µA |
| IDD(OFF1) | | $R_{ext}$ = 980 Ω, OE = high, OUT0 to OUT7 = ON | | 5 | 8 | mA |
| IDD(OFF2) | | $R_{ext}$ = 200 Ω, OE = high, OUT0 to OUT15 = ON | | 13 | 20 | |
| IDD(ON1) | Supply current (ON) | $R_{ext}$ = 980 Ω, OE = low, OUT0 to OUT15 = ON | | 6 | 8 | |
| IDD(ON2) | | $R_{ext}$ = 200 Ω, OE = low, OUT0 to OUT15 = ON | | 13 | 20 | |
| Tsd | Thermal shutdown (3) | | | 170 | | °C |

1. Test performed with all outputs turned on, but only one output loaded at a time.
2. $D_{IOL}$+ = (($I_{OLmax}$ - $I_{OLmean}$)/ $I_{OLmean}$)*100, $D_{IOL}$ - = (($I_{OLmin}$ - $I_{OLmean}$)/ $I_{OLmean}$)*100, where $I_{OLmean}$ = ($I_{OLout1}$+$I_{OLout2}$+…+$I_{OLout16}$) / 16.
3. Not tested, guaranteed by design.

## 3.1 Switching characteristics

$V_{DD}$ = 5 V, $T_j$ = 25 °C, unless otherwise specified.

**Table 8. Switching characteristics (1)(2)**

| Symbol | Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $f_{clk}$ | Clock frequency | | Cascade operation | | | | 30 | MHz |
| tPLH1 | CLK-OUTn<br>LE\DM1 = H<br>OE\DM2 = L | Propagation delay time<br>("L" to "H") | VIH = VDD<br>VIL = GND<br>CL = 10 pF<br>Io = 20 mA<br>VL = 3 V<br>$R_{ext}$ = 1 KΩ<br>RL = 60 Ω | $V_{DD}$= 3.3 V | | 40 | 45 | ns |
| | | | | $V_{DD}$ = 5 V | | 20 | 45 | |
| tPLH2 | LE\DM1-OUTn<br>OE\DM2 = L | | | $V_{DD}$ = 3.3 V | | 51 | 80 | ns |
| | | | | $V_{DD}$ = 5 V | | 32 | 50 | |
| tPLH3 | OE\DM2-OUTn<br>LE\DM1 = H | | | $V_{DD}$ = 3.3 V | | 50 | 80 | ns |
| | | | | $V_{DD}$ = 5 V | | 30 | 50 | |
| tPLH | CLK - SDO | | | $V_{DD}$ = 3.3 V | | 22 | 35 | ns |
| | | | | $V_{DD}$ = 5 V | | 15 | 25 | |
| tPHL1 | CLK-OUTn<br>LE\DM1 = H<br>OE\DM2 = L | Propagation delay time<br>("H" to "L") | | $V_{DD}$ = 3.3 V | | 15 | 25 | ns |
| | | | | $V_{DD}$ = 5 V | | 12 | 20 | |
| tPHL2 | LE\DM1-OUTn<br>OE\DM2 = L | | | $V_{DD}$ = 3.3 V | | 13 | 25 | ns |
| | | | | $V_{DD}$ = 5 V | | 10 | 15 | |
| tPHL3 | OE\DM2-OUTn<br>LE\DM1 = H | | | $V_{DD}$ = 3.3 V | | 12 | 20 | ns |
| | | | | $V_{DD}$ = 5 V | | 10 | 15 | |
| tPHL | CLK - SDO | | | $V_{DD}$ = 3.3 V | | 25 | 40 | ns |
| | | | | $V_{DD}$ = 5 V | | 18 | 25 | |
| $t_{ON}$ | Output rise time<br>10~90 % of voltage waveform | | | $V_{DD}$ = 3.3 V | | 35 | 55 | ns |
| | | | | $V_{DD}$ = 5 V | | 10 | 20 | |
| $t_{OFF}$ | Output fall time<br>90~10 % of voltage waveform | | | $V_{DD}$ = 3.3 V | | 4 | 10 | ns |
| | | | | $V_{DD}$ = 5 V | | 3 | 8 | |
| tr | CLK rise time(3) | | | | | | 5 | µs |
| tf | CLK fall time(3) | | | | | | 5 | |

1. All table limits are guaranteed by design.
2. Not tested in production.
3. If devices are connected in cascade and tr or tf is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

# 4 Equivalent circuit and outputs

**Figure 2. $\overline{\text{OE/DM2}}$ terminal**

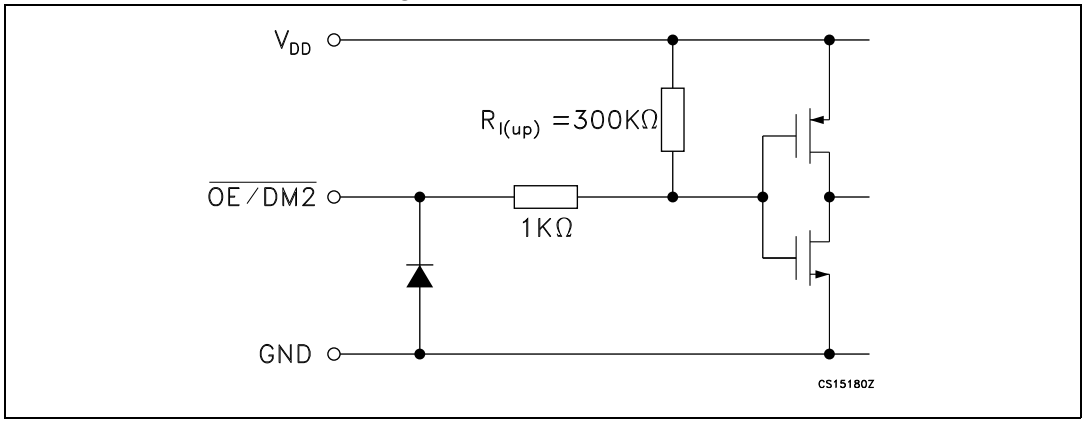



**Figure 3. LE/DM1 terminal**

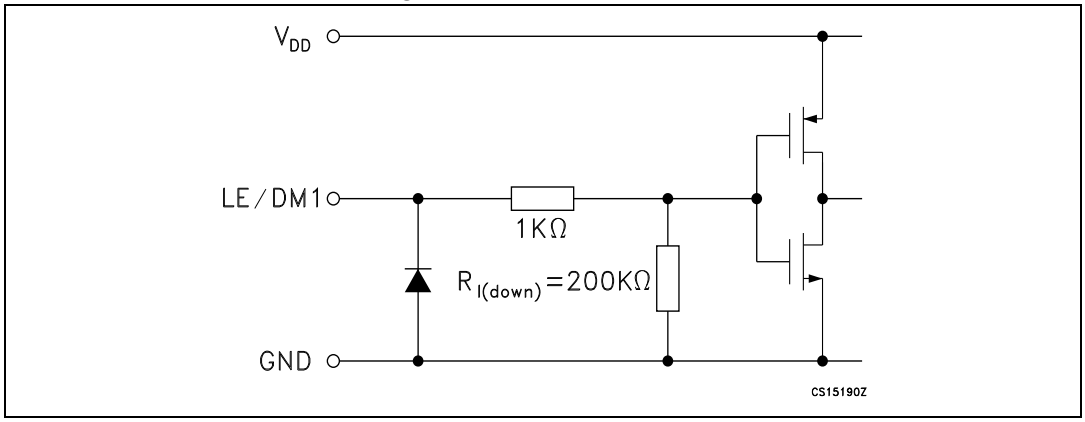



**Figure 4. CLK, SDI terminal**

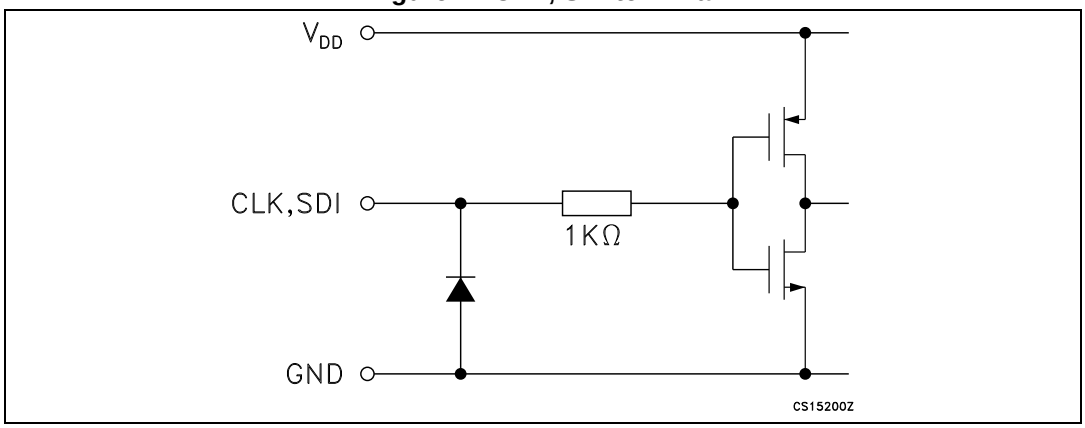


**Figure 5. SDO terminal**

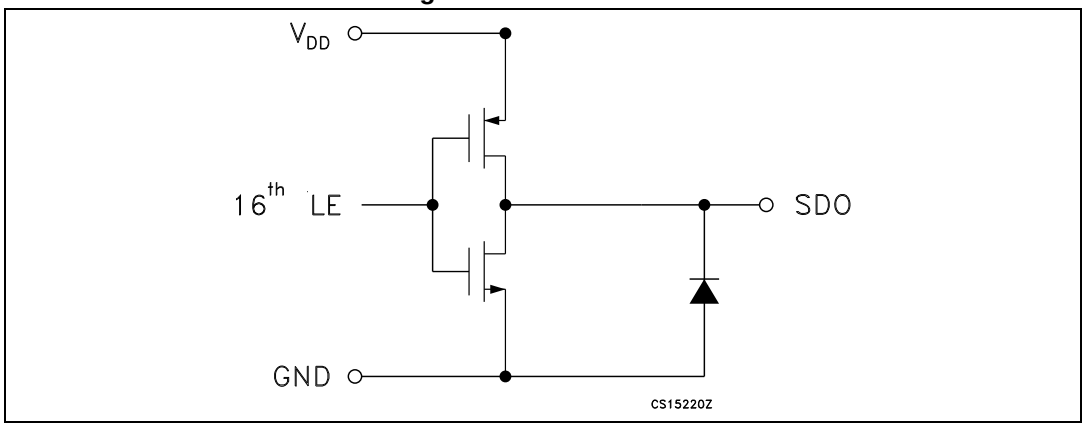
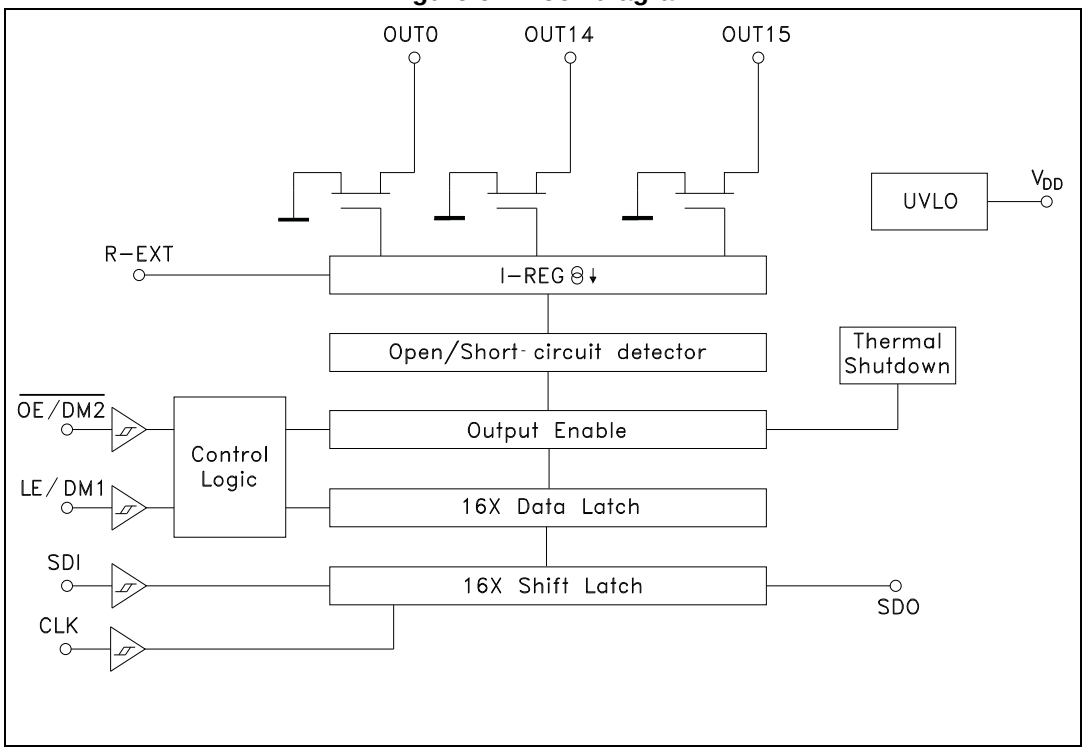



**Figure 6. Block diagram**



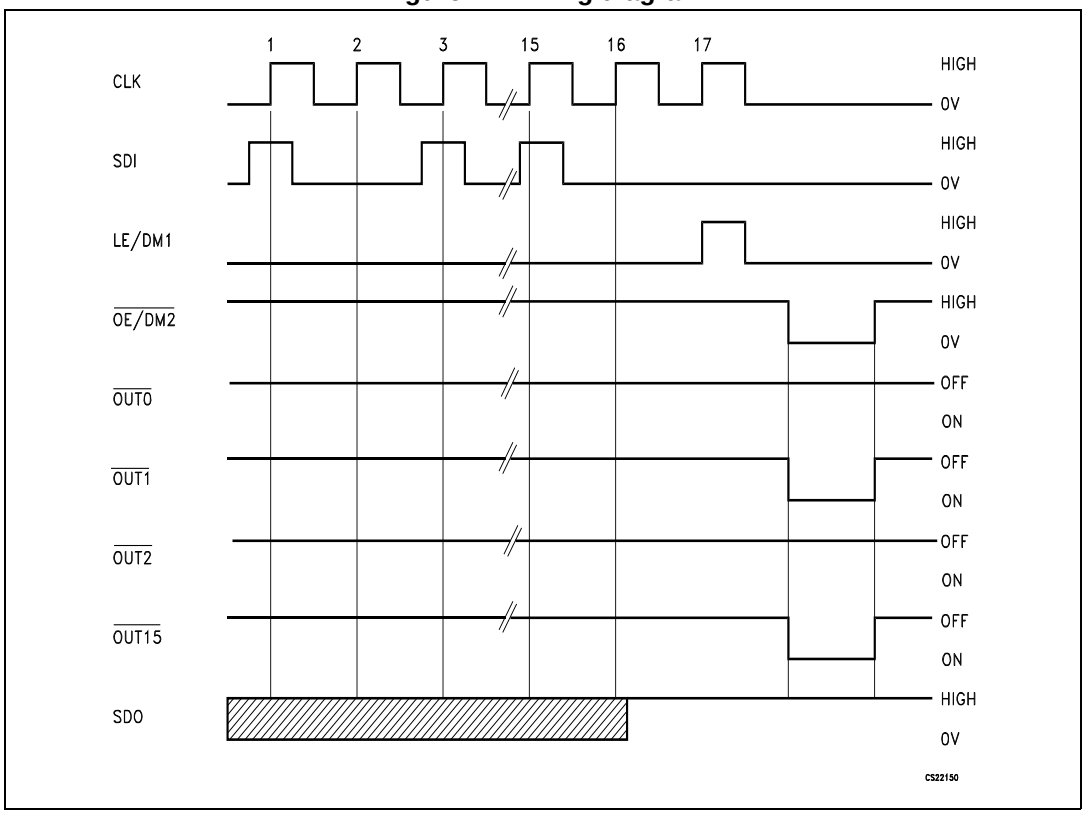
# 5 Timing diagrams

**Table 9. Truth table**

| Clock | LE/DM1 | $\overline{\text{OE/DM2}}$ | Serial-in | $\overline{\text{OUT0}}$..... $\overline{\text{OUT7}}$..... $\overline{\text{OUT15}}$ | SDO |
|---|---|---|---|---|---|
| ⎍ | H | L | Dn | Dn..... Dn - 7..... Dn -15 | Dn - 15 |
| ⎍ | L | L | Dn + 1 | No change | Dn - 14 |
| ⎍ | H | L | Dn + 2 | Dn + 2..... Dn - 5..... Dn -13 | Dn - 13 |
| ⎎ | X | L | Dn + 3 | Dn + 2..... Dn - 5..... Dn -13 | Dn - 13 |
| ⎎ | X | H | Dn + 3 | OFF | Dn - 13 |

*Note: OUTn = ON when Dn = H OUTn = OFF when Dn = L.*

**Figure 7. Timing diagram**




*Note: Latch and output enable are level-sensitive and they are not synchronized with rising or falling edge of CLK signal. When LE/DM1 terminal is low level, the latch circuits hold the previous set of data. When LE/DM1 terminal is high level, the latch circuits refresh new set of data from SDI chain. When OE/DM2 terminal is at low level, the output terminals - Out0 to Out15 respond to data in the latch circuits, either '1' ON or '0' OFF. When OE/DM2 terminal is at high level, all output terminals are switched OFF.*

**Figure 8. Clock, serial-in, serial-out**

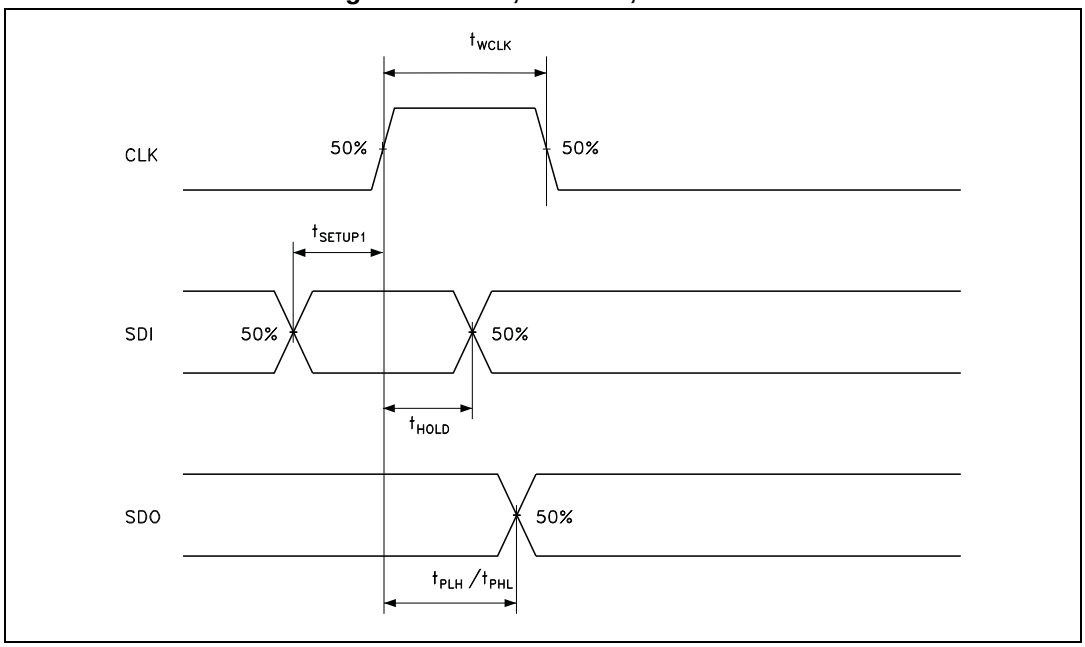


**Figure 9. Clock, serial-in, latch, enable, outputs**

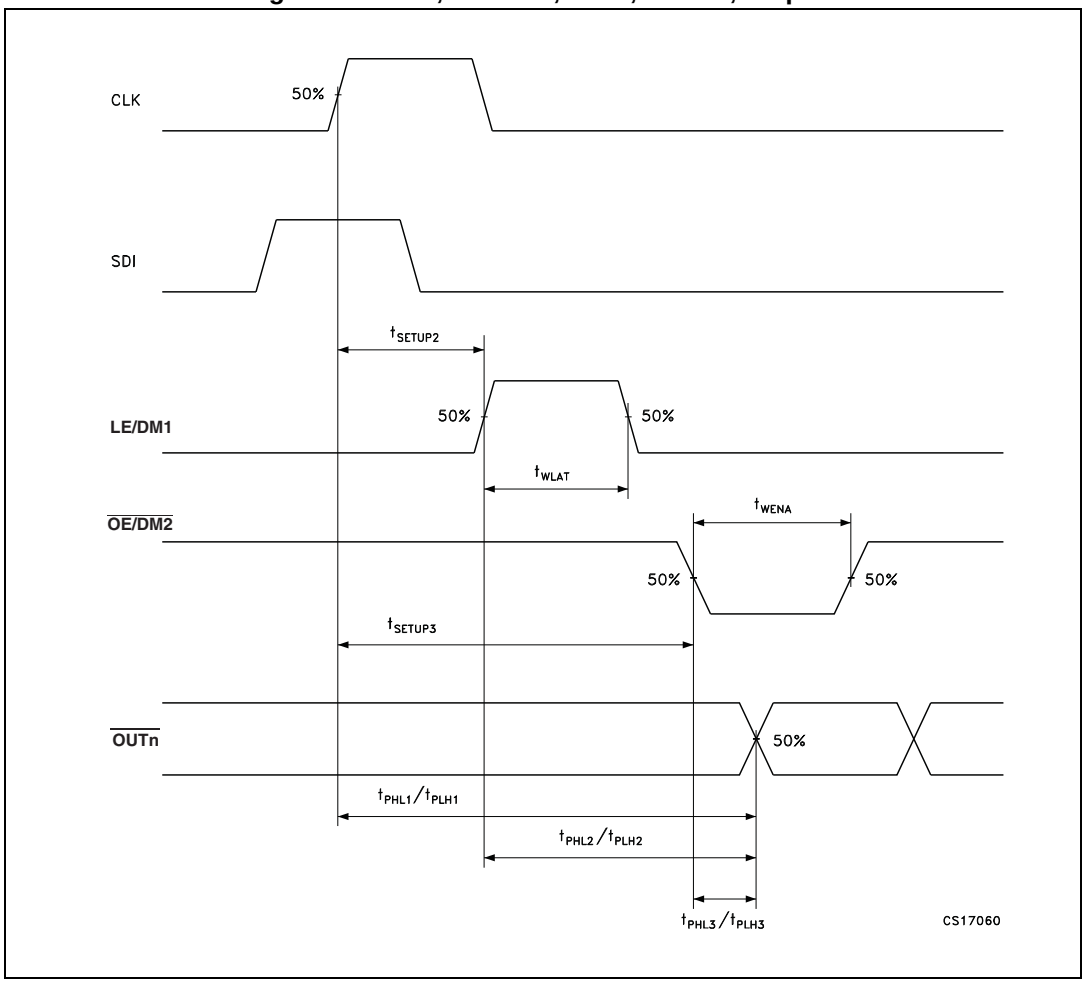
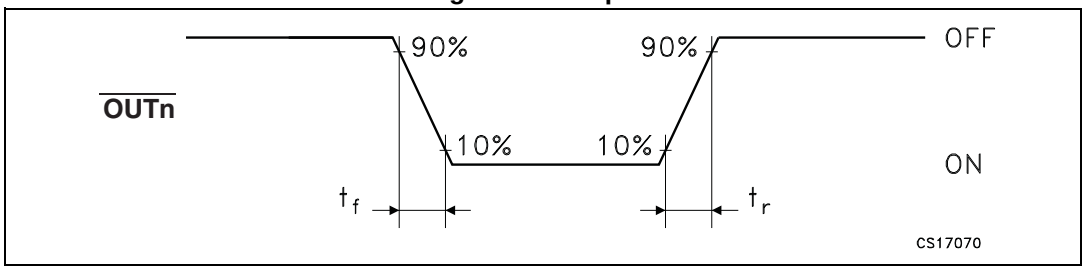



**Figure 10. Outputs**



# 6 Typical characteristics

**Figure 11. Output current-$R_{EXT}$ resistor**

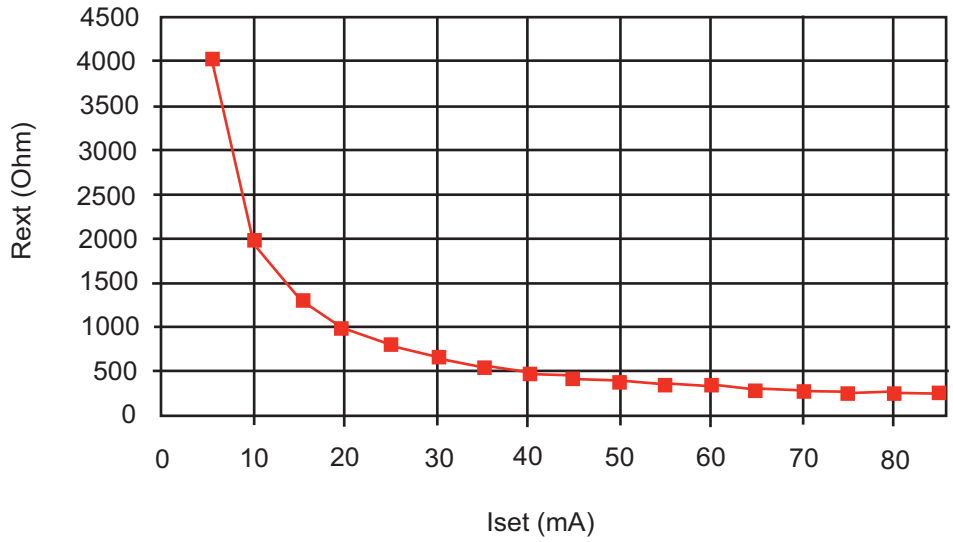



**Table 10. Output current-$R_{EXT}$ resistor**

| $R_{EXT}(\Omega)$ | Output current (mA) |
|---|---|
| 976 | 20 |
| 780 | 25 |
| 652 | 30 |
| 560 | 35 |
| 488 | 40 |
| 433 | 45 |
| 389 | 50 |
| 354 | 55 |
| 325 | 60 |
| 300 | 65 |
| 278 | 70 |
| 259 | 75 |
| 241 | 80 |
| 229 | 85 |

Conditions:

– Temperature = 25 °C, $V_{DD}$ = 3.3 V; 5.0 V, $I_{SET}$ = 3 mA; 5 mA; 10 mA; 20 mA; 50 mA; 80 mA.

**Figure 12. $I_{SET}$ vs. dropout voltage ($V_{drop}$)**

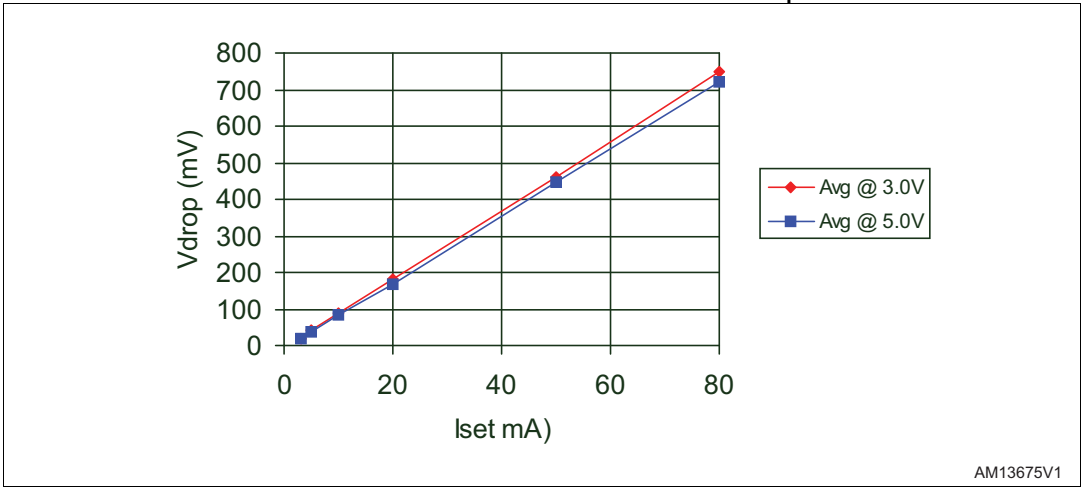
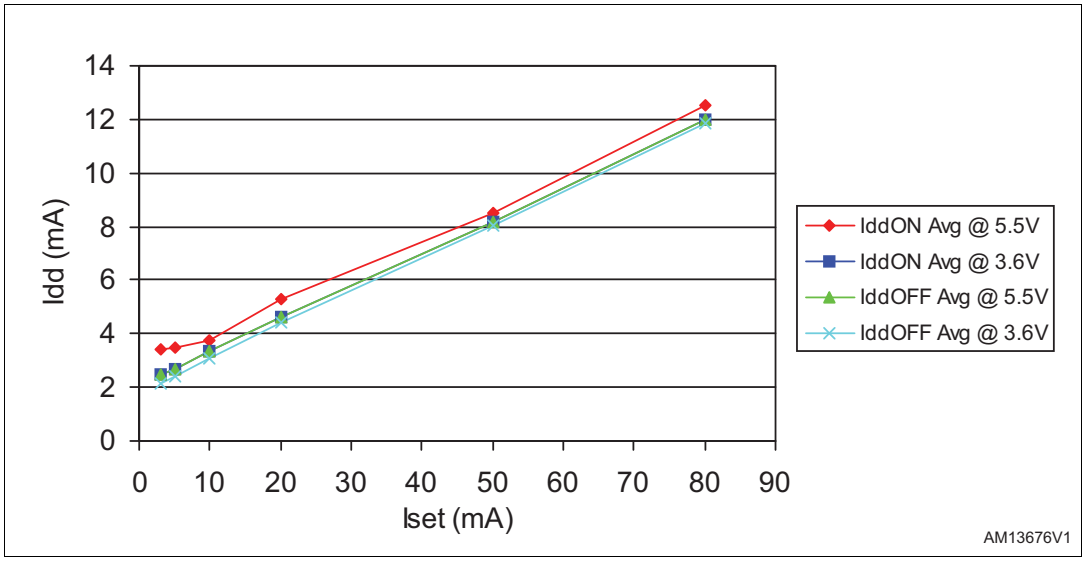



**Table 11. $I_{SET}$ vs. dropout voltage ($V_{drop}$)**

| Iout (mA) | Avg @ 3.0 V | Avg @ 5.0 V |
|---|---|---|
| 3 | 19.33 | 22.66 |
| 5 | 36.67 | 40.33 |
| 10 | 77.33 | 80 |
| 20 | 158.67 | 157.33 |
| 50 | 406 | 406 |
| 80 | 692 | 668 |

**Figure 13. $I_{DD}$ ON/OFF**



# 7 Detection mode functionality

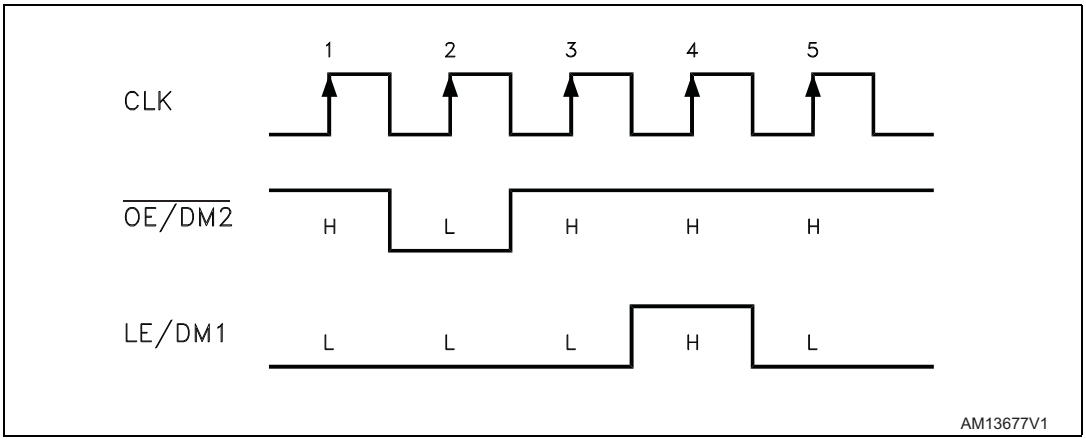
## 7.1 Phase one: “entering in detection mode“

From the “normal mode” condition the device can switch to the “error mode” by a logic sequence on the $\overline{OE}$/DM2 and LE/DM1 pins as shown in the following table and diagram:

**Table 12. Entering in detection truth table**

| CLK | 1° | 2° | 3° | 4° | 5° |
|---|---|---|---|---|---|
| $\overline{OE}$/DM2 | H | L | H | H | H |
| LE/DM1 | L | L | L | H | L |

**Figure 14. Entering in detection timing diagram**

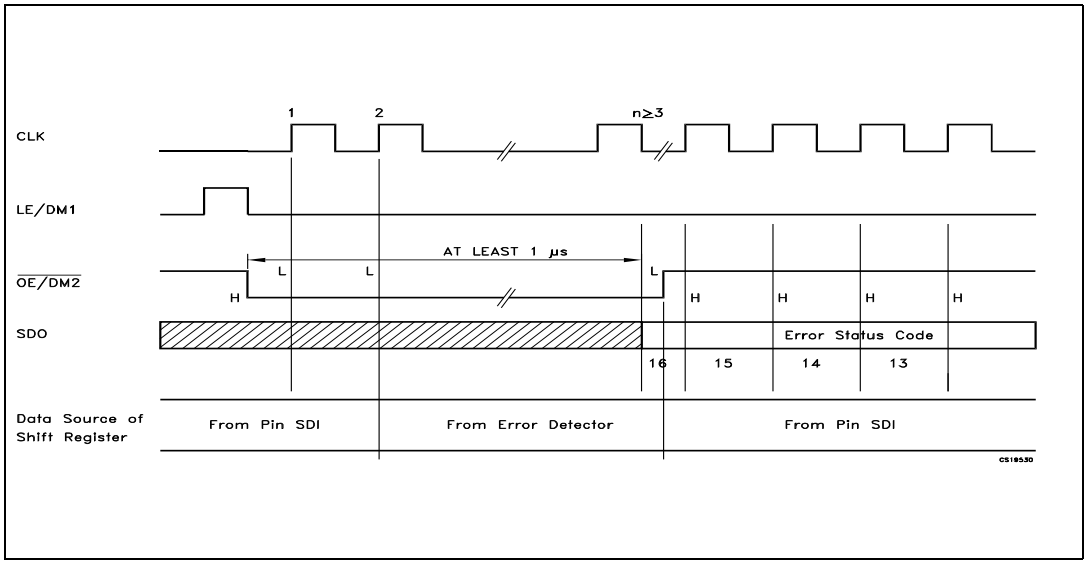



After these five CLK cycles the device goes into the “error detection mode” and at the 6$^{th}$ rising edge of CLK the SDI data are ready for sampling.

## 7.2 Phase two: “error detection”

The 16 data bits must be set to “1” in order to set ON all the outputs during the detection. The data are latched by LE/DM1 and after that the outputs are ready for the detection process. When the microcontroller switches the $\overline{OE}$/DM2 to LOW, the device drives the LEDs in order to analyze if an OPEN or SHORT condition has occurred.

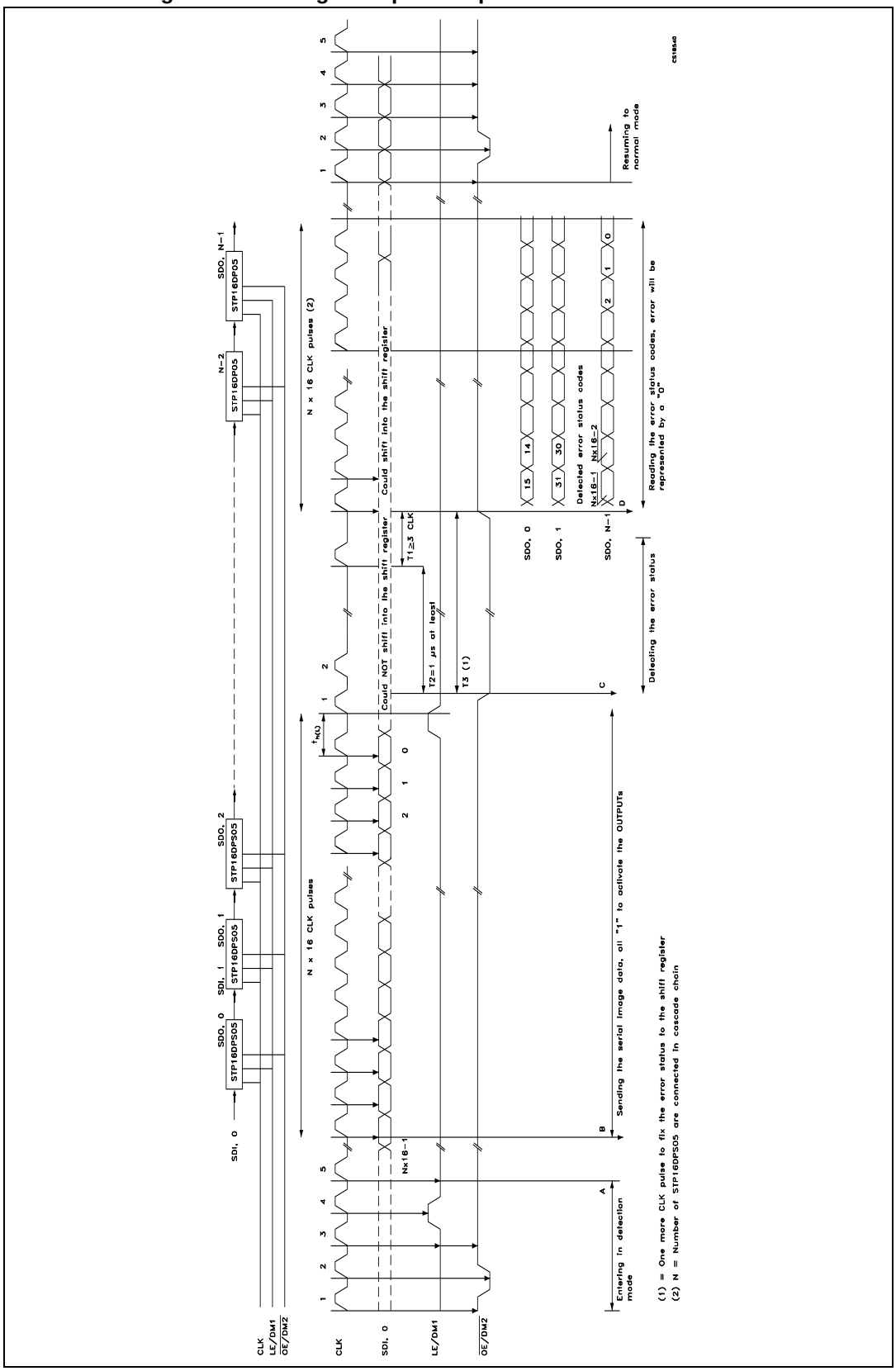
**Figure 15. Detection diagram**




The LED status is detected at least in 1 microsecond (minimum) and after this time the microcontroller sets $\overline{OE}$/DM2 in high state and the output data detection result goes to the microprocessor via SDO.

Detection mode and normal mode both use the same data format. As soon as all the detection data bits are available on the serial line, the device may go back to normal mode of operation. To re-detect the status, the device must go back in normal mode and re-enter error detection mode.

**Figure 16. Timing example for open and/or short detection**



## 7.3 Phase three: “resuming to normal mode”

The sequence for re-entering in normal mode is shown in the following table and diagram:

**Figure 17. Resuming to normal mode timing diagram**

| CLK | 1° | 2° | 3° | 4° | 5° |
|---|---|---|---|---|---|
| $\overline{\text{OE}}$/DM2 | H | L | H | H | H |
| LE/DM1 | L | L | L | L | L |

*Note: For proper device operation the “entering in detection” sequence must be followed by a “resume mode” sequence, it is not possible to insert consecutive equal sequences.*

## 7.4 Error detection conditions

$V_{DD}$ = 3.3 to 5 V temperature range -40 to 125 °C

**Table 13. Detection conditions**

| Configuration | Detection mode | Detection results | | |
|---|---|---|---|---|
| **SW-1 or SW-3b** | Open line or output short to GND detected | ==> $I_{ODEC} \leq 0.5 \times I_O$ | No error detected | ==> $I_{ODEC} \geq 0.5 \times I_O$ |
| **SW-2 or SW-3a** | Short on LED or short to V-LED detected | ==> $V_O \geq 2.4$ V | No error detected | ==> $V_O \leq 2.2$ V |

*Note: Where: $I_O$ =* the output current programmed by the $R_{EXT}$, $I_{ODEC}$ = the detected output current in detection mode.

**Figure 18. Detection circuit**

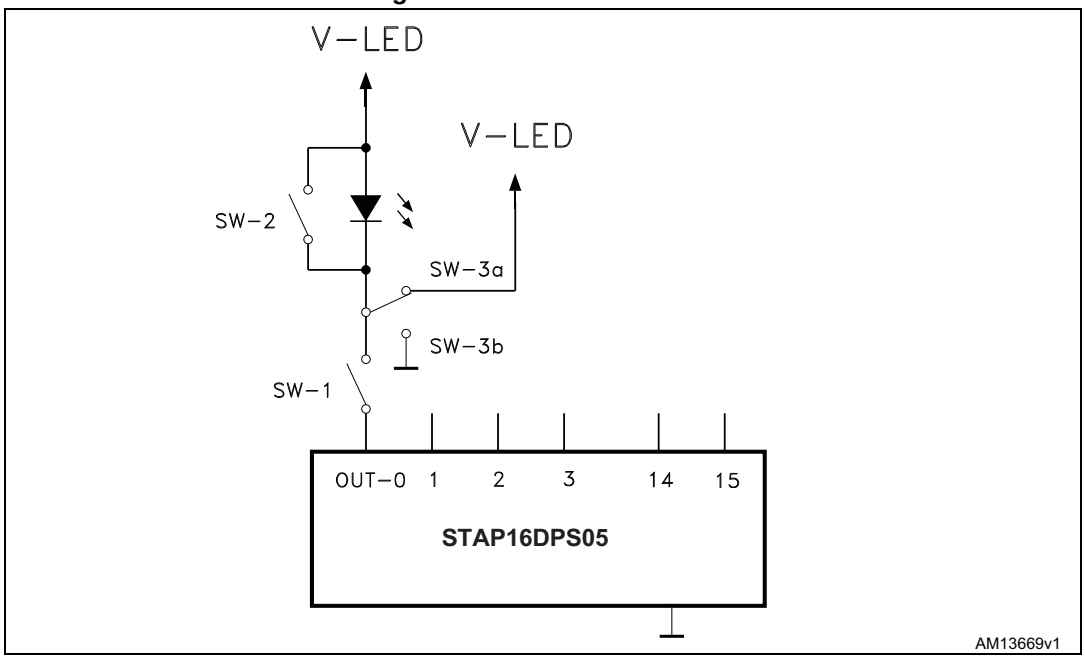
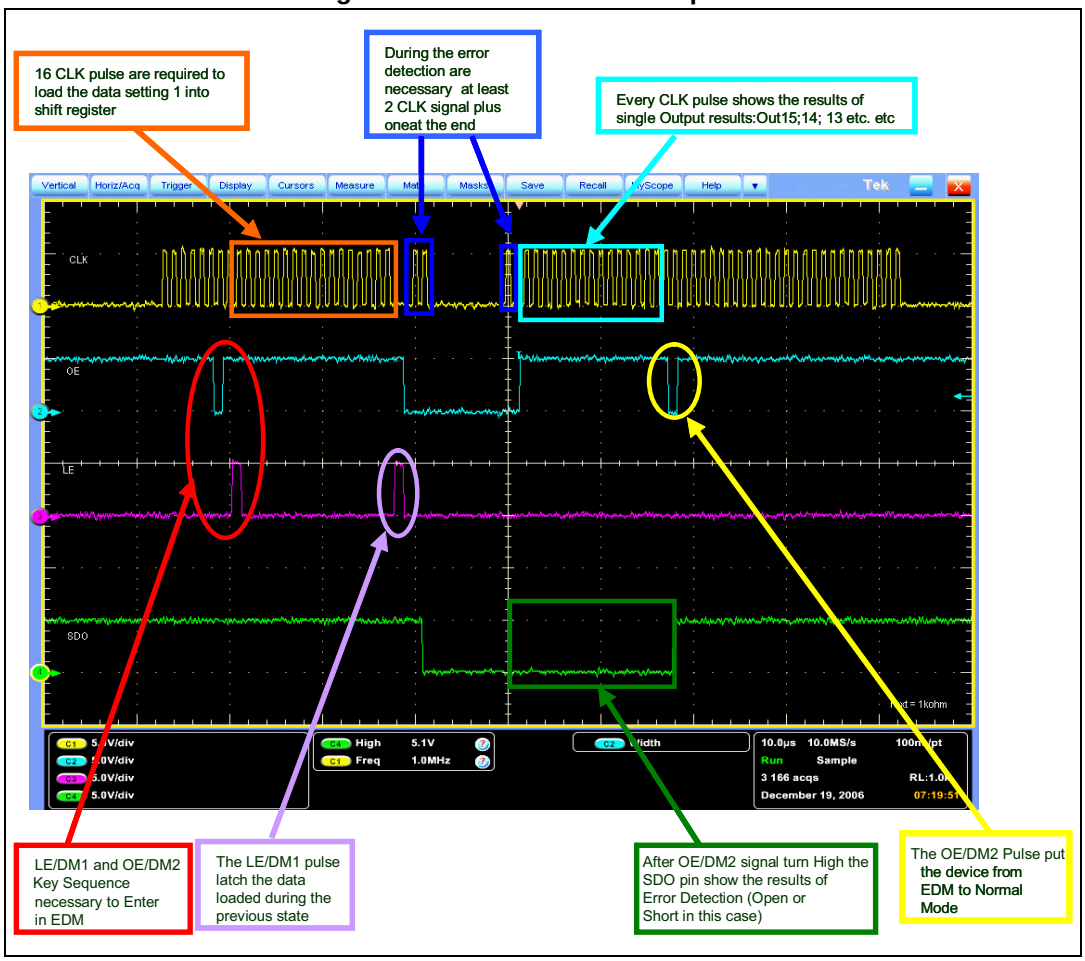
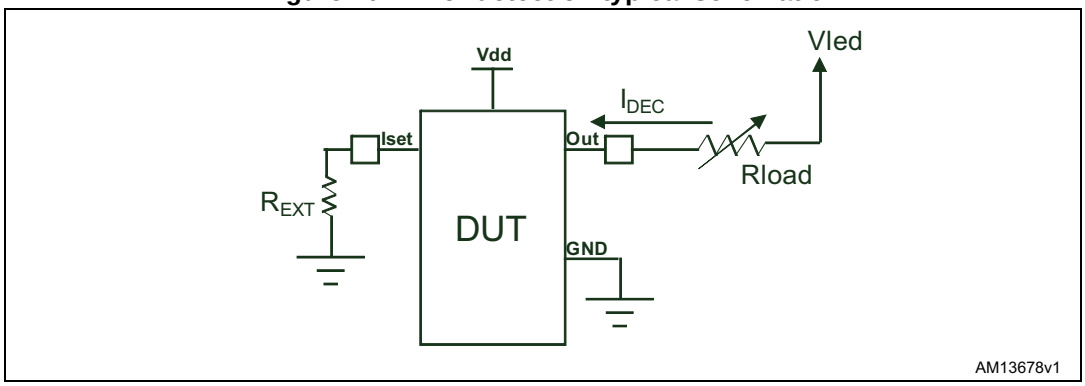


**Figure 19. Error detection sequence**




Typical schematic used to perform the error detection:

**Figure 20. Error detection typical schematic**




$I_{ODEC}$ can be measured as follows:

$I_{ODEC}$ = (Vled-Vload) / Rload

*Table 14* and *Table 15* show respectively the $I_{ODEC}$ average value at 3.3 V and 5.0 V.

The $I_{ODEC}$ is the current value recognized by the device output open error detection.

Table 14. $I_{ODEC}$ average value at 3.3 V

| Vdd (V) | Iset (mA) | $R_{EXT}$ (Ω) | Iout AVG (mA) |
|---|---|---|---|
| 3.3 | 5 | 4270 | 2.097 |
| | 10 | 2056 | 6.79 |
| | 20 | 1006 | 10.46 |
| | 50 | 382 | 26.92 |
| | 80 | 251 | 35.03 |

Table 15. $I_{ODEC}$ average value at 5 V

| Vdd (V) | Iset (mA) | $R_{EXT}$ (Ω) | Iout AVG (mA) |
|---|---|---|---|
| 5 | 5 | 4270 | 1.98 |
| | 10 | 2056 | 6.09 |
| | 20 | 1006 | 9.67 |
| | 50 | 382 | 25.54 |
| | 80 | 251 | 38.9 |

## 7.5 Auto power-saving

The auto power-saving feature minimizes the quiescent current if no active data is detected on the latches and auto powers-up the device as the first active data is latched.

**Figure 21. Auto power-saving feature**




Conditions:

- Temp. = 25 °C, $V_{DD}$ = 3.3 V, Vin = $V_{DD}$, VLed = 3.0 V, Iset = 20 mA
- Ch1 (yellow) = $I_{DD}$, Ch2 (blue) = SDI, Ch3 (purple) = LE/DM1, Ch4 (green) = CLK

Idd consumption:

- Idd (normal operation) = 5.15 mA
- Idd (shutdown condition) = 163 µA

**Figure 22. Delay LE-OUT**




After 16 clock cycles without data change, the auto power-saving mode starts as expected. Delay TLE-OUT = 1.053 µs

Conditions:

- Temp. = 25 °C, $V_{DD}$ = 3.3 V, Vin = $V_{DD}$, VLed = 3.0 V, Iset = 20 mA
- Ch1 (yellow) = CLK, Ch2 (blue) = SDI, Ch3 (purple) = LE/DM1, Ch4 (green) = IOUT

**Figure 23. Auto power-saving behavior**




*Note: When the device goes from auto power-saving to normal operating condition, the first output switching ON shows the $T_{ON}$ condition as seen in the plot above.*

*Temp. = 25°C, $V_{DD}$ = 3.3 V, Vin = $V_{DD}$, VLed = 3.0 V, Iset = 20 mA*

*Ch1 (yellow) = IDD, Ch2 (blue) = SDI, Ch3 (purple) = LE/DM1, Ch4 (green) = CLK.*

# 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 8.1 TSSOP24 exposed pad package information

**Figure 24. TSSOP24 exposed pad package outline**

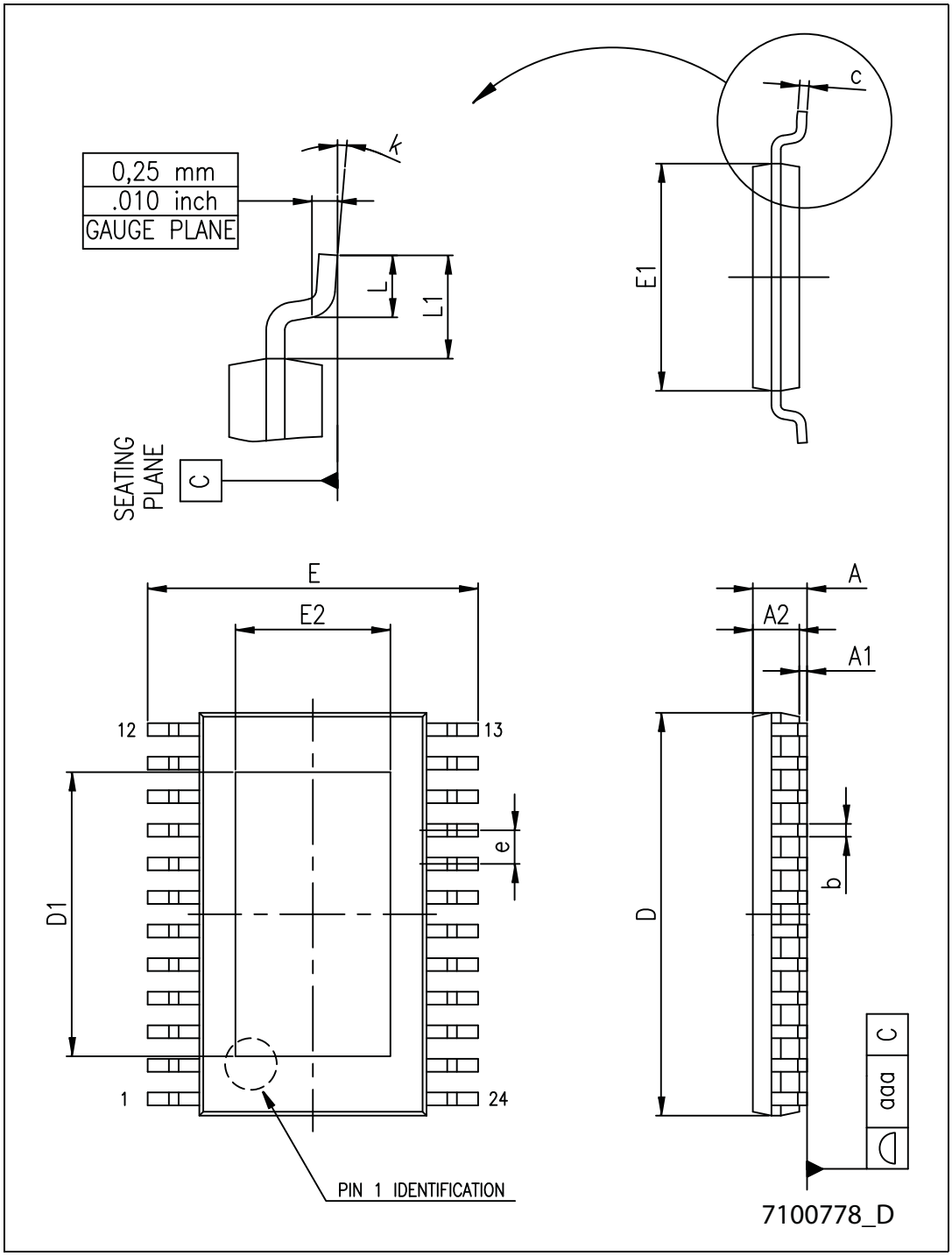


Table 16. TSSOP24 exposed pad mechanical data

| Symbol | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | | 1.20 |
| A1 | | | 0.15 |
| A2 | 0.80 | 1.00 | 1.05 |
| b | 0.19 | | 0.30 |
| c | 0.09 | | 0.20 |
| D | 7.70 | 7.80 | 7.90 |
| D1 | 4.80 | 5.00 | 5.2 |
| E | 6.20 | 6.40 | 6.60 |
| E1 | 4.30 | 4.40 | 4.50 |
| E2 | 3.00 | 3.20 | 3.40 |
| e | | 0.65 | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | | 1.00 | |
| k | 0 | | 8 |
| aaa | | | 0.10 |

## 8.2 TSSOP24 exposed pad packing information

**Figure 25. TSSOP24 exposed pad tape and reel outline**

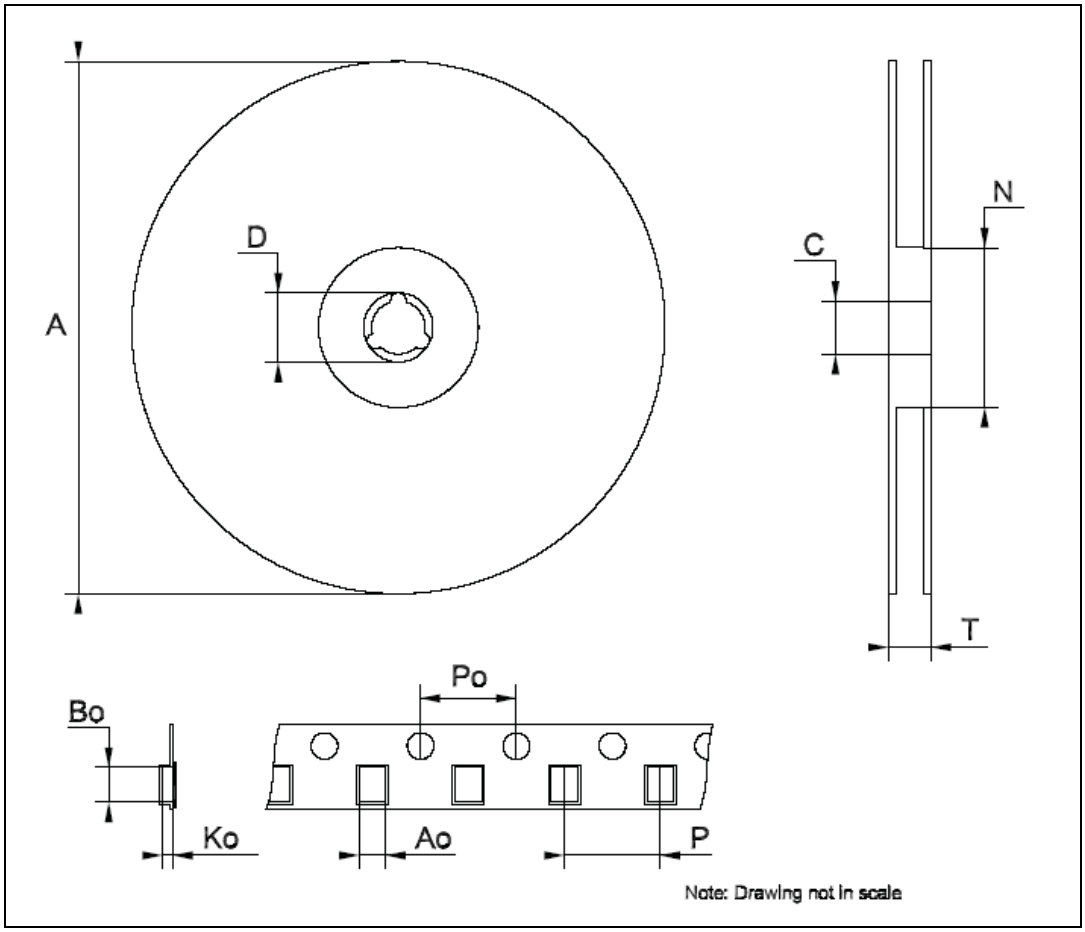


Table 17. TSSOP24 exposed pad tape and reel mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | | 330 |
| C | 12.8 | | 13.2 |
| D | 20.2 | | |
| N | 60 | | |
| T | | | 22.4 |
| Ao | 6.8 | | 7 |
| Bo | 8.2 | | 8.4 |
| Ko | 1.7 | | 1.9 |
| Po | 3.9 | | 4.1 |
| P | 11.9 | | 12.1 |

# 9 Revision history

Table 18. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 21-May-2013 | 1 | Initial release. |
| 01-Jul-2013 | 2 | Added footnote in Table 8: Switching characteristics. |
| 11-Oct-2013 | 3 | Modified $T_{OPR}$ value in Table 4: Absolute maximum ratings. |
| 10-Mar-2014 | 4 | Modified footnote 1 in Table 8: Switching characteristics.<br>Added footnote 2 in Table 8: Switching characteristics.<br>Updated Table 3: Pin description. |
| 05-Jun-2014 | 5 | Updated Table 16: TSSOP24 exposed pad mechanical data.<br>Minor text changes. |
| 10-Nov-2015 | 6 | Updated features in cover page.<br>Minor text changes. |

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