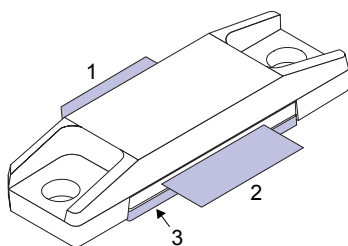


LDMOS avionics radar transistor



STAC780-2B



Features

Order code	Frequency	V _{DD}	P _{OUT}	Gain	Efficiency
STAC1011-350	1030 to 1090 MHz	28 V	350 W	15 dB	53 %

- Excellent thermal stability
- Common source configuration
- P_{OUT} = 350W with 15 dB gain over 1030 to 1090 MHz
- ST air-cavity STAC packaging technology

Applications

- Avionics

Description

The STAC1011-350 is a common source N-channel enhancement-mode lateral field-effect RF power transistor designed for avionics applications at frequencies range 1030 to 1090 MHz.

Pin connection

Pin	Connection
1	Drain
2	Gate
3	Source (bottom side)

Product status link

[STAC1011-350](#)

Product summary

Order code	STAC1011-350
Marking	1011-350
Package	STAC780-2B
Packing	Tube
Base/bulk quantity	15/90

1 Electrical data

1.1 Maximum ratings

Table 1. Absolute maximum ratings ($T_{CASE} = +25\text{ °C}$)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	± 20	V
P_{DISS}	Power dissipation (at $T_{CASE} = +70\text{ °C}$)	1440	W
T_J	Maximum operating junction temperature	+200	°C
T_{STG}	Storage temperature range	-65 to +150	°C

1.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Junction-case thermal resistance	0.09	°C/W

Note: Thermal data at 50 μs - 2%

1.3 ESD protection characteristics

Table 3. ESD protection

Symbol	Test methodology	Class
HBM	Human body model (per JESD22-A114)	2

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

2.1 Static

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_{DS} = 20\text{ mA}$	80			V
I_{DSS}	Zero gate voltage drain leakage current	$V_{GS} = 0\text{ V}$, $V_{DS} = 28\text{ V}$			2	μA
I_{GSS}	Gate-source leakage current	$V_{GS} = 15\text{ V}$, $V_{DS} = 0\text{ V}$			1	μA
$V_{GS(Q)}$	Gate quiescent voltage	$V_{DS} = 28\text{ V}$, $I_{DS} = 150\text{ mA}$	2.0		5.0	V
$V_{DS(on)}$	Drain-source on voltage	$V_{GS} = 10\text{ V}$, $I_{DS} = 6\text{ A}$		550	600	mV
G_{FS}	Forward transconductance	$V_{DS} = 10\text{ V}$, $I_{DS} = 6\text{ A}$	2.5			S

2.2 Dynamic

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f	Frequency		1030		1090	MHz
P_{OUT}	Output power	$P_{IN} = 15\text{ W}$	350	370		W
G_{PS}	Power gain	$P_{OUT} = 350\text{ W}$	13	15		dB
η_D	Drain efficiency	$P_{OUT} = 350\text{ W}$	50	53		%
t_r	Rise time	$P_{OUT} = 350\text{ W}$			50	ns
t_f	Fall time	$P_{OUT} = 350\text{ W}$			25	ns
ΔG_{PS}	Gain variation	$P_{OUT} = 350\text{ W}$, gain droop within the pulse			0.2	dB
VSWR	Load mismatch	All phase angles at $P_{OUT} = 350\text{ W}$			10:1	

Note: $V_{DD} = 36\text{ V}$, $I_{DQ} = 150\text{ mA}$, pulse width = 50 μs , duty cycle = 2%.

3 Impedance data

Figure 1. Impedance data

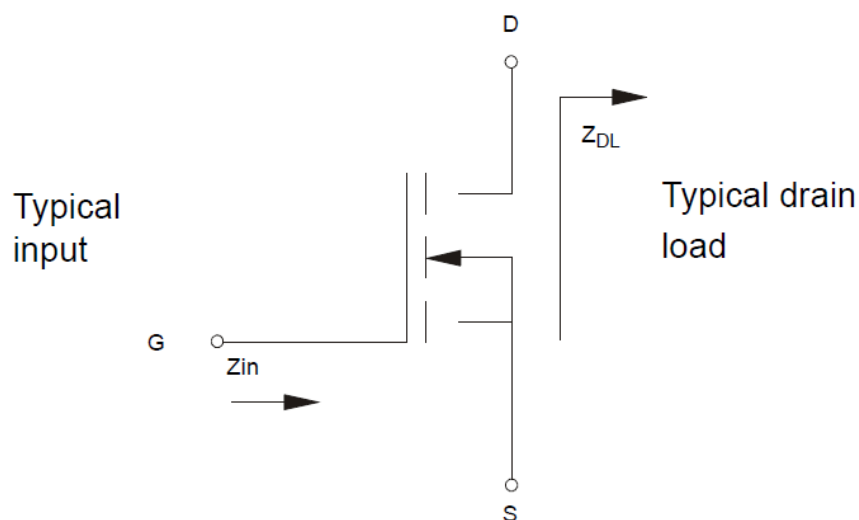


Table 6. Impedance data

Frequency (MHz)	Z_{source} (Ohm)	Z_{load} (Ohm)
1030	$1+j0.126$	$1.12+j0.242$
1060	$0.855+j0.417$	$0.929+j0.560$
1090	$0.709+j0.764$	$0.752+j0.881$

4 Typical performances

Figure 2. Output power vs gain and supply voltage at 1030 MHz

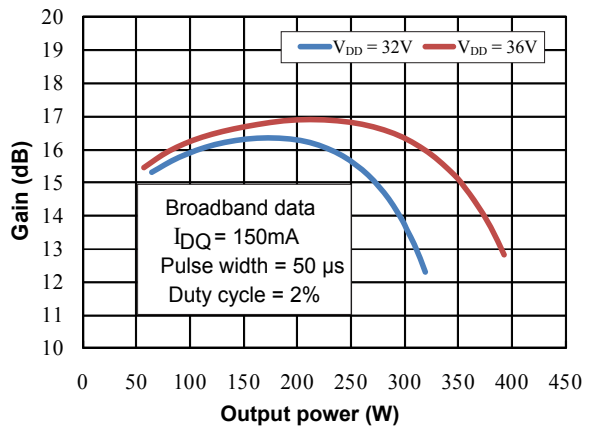


Figure 3. Output power and efficiency vs frequency - broadband data

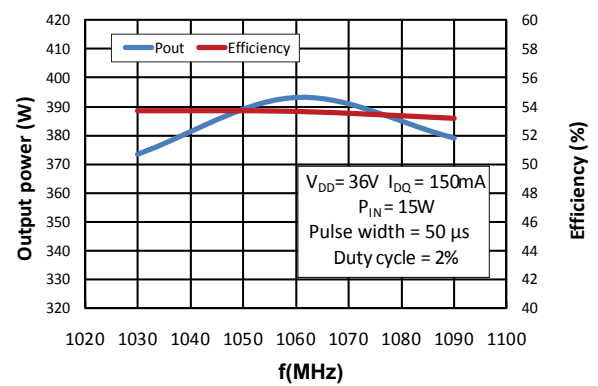


Figure 4. Output power vs gain and supply voltage at 1060 MHz

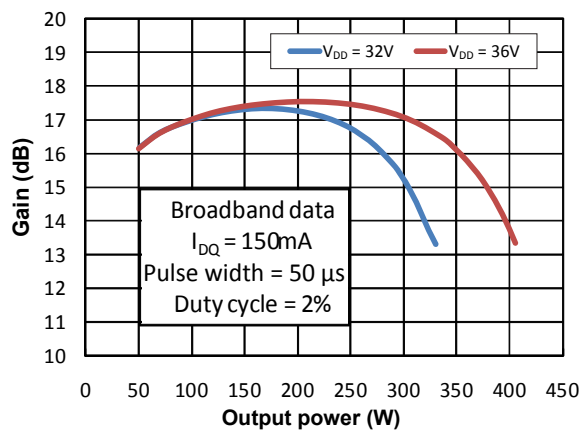


Figure 5. Gain and input return loss vs frequency - broadband data

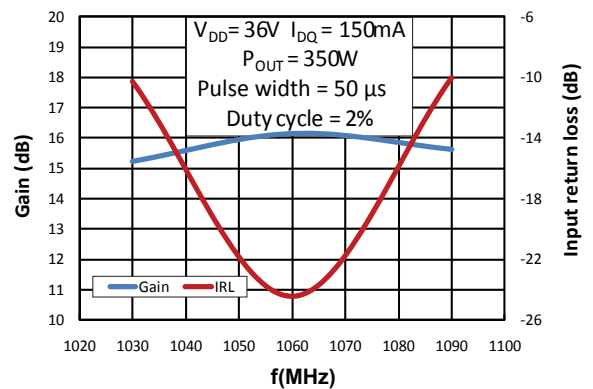
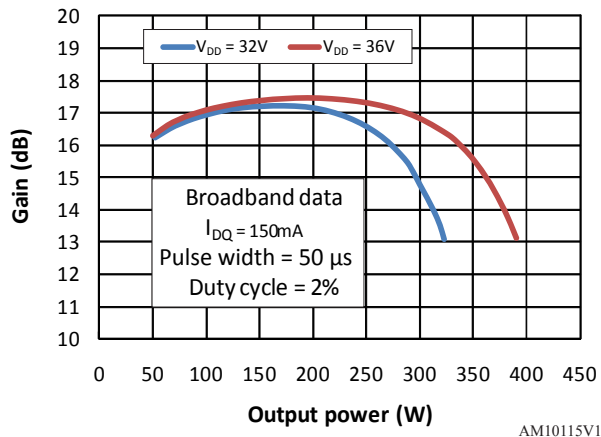
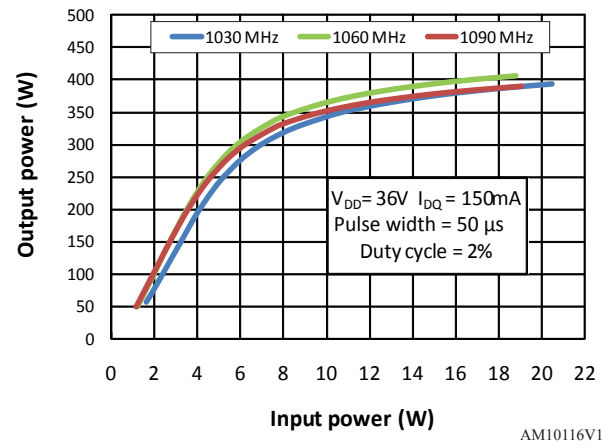
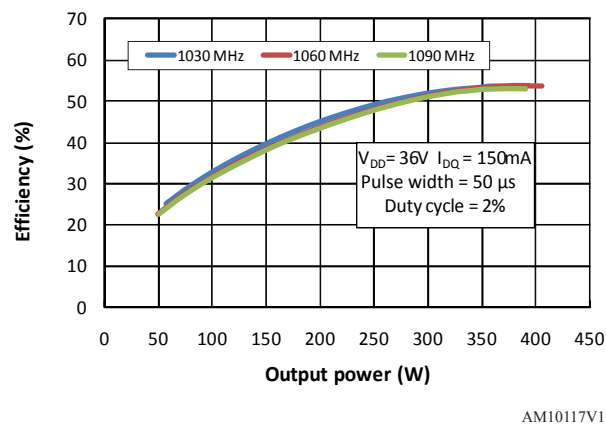
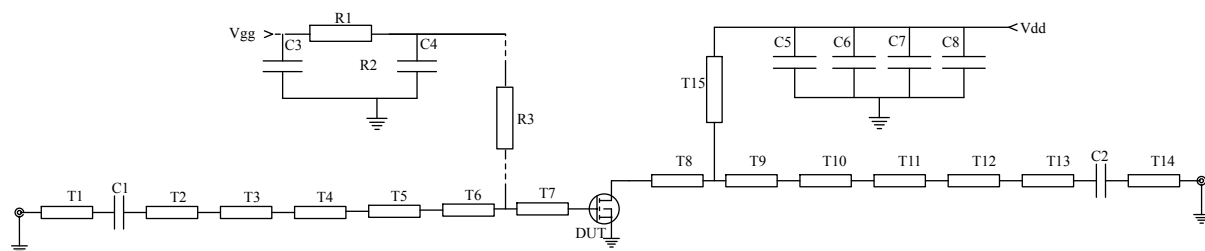


Figure 6. Output power vs gain and supply voltage at 1090 MHz

Figure 7. Output power vs input power - broadband data

Figure 8. Efficiency vs output power broadband data


5 Test circuit

5.1 Electrical schematic and BOM

Figure 9. Broadband 1030-1090 MHz electrical schematic



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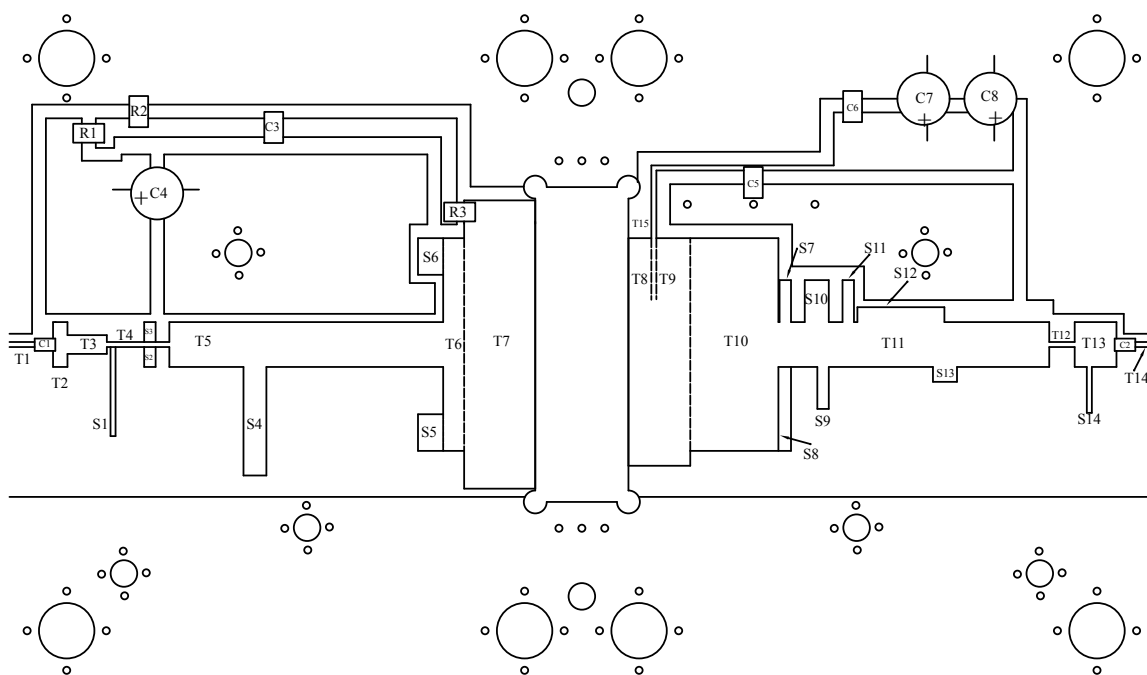
Table 7. Component list

Component	Description	Dimension (X,Y)	Values
TL1	Stripline	L=0.111" W=0.022"	
TL2	Stripline	L=0.063" W=0.196"	
TL3	Stripline	L=0.172" W=0.082"	
TL4	Stripline	L=0.273" W=0.022"	
TL5	Stripline	L=1.196" W=0.196"	
TL6	Stripline	L=0.092" W=0.929"	
TL7	Stripline	L=0.311" W=1.259"	
TL8	Stripline	L=0.100" W=0.994"	
TL9	Stripline	L=0.148" W=0.994"	
TL10	Stripline	L=0.385" W=0.929"	
TL11	Stripline	L=1.183" W=0.196"	
TL12	Stripline	L=0.111" W=0.022"	
TL13	Stripline	L=0.183" W=0.196"	
TL14	Stripline	L=0.145" W=0.022"	
TL15	Stripline	L=0.741" W=0.022"	
S1	Shim	L=0.022" W=0.389"	
S2	Shim	L=0.050" W=0.087"	
S3	Shim	L=0.050" W=0.087"	
S4	Shim	L=0.100" W=0.0474"	
S5	Shim	L=0.110" W=0.160"	
S6	Shim	L=0.110" W=0.160"	
S7	Shim	L=0.050" W=0.183"	
S8	Shim	L=0.055" W=0.366"	
S9	Shim	L=0.050" W=0.183"	
S10	Shim	L=0.105" W=0.183"	
S11	Shim	L=0.050" W=0.183"	

Component	Description	Dimension (X,Y)	Values
S12	Shim	L=0.380" W=0.065"	
S13	Shim	L=0.105" W=0.065"	
S14	Shim	L=0.022" W=0.200"	
C8	1000 μ F, 63 V electrolytic capacitor		1000 μ F
C7	100 μ F, 100 V electrolytic capacitor		100 μ F
C6	ATC700B122JT 50 X		1200 pF
C5	ATC100B330KW500X		33 pF
C4	ATC100B101KW500X		100 pF
C3	220 μ F, 63 V electrolytic capacitor		220 pF
C2	ATC100A300JP 150X		30 pF
C1	ATC100A300JP 150X		30 pF
R3	CR1206-4W-132JB		1.3 k Ω
R2	CR1206-4W-681JB		680 Ω
R1	CR1206-4W-361JB		360 Ω
PCB	Rogers Duroid 6010 Er = 10.2, Th = 0.64 mm	3X5"	

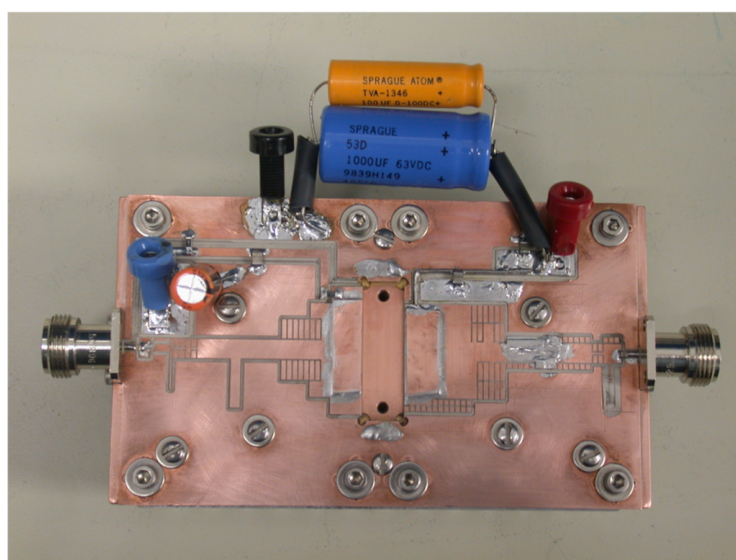
5.2 Layout

Figure 10. Broadband 1030-1090 MHz test circuit layout



AM12368v1

Figure 11. Demonstration board picture



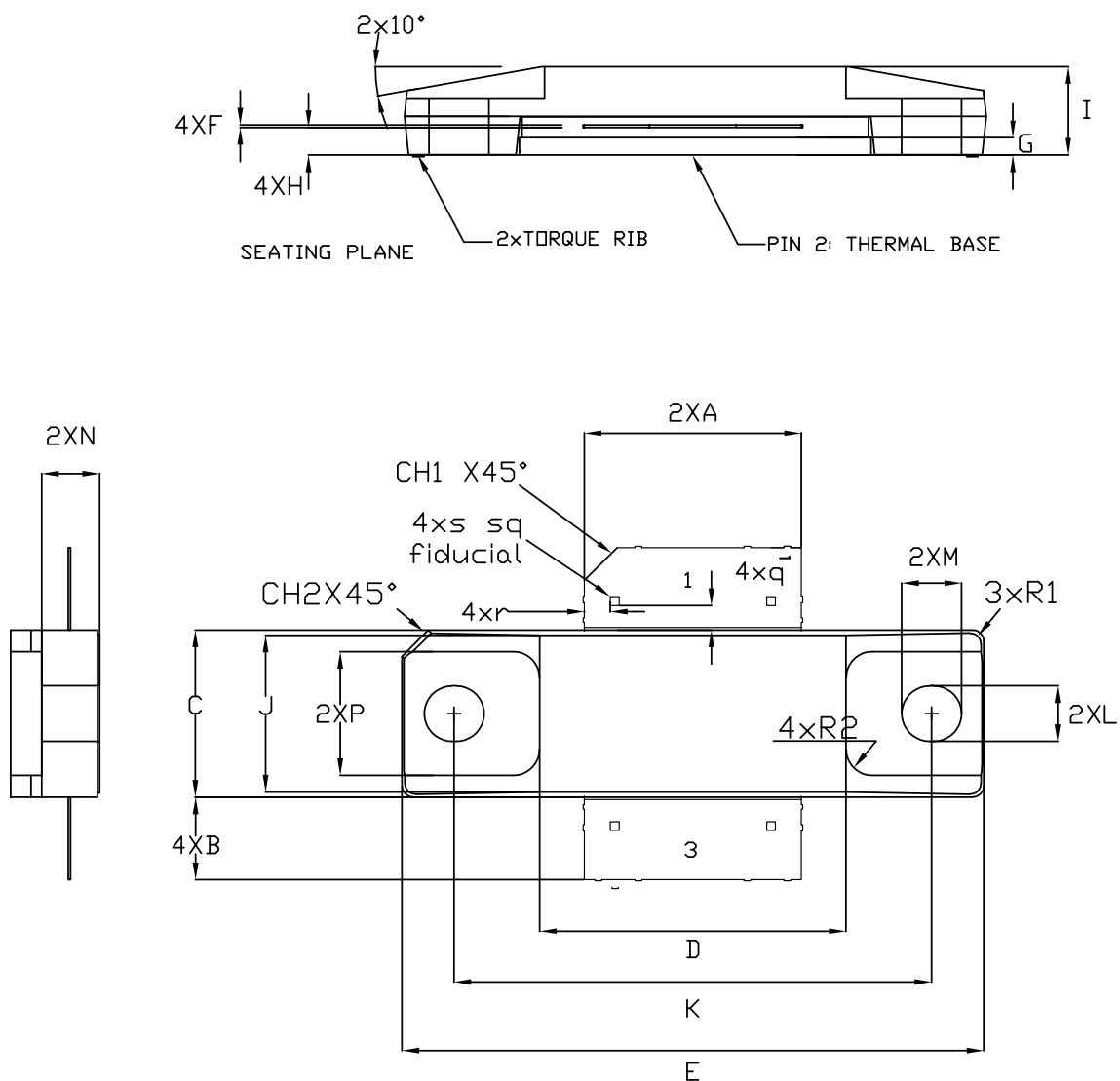
AM12369v1

6 **Package information**

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 STAC780-2B package information

Figure 12. STAC780-2B package outline



PIN	CONNECTION
1	DRAIN
2	SOURCE
3	GATE

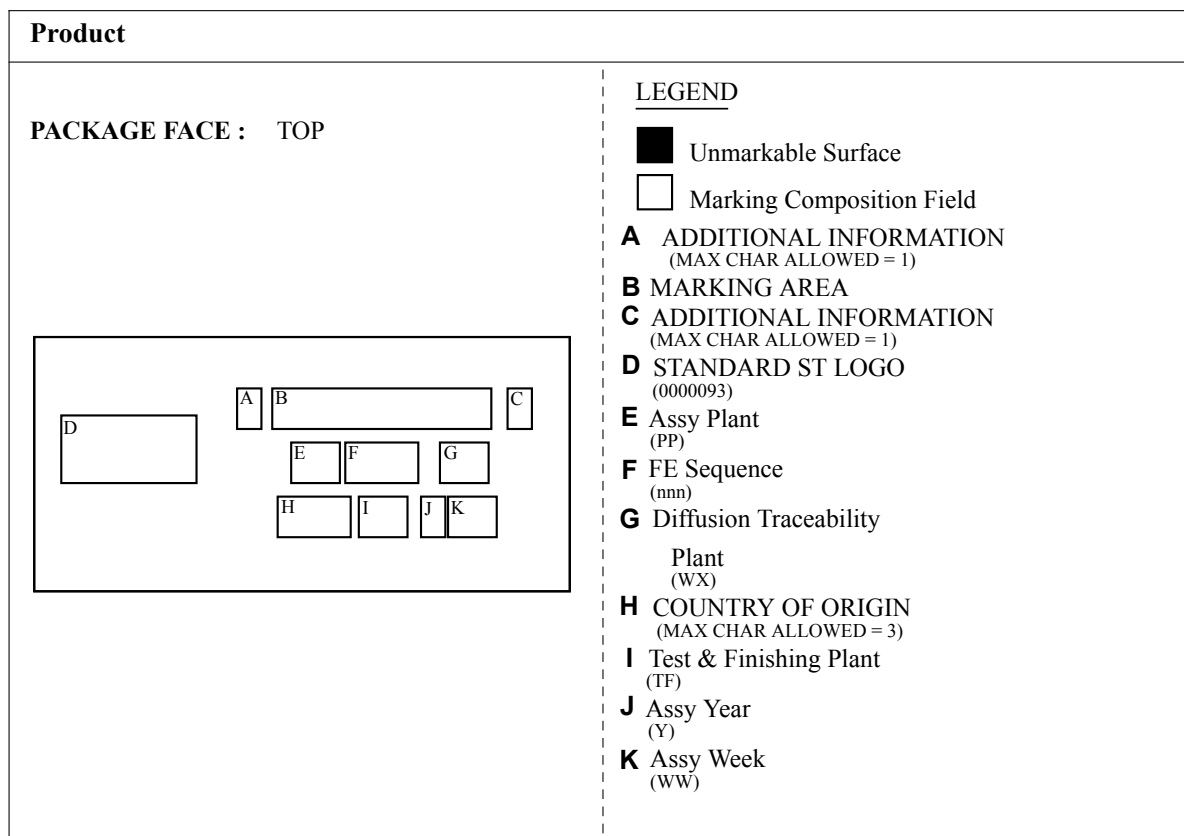
DM00481924_2

Table 8. STAC780-2B mechanical data

Ref.	Millimeters		
	Min.	Typ.	Max.
A	12.65		12.75
B	4.57		5.08
C	9.65		9.91
D	17.78		18.08
E	33.88		34.19
F	0.11		0.17
G	0.97		1.14
H	1.52		1.70
I	4.83		5.33
J	9.52		9.78
K	27.69		28.19
L	3.20	3.25	3.30
M	3.43	3.51	3.58
N	3.30	3.38	3.45
p	7.14	7.21	7.29
q		1.37	
r		1.52	
R1		0.63	
R2		1.52	
s		0.51	
θ		10°	
CH1		2.72	
CH2		1.52	

6.2 STAC780-2B marking information

Figure 13. STAC780-2B marking information



CD00362879_13

Revision history

Table 9. Document revision history

Date	Version	Changes
25-Jul-2011	1	First release
12-Sep-2011	2	Inserted <i>Section 5: Circuit and BOM</i> .
13-Sep-2011	3	Updated dimensions in <i>Table 8: STAC265B mechanical data</i> .
06-Jun-2012	4	– Modified: <i>Figure 10</i> – Added: <i>Figure 11</i> – Updated the entire <i>Table 7</i>
24-Sep-2012	5	Updated title on the cover page. Updated <i>Table 4</i> .
20-May-2014	6	Updated <i>Figure 12: Package dimensions</i> . Minor text changes. Document status promoted from preliminary to production data.
16-Apr-2020	7	Updated Section 6.1 STAC780-2B package information . Added Section 1.3 ESD protection characteristics . Minor text changes.

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