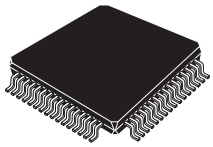
STA306

MULTICHANNEL DIGITAL AUDIO PROCESSOR WITH DDX™

PRODUCT PREVIEW

- 6 DDX™ Channels Capability (24 bit)
- From 32kHz to 192kHz Input Sample Rates Supported
- Volume Control from 0 to -127 dB (0.5 dB steps)
- Variable Digital Gain from 0 to 24dB (0.5dB steps) with Digital Limiter Functionality and Variable Attack and Release Time
- I2S Inputs and Outputs
- Individual Channel and Master Gain/ Attenuation
- Individual Channel Mute and Zero Input Detect Auto-Mute
- Selectable Serial Audio Data Interface
- Bass/Treble Controls
- Channel Mapping of any Input to any Processing/DDX™ Channel
- Active Crossover Capability
- DC Blocking Selectable High-Pass Filter
- Selectable Bass Management on Channel 6
- Selectable Adjacent Channel Mixing Capability
- Selectable Clock Input Ratio
- Selectable De-emphasis
- Selectable DDX™ Ternary, or Binary PWM output
- AM Interference Reduction Mode
- I2C Control



TQFP64
ORDERING NUMBER: STA306

DESCRIPTION

The STA306 is a single chip solution for digital audio processing and control in multi-channel applications. It provides output capabilities for DDX™ (Direct Digital Amplification). In conjunction with a DDX™ power device, it provides high-quality, high-efficiency, all digital amplification. The device is extremely versatile allowing for input of most digital formats including 192kHz, 24-bit DVD-Audio.

The internal 24-bit DSP allows for high resolution processing at all standard input sample frequencies. Processing includes volume control, filtering, bass management, gain compression/limiting and PCM and DDX™ outputs. Filtering includes five user-programmable 28-bit biquads for EQ per channel, as well as bass, treble and DC blocking. External clocking can be provided at 4 different ratios of the input sample frequency. All sample frequencies are upsampled for processing. Each internal processing channel can receive any input channel, allowing flexibility and the ability to perform active digital crossover for powered loudspeaker systems.

The serial audio data interface accepts many different formats, including the popular I2S format. STx-channels of DDX processing are performed.

This is preliminary information on a new product foreseen to be developed. Details are subject to change without notice.

BLOCK DIAGRAM

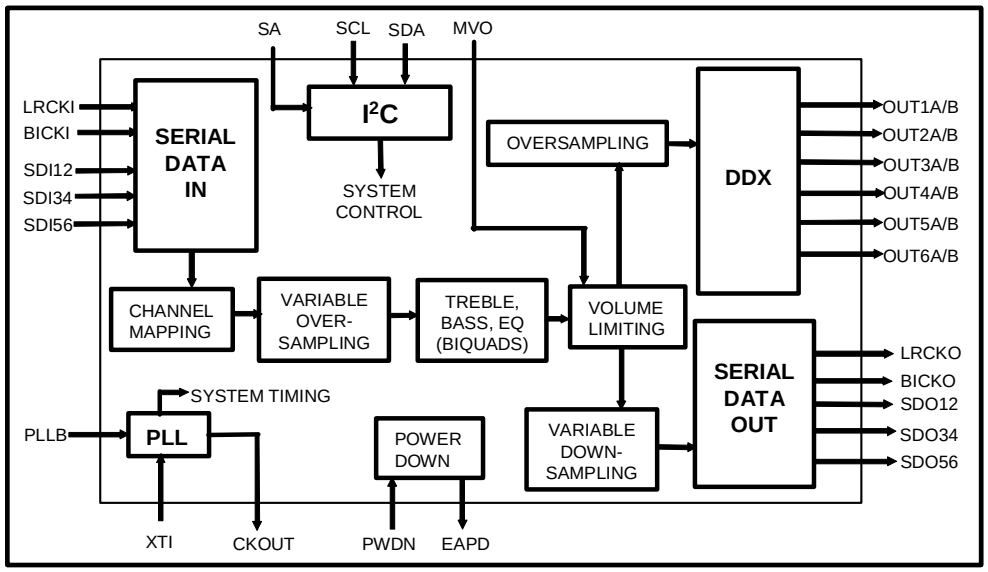
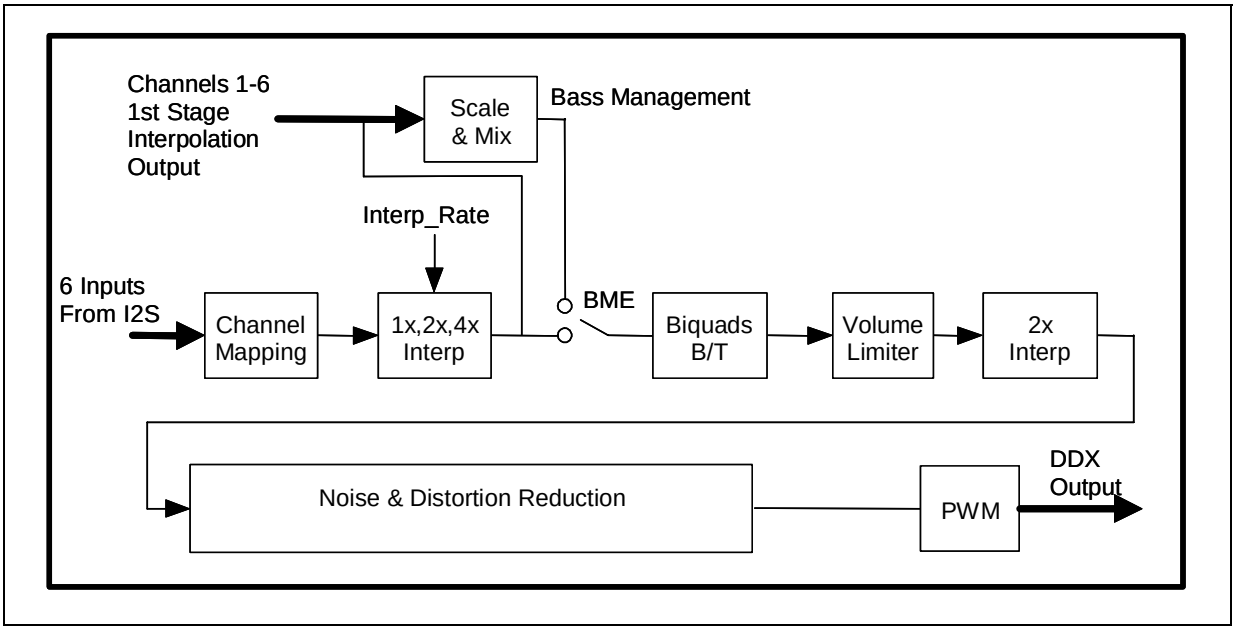
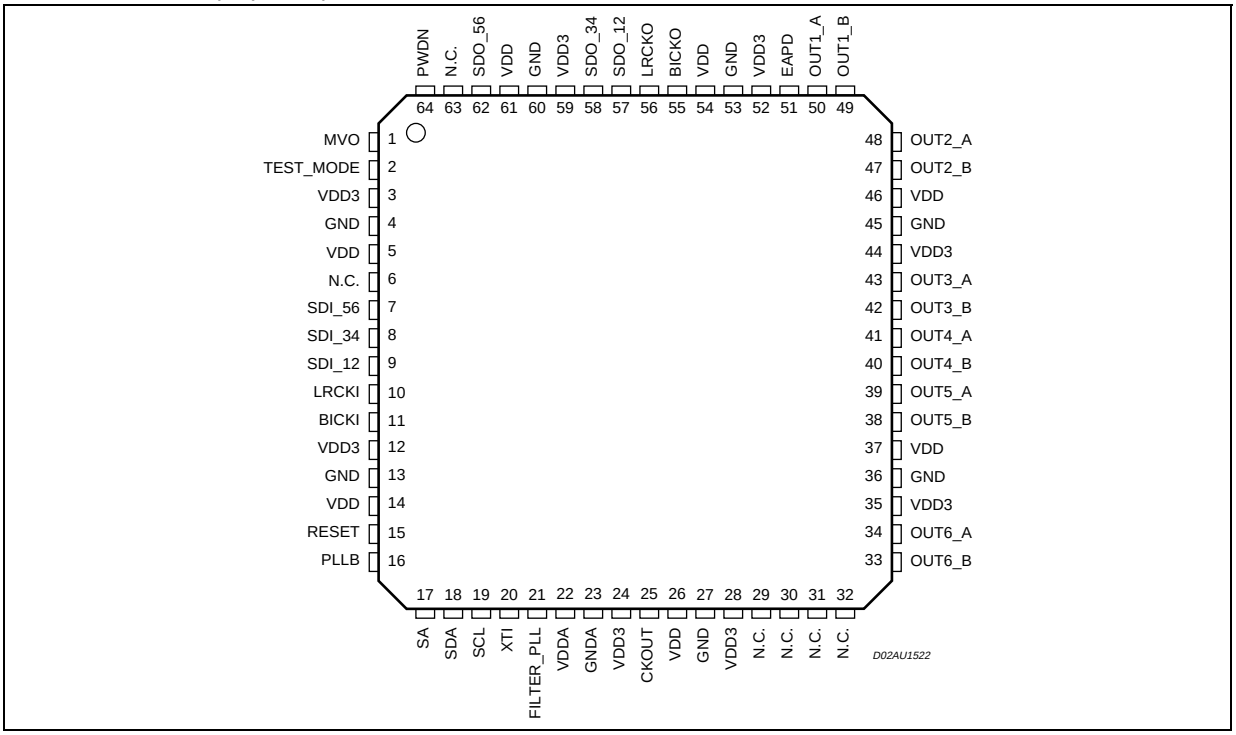


Figure 1. Signal Flow Diagram



IN CONNECTION (Top view)



PIN FUNCTION

PIN	NAME	TYPE	DESCRIPTION	PAD TYPE
1	MVO	I	Master Volume Override	CMOS Input Buffer with Pull-Down
3, 12, 24, 28, 35, 44, 52, 59	VDD3		3.3V Digital Supply	3.3V Digital Power Supply Voltage (pad ring)
2, 4, 13, 27, 36, 45, 53, 60	GND		Digital Ground	Digital Ground
5, 14, 26, 37, 46, 54, 61	VDD		2.5V Digital Supply	2.5V Digital Power Supply Voltage (core + ring)
7	SDI_56	I	Input I2S Serial Data Channels 5 & 6	5V Tolerant TTL Input Buffer
8	SDI_34	I	Input I2S Serial Data Channels 3 & 4	5V Tolerant TTL Input Buffer
9	SDI_12	I	Input I2S Serial Data Channels 1 & 2	5V Tolerant TTL Input Buffer
10	LRCKI	I	Inputs I2C Left/Right Clock	5V Tolerant TTL Input Buffer
11	BICKI	I	Inputs I2C Serial Clock	5V Tolerant TTL Input Buffer
15	RESET	I	Global Reset	5V Tolerant TTL Schmitt Trigger Input Buffer
16	PLLB	I	PLL Bypass	CMOS Input Buffer with Pull-Down
17	SA	I	Select Address (I2C)	CMOS Input Buffer with Pull-Down
18	SDA	I/O	I2C Serial Data	Bidirectional Buffer: 5V Tolerant TTL Schmitt Trigger Input; 3.3V Capable 2 mA Slew-rate control Output;
19	SCL	I	I2C Serial Clock	5V Tolerant TTL Schmitt Trigger Input Buffer

PIN FUNCTION (continued)

PIN	NAME	TYPE	DESCRIPTION	PAD TYPE
20	XTI	I	Crystal Oscillator Input (Clock Input)	3.3V Tolerant TTL Schmitt Trigger Input Buffer
21	FILTER_PLL		PLL Filter	Analog Pad
22	VDDA		PLL 2.5V Supply	2.5V Analog Power Supply Voltage
23	GNDA		PLL Ground	Analog Ground
25	CKOUT	O	Clock Output	3.3V Capable TTL Tristate 4mA Output Buffer
33	OUT6_B	O	PWM Channel 6 Output B	3.3V Capable TTL 2mA Output Buffer
34	OUT6_A	O	PWM Channel 6 Output A	3.3V Capable TTL 2mA Output Buffer
38	OUT5_B	O	PWM Channel 5 Output B	3.3V Capable TTL 2mA Output Buffer
39	OUT5_A	O	PWM Channel 5 Output A	3.3V Capable TTL 2mA Output Buffer
40	OUT4_B	O	PWM Channel 4 Output B	3.3V Capable TTL 2mA Output Buffer
41	OUT4_A	O	PWM Channel 4 Output A	3.3V Capable TTL 2mA Output Buffer
42	OUT3_B	O	PWM Channel 3 Output B	3.3V Capable TTL 2mA Output Buffer
43	OUT3_A	O	PWM Channel 3 Output A	3.3V Capable TTL 2mA Output Buffer
47	OUT2_B	O	PWM Channel 2 Output B	3.3V Capable TTL 2mA Output Buffer
48	OUT2_A	O	PWM Channel 2 Output A	3.3V Capable TTL 2mA Output Buffer
49	OUT1_B	O	PWM Channel 1 Output B	3.3V Capable TTL 2mA Output Buffer
50	OUT1_A	O	PWM Channel 1 Output A	3.3V Capable TTL 2mA Output Buffer
51	EAPD	O	External Amplifier Power Down	3.3V Capable TTL 2mA Output Buffer
55	BICKO	O	Output I2S Serial Clock	3.3V Capable TTL 2mA Output Buffer
56	LRCKO	O	Output I2S Left/Right Clock	3.3V Capable TTL 2mA Output Buffer
57	SDO_12	O	Output I2S Serial Data Channels 1 & 2	3.3V Capable TTL 2mA Output Buffer
58	SDO_34	O	Output I2S Serial Data Channels 3 & 4	3.3V Capable TTL 2mA Output Buffer
62	SDO_56	O	Output I2S Serial Data Channels 5 & 6	3.3V Capable TTL 2mA Output Buffer
63	SDO_78	O	Output I2S Serial Data Channels 7 & 8	3.3V Capable TTL 2mA Output Buffer
64	PWDN	I	Device Powerdown	5V Tolerant TTL Schmitt Trigger Input Buffer

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{DD_3.3}$	3.3V I/O Power Supply	-0.5 to 4	V
$V_{DD_2.5}$	2.5V Logic Power Supply	-0.5 to 3.3	V
V_i	Voltage on input pins	-0.5 to (VDD+0.5)	V
V_o	Voltage on output pins	-0.5 to (VDD+0.3)	V
T_{stg}	Storage Temperature	-40 to +150	°C
T_{amb}	Ambient Operating Temperature	-20 to +85	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj\text{-}amb}$	Thermal resistance Junction to Ambient	85	°C/W

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{DD_3.3}$	I/O Power Supply	3.0 to 3.6	V
$V_{DD_2.5}$	Logic Power Supply	2.3 to 2.7	V
T_j	Operating Junction Temperature	-20 to +125	°C

ELECTRICAL CHARACTERISTCS (V_{DD3} = 3.3V ± 0.3V; V_{DD} = 2.5V ± 0.2V; T_{amb} = 0 to 70 °C; unless otherwise specified)

GENERAL INTERFACE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
I_{il}	Low Level Input no pull-up	V_i = 0V			1	µA	1
I_{ih}	High Level Input no pull-down	$V_i = V_{DD3}$			2	µA	1
I_{OZ}	Tristate output leakage without pullup/down	$V_i = V_{DD3}$			2	µA	1
V_{esd}	Electrostatic Protection	Leakage < 1µA	2000			V	2

Note 1: The leakage currents are generally very small, < 1na. The values given here are maximum after an electrostatic stress on the pin.
Note 2: Human Body Model

DC ELECTRICAL CHARACTERISTICS: 3.3V BUFFERS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
V_{ILhyst}	Low Level Threshold	Input Falling	0.8		1.35	V
V_{IHhyst}	High Level Threshold	Input Rising	1.3		2.0	V
V_{hyst}	Schmitt Trigger Hysteresis		0.3		0.8	V
V_{ol}	Low Level Output	Iol = 100uA			0.2	V
V_{oh}	High Level Output	Ioh = -100uA Ioh = -2mA	VDD3-0.2 2.4			V V

DC ELECTRICAL CHARACTERISTICS: 2.5V BUFFERS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{ILst}	Low Level Input Voltage	Schmitt input			0.26*VDD	V
V_{IHst}	High Level Input Voltage	Schmitt input	0.7*VDD			V
V_{ILhyst}	Low Level Threshold	non Schmitt, Input Falling		0.5*VDD		V
V_{IHhyst}	High Level Threshold	non Schmitt, Input Rising	1.3	0.5*VDD	2.0	V
V_{hyst}	Schmitt Trigger Hysteresis		0.23*VDD			V
V_{OL}	Low Level Output	Note 1			0.15*VDD	V
V_{OH}	High Level Output	Note 1	0.85*VDD			V

Notes: 1. Source/Sink current under worst-case conditions.

1.0 PIN DESCRIPTION

1.1 MVO: Master Volume Override

This pin enables the user to bypass the Volume Control on all channels. When MVO is pulled High, the Master Volume Register is set to 00h, which corresponds to its Full Scale setting. The Master Volume Register Setting offsets the individual Channel Volume Settings, which default to 0dB.

1.2 SDI_12 through 56: Serial Data In

Audio information enters the device here. Six format choices are available including I2S, left- or right-justified, LSB or MSB first, with word widths of 16, 18, 20 and 24 bits.

1.3 RESET

Driving this pin (low) turns off the outputs and returns all settings to their defaults.

1.4 I2C

The SA, SDA and SCL pins operate per the Philips I2C specification. See Section 2.

1.5 PLL: Phase Locked Loop

The phase locked loop section provides the System Timing Signals and CKOUT.

1.6 CKOUT: Clock Out

System synchronization and master clocks are provided by the CKOUT.

1.7 OUT1 through OUT6: PWM Outputs

The PWM outputs provide the input signal for the power devices.

1.8 EAPD: External Amplifier Power-Down

This signal can be used to control the power-down of DDX power devices.

1.9 SDO_12 through 56: Serial Data Out

Audio information exits the device here. Six different format choices are available including I2S, left- or right-justified, LSB or MSB first, with word widths of 16, 18, 20 and 24 bits.

1.10 PWDN: Device Power-Down

This puts the STA306 into a low-power state via appropriate power-down sequence. Pulling PWDN low begins power-down sequence, and EAPD goes low ~30ms later.

2.0 II2C BUS SPECIFICATION

The STA306 supports the I2C protocol. This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The STA306 is always a slave device in all of its communications.

2.1 COMMUNICATION PROTOCOL

2.1.1 Data Transition or change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition.

2.1.2 Start Condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

2.1.3 Stop Condition

STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between STA306 and the bus master.

2.1.4 Data Input

During the data input the STA306 samples the SDA signal on the rising edge of clock SCL. For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

2.2 DEVICE ADDRESSING

To start communication between the master and the STA306, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8-bits (MSB first) corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifiers, corresponding to the I2C bus definition. In the STA306 the I2C interface has two device addresses depending on the SA pin configuration, 0x30 or 0011000x when SA = 0, and 0x32 or 0011001x when SA = 1.

The 8th bit (LSB) identifies read or write operation RW, this bit is set to 1 in read mode and 0 for write mode. After a START condition the STA306 identifies on the bus the device address and if a match is found, it acknowledges the identification on SDA bus during the 9th bit time. The byte following the device identification byte is the internal space address.

2.3 WRITE OPERATION

Following the START condition the master sends a device select code with the RW bit set to 0. The STA306 acknowledges this and the writes for the byte of internal address. After receiving the internal byte address the STA306 again responds with an acknowledgement.

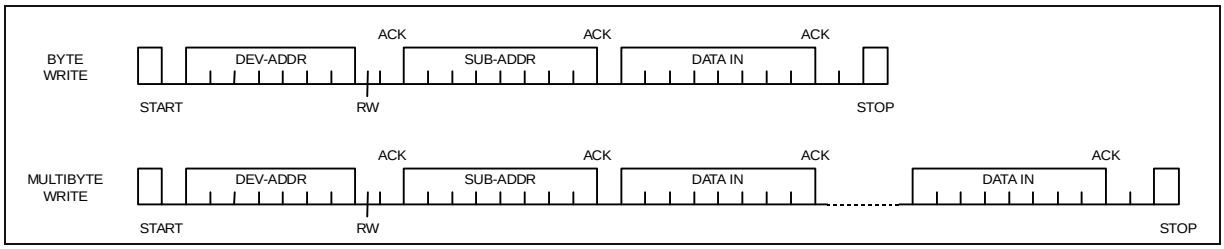
2.3.1 Byte Write

In the byte write mode the master sends one data byte, this is acknowledged by the STA306. The master then terminates the transfer by generating a STOP condition.

2.3.2 Multi-byte Write

The multi-byte write modes can start from any internal address. The master generating a STOP condition terminates the transfer.

Write Mode Sequence



Read Mode Sequence

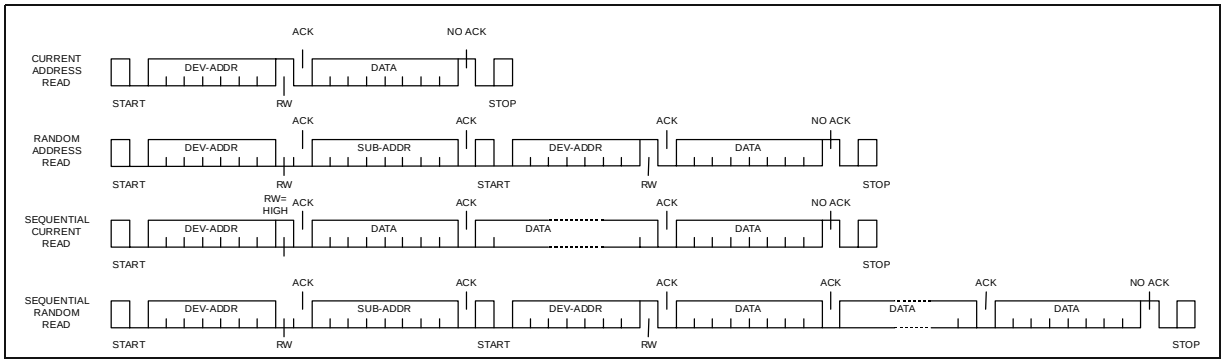


Table 1. Register summary

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
00h	**ConfA**	MPC	HPE	BME	IR1	IR0	MCS2	MCS1	MCS0
01h	**ConfB**	DRC	ZCE	SAIFB	SAI2	SAI1	SAI0	ZDE	DSPB
02h	**ConfC**	HPB	RES	RES	RES	RES	RES	OM1	OM0
03h	**ConfD**	BQL	PSL	COS1	COS0	C78BO	C56BO	C34BO	C12BO
04h	**ConfE**	RES	SAOFB	SAO2	SAO1	SAO0	DEMP	VOLEN	MIXE
05h	**ConfF**	EAPD				AME	COD	I2SD	PWMD
06h	**Mmute**								MMute
07h	**Mvol**	MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
08h	**Cmute**	C8M	C7M	C6M	C5M	C4M	C3M	C2M	C1M
09h	**C1Vol**	C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0Ah	**C2Vol**	C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0Bh	**C3Vol**	C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0Ch	**C4Vol**	C4V7	C4V6	C4V5	C4V4	C4V3	C4V2	C4V1	C4V0
0Dh	**C5Vol**	C5V7	C5V6	C5V5	C5V4	C5V3	C5V2	C5V1	C5V0
0Eh	**C6Vol**	C6V7	C6V6	C6V5	C6V4	C6V3	C6V2	C6V1	C6V0
0Fh	**C7Vol**	C7V7	C7V6	C7V5	C7V4	C7V3	C7V2	C7V1	C7V0

10h	**C8Vol**	C8V7	C8V6	C8V5	C8V4	C8V3	C8V2	C8V1	C8V0
11h	**C12im**		C2IM2	C2IM1	C2IM0		C1IM2	C1IM1	C1IM0
12h	**C34im**		C4IM2	C4IM1	C4IM0		C3IM2	C3IM1	C3IM0
13h	**C56im**		C6IM2	C6IM1	C6IM0		C5IM2	C5IM1	C5IM0
14h	**C78im**		C8IM2	C8IM1	C8IM0		C7IM2	C7IM1	C7IM0
15h	**C1234ls**	C4LS1	C4LS0	C3LS1	C3LS0	C2LS1	C2LS0	C1LS1	C1LS0
16h	**C5678ls**	C8LS1	C8LS0	C7LS1	C7LS0	C6LS1	C6LS0	C5LS1	C5LS0
17h	**L1ar**	L1R3	L1R2	L1R1	L1R0	L1A3	L1A2	L1A1	L1A0
18h	**L1atrt**	L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
19h	**L2ar**	L2R3	L2R2	L2R1	L2R0	L2A3	L2A2	L2A1	L2A0
1Ah	**L2atrt**	L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
1Bh	**Tone**	TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
1Ch	**Cfaddr**	CFA7	CFA6	CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
1Dh	**B2cf1**	C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
1Eh	**B2cf2**	C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
1Fh	**B2cf3**	C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
20h	**B0cf1**	C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
21h	**B0cf2**	C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
22h	**B0cf3**	C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
23h	**A2cf1**	C3B23	C3B22	C3B21	C3B20	C3B19	C3B18	C3B17	C3B16
24h	**A2cf2**	C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
25h	**A2cf3**	C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
26h	**A1cf1**	C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
27h	**A1cf2**	C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
28h	**A1cf3**	C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
29h	**B1cf1**	C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
2Ah	**B1cf2**	C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
2Bh	**B1cf3**	C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
2Ch	**Cfud**							WA	W1
2Dh	**DC1**	RES	RES	RES	RES	RES	RES	RES	RES
2Eh	**DC2**	RES	RES	RES	RES	RES	RES	RES	RES
2Fh	**BIST1**	RES	RES	RES	RES	RES	RES	RES	RES
30h	**BIST2**				RES	RES	RES	RES	RES

3.0 CONFIGURATION REGISTER A (ADDRESS 00H)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	MPC	HPE	BME	IR1	IR0	MCS2	MCS1	MCS0
RST	1	0	0	0	0	0	1	1

3.0.1 Master Clock Select

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	1	MCS0	Master Clock Select : Selects the ratio between the input I^2S sample frequency and the input clock.
1	R/W	1	MCS1	
2	R/W	0	MCS2	

The STA306 will support sample rates of 32kHz, 44.1kHz, 48Khz, 88.2kHz, 96kHz, 176.4kHz, and 192kHz. Therefore the internal clock will be:

– 65.536Mhz for 32kHz

– 90.3168Mhz for 44.1khz, 88.2kHz, and 176.4kHz

– 98.304Mhz for 48kHz, 96kHz, and 192kHz

The external clock frequency provided to the XTI pin must be a multiple of the input sample frequency(fs). The relationship between the input clock and the input sample rate is determined by both the MCSx and the IRx (Input Rate) register bits. The MCSx bits determine the PLL factor generating the internal clock and the IRx bits determine the oversampling ratio used internally.

Input Sample Rate *fs* (kHz)	IR	MCS(2..0)				
		1xx	011	010	001	000
32, 44.1, 48	00	128fs	256fs	384fs	512fs	768fs
88.2, 96	01	64fs	128fs	192fs	256fs	384fs
176.4, 192	10	64fs	128fs	192fs	256fs	384fs

3.0.2 Interpolation Ratio Select

BIT	R/W	RST	NAME	DESCRIPTION
3	R/W	0	IR0	Interpolation Ratio Select : Selects internal interpolation ratio based on input I^2S sample frequency
4	R/W	0	IR1	

The STA306 has variable interpolation (oversampling) settings such that internal processing and DDX output rates remain consistent. The first processing block interpolates by either 4 times, 2 times, or 1 time (pass-through). The IR bits determine the oversampling ratio of this interpolation.

Table 2. IR bit settings as a function of Input Sample Rate.

Input Sample Rate *Fs*	IR(1,0)	1st Stage Interpolation Ratio
32kHz	00	4 times oversampling
44.1kHz	00	4 times oversampling
48kHz	00	4 times oversampling
88.2kHz	01	2 times oversampling
96kHz	01	2 times oversampling
176.4kHz	10	Pass-Through
192kHz	10	Pass-Through

3.0.3 Bass Management Enable

BIT	R/W	RST	NAME	DESCRIPTION
5	R/W	0	BME	Bass Management Enable : 0 – No Bass Management 1 – Bass Management operation on channel 6, scale and add inputs

Channel 6 of the STA306 features a bass management mode that enables redirection of information in all other channels to this channel and which can then be filtered appropriately using the EQ(Biquad) section. Setting the BME bit selects the output of the scale and mix block for channel 6 instead of the output of the channel mapping block. The settings for the scale and mix block are provided by the CxBMS registers

3.0.4 Max Power Correction

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	1	MPC	Max Power Correction : Setting of 1 enables DDX correction for THD reduction near maximum power output.

Setting the MPC bit turns on special processing that corrects the DDX power device at high power. This mode should lower the THD+N of a full DDX system at maximum power output and slightly below. This mode will only be operational in OM= 00 or 10.

3.1 Configuration Register B (address 01h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	DRC	ZCE	SAIFB	SAI2	SAI1	SAI0	ZDE	DSPB
RST	0	1	0	0	0	0	1	0

3.1.1 DSP Bypass

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	DSPB	DSP Bypass Bit : 0 – Normal Operation 1 – Bypass of Biquad and Bass/Treble Functionality

Setting the DSPB bit bypasses the biquad and bass/treble functionality of the STA306.

3.1.2 Zero-Detect Mute Enable

BIT	R/W	RST	NAME	DESCRIPTION
1	R/W	1	ZDE	Zero-Detect Mute Enable : Setting of 1 enables the automatic zero-detect mute

Setting the ZDE bit enables the zero-detect automatic mute.

The zero-detect circuit looks at the input data to each processing channel after the channel mapping block. If any channel receives 2048 consecutive zero value samples (regardless of fs) then that individual channel is muted if this function is enabled.

Serial Audio Input Interface Format

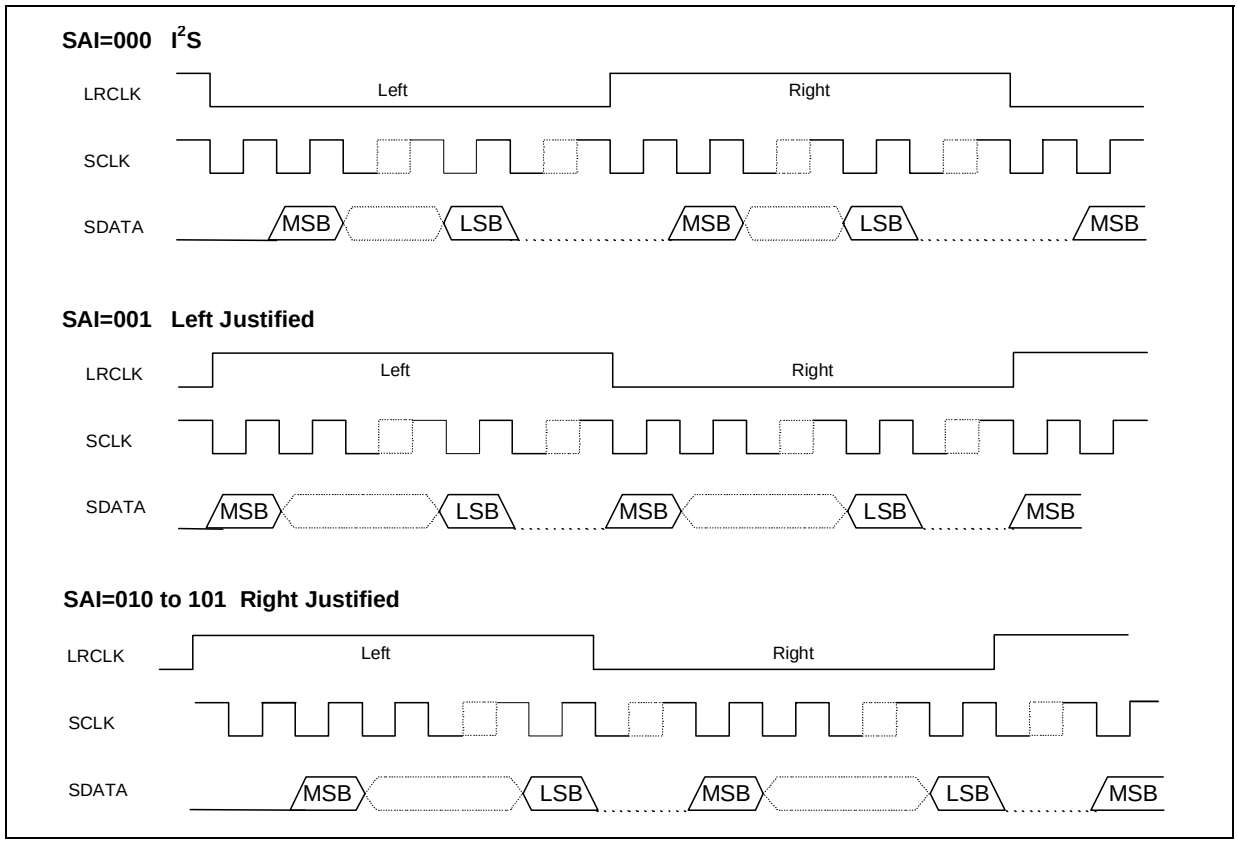
BIT	R/W	RST	NAME	DESCRIPTION
2	R/W	0	SAI0	Serial Audio Input Interface Format : Determines the interface format of the input serial digital audio interface.
3	R/W	0	SAI1	
4	R/W	0	SAI2	

The STA306 features a configurable digital serial audio interface. The settings of the SAIx bits determine how the input to this interface is interpreted. Six formats are accepted.

Table 3. Interface format as a function of SAI bits.

SAI(2..0)	Interface Format
000	I^2S
001	Left-Justified Data
010	Right-Justified 16-bit Data
011	Right-Justified 18-bit Data
100	Right-Justified 20-bit Data
101	Right-Justified 24-bit Data

Figure 2. Serial Audio Signals



3.1.3 Serial Audio Input Interface First Bit

BIT	R/W	RST	NAME	DESCRIPTION
5	R/W	0	SAIFB	Determines MSB or LSB first for all SAI formats 0 – MSB First, 1 – LSB First

3.1.4 Zero-Crossing Volume Enable

BIT	R/W	RST	NAME	DESCRIPTION
6	R/W	1	ZCE	Zero-Crossing Volume Enable : 1 – Volume adjustments will only occur at digital zero-crossings 0 – Volume adjustments will occur immediately

The ZCE bit enables zero-crossing volume adjustments. When volume is adjusted on digital zero-crossings, "zipper noise" is eliminated

3.1.5 Dynamic Range Compression/Anti-Clipping Bit

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	0	DRC	Dynamic Range Compression/Anti-Clipping 0 – Limiters act in Anti-Clipping Mode 1- Limiters act in Dynamic Range Compression Mode

Both limiters can be used in one of two ways, anti-clipping or dynamic range compression. When used in anti-clipping mode the limiter threshold values are constant and dependent on the gain/attenuation settings applied to the input signal. In dynamic range compression mode the limiter threshold values vary with the volume settings allowing for limiting to occur independently of the gain/attenuation but dependent on the input signal

3.2 Configuration Register C (address 02h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	HPB	RES	RES	RES	RES	RES	OM1	OM0
RST	0	1	1	1	1	1	0	0

3.2.1 DDX Power Output Mode

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	OM0	DDX Power Output Mode : Selects configuration of DDX output.
1	R/W	0	OM1	

The DDX Power Output Mode selects how the DDX output timing is configured. Different power devices use different output modes. The DDX recommended use is OM = 00. The variable mode uses the OMVx bits for adjustment

OM(1,0)	Output Stage - Mode
00	Fixed Compensation
01	RESERVED
10	Full Power Mode recommended for STA500 and STA505
11	RESERVED

3.2.2 High-Pass Filter Bypass

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	0	HPB	High-Pass Filter Bypass Bit. Setting of one bypasses internal AC coupling digital high-pass filter

The STA306 features an internal digital high-pass filter for the purpose of AC coupling. The purpose of this filter is to prevent DC signals from passing through a DDX amplifier. DC signals can cause speaker damage

3.3 Configuration Register D (address 03h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	BQL	PSL	COS1	COS0	C78BO	C56BO	C34BO	C12BO
RST	0	0	1	0	0	0	0	0

3.3.1 Binary Output Enable Registers

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	C12BO	Channels 1&2, 3&4, 5&6 Binary Output Mode Enable Bits. A setting of 0 indicates ordinary DDX tri-state output. A setting of 1 indicates binary output mode.
1	R/W	0	C34BO	
2	R/W	0	C56BO	
3	R/W	0	C78BO	

Each two-channel pair of outputs can be set to output a binary PWM stream. In this mode, output A

of a channel will be considered the positive output and output B is negative inverse. For example, setting C34BO = 1 sets channels 3&4 to Binary Output (PWM) Mode.

3.3.2 Clock Output Select

BIT	R/W	RST	NAME	DESCRIPTION
4	R/W	0	COS0	Clock Output Select
5	R/W	1	COS1	Clock Output Select

The Clock Output Select register selects the frequency of the clock output pin relative to the PLL clock output. The PLL clock runs at 2048fs for 32, 44.1, and 48kHz, at 1024fs for 88.2kHz and 96 kHz, and at 512fs for 176.4kHz and 192kHz.

COS(1,0)	CKOUT Frequency
01	PLL Output/4
10	PLL Output/8
11	PLL Output/16

3.3.3 Post-Scale Link

BIT	R/W	RST	NAME	DESCRIPTION
6	R/W	0	PSL	Post-Scale Link :0 – Each Channel uses individual Post-Scale value 1 - Each Channel uses Channel 1 Post-Scale value

For multi-channel applications, the post-scale values can be linked to the value of channel 1 for ease of use and update the values faster.

3.3.4 Biquad Coefficient Link

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	0	BQL	Biquad Link : 0 – Each Channel uses coefficient values 1- Each Channel uses Channel 1 coefficient values

For ease of use, all channels can use the biquad coefficients loaded into the Channel 1 Coefficient RAM space by setting the BQL bit to 1. Then any EQ updates would only have to be performed once.

3.4 Configuration Register E (address 04h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	RES	SAOFB	SAO2	SAO1	SAO0	DEMP	VOLEN	MIXE
RST	0	0	0	0	0	0	1	0

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	MIXE	Mix Enable: 0 – Normal Operation 1 - Adjacent Channel Mix Mode

The scale and mix functionality can be used to mix adjacent channels instead of for bass management. By setting this bit(BME must be set to 0) odd channels will be mixed with their adjacent even channel and output in the place of the even channel. The odd channel wills pass-through unscaled. The values used for this function are the same as for bass management. Since this function occurs post channel mapping a large number of possibilities are present for two channel mixing. Up to four mixed channels can be obtained.

BIT	R/W	RST	NAME	DESCRIPTION
1	R/W	1	VOLEN	Volume Enable: 0 – Volume Operation Bypassed 1 - Volume Operation Normal

When VOLEN set to 1, volume operation is normal. When set to 0, volume operation is bypassed and the volume stages are all set to pass-through. This also eliminates the digital volume offset of ~-0.6dB that is used to map full-scale digital input to full DDX modulation output.

BIT	R/W	RST	NAME	DESCRIPTION
2	R/W	0	DEMP	Deemphasis : 0 – No Deemphasis, 1- Deemphasis

By setting this bit to one deemphasis will implemented on all channels. When this is used it takes the place of biquad #1 in each channel and any coefficients using biquad #1 will be ignored. DSPB(DSP Bypass) bit must be set to 0 for Deemphasis to function.

BIT	R/W	RST	NAME	DESCRIPTION
3	R/W	0	SAO0	Serial Audio Output Interface Format : Determines the interface format of the output serial digital audio interface.
4	R/W	0	SAO1	
5	R/W	0	SAO2	

The STA306 features a configurable digital serial audio interface. The settings of the SAIx bits determine how the output to this interface is interpreted. Six formats are accepted.

Table 4. Interface format as a function of SAO bits.

SAO(2..0)	Interface Format
000	I^2S
001	Left-Justified Data
010	Right-Justified 16-bit Data
011	Right-Justified 18-bit Data
100	Right-Justified 20-bit Data
101	Right-Justified 24-bit Data

BIT	R/W	RST	NAME	DESCRIPTION
6	R/W	0	SAOFB	Determines MSB or LSB first for all SAO formats; 0 – MSB First 1 – LSB First

3.5 Configuration Register F (address 05h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	EAPD				AME	COD	SID	PWMD
RST	0				0	0	0	0

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	PWMD	PWM Output Disable: 0 – PWM Output Normal 1- No PWM Output
1	R/W	0	SID	Serial Interface(I^2S Out) Disable: 0 – I^2S Output Normal 1- No I^2S Output
2	R/W	0	COD	Clock Output Disable: 0 – Clock Output Normal 1- No Clock Output
3	R/W	0	AME	AM Mode Enable : 0 – Normal DDX operation. 1 – AM reduction mode DDX operation.

The STA306 features a DDX processing mode that minimizes the amount of noise generated in frequency range of AM radio. This mode is intended to be used when DDX is operating in a device with an AM tuner active. The SNR of the DDX processing is reduced to ~83dB in this mode, which is still greater than the SNR of AM radio.

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	0	EAPD	External Amplifier Power Down: 0 – External Power Stage Power Down Active 1 - Normal Operation

This output bit, on pin 51 of the device, is used to mute the DDX Power Devices for Power-Down.

3.6 Master Mute Register (address 06h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME								MMUTE
RST								0

3.7 Master Volume Register (address 07h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
RST	1	1	1	1	1	1	1	1

3.8 Channels 1,2,3,4,5,6 Mute (address 08h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C8M	C7M	C6M	C5M	C4M	C3M	C2M	C1M
RST	0	0	0	0	0	0	0	0

3.9 Channel 1 Volume (address 09h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
RST	0	0	1	1	0	0	0	0

3.10 Channel 2 Volume (address 0Ah)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
RST	0	0	1	1	0	0	0	0

3.11 Channel 3 Volume (address 0Bh)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
RST	0	0	1	1	0	0	0	0

3.12 Channel 4 Volume (address 0Ch)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C4V7	C4V6	C4V5	C4V4	C4V3	C4V2	C4V1	C4V0
RST	0	0	1	1	0	0	0	0

3.13 Channel 5 Volume (address 0Dh)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C5V7	C5V6	C5V5	C5V4	C5V3	C5V2	C5V1	C5V0
RST	0	0	1	1	0	0	0	0

3.14 Channel 6 Volume (address 0Eh)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C6V7	C6V6	C6V5	C6V4	C6V3	C6V2	C6V1	C6V0
RST	0	0	1	1	0	0	0	0

The Volume structure of the STA306 consists of individual volume registers for each channel and a master volume register that provides an offset to each channels volume setting. The individual channel volumes are adjustable in 0.5dB steps from +24dB to -103dB. As an example if C5V = 0Bh or +18.5dB and MV = 21h or -16.5dB, then the total gain for channel 5 = +2dB. The Master Mute when set to 1 will mute all channels at once, whereas the individual channel mutes(CxM) will mute only that channel. Both the Master Mute and the Channel Mutes provide a "soft mute" with the volume ramping down to mute in 8192 samples from the maximum volume setting at the internal processing rate(~192kHz). A "hard mute" can be obtained by commanding a value of all 1's(255) to any channel volume register or the master volume register. When volume offsets are provided via the master volume register any channel that whose total volume is less than -103dB will be muted. All changes in volume take place at zero-crossings when ZCE = 1(configuration register B) on a per channel basis as this creates the smoothest possible volume transitions. When ZCE=0, volume updates will occur immediately.

Table 5. Master Volume Offset as a function of MV(7..0).

MV(7..0)	Volume Offset from Channel Value
00000000(00h)	0dB
00000001(01h)	-0.5dB
00000010(02h)	-1dB
…	…
01001100(4Ch)	-38dB
…	…
11111110(FEh)	-127dB
11111111(FFh)	Hard Master Mute

Channel Volume as a function of CxV(7..0)

CxV(7..0)	Volume
00000000(00h)	+24dB
00000001(01h)	+23.5dB
00000010(02h)	+23dB
…	…
00101111(2Fh)	+0.5dB
00110000(30h)	0dB
00110001(31h)	-0.5dB
…	…
11111110(FEh)	-103dB
11111111(FFh)	Hard Channel Mute

3.15 Channel Input Mapping Channels 1 & 2 (address 11h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME		C2IM2	C2IM1	C2IM0		C1IM2	C1IM1	C1IM0
RST		0	0	1		0	0	0

3.16 Channel Input Mapping Channels 3 & 4 (address 12h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME		C4IM2	C4IM1	C4IM0		C3IM2	C3IM1	C3IM0
RST		0	1	1		0	1	0

3.17 Channel Input Mapping Channels 5 & 6 (address 13h)

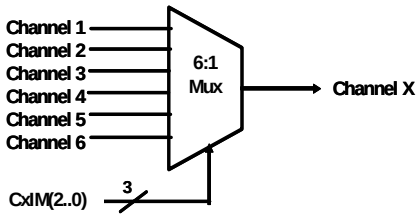
BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME		C6IM2	C6IM1	C6IM0		C5IM2	C5IM1	C5IM0
RST		1	0	1		1	0	0

Each channel received via I2S can be mapped to any internal processing channel via the Channel Input Mapping registers. This allows for flexibility in processing, simplifies output stage designs, and enables the ability to perform crossovers. The default settings of these registers map each I2S input channel to its corresponding processing channel.

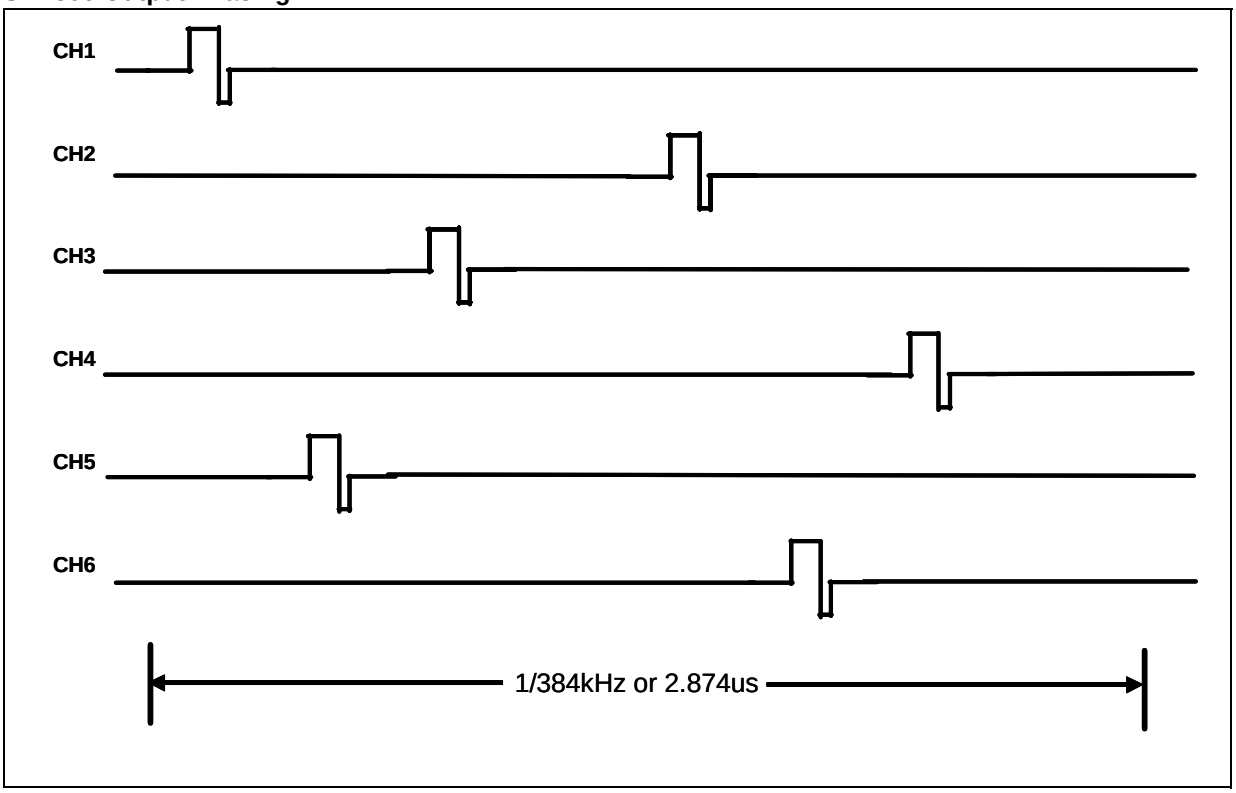
For example, to map input 2 to Channel 5, set Address 11h, bits D6, D5 and D4 to 100. Now, inputs 2 and 5 go to Channel 5.

Table 6. Channel Mapping as a function of CxIM bits

CxIM(2..0)	I^2S Input Mapped to:
000	Channel 1
001	Channel 2
010	Channel 3
011	Channel 4
100	Channel 5
101	Channel 6



STA306 Output Phasing



3.18 Channel Limiter Select Channels 1,2,3,4 (address 15h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C4LS1	C4LS0	C3LS1	C3LS0	C2LS1	C2LS0	C1LS1	C1LS0
RST	0	0	0	0	0	0	0	0

3.19 Channel Limiter Select Channels 5,6 (address 16h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C8LS1	C8LS0	C7LS1	C7LS0	C6LS1	C6LS0	C5LS1	C5LS0
RST	0	0	0	0	0	0	0	0

3.20 Limiter 1 Attack/Release Rate (address 17h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	L1R3	L1R2	L1R1	L1R0	L1A3	L1A2	L1A1	L1A0
RST	1	0	1	0	0	1	1	0

3.21 Limiter 1 Attack/Release Threshold (address 18h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
RST	0	1	1	0	0	1	1	1

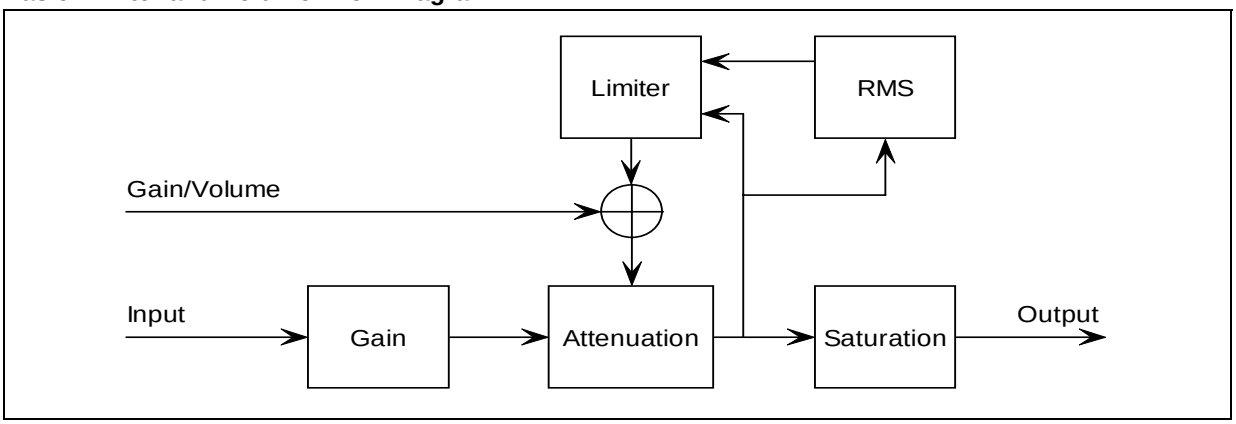
3.22 Limiter 2 Attack/Release Rate (address 19h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	L2R3	L2R2	L2R1	L2R0	L2A3	L2A2	L2A1	L2A0
RST	1	0	1	0	0	1	1	0

3.23 Limiter 2 Attack/Release Threshold (address 1Ah)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
RST	0	1	1	0	0	1	1	1

Basic Limiter and Volume Flow Diagram.



A limiter is basically a variable gain device, where the amount of gain applied depends on the input signal level. As the name implies, compression limits the dynamic range of the signal.

The STA306 includes 2 independent limiter blocks.

The purpose of the limiters is to automatically reduce the dynamic range of the input signal to prevent the outputs from clipping in anti-clipping mode or to actively reduce the dynamic range for a better listening environment such as a night-time listening mode which is often needed for DVDs. The two modes are selected via the DRC bit in Configuration Register B; address 0x02, bit 7.

Each channel can be mapped to either limiter or not mapped. Non-mapped channels will clip when 0dBFS is exceeded. Each limiter will look at the present value of each channel that is mapped to it, select the maximum absolute value of all these channels, perform the limiting algorithm on that value, and then, if needed, adjust the gain of the mapped channels in unison.

The limiter attack thresholds are determined by the LxAT registers. It is recommended in anti-clipping mode to set this to 0dBFS, which corresponds to the maximum unclipped output power of a DDX amplifier. Since gain can be added digitally within the STA306 it is possible to exceed 0dBFS or any other LxAT setting. When this occurs, the limiter, when active, will automatically start reducing the gain. The rate at which the gain is reduced when the attack threshold is exceeded is dependent upon the attack rate register setting for that limiter. The gain reduction occurs on a peak-detect algorithm.

The release of limiter (uncompression), when the gain is again increased, is dependent on a RMS-detect algorithm. The output of the volume/limiter block is passed through a RMS filter. The output of this filter is compared to the release threshold, determined by the Release Threshold register. When the RMS filter output falls below the release threshold, the gain is again increased (uncompressed) at a rate dependent upon the Release Rate register. The gain can never be increased past its set value and therefore the release will only occur if the limiter has already reduced the gain.

The release threshold value can be used to set what is effectively a minimum dynamic range, this is helpful as over-limiting can reduce the dynamic range to virtually zero and cause program material to sound "lifeless". In AC mode the attack and release thresholds are set relative to full-scale. In DRC mode the attack threshold is set relative to the maximum volume setting of the channels mapped to that limiter and the release threshold is set relative to the maximum volume setting plus the attack threshold.

Table 7. Channel Limiter Mapping as a function of CxLS bits.

CxLS(1,0)	Channel Limiter Mapping
00	Channel has limiting disabled
01	Channel is mapped to limiter #1
10	Channel is mapped to limiter #2

Table 8. Limiter Attack Rate as a function of LxA bits.

LxA(3..0)	Attack Rate dB/ms
0001	
0010	
0011	
LxA(3..0)	1.3536
0000	0.9024
0110	0.4512
0111	0.2256
1000	0.1504
1001	0.1123
1010	0.0902
1011	0.0752
1100	0.0645
1101	0.0564
1110	0.0501
1111	0.0451

note: Shaded areas are Default Settings

Table 9. Limiter Release Rate and Uncompression Threshold as a function of LxR bits

LxR(3..0)	Release Rate dB/ms
0000	0.5116
0001	0.1370
0010	0.0744
0011	0.0499
0100	0.0360
0101	0.0299
0110	0.0264
0111	0.0208
1000	0.0198
1001	0.0172
1010	0.0147
1011	0.0137
1100	0.0134
1101	0.0117
1110	0.0110
1111	0.0104

Table 10. Limiter Attack Threshold as a function of LxAT bits.

LxAT(3..0)	AC(dB relative to FS)	DRC(db relative to Volume)
0000	-12	-22
0001	-10	-20
0010	-8	-18
0011	-6	-16
0100	-4	-14
0101	-2	-12
0110	0	-10
0111	+2	-8
1000	+3	-7
1001	+4	-6
1010	+5	-5
1011	+6	-4
1100	+7	-3
1101	+8	-2
1110	+9	-1
1111	+10	0

Table 11. Limiter Release Threshold as a function of LxRT bits

LxRT(3..0)	AC(dB relative to FS)	DRC(db relative to Volume + LxAT)
0000	•	•
0001	-23dB	-33dB
0010	-16.9dB	-26.9dB
0011	-13.4dB	-23.4dB
0100	-10.9dB	-20.9dB
0101	-9.0dB	-19.0dB
0110	-7.4dB	-17.4dB
0111	-6.0dB	-16.0dB
1000	-4.9dB	-14.9dB
1001	-3.8dB	-13.8dB
1010	-2.9dB	-12.9dB
1011	-2.1dB	-12.1dB
1100	-1.3dB	-11.3dB
1101	-0.65dB	-10.65dB
1110	0dB	-10dB
1111	+0.6dB	-9.4dBdB

3.24 Bass and Treble Tone Control(address 1Bh)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
RST	0	1	1	1	0	1	1	1

The STA306 contains bass and treble tone control adjustments. These are selectable from +12dB to -12dB of boost or cut. These are 1st order shelving filters with a corner frequency of 150Hz for bass and 3kHz for treble. Any gain introduced in the tone controls will carry through to the volume and limiting block without saturation.

Table 12. Tone Control Boost/Cut as a function of BTC and TTC bits

BTC(3..0)/TTC(3..0)	Boost/Cut
0000	-12dB
0001	-12dB
…	…
0111	-4dB
0110	-2dB
0111	0dB
1000	+2dB
1001	+4dB
…	…
1101	+12dB
1110	+12dB
1111	+12dB

3.25 Coefficient Address Register (address 1Ch)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	CFA7	CFA6	CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
RST	0	0	0	0	0	0	0	0

3.26 Coefficient b2 Data Register Bits 23..16 (address 1Dh)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
RST	0	0	0	0	0	0	0	0

3.27 Coefficient b2 Data Register Bits 15..8 (address 1Eh)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
RST	0	0	0	0	0	0	0	0

3.28 Coefficient b2 Data Register Bits 7..0 (address 1Fh)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
RST	0	0	0	0	0	0	0	0

3.29 Coefficient b0 Data Register Bits 23..16 (address 20h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
RST	0	0	0	0	0	0	0	0

3.30 Coefficient b0 Data Register Bits 15..8 (address 21h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
RST	0	0	0	0	0	0	0	0

3.31 Coefficient b0 Data Register Bits 7..0 (address 22h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
RST	0	0	0	0	0	0	0	0

3.32 Coefficient a2 Data Register Bits 23..16 (address 23h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C3B23	C3B22	C3B21	C3B20	C3B19	C3B18	C3B17	C3B16
RST	0	0	0	0	0	0	0	0

3.33 Coefficient a2 Data Register Bits 15..8 (address 24h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
RST	0	0	0	0	0	0	0	0

3.34 Coefficient a2 Data Register Bits 7..0 (address 25h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
RST	0	0	0	0	0	0	0	0

3.35 Coefficient a1 Data Register Bits 23..16 (address 26h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
RST	0	0	0	0	0	0	0	0

3.36 Coefficient a1 Data Register Bits 15..8 (address 27h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
RST	0	0	0	0	0	0	0	0

3.37 Coefficient a1 Data Register Bits 7..0 (address 28h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
RST	0	0	0	0	0	0	0	0

3.38 Coefficient b1 Data Register Bits 23..16 (address 29h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
RST	0	0	0	0	0	0	0	0

3.39 Coefficient b1 Data Register Bits 15..8 (address 2Ah)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
RST	0	0	0	0	0	0	0	0

3.40 Coefficient b1 Data Register Bits 7..0 (address 2Bh)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
RST	0	0	0	0	0	0	0	0

3.41 Coefficient Write Control Register (address 2Ch)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
NAME							WA	W1
RST								

Coefficients for EQ and Bass Management are handled internally in the STA306 via RAM. Access to this RAM is available to the user via an I2C register interface. A collection of I2C registers is dedicated to this function. One contains a coefficient base address, five sets of three store the values of the 24-bit coefficients to be written or that were read, and one contains bits used to control the writing of the coefficient(s) to RAM. The following are step instructions for reading and writing coefficients.

Reading a coefficient from RAM

- write 8-bit address to I2C register 1Ch
- ead top 8-bits of coefficient in I2C address 1Dh
- ead middle 8-bits of coefficient in I2C address 1Eh
- ead bottom 8-bits of coefficient in I2C address 1Fh

Writing a single coefficient to RAM

- write 8-bit address to I2C register 1Ch
- write top 8-bits of coefficient in I2C address 1Dh
- write middle 8-bits of coefficient in I2C address 1Eh
- write bottom 8-bits of coefficient in I2C address 1Fh
- write 1 to W1 bit in I2C address 2Bh

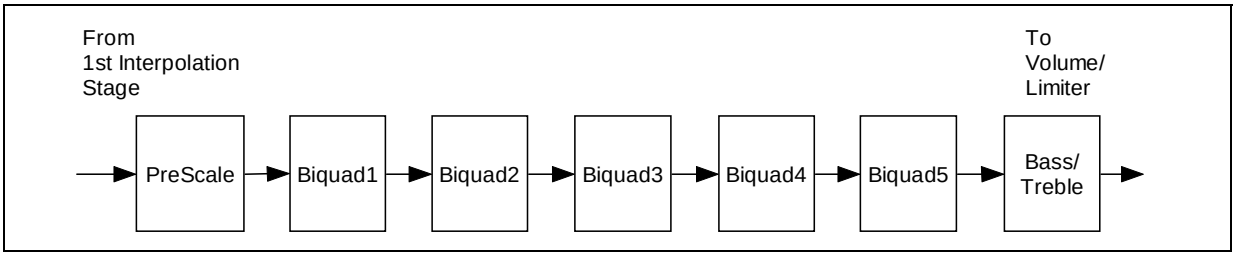
Writing a set of coefficients to RAM

- write 8-bit starting address to I2C register 1Ch
- write top 8-bits of coefficient b2 in I2C address 1Dh
- write middle 8-bits of coefficient b2 in I2C address 1Eh
- write bottom 8-bits of coefficient b2 in I2C address 1Fh
- write top 8-bits of coefficient b0 in I2C address 20h
- write middle 8-bits of coefficient b0 in I2C address 21h
- write bottom 8-bits of coefficient b0 in I2C address 22h
- write top 8-bits of coefficient a2 in I2C address 23h
- write middle 8-bits of coefficient a2 in I2C address 24h
- write bottom 8-bits of coefficient a2 in I2C address 25h
- write top 8-bits of coefficient a1 in I2C address 26h
- write middle 8-bits of coefficient a1 in I2C address 27h
- write bottom 8-bits of coefficient a1 in I2C address 28h
- write top 8-bits of coefficient b1 in I2C address 29h
- write middle 8-bits of coefficient b1 in I2C address 2Ah
- write bottom 8-bits of coefficient b1 in I2C address 2Bh
- write 1 to WA bit in I2C address 2Ch

The mechanism for writing a set of coefficients to RAM provides a method of updating the five coefficients corresponding to a given biquad (filter) simultaneously to avoid possible unpleasant acoustic side effects. When using this technique, the 8-bit address would specify the address of the biquad b2 coefficient (e.g. 0, 5, 10, 15, …, 50, … 195 decimal), and the STA306 will generate the RAM addresses as offsets from this base value to write the complete set of coefficient data.

Equalization:

Figure 3. Data Flow for single channel Biquad / Bass / Treble block.:



Five user-programmable 28-bit biquads are available per channel in the STA306. These biquads run at 192kHz for 48kHz, 96kHz, or 192kHz input and at 176.4kHz for 44.1kHz, 88.2kHz, and 176.4kHz input. The PreScale block is used for attenuation when filters are to be designed that boost frequencies above 0dBFS. This is a

single 28-bit signed multiply, with 800000h = -1 and 7FFFFFh = 0.9999998808. These values are labeled CxPS, with x representing the channel. The biquads use this equation:

Y[n] = 2(b0/2)X[n] + 2(b1/2)X[n-1] + b2X[n-2] - 2(a1/2)Y[n-1] - a2Y[n-2]

= b0X[n] + b1X[n-1] + b2X[n-2] - a1Y[n-1] - a2Y[n-2]

Y[n] represents the output and X[n] represents the input. Coefficients are defined in the following manner:

CxHx0 = b2
CxHx1 = b0/2
CxHx2 = -a2
CxHx3 = -a1/2
CxHx4 = b1/2

The first x represents the channel and the second the biquad number. For example C3H41 is the b0/2 coefficient in the fourth series biquad in channel 3. The biquad link bit allows all channels to use the coefficients of channel 1.

Bass Management

Channel 6 provides the ability to scale and mix all channels before the biquad block. This allows for information from any channel to be redirected to this channel and then filtered appropriately for a subwoofer application. When the BME bit is set (bit D5 of Configuration Register A, at address 00h) the input to the biquad section is routed from the scale and mix block instead of the normal channel 6 1st stage interpolation output.

Eight scaling coefficients are provided to perform this function. They are labeled CxBMS with x representing the channel that is being scaled. Each input channel is multiplied by its corresponding scale factor and summed. The output of the summation is the output of the scale and mix block.

Post-Scale

The STA306 provides one additional multiplication after the last interpolation stage and before the distortion compensation on each channel. This is a 24-bit signed fractional multiply. The scale factor for this multiply is loaded into RAM using the same I2C registers as the biquad coefficients and the bass-management. All channels can use the channel 1 by setting the post-scale link bit.

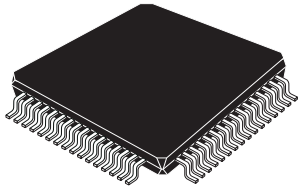
RAM Block for Biquads and Bass Management:

Index (Decimal)	Index (Hex)		Coefficient	Default
0	00h	Channel 1 - Biquad 1	C1H10($b_{2)}$	000000h
1	01h		C1H11(b0/2)	3FFFFFh
2	02h		C1H12(a2)	000000h
3	03h		C1H13(a1/2)	000000h
4	04h		C1H14(b1/2)	000000h
5	05h	Channel 1 - Biquad 2	C1H20	000000h
…	…	…	…	…

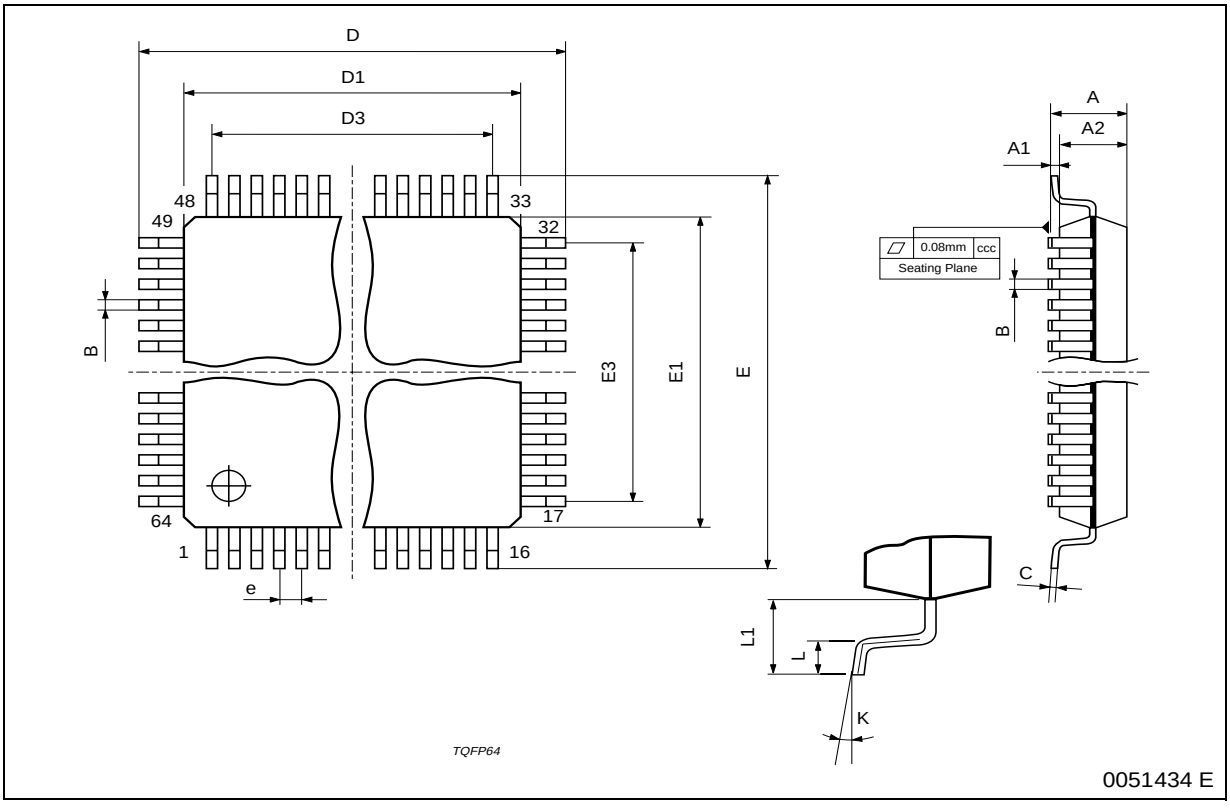
24	18h	Channel 1 - Biquad 5	C1H54	000000h
25	19h	Channel 2 - Biquad 1	C2H10	000000h
26	1Ah		C2H11	3FFFFFh
…	…	…	…	…
45	2Dh	Distortion Compensation	DCC 23…0	000000h
…	…	…	…	…
49	31h	Channel 2 - Biquad 5	C2H54	000000h
50	32h	Channel 3 - Biquad 1	C3H10	000000h
…	…	…	…	…
200	C8h	Channel 1 - Pre-Scale	C1PS	800000h
201	C9h	Channel 2 – Pre-Scale	C2PS	800000h
202	CAh	Channel 3 – Pre-Scale	C3PS	800000h
…	…	…	…	…
208	D0h	Channel 1 – BassM Scale	C1BMS	000000h
209	D1h	Channel 2 – BassM Scale	C2BMS	000000h
…	…	…	…	…
216	D8h	Channel 1 – Post-Scale	C1PS	800000h
217	D9h	Channel 2 – Post-Scale	C2PS	800000h
…	…	…	…	…
224	F0h	Not Used		
…	…	…	…	…
255	FFh	Not Used		

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.0066	0.0086	0.0086
C	0.09			0.0035		
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		7.50			0.295	
e		0.50			0.0197	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		7.50			0.295	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0393	
K	0° (min.), 3.5° (min.), 7°(max.)					
ccc			0.080			0.0031

OUTLINE AND MECHANICAL DATA



TQFP64 (10 x 10 x 1.4mm)



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